HARRIS SEMICONDUCTOR

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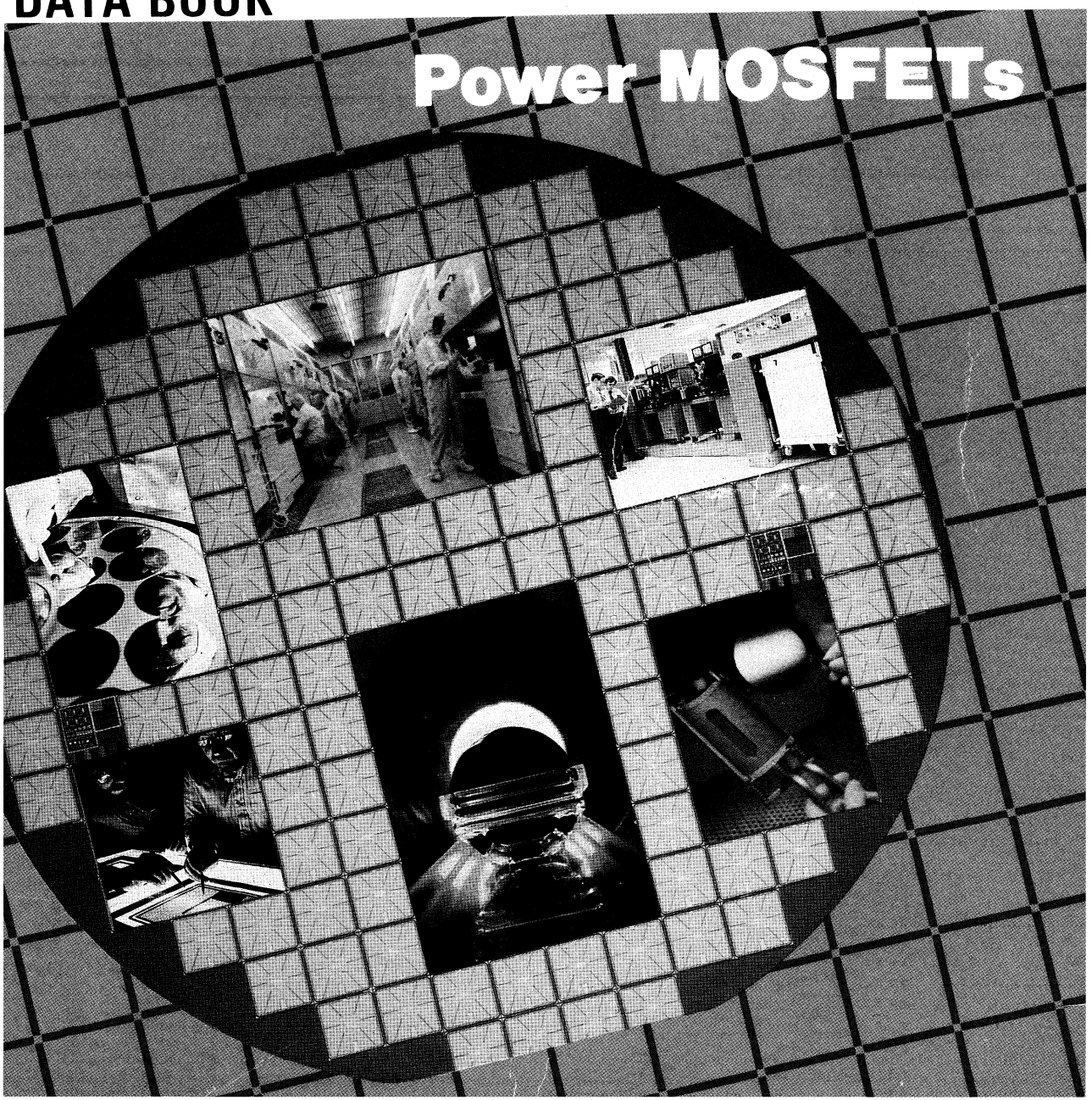
DATA BOOK

Power MOSFETs



Power MOSFETs

Harris Semiconductor offers an extensive line of power MOSFET products for use in a wide range of consumer, industrial, and high-reliability applications. This Data Book contains detailed technical information on the broad line of more than 850 power MOSFETs, including standard power MOSFETs (the popular RF-series types, the IRF-series of industry replacement types, and JEDEC types), MegaFETs, logic-level power MOSFETs (L^2FETs), ruggedized power MOSFETs, IGBT/COMFETs (conductivity-modulated FETs), advanced discrete, high-reliability power MOSFETs, and radiation-hardened MOSFETs.

The Data Book is divided into fourteen major sections. The first section includes a complete index to types and industry replacement guides. Brief profiles of the various product categories are then presented.

Separate data sections provide definitive ratings and characteristics for each major category of devices. Within each section, data pages for individual devices are included, as nearly as possible, in alpha-numerical sequence. Because some devices are grouped together to show similarity of function or data, some individual type numbers may be out of sequence. If you don't find the type number that you are looking for where you expect it to be, check the **Index to Devices.**

The Data Book also includes dimensional outlines of the various packages used and application notes on **Harris Semiconductor** power MOSFETs.

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RFP15N06	3-424	1478
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2N6661	RFL1N10
2N6755	2N6755
2N6756	2N6756
2N6757	2N6757
2N6758	2N6758
2N6759	2N6759
2N6760	2N6760
2N6751	2N6761
2N6762	2N6762
2N6763	2N6763
2N6764	2N6764
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2N6767	2N6767
2N6768	2N6768
2N6769	2N6769
2N6770	2N6770
2N6782	2N6782
2N6784	2N6784
2N6786	2N6782
2N6788	2N6788
2N6790	2N6790
2N6792	2N6792
2N6794	2N6794
2N6796	2N6796
2N6798	2N6798
2N6800	2N6800
2N6802	2N6802
2SJ101	RFP12P08
2SJ102	RFP12P08
2SJ112	2N6898
2SJ113	RFH25P10
2SJ127	RFP10P12
2SK294	IRF522
2SK295	IRF522
2SK296	IRF723
2SK308	RFM10N12
2SK310	IRF732
2SK311	RFM3N45
2SK312	IRF453
2SK313	IRF453
2SK319	IRF730
2SK345	IRF521
2SK346	IRF521
2SK349	RFH10N45
2SK382	RFP3N50
2SK383	RFP15N12
2SK398	RFM12N10
2SK401	IRF351
2SK408	RFP2N18
2SK409	RFP2N18
2SK412	RFH12N35
2SK428	RFP15N06
2SK440	IRF630
2SK512	IRF450
2SK549	RFP15N06
2SK550	RFP25N06
2SK551	RFP15N12
2SK552	RFP6N45
2SK553	RFP6N45
2SK556	RFH10N45
2SK557	RFH10N50
2SK558	RFHI0N50
2SK561	RFM25N06
BSR80	RFP4N05
BSR81	IRF513
BSR82	RFP2N08
BSS93	IRFF212

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BUP60	RFM7N35
BUP61	IRF331
BUP62	RFM7N40
BUP63	IRF330
BUP64	RFM6N45
BUP65	IRF431
BUP66	RFM6N50
BUP67	IRF430
BUP68	RFM7N35
BUP69	RFM7N40
BUP70	RFM6N45
BUP71	RFM6N50
BUZ10	RFP25N05
BUZ10B	IRF533
BUZ11A	RFP25N05
BUZ14	RFK45N05
BUZ14A	IRF153
BUZ14C	IRF131
BUZ14D	IRF133
BUZ15	RFK45N05
BUZ17	RFK45N05
BUZ20	RFP12N10
BUZ20A	IRF532
BUZ20B	IRF520
BUZ21	RFP18N10
BUZ23	RFM12N10
BUZ23A	IRF130
BUZ23B	IRF152
BUZ24	RFK35N10
BUZ25	RFM18N10
BUZ30	IRF632
BUZ32	IRF630
BUZ32A	IRF631
BUZ32B	IRF632
BUZ32C	IRF633
BUZ33	IRF220
BUZ33A	IRF232
BUZ33B	IRF233
BUZ34	IRF240
BUZ35	IRF230
BUZ35A	IRF231
BUZ36	IRF240
BUZ40	IRF822
BUZ41A	IRF830
BUZ41B	IRF431
BUZ42	IRF832
BUZ42A	IRF833
BUZ42B	IRF820
BUZ42C	IRF821
BUZ42D	IRF822
BUZ43	IRF422
BUZ44A	IRF430
BUZ44B	IRF831
BUZ45	RFM10N50
BUZ45A	RFM10N50
BUZ45B	IRF452
BUZ46	IRF432
BUZ46A	IRF433
BUZ46B	IRF821
BUZ60	IRF730
BUZ60A	IRF731
BUZ60B	IRF732
BUZ60C	IRF733
BUZ60D	IRF720
BUZ63	IRF330
BUZ63A	IRF331
BUZ63B	IRF332
BUZ63C	IRF333
BUZ63D	IRF730

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BUZ64	IRF352
BUZ67	IRF352
BUZ71	RFP25N05
BUZ71A	RFP25N05
BUZ72	RFP12N10
BUZ72A	IRF532
BUZ73	IRF630
BUZ73A	IRF632
BUZ74	IRF820
BUZ74A	IRF822
BUZ76	IRF720
BUZ76A	IRF732
BUZ201	IRF352
BUZ210	RFM10N50
BUZ211	RFM10N50
BUZ351	RFH12N40
BUZ353	RFH10N50
BUZ354	RFH10N50
D82AK2	IRFD1Z1
D82AL2	IRFD1Z0
D82AM2	IRFD2Z1
D82AN2	IRFD2Z0
D84BK1	IRF511
D84BK2	IRF511
D84BL1	IRF510
D84BL2	IRF510
D84BM1	IRF611
D84BM2	IRF611
D84BN1	IRF610
D84BN2	IRF610
D84BQ1	IRF723
D84BQ2	IRF722
D84CK1	IRF521
D84CK2	IRF521
D84CL1	IRF520
D84CL2	IRF520
D84CM1	IRF621
D84CM2	IRF621
D84CN1	IRF620
D84CN2	IRF620
D84CQ1	IRF721
D84CQ2	IRF720
D84CR1	IRF821
D84CR2	IRF820
D84DK1	IRF531
D84DK2	IRF531
D84DL1	IRF530
D84DL2	IRF530
D84DM1	IRF631
D84DM2	IRF631
D84DN1	IRF630
D84DN2	IRF630
D84DQ1	IRF731
D84DQ2	IRF730
D84DR1	IRF831
D84DR2	IRF830
D84EM1	IRF641
D84EM2	IRF641
D86DK1	IRF131
D86DK2	IRF131
D86DL1	IRF130
D86DL2	IRF130
D86DM1	RFM10N12
D86DM2	IRF631
D86DN1	IRF230
D86DN2	IRF230
D86DQ1	IRF331
D86DQ2	IRF330
D86DR1	IRF431
D86DR2	IRF430

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D86EM2	IRF241
D86EN1	IRF240
D86EN2	IRF240
D86FK1	RFK45N05
D86FK2	RFK45N06
D86FL1	RFK35N08
D86FL2	IRF150
D86FM1	IRF251
D86FM2	IRF251
D86FN1	IRF250
D86FN2	IRF250
D86FQ1	IRF351
D86FQ2	IRF350
D86FR1	IRF451
D86FR2	IRF450
D88FK1	IRFP151
D88FK2	IRFP151
D88FL1	IRFP150
D88FL2	IRFP150
D88FM1	IRFP251
D88FM2	IRFP251
D88FN1	IRFP250
D88FN2	IRFP250
D88FQ1	IRFP351
D88FQ2	IRFP350
D88FR1	IRFP451
D88FR2	IRFP450
GF2A10	IRFD110R
GF2A13	IRFD120R
GF2B06	IRFD210R
GF2B08	IRFD220R
GF2D04	IRFD310R
GF2D05	IRFD320R
GF4A4	IRF510R
GF4A8	IRF520R
GF4A14	IRF530R
GF4A27	IRF540R
GF4B2	IRF610R
GF4B5	IRF620R
GF4B9	IRF630R
GF4B18	IRF640R
GF4D1	IRF710R
GF4D3	IRF720R
GF4D5	IRF730R
GF4D10	IRF740R
GF4E2	IRF820R
GF4E4	IRF830R
GF4E8	IRF840R
GF6A14	IRF130R
GF6A27	IRF140R
GF6A40	IRF150R
GF6B9	IRF230R
GF6B18	IRF240R
GF6B30	IRF250R
GF6D5	IRF330R
GF6D10	IRF340R
GF6D15	IRF350R
GF6E4	IRF430R
GF6E8	IRF440R
GF6E13	IRF450R
GF8A40	IRFP150R
GF8B30	IRFP250R
GF8D15	IRFP350R
GF8E13	IRFP450R
GF14A35	IRFF110R
GF14A60	IRFF120R
GF14A80	IRFF130R
GF14B22	IRFF210R
GF14B35	IRFF220R

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GF14B55	IRFF230R
GF14D14	IRFF310R
GF14D25	IRFF320R
GF14D35	IRFF330R
GF14E16	IRFF420R
GF14E28	IRFF430R
IRF120	IRF120
IRF121	IRF121
IRF122	IRF122
IRF123	IRF123
IRF130	IRF130
IRF131	IRF131
IRF132	IRF132
IRF133	IRF133
IRF150	IRF150
IRF151	IRF151
IRF152	IRF152
IRF153	IRF153
IRF220	IRF220
IRF221	IRF221
IRF222	IRF222
IRF223	IRF223
IRF230	IRF230
IRF231	IRF231
IRF232	IRF232
IRF233	IRF233
IRF240	IRF240
IRF241	IRF241
IRF243	IRF243
IRF250	IRF250
IRF251	IRF251
IRF252	IRF252
IRF253	IRF253
IRF320	IRF320
IRF321	IRF321
IRF322	IRF322
IRF323	IRF323
IRF330	IRF330
IRF331	IRF331
IRF332	IRF332
IRF333	IRF333
IRF350	IRF350
IRF351	IRF351
IRF352	IRF352
IRF353	IRF353
IRF420	IRF420
IRF421	IRF421
IRF422	IRF422
IRF423	IRF423
IRF430	IRF430
IRF431	IRF431
IRF432	IRF432
IRF433	IRF433
IRF450	IRF450
IRF451	IRF451
IRF452	IRF452
IRF453	IRF453
IRF510	IRF510
IRF511	IRF511
IRF512	IRF512
IRF513	IRF513
IRF520	IRF520
IRF521	IRF521
IRF522	IRF522
IRF523	IRF523
IRF530	IRF530
IRF531	IRF531
IRF532	IRF532
IRF533	IRF533
IRF610	IRF610

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IRF611	IRF611
IRF612	IRF612
IRF613	IRF613
IRF620	IRF620
IRF621	IRF621
IRF622	IRF622
IRF623	IRF623
IRF630	IRF630
IRF631	IRF631
IRF632	IRF632
IRF633	IRF633
IRF641	IRF641
IRF643	IRF643
IRF710	IRF722
IRF711	IRF723
IRF712	IRF722
IRF713	IRF722
IRF720	IRF720
IRF721	IRF721
IRF722	IRF722
IRF723	IRF723
IRF730	IRF730
IRF731	IRF731
IRF732	IRF732
IRF733	IRF733
IRF820	IRF820
IRF821	IRF821
IRF822	IRF822
IRF823	IRF823
IRF830	IRF830
IRF831	IRF831
IRF832	IRF832
IRF833	IRF833
IRF9130	RFM12P10
IRF9131	RFM12P08
IRF9132	RFM8P10
IRF9133	RFM8P08
IRF9140	RFK25P10
IRF9141	RFK25P08
IRF9142	RFM12P10
IRF9143	RFM12P08
IRF9231	RFM10P15
IRF9233	RFM5P15
IRF9241	RFM10P15
IRF9242	RFM10P15
IRF9510	RFP5P12
IRF9511	RFP5P12
IRF9512	RFP5P12
IRF9513	RFD5P12
IRF9520	RFP6P10
IRF9521	RFP6P08
IRF9522	RFP6P10
IRF9523	RFP6P08
IRF9530	RFP12P10
IRF9531	RFP12P08
IRF9532	RFP8P10
IRF9533	RFP8P08
IRF9542	RFP12P10
IRF9543	RFP12P08
IRF9611	RFP5P15
IRF9613	RFP5P15
IRF9621	RFP6P08
IRF9623	RFP6P08
IRF9631	RFP12P08
IRF9633	RFP12P08
IRF9641	RFP10P15
IRF9643	RFP10P15
IRFD1Z0	IRFD1Z0
IRFD1Z1	IRFD1Z1
IRFD1Z2	IRFD1Z2

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INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
IRFD1Z3	IRFD1Z3
IRFF110	IRFF110
IRFF111	IRFF111
IRFF112	IRFF112
IRFF113	IRFF113
IRFF120	IRFF120
IRFF121	IRFF121
IRFF122	IRFF122
IRFF123	IRFF123
IRFF130	IRFF130
IRFF131	IRFF131
IRFF132	IRFF132
IRFF133	IRFF133
IRFF210	IRFF210
IRFF211	IRFF211
IRFF212	IRFF212
IRFF213	IRFF213
IRFF220	IRFF220
IRFF221	IRFF221
IRFF222	IRFF222
IRFF223	IRFF223
IRFF230	IRFF230
IRFF231	IRFF231
IRFF232	IRFF232
IRFF233	IRFF233
IRFF320	IRFF320
IRFF321	IRFF321
IRFF322	IRFF322
IRFF323	IRFF323
IRFF330	IRFF330
IRFF331	IRFF331
IRFF332	IRFF332
IRFF333	IRFF333
IRFF420	IRFF420
IRFF421	IRFF421
IRFF422	IRFF422
IRFF423	IRFF423
IRFF430	IRFF430
IRFF431	IRFF431
IRFF432	IRFF432
IRFF433	IRFF433
IRFZ20	RFP25N05
IRFZ22	RFP25N05
IRFZ32	RFP25N05
IVN5000TND	RFL2N05
IVN5000TNE	RFL2N06
IVN5000TNF	RFL1N08
IVN5000TNH	RFL1N10
IVN5000SND	RFL2N05
IVN5000SNE	RFL2N06
IVN5000SNF	RFL1N08
IVN5000SNH	RFL1N10
IVN5001TND	RFL2N05
IVN5001TNE	RFL2N06
IVN5001TNF	RFL1N08
IVN5001TNH	RFL1N10
IVN5001SND	RFL2N05
IVN5001SNE	RFL2N06
IVN5001SNF	RFL1N08
IVN5001SNH	RFL1N10
IVN5200HND	IRF523
IVN5200HNE	IRF523
IVN5200HNF	IRF522
IVN5200HNH	IRF522
IVN5200KND	IRF123
IVN5200KNE	IRF123
IVN5200KNF	IRF122
IVN5200KNH	IRF122
IVN5200TND	IRFF123
IVN5200TNE	IRFF123

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
IVN5200TNF	IRFF122
IVN5200TNH	IRFF122
IVN5201CND	IRF523
IVN5201CNE	IRF523
IVN5201CNF	IRF522
IVN5201CNH	IRF522
IVN5201KND	IRF123
IVN5201KNE	IRF123
IVN5201KNF	IRF122
IVN5201KNH	IRF122
IVN5201TND	IRFF123
IVN5201TNE	IRFF123
IVN5201TNF	IRFF122
IVN5201TNH	IRFF122
IVN6000CNE	IRF523
IVN6000CNF	IRF522
IVN6000CNH	IRF522
IVN6000CNR	IRF722
IVN6000CNS	IRF722
IVN6000CNT	IRF821
IVN6000CNU	IRF822
IVN6000KNE	IRF123
IVN6000KNF	IRF122
IVN6000KNH	IRF122
IVN6000KNR	IRF322
IVN6000KNS	IRF322
IVN6000KNT	IRF421
IVN6000KNU	IRF422
IVN6000TNE	IRFF113
IVN6000TNF	IRFF112
IVN6000TNH	IRFF112
IVN6000TNR	IRFF322
IVN6000TNS	IRFF322
IVN6000TNT	IRFF423
IVN6000TNU	IRFF422
IVN6001CNE	IRF523
IVN6001CNF	IRF522
IVN6001CNH	IRF522
IVN6001KNE	IRF123
IVN6001KNF	IRF122
IVN6001KNH	IRF122
IVN6001TNE	IRFF113
IVN6001TNF	IRFF112
IVN6001TNH	IRFF112
IVN6002CND	IRF523
IVN6002KND	IRF123
IVN6002TND	IRFF113
IVN6100TNS	IRFF312
IVN6100TNT	IRFF423
IVN6100TNU	IRFF423
IVN6200ANE	IRF531
IVN6200ANF	RFP12N08
IVN6200ANH	RFP12N10
IVN6200ANM	RFP8N20
IVN6200ANP	RFP8N20
IVN6200ANS	IRF732
IVN6200ANT	IRF831
INV6200ANU	IRF830
IVN6200CND	IRF521
IVN6200CNE	IRF533
IVN6200CNF	IRF532
IVN6200CNH	IRF532
IVN6200CNM	RFP8N20
IVN6200CNP	RFP8N20
IVN6200CNR	RFP4N40
IVN6200CNS	IRF730
IVN6200CNT	IRF831
IVN6200CNU	IRF831
IVN6200KNE	IRF133
IVN6200KNF	IRF132

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
IVN6200KNH	IRF132
IVN6200KNM	RFM8N20
IVN6200KNP	IRF353
IVN6200KNR	RFM4N40
IVN6200KNS	IRF332
IVN6200KNT	IRF431
IVN6200KNU	IRF432
IVN6300SNE	RFL2N06
IVN6300SNF	RFL1N08
IVN6300SNH	RFL1N10
IVN6300SNM	RFL1N20
IVN6300SNP	IRFF313
IVN6300SNS	IRFF312
IVN6300SNT	IRFF423
IVN6300SNU	IRFF422
IVN6660	RFL1N08
IVN6661	RFL1N08
MTH7N45	RFH10N45
MTH7N50	RFH10N50
MTH8N35	RFH12N35
MTH8N40	RFH12N40
MTH15N12	IRF251
MTH15N15	IRF251
MTH15N18	RFH25N18
MTH15N20	RFH25N20
MTH25N08	RFK35N08
MTH25N10	RFH35N10
MTM2N45	RFM3N45
MTM2N50	RFM3N50
MTM3N35	RFM4N35
MTM3N40	RFM4N40
MTM4N45	2N6762
MTM4N50	2N6762
MTM5N18	RFM8N18
MTM5N20	RFM8N20
MTM5N35	IRF330
MTM5N40	IRF330
MTM7N12	RFM8N18
MTM7N15	RFM8N18
MTM7N18	IRF232
MTM7N20	RFM8N20
MTM7N45	RFM10N45
MTM7N50	RFM10N50
MTM8N08	2N6757
MTM8N10	2N6758
MTM8N12	2N6757
MTM8N15	2N6757
MTM8N18	RFM8N18
MTM8N20	RFM8N20
MTM10N05	RFM15N05
MTM10N06	RFM15N06
MTM10N08	RFM12N08
MTM10N10	RFM12N10
MTM10N12	RFM10N12
MTM10N15	RFM10N15
MTM12N05	RFM15N05
MTM12N06	RFM15N06
MTM12N08	RFM12N08
MTM12N10	RFM12N10
MTM12N12	IRF230
MTM12N15	IRF230
MTM12N18	RFM12N18
MTM12N20	RFM12N20
MTM15N05	RFM15N05
MTM15N06	RFM15N06
MTM15N12	RFM15N12
MTM15N15	RFM15N15
MTM15N18	RFK25N18
MTM15N20	RFK25N20
MTM15N35	RFM12N35

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INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
MTM15N40	RFM12N40
MTM15N45	IRF450
MTM15N50	IRF451
MTM20N08	RFM18N08
MTM20N10	RFM18N10
MTM20N12	RFK30N12
MTM20N15	RFK30N15
MTM25N05	RFM25N05
MTM25N06	RFM25N06
MTM25N08	RFK35N08
MTM25N10	RFK35N10
MTM35N05	RFK45N05
MTM35N06	RFK45N06
MTM40N18	IRF250
MTM40N20	IRF250
MTM45N12	RFK30N12
MTM45N15	RFK30N15
MTM8P08	RFM8P08
MTM8P10	RFM8P10
MTP1N45	RFP3N45
MTP1N50	RFP3N50
MTP2N18	RFP2N18
MTP2N20	RFP2N20
MTP2N25	IRF721
MTP2N35	RFP4N35
MTP2N40	RFP4N40
MTP2N45	RFP3N45
MTP2N50	RFP3N50
MTP3N12	IRF623
MTP3N15	IRF623
MTP3N35	RFP3N45
MTP3N40	RFP3N50
MTP4N08	IRF510
MTP4N10	IRF510
MTP4N45	RFP6N45
MTP4N50	RFP6N50
MTP5N05	RFP6P08
MTP5N06	RFP6P08
MTP5N18	RFP8N18
MTP5N20	RFP8N20
MTP5N35	RFP7N35
MTP5N40	RFP7N40
MTP7N12	RFP8N18
MTP7N15	RFP8N18
MTP7N18	RFP8N18
MTP7N20	RFP8N20
MTP8N08	RFP8N18
MTP8N10	RFP8N18
MTP8N12	RFP10N12
MTP8N15	RFP10N15
MTP8N18	RFP8N18
MTP8N20	RFP8N20
MTP10N05	RFP15N05
MTP10N06	RFP15N06
MTP10N08	RFP12N08
MTP10N10	RFP12N10
MTP10N12	RFP10N12
MTP10N15	RFP10N15
MTP12N05	RFP15N05
MTP12N06	RFP15N06
MTP12N08	RFP12N08
MTP12N10	RFP12N10
MTP12N18	RFP12N18
MTP12N20	RFP12N20
MTP15N05	RFP15N05
MTP15N06	RFP15N06
MTP15N12	RFP15N12
MTP15N15	RFP15N15
MTP20N08	RFP18N08
MTP25N05	RFP25N05

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
MTP25N06	RFP25N06
MTP8P08	RFP8P08
MTP8P10	RFP8P10
NOS100B	RFL1N15
NOS101B	RFL1N12
NOS102B	RFL1N08
PA40N200LM	IRF131
PA40N200LT	IRF531
PA40N200SM	IRF131
PA40N200ST	IRF531
PA40N280LM	IRF132
PA40N280LT	IRF532
PA40N280SM	IRF132
PA40N280ST	IRF532
PA40N300LM	IRF121
PA40N300LT	IRF521
PA40N300SM	IRF121
PA40N300ST	IRF521
PA75N150LM	RFM15N06
PA75N150LT	RFP15N06
PA75N150SM	RFM15N06
PA75N150ST	RFP15N06
PA125N40LM	RFK45N06
PA125N40LP	RFK45N06
PA125N40SM	RFK45N06
PA125N60LM	RFH45N06
PA125N60LP	RFH45N06
PA125N60SM	RFK45N06
PA125N60SP	RFH45N06
PB40N400LM	IRF122
PB40N400LT	IRF522
PB40N400SM	IRF122
PB40N400ST	IRF522
PB75N180LM	IRF130
PB75N180LT	IRF530
PB75N180SM	IRF130
PB75N180ST	IRF530
PB125N60LM	IRF150
PB125N60LP	RFH35N10
PB125N60SM	IRF150
PB125N60SP	RFH35N10
PB125N80LM	IRF152
PB125N80LP	RFH35N10
PB125N80SM	IRF152
PB125N80SP	RFH35N10
PC40N500LM	IRF231
PC40N500LT	IRF631
PC40N500SM	IRF231
PC40N500ST	IRF631
PC40N800LM	IRF221
PC40N800LT	IRF621
PC40N800SM	IRF221
PC40N800ST	IRF621
PC75N250LM	IRF243
PC75N250LT	IRF643
PC75N250SM	IRF243
PC75N250ST	IRF643
PC75N400LM	IRF231
PC75N400LT	IRF631
PC75N400SM	IRF231
PC75N400ST	IRF631
PC125N130LM	IRF253
PC125N130LP	RFH30N15
PC125N130SM	IRF253
PC125N130SP	RFH30N15
PC125N180LM	IRF241
PC125N180LP	RFH30N15
PC125N180LT	IRF641
PC125N180SM	IRF241
PC125N180SP	RFH30N15

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
PM509P	IRF523
PM510P	IRF521
PM512M	IRF131
PM512P	IRF531
PM604P	IRF511
PM605P	IRF523
PM608M	IRF121
PM608P	IRF521
PM609P	IRF521
PM610P	IRF521
PM612M	IRF131
PM612P	IRF531
PM614M	IRF131
PM614P	IRF531
PM804P	IRF510
PM805P	IRF522
PM808M	RFM12N08
PM808P	RFP12N08
PM814M	IRF131
PM814P	IRF531
PM1003P	IRF512
PM1004P	IRF510
PM1006M	IRF122
PM1006P	IRF522
PM1010M	RFM12N10
PM1010P	RFP12N10
PM1203P	IRF621
PM1204P	IRF631
PM1206M	RFM10N12
PM1206P	RFP10N12
PM1210M	RFM15N12
PM1210P	RFP15N12
PM1503P	IRF623
PM1504P	IRF623
PM1506M	IRF631
PM1506P	IRF231
PM1510M	RFM10N15
PM1510P	RFP10N15
SEF120	IRF120
SEF121	IRF121
SEF122	IRF122
SEF123	IRF123
SEF130	IRF130
SEF131	IRF131
SEF132	IRF132
SEF133	IRF133
SEF150	IRF150
SEF151	IRF151
SEF152	IRF152
SEF153	IRF153
SEF220	IRF220
SEF221	IRF221
SEF222	IRF222
SEF223	IRF223
SEF230	IRF230
SEF231	IRF231
SEF232	IRF232
SEF233	IRF233
SEF240	IRF240
SEF241	IRF241
SEF243	IRF243
SEF320	IRF320
SEF321	IRF321
SEF322	IRF322
SEF323	IRF323
SEF330	IRF330
SEF331	IRF331
SEF332	IRF332
SEF333	IRF333
SEF420	IRF420

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INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
SEF421	IRF421
SEF422	IRF422
SEF423	IRF423
SEF430	IRF430
SEF431	IRF431
SEF432	IRF432
SEF433	IRF433
SEF510	IRF510
SEF511	IRF511
SEF512	IRF512
SEF513	IRF513
SEF520	IRF520
SEF521	IRF521
SEF522	IRF522
SEF523	IRF523
SEF530	IRF530
SEF531	IRF531
SEF532	IRF532
SEF533	IRF533
SEF620	IRF620
SEF621	IRF621
SEF622	IRF620
SEF623	IRF623
SEF630	IRF620
SEF631	IRF631
SEF632	IRF632
SEF633	IRF633
SEF710	IRF722
SEF711	IRF723
SEF712	IRF722
SEF713	IRF722
SEF720	IRF720
SEF721	IRF721
SEF722	IRF722
SEF723	IRF723
SEF730	IRF730
SEF731	IRF731
SEF732	IRF732
SEF733	IRF733
SEF820	IRF820
SEF821	IRF821
SEF822	IRF822
SEF823	IRF823
SEF830	IRF830
SEF831	IRF831
SEF832	IRF832
SEF833	IRF833
SEFF120	IRFF120
SEFF121	IRFF121
SEFF122	IRFF122
SEFF123	IRFF123
SEFH7N45	RFH10N45
SEFH7N50	RFH10N50
SEFH8N35	RFH12N35
SEFH8N40	RFH12N40
SEFH15N18	RFH25N18
SEFH15N20	RFH25N20
SEFH25N08	RFH35N08
SEFH25N10	RFH35N10
SEFH35N05	RFH45N05
SEFH35N06	RFH45N06
SEFM2N45	IRF423
SEFM3N35	IRF323
SEFM3N40	IRF322
SEFM4N45	IRF431
SEFM4N50	IRF430
SEFM5N18	RFM8N18
SEFM5N20	RFM8N20
SEFM5N35	RFM7N35
SEFM5N40	RFM7N40

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
SEFM7N45	RFK10N45
SEFM7N50	RFK10N50
SEFM8N18	IRF230
SEFM8N20	IRF230
SEFM10N05	IRF133
SEFM10N06	IRF133
SEFM10N08	IRF120
SEFM10N10	IRF120
SEFM12N05	IRF131
SEFM12N06	IRF131
SEFM12N08	RFM12N08
SEFM12N10	RFM12N10
SEFM15N05	RFM15N05
SEFM15N06	RFM15N06
SEFM15N18	RFK25N18
SEFM15N20	RFK25N20
SEFM25N05	RFM25N05
SEFM25N06	RFM25N06
SEFM25N08	RFK35N08
SEFM25N10	RFK35N10
SEFM35N05	FRK45N05
SEFM35N06	RFK45N06
SEFP2N45	IRF823
SEFP3N35	IRF323
SEFP3N40	IRF322
SEFP4N45	IRF831
SEFP4N50	IRF830
SEFP5N05	IRF123
SEFP5N06	IRF123
SEFP5N18	RFP8N18
SEFP5N20	RFP8N20
SEFP5N35	IRF331
SEFP5N40	IRF330
SEFP8N18	RFP12N18
SEFP8N20	RFP12N10
SEFP10N05	IRF133
SEFP10N06	IRF133
SEFP10N08	RFP12N08
SEFP10N10	RFP12N10
SEFP12N05	RFP15N05
SEFP12N06	RFP15N06
SEFP12N08	RFP12N08
SEFP12N10	RFP12N10
SEFP15N05	RFP15N05
SEFP15N06	RFP15N06
SEFP25N05	RFP25N05
SEFP25N06	RFP25N06
SGSP101	IRFF110
SGSP102	RFL1N08
SGSP111	IRFF120
SGSP112	IRFF120
SGSP116	IRFF230
SGSP117	IRFF330
SGSP119	IRFF430
SGSP121	IRFF131
SGSP122	IRFF131
SGSP130	IRFF421
SGSP131	IRFF322
SGSP132	IRFF323
SGSP139	IRFF420
SGSP151	IRFF122
SGSP152	IRFF122
SGSP154	IRFF423
SGSP157	IRFF121
SGSP158	IRFF121
SGSP301	RFP2N10
SGSP302	RFP2N10
SGSP311	IRF520
SGSP312	IRF520
SGSP316	IRF723

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
SGSP317	IRF632
SGSP319	IRF820
SGSP321	RFP15N06
SGSP322	RFP15N05
SGSP330	IRF821
SGSP331	IRF722
SGSP332	IRF723
SGSP351	IRF522
SGSP352	IRF522
SGSP354	IRF823
SGSP357	IRF521
SGSP358	IRF521
SGSP361	RFP15N05
SGSP362	RFP18N08
SGSP364	IRF831
SGSP365	IRF730
SGSP366	IRF731
SGSP367	RFP12N20
SGSP369	IRF830
SGSP381	RFP25N06
SGSP382	RFP25N05
SGSP422	RFH45N08
SGSP461	RFH35N10
SGS462	RFH35N08
SGSP463	RFH12N35
SGSP464	RFH10N45
SGSP465	RFH12N40
SGSP466	RFH12N35
SGSP467	RFH12N35
SGSP469	RFH10N50
SGSP471	RFH35N10
SGSP472	RFH35N08
SGSP474	RFH10N45
SGSP475	RFH12N40
SGSP476	RFH12N35
SGSP477	RFH25N20
SGSP479	RFH10N50
SGSP481	RFH35N08
SGSP482	RFH35N08
SGSP491	RFH45N06
SGSP492	RFH45N05
SGSP511	IRF120
SGSP512	IRF120
SGSP516	IRF331
SGSP517	IRF232
SGSP519	IRF420
SGSP530	IRF421
SGSP531	IRF322
SGSP532	IRF323
SGSP561	RFM18N10
SGSP562	RFM18N08
SGSP563	IRF353
SGSP564	IRF431
SGSP565	IRF330
SGSP566	IRF331
SGSP567	RFM12N20
SGSP569	IRF430
SGSP571	RFK35N10
SGSP572	RFK35N08
SGSP573	IRF351
SGSP574	RFM10N45
SGSP577	RFH25N20
SGSP579	RFM10N50
SGSP581	RFK45N06
SGSP582	RFK45N05
SGSP591	RFK45N06
SGSP592	RFK45N05
TN0106N2	RFL1N08
TN0110N2	RFL1N10
TN0520N2	RFL1N20

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INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
UNF120	IRF120
UNF121	IRF121
UNF122	IRF122
UNF123	IRF123
UNF130	IRF130
UNF131	IRF131
UNF132	IRF132
UNF133	IRF133
UNF150	IRF150
UNF151	IRF151
UNF152	IRF152
UNF153	IRF153
UNF220	IRF220
UNF221	IRF221
UNF222	IRF222
UNF223	IRF223
UFN230	IRF230
UFN231	IRF231
UNF232	IRF232
UFN233	IRF233
UFN240	IRF240
UFN241	IRF241
UFN243	IRF243
UFN250	IRF250
UFN251	IRF251
UFN252	IRF252
UFN253	IRF253
UFN320	IRF320
UFN321	IRF321
UFN322	IRF322
UFN323	IRF323
UFN330	IRF330
UFN331	IRF331
UFN332	IRF332
UFN333	IRF333
UFN350	IRF350
UFN351	IRF351
UFN352	IRF352
UFN353	IRF353
UFN420	IRF420
UFN421	IRF421
UFN422	IRF422
UFN423	IRF423
UFN430	IRF430
UFN431	IRF431
UFN432	IRF432
UFN433	IRF433
UFN450	IRF450
UFN451	IRF451
UFN452	IRF452
UFN453	IRF453
UFN510	IRF510
UFN511	IRF511
UFN512	IRF512
UFN513	IRF513
UFN520	IRF520
UFN521	IRF521
UFN522	IRF522
UFN523	IRF523
UFN530	IRF530
UFN531	IRF531
UFN532	IRF532
UFN533	IRF533
UFN610	IRF610
UFN611	IRF611
UFN612	IRF612
UFN613	IRF613
UFN620	IRF620
UFN621	IRF621
UFN622	IRF622

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
UFN623	IRF623
UFN630	IRF630
UFN631	IRF631
UFN632	IRF632
UFN633	IRF633
UFN641	IRF641
UFN643	IRF643
UFN710	IRF722
UFN711	IRF723
UFN712	IRF722
UFN713	IRF723
UFN720	IRF720
UFN721	IRF721
UFN722	IRF722
UNF723	IRF723
UFN730	IRF730
UFN731	IRF731
UFN732	IRF732
UFN733	IRF733
UFN820	IRF820
UFN821	IRF821
UFN822	IRF822
UFN823	IRF823
UFN830	IRF830
UFN831	IRF831
UFN832	IRF832
UFN833	IRF833
UFNF432	IRFF432
UFNF433	IRFF433
UFNF110	IRFF110
UFNF111	IRFF111
UFNF112	IRFF112
UFNF113	IRFF113
UFNF120	IRFF120
UFNF121	IRFF121
UFNF122	IRFF122
UFNF123	IRFF123
UFNF130	IRFF130
UFNF131	IRFF131
UFNF132	IRFF132
UFNF133	IRFF133
UFNF210	IRFF210
UFNF211	IRFF211
UFNF212	IRFF212
UFNF213	IRFF213
UFNF220	IRFF220
UFNF221	IRFF221
UFNF222	IRFF222
UFNF223	IRFF223
UFNF230	IRFF230
UFNF231	IRFF231
UFNF232	IRFF232
UFNF233	IRFF233
UFNF320	IRFF320
UFNF321	IRFF321
UFNF322	IRFF322
UFNF323	IRFF323
UFNF330	IRFF330
UFNF331	IRFF331
UFNF332	IRFF332
UFNF333	IRFF333
UFNF420	IRFF420
UFNF421	IRFF421
UFNF422	IRFF422
UFNF423	IRFF423
UFNF430	IRFF430
UFNF431	IRFF431
UFNF432	IRFF432
UFNF433	IRFF433
VM1210N1	RFM12N10

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
VN10KE	IRFF113
VN30AB	RFL2N05
VN35AA	IRF513
VN35AB	RFL2N05
VN35AK	RFL2N05
VN40AD	IRF513
VN46AD	IRF513
VN64GA	IRF133
VN66AD	IRF513
VN66AK	RFL2N06
VN67AA	IRF513
VN67AB	RFL2N06
VN67AD	IRF513
VN67AK	RFL2N06
VN88AD	IRF510
VN89AB	RFL1N08
VN89AD	IRF512
VN90AA	IRF512
VN90AB	RFL1N10
VN98AK	RFL1N10
VN99AA	IRF512
VN99AK	RFL1N10
VN0104N2	RFL1N08
VN0104N5	IRF513
VN0106N2	RFL1N08
VN0106N5	IRF513
VN0109N2	RFL1N10
VN0109N4	IRFF112
VN0109N5	RFP2N10
VN0110N2	IRFF112
VN0110N5	IRF512
VN0114N2	IRFF223
VN0114N5	IRF611
VN0116N2	RFL1N18
VN0116N5	RFP2N18
VN0120N2	RFL1N20
VN0120N5	RFP2N20
VN0204N2	RFL2N05
VN0204N5	IRF513
VN0206N2	RFL2N06
VN0206N5	IRF513
VN0210N2	RFL1N10
VN0210N5	IRF512
VN0215N2	IRFF231
VN0215N5	IRF633
VN0216N2	RFL1N18
VN0216N5	RFP2N18
VN0220N2	RFL1N20
VN0220N5	RFP2N20
VN0300B	RFL2N05
VN0300D	RFP4N05
VN0330N1	IRF353
VN0330N2	IRFF331
VN0335N1	IRF323
VN0335N2	IRFF323
VN0335N5	IRF723
VN0340N1	IRF320
VN0340N2	IRFF322
VN0340N5	IRF322
VN0345N1	IRF421
VN0345N2	IRFF423
VN0345N5	IRF823
VN0350N1	IRF420
VN0350N2	IRFF422
VN0350N5	IRF822
VN0400A	RFM15N05
VN0400D	RFP15N05
VN0401A	RFM15N05
VN0401D	RFP15N05
VN0430N1	IRF351

Industry Replacement Guide

Power MOSFETs

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
VN0435N1	IRF351
VN0440N1	IRF350
VN0445N1	IRF451
VN0450N1	IRF450
VN0545N2	IRFF423
VN0600A	RFM25N06
VN0600D	RFP25N06
VN0601A	RFM15N06
VN0601D	RFP15N06
VN0800A	RFM18N08
VN0800D	RFP18N08
VN0801A	RFM12N08
VN0801D	RFP12N08
VN1000A	IRF130
VN1000D	IRF530
VN1001A	IRF132
VN1001D	IRF532
VN1106N1	IRF121
VN1106N2	IRFF111
VN1106N5	IRF511
VN1110N1	IRF122
VN1110N2	IRFF130
VN1110N5	IRF522
VN1116N1	IRF222
VN1116N2	IRFF222
VN1116N5	IRF613
VN1120N1	IRF222
VN1120N2	IRFF212
VN1120N5	IRF612
VN1156N1	IRF231
VN1156N2	IRFF231
VN1156N5	IRF631
VN1200A	RFM15N12
VN1200D	RPF15N12
VN1201A	RFM15N12
VN1201D	RFP15N12
VN1204N1	IRF121
VN1204N2	IRFF121
VN1204N5	IRF521
VN1206B	RFL1N12
VN1206D	RFP2N12
VN1206N1	IRF121
VN1206N2	IRFF121
VN1206N3	IRF521
VN1210N2	IRFF120
VN1210N5	IRF520
VN1215N1	IRF241
VN1215N2	IRFF231
VN1215N5	IRF641

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
VN1216N1	IRF220
VN1216N2	IRFF220
VN1216N5	IRF620
VN1220N1	IRF220
VN1220N2	IRFF220
VN1220N5	IRF620
VN1304N2	RFL1N08
VN1306N2	RFL1N08
VN1310N2	RFL1N10
VN1315N2	IRFF213
VN1320N2	IRFF212
VN1706B	RFL1N18
VN1706D	RFP2N18
VN2345N1	RFM6N45
VN2345N5	RFP6N45
VN2350N1	RFM6N50
VN2350N5	RFP6N50
VN2406B	IRF723
VN3500A	RFM7N35
VN3500D	RFP7N35
VN3501A	IRF331
VN3501D	IRF731
VN4000A	RFM7N40
VN4000D	RFP7N40
VN4001A	IRF330
VN4001D	IRF730
VN4501A	RFM6N45
VN4501D	RFP6N45
VN4502A	IRF431
VN4502D	IRF831
VN5001A	RFM6N50
VN5001D	IRF430
VN5002	RFP6N50
VN5002A	IRF430
VN5002D	IRF830
VP0104N2	RFL1P08
VP0104N5	RFP2P08
VP0106N2	RFL1P08
VPO106N5	RFP2P08
VPO109N5	RFP2P08
VPO204N2	RFL1P08
VP0204N5	RFP2P08
VPO206N2	RFL1P08
VPO206N5	RFP2P08
VP0210N2	RFL1P10
VP1106N1	RFM6P08
VP1106N5	RFP6P08
VP1110N1	RFM6P10
VP1110N5	RFP6P10

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
ZVN0102B	IRFF113
ZVN0102L	IRF513
ZVN0106B	RFL1N08
ZVN0106L	RFP2N08
ZVN0108B	RFL1N08
ZVN0108L	RFP2N08
ZVN2104B	IRFF113
ZVN2104L	IRF513
ZVN2106B	IRFF113
ZVN2106L	IRF513
ZVN2110B	RFL1N10
ZVN2110L	RFP2N10
ZVN2202B	IRFF123
ZVN2202L	IRF523
ZVN2202M	IRF123
ZVN2204B	IRFF123
ZVN2204L	IRF523
ZVN2204M	IRF123
ZVN2206B	IRFF123
ZVN2206L	IRF523
ZVN2206M	IRF123
ZVN2208B	IRFF112
ZVN2208L	IRF512
ZVN2208M	IRF122
ZVN2210B	IRFF112
ZVN2210L	IRF512
ZVN2210M	IRF122
ZVN2215B	IRFF213
ZVN2215L	IRF613
ZVN2215M	IRF223
ZVN2220B	IRFF212
ZVN2220L	IRF612
ZVN2220M	IRF222
ZVP0102B	RFL1P08
ZVP0102L	RFP2P08
ZVP2104B	RFL1P08
ZVP2104L	RFP2P08
ZVP2106B	RFL1P08
ZVP2106L	RFP2P08
ZVP2202L	RFP6P08
ZVP2202M	RFM6P08
ZVP2204L	RFP6P08
ZVP2204M	RFM6P08
ZVP2206L	RFP6P08
ZVP2206M	RFM6P08
ZVP2208M	RFM6P08
ZVP2210M	RFM6P10
ZVP2215L	RFP5P15
ZVP2215M	RFM5P15

Product Profiles

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Standard Power MOSFETs

Power MOSFETs

The line of solid state power devices includes a series of standard state-of-the-art n- and p-channel enhancement-mode field-effect transistors. These power MOSFETs are designed for such applications as dc-to-dc converters, motor drive and control circuits, solenoid and relay drive circuits, linear and switching regulators, drivers for high-power bipolar devices, and automotive load switching and control circuits.

The designs of power MOSFET structures are optimized to achieve simultaneously high voltage, current, and dissipation capability, together with fast switching speeds, on competitively sized chips. The critical considerations are:

1. A low on-state resistance, $r_{DS(ON)}$, from the drain to the source.
2. The resistivity and spacings of the silicon layers necessary to assure the required drain-to-source voltage breakdown capability.
3. A uniform gate-to-source threshold voltage.
4. A structure to minimize the effect of device junction capacitances on switching speed.

The resultant structures feature low leakage currents, good thermal characteristics (low thermal resistance and excellent thermal stability), large safe-operating areas, and high operating efficiencies.

Features

- Fast switching speeds and low switching losses, both of which are independent of temperature.
- Minimal storage time and no temperature-dependent delay times.
- High resistance to thermal runaway.
- Simple drive circuitry.
- Safe operating area limited only by device dissipation ratings.
- Stable gain and switching response over a wide temperature range.

Operation

A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the positive electric charge on the gate converts the p-region beneath the gate to an n-type region. This surface-inversion phenomenon allows current to flow between the drain and source through an n-type material. In effect, the MOSFET becomes an n-n-n device when in this state. The region between the drain and source can then be represented as a temperature-dependent resistor.

Further development has expanded the power MOSFET line to include the following families of devices:

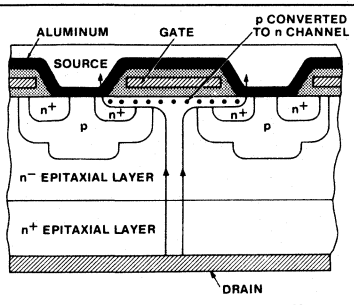
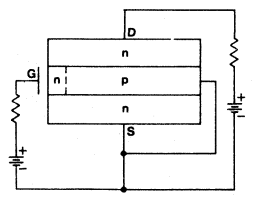
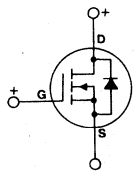
1. Logic-Level Power MOSFETs-L²FETs, devices which allow on-off switching directly from logic-level voltage of 5 volts rather than the nominal 10 volts required for standard power MOSFETs.
2. Insulated-Gate Bipolar Transistors (COMFETs or IGTs), devices which combine the characteristics of a power MOS transistor and a bipolar transistor, making them cost-effective for many power switching and control applications.
3. Rugged Power MOSFETs, devices which are designed, tested and guaranteed to withstand a specific level of electrical stress in the breakdown avalanche mode of operation.

Packaged Devices and Chips

The power MOSFET product line currently includes more than 800 types. The GE- and RF-series are identified by a coded type number which indicates the current and voltage ratings, whether n-or p-channel, and specifies the package type.

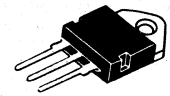
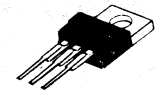
The devices are supplied in nine package styles: TO-204, TO-205, TO-218, TO-220, TO-247, TO-251, TO-252, and a 4-pin DIP. Power MOSFET chips are also available for use in hybrid circuits. Chips may be purchased either in wafer form or as separated die.

N-CHANNEL POWER MOSFET (STANDARD & L²FET)

Cross section of chip structure	Junction diagram showing biasing arrangements	Schematic symbol
		

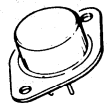
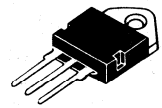
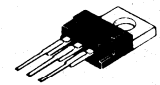
Standard Power MOSFETs

RF and BUZ-Series Power MOSFETs — N-Channel

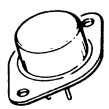
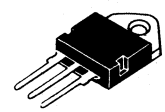
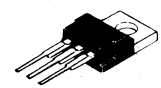
Maximum Ratings N-Channel / Package						
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205	TO-218	TO-220
50	2	0.75		RFL2N05		
	4	0.60				RFP4N05
	15	0.14	RFM15N05			RFP15N05
	25	0.07	RFM25N05			
	25	0.047				RFP25N05
	30	0.04				BUZ11
	45	0.04	RFK45N05		RFH45N05	
60	2	0.75		RFL2N06		
	4	0.60				RFP4N06
	15	0.14	RFM15N06			RFP15N06
	25	0.07	RFM25N06			RFP25N06
	45	0.04	RFK45N06		RFH45N06	
80	1	1.20		RFL1N08		
	2	1.05				RFP2N08
	12	0.20	RFM12N08			RFP12N08
	18	0.10	RFM18N08			RFP18N08
	35	0.055	RFK35N08		RFH35N08	
100	1	4.50		RFL1N10		
	2	1.05				RFP2N10
	9	0.25				BUZ72A
	12	0.20	RFM12N10			RFP12N10/BUZ20
	18	0.10	RFM18N10			RFP18N10
	35	0.055	RFK35N10		RFH35N10	
120	1	1.90		RFL1N12		
	2	1.75				RFP2N12
	4	0.40		RFL4N12		
	10	0.30	RFM10N12			RFP10N12
	15	0.15	RFM15N12			RFP15N12
	30	0.075	RFK30N12		RFH30N12	
150	1	1.90		RFL1N15		
	2	1.75				RFP2N15
	4	0.40		RFL4N15		
	10	0.30	RFM10N15			RFP10N15
	15	0.15	RFM15N15			RFP15N15
	30	0.075	RFK30N15		RFH30N15	
180	1	3.65		RFL1N18		
	2	3.50				RFP2N18
	8	0.50	RFM8N18			RFP8N18
	12	0.25	RFM12N18			RFP12N18
	25	0.15	RFK25N18		RFH25N18	
200	1	3.65		RFL1N20		
	2	3.50				RFP2N20
	5.8	0.6				BUZ73A
	8	0.50	RFM8N20			RFP8N20
	12	0.25	RFM12N20			RFP12N20
	25	0.15	RFK25N20		RFH25N20	
350	4	1.50	RFM4N35			RFP4N35
	7	0.75	RFM7N35			RFP7N35
	12	0.38	RFM12N35		RFH12N35	

Standard Power MOSFETs

RF and BUZ-Series Power MOSFETs — N-Channel

Maximum Ratings N-Channel / Package						
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205	TO-218	TO-220
400	4	1.50	RFM4N40			RFP4N40
	7	0.75	RFM7N40			RFP7N40
	12	0.38	RFM12N40		RFH12N40	
	4.5	1.50				BUZ60B
	5.5	1.00				BUZ60
	3.0	1.8				BUZ76
	2.6	2.5				BUZ76A
	11.5	0.4			BUZ351	
450	3	2.50	RFM3N45			RFP3N45
	6	1.25	RFM6N45			RFP6N45
	10	0.60	RFM10N45		RFH10N45	
500	3	2.50	RFM3N50			RFP3N50
	4.5	1.50				BUZ41A
	6	1.25	RFM6N50			RFP6N50
	8.3	0.80	BUZ45A			
	9.6	0.60	BUZ45			
	10	0.60	RFM10N50		RFH10N50	
	10	0.50	BUZ45B			

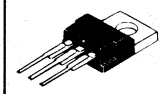
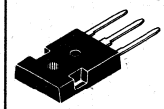
RF-Series Power MOSFETs — P-Channel

Maximum Ratings P-Channel / Package						
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205	TO-218	TO-220
80	1	3.15		RFL1P08		
	2	3.00				RFP2P08
	6	0.60	RFM6P08			RFP6P08
	8	0.40	RFM8P08			RFP8P08
	12	0.30	RFM12P08			RFP12P08
	25	0.15	RFK25P08		RFH25P08	
100	1	3.15		RFL1P10		
	1.5	3.65		2N6895*		
	2	3.00				RFP2P10
	6	0.60	RFM6P10			RFP6P10
	6	0.60	2N6896*			
	8	0.40	RFM8P10			RFP8P10
	12	0.30	RFM12P10			RFP12P10
	12	0.30	2N6897*			
	25	0.20	2N6898*			
	25	0.15	RFK25P10		RFH25P10	
120	5	1.00	RFM5P12			RFP5P12
	10	0.50	RFM10P12			RFP10P12
150	5	1.00	RFM5P15			RFP5P15
	10	0.50	RFM10P15			RFP10P15

*QPL approved types

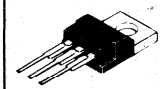
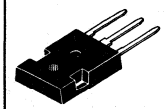
Standard Power MOSFETs

IRF-Series Power MOSFETs — N-Channel

Maximum Ratings N-Channel / Package							
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205	TO-220	TO-247	4-Pin DIP
60	0.40	3.20					IRFD1Z3
	0.50	2.40					IRFD1Z1
	0.80	0.80					IRFD113
	1	0.60					IRFD111
	1.1	0.40					IRFD123
	1.3	0.30					IRFD121
	3	0.80		IRFF113			
	3.50	0.60		IRFF111			
	3.50	0.80			IRF513		
	4	0.60			IRF511		
	5	0.40		IRFF123			
	6	0.30	IRF121				
	7	0.25		IRFF133			
	7	0.40	IRF123		IRF523		
	8	0.18		IRFF131			
	8	0.30		IRFF121	IRF521		
	12	0.25	IRF133		IRF533		
	14	0.18	IRF131		IRF531		
	24	0.11	IRF143		IRF543		
	27	0.085	IRF141		IRF541		
	33	0.08	IRF153			IRFP153	
	40	0.055	IRF151			IRFP151	
100	0.4	3.20					IRFD1Z2
	0.5	2.40					IRFD1Z0
	0.80	0.80					IRFD112
	1	0.60					IRFD110
	1.10	0.40					IRFD122
	1.30	0.30					IRFD120
	3	0.80		IRFF112			
	3.50	0.60		IRFF110			
	3.50	0.80			IRF512		
	4	0.60			IRF510		
	5	0.4		IRFF122			
	6	0.30		IRFF120			
	7	0.25		IRFF132			
	7	0.40	IRF122		IRF522		
	8	0.18		IRFF130			
	8	0.30	IRF120		IRF520		
	12	0.25	IRF132		IRF532		
	14	0.18	IRF130		IRF530		
	24	0.11	IRF142		IRF542		
	27	0.085	IRF140		IRF540		
	33	0.08	IRF152			IRFP152	
	40	0.055	IRF150			IRFP150	
150	0.25	7.50					IRFD2Z3
	0.32	5.00					IRFD2Z1
	0.45	2.40					IRFD213
	0.60	1.50					IRFD211
	0.70	1.20					IRFD223
	0.80	0.80					IRFD221
	1.80	2.40		IRFF213			
	2	2.40			IRF613		
	2.20	1.50		IRFF211			
	2.50	1.50			IRF611		
	3	1.20		IRFF223			
	3.50	0.80		IRFF221			
	4	1.20	IRF223		IRF623		
	4.50	0.60		IRFF233			
	5	0.80	IRF221		IRF621		
	5.5	0.40		IRFF231			

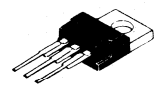
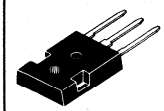
Standard Power MOSFETs

IRF-Series Power MOSFETs — N-Channel (Cont'd)

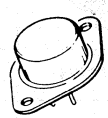
Maximum Ratings N-Channel / Package							
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205	TO-220	TO-247	4-Pin DIP
150	8	0.60	IRF233		IRF633		
	9	0.40	IRF231		IRF631		
	16	0.22	IRF243		IRF643		
	18	0.18	IRF241		IRF641		
	25	0.12	IRF253			IRFP253	
	30	0.085	IRF251			IRFP251	
200	0.25	7.50					IRFD2Z2
	0.32	5.00					IRFD2Z0
	0.45	2.40					IRFD212
	0.60	1.50					IRFD210
	0.70	1.20					IRFD222
	0.80†	0.80					IRFD220
	1.80	2.40		IRFF212			
	2	2.40			IRF612		
	2.20	1.50		IRFF210			
	2.50	1.50			IRF610		
	3	1.20		IRFF222			
	3.50	0.80		IRFF220			
	4	1.20	IRF222		IRF622		
	4.50	0.60		IRFF232			
	5	0.80	IRF220		IRF620		
	5.50	0.40		IRFF230			
	8	0.60	IRF232		IRF632		
	9	0.40	IRF230		IRF630		
	16	0.22	IRF242		IRF642		
	18	0.18	IRF240		IRF640		
	25	0.12	IRF252			IRFP252	
	30	0.085	IRF250			IRFP250	
350	0.30	5.00					IRFD313
	0.40	3.60					IRFD311
	0.40	2.50					IRFD323
	0.50	1.80					IRFD321
	1.15	5.00		IRFF313			
	1.30	5.00			IRF713		
	1.35	3.60		IRFF311			
	1.50	3.60			IRF711		
	2	2.50		IRFF323			
	2.50	1.80		IRFF321			
	2.50	2.50	IRF323		IRF723		
	3	1.80	IRF321	IRFF333	IRF721		
	3.50	1.00		IRFF331			
	4.50	1.50	IRF333		IRF733		
	5.50	1.00	IRF331		IRF731		
	8	0.80	IRF343		IRF743		
	10	0.55	IRF341		IRF741		
	13	0.40	IRF353			IRFP353	
	15	0.30	IRF351			IRFP351	
400	0.30	5.00					IRFD312
	0.40	3.60					IRFD310
	0.40	2.50					IRFD322
	0.50	1.80					IRFD320
	1.15	5.00		IRFF312			
	1.30	5.00			IRF712		
	1.35	3.60		IRFF310			
	1.50	3.60			IRF710		
	2	2.50		IRFF322			
	2.50	2.50	IRF322		IRF722		
	2.50	1.80		IRFF320			
	3	1.50		IRFF332			

Standard Power MOSFETs

IRF-Series Power MOSFETs — N-Channel (Cont'd)

Maximum Ratings N-Channel / Package							
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205	TO-220	TO-247	4-Pin DIP
400	3	1.80	IRF320		IRF720		
	3.50	1.00		IRFF330			
	4	1.50	IRF332				
	4.50	1.50			IRF732		
	5	1.00			IRF730		
	5.5	1.00	IRF330				
	8	0.80	IRF342		IRF742		
	10	0.55	IRF340		IRF740		
	13	0.40	IRF352			IRFP352	
	15	0.30	IRF350			IRFP350	
450	1.40	4.00		IRFF423			
	1.60	3.00		IRFF421			
	2	4.00	IRF423		IRF823		
	2.25	2.00		IRFF433			
	2.50	3.00	IRF421		IRF821		
	2.75	1.50		IRFF431			
	4	2.00	IRF433		IRF833		
	4.50	1.50	IRF431		IRF831		
	7	1.10	IRF443		IRF843		
	8	0.85	IRF441		IRF841		
	12	0.50	IRF453			IRFP453	
	13	0.40	IRF451			IRFP451	
500	1.40	4.00		IRFF422			
	1.60	3.00		IRFF420			
	2	4.00	IRF422		IRF822		
	2.25	2.00		IRFF432			
	2.50	3.00	IRF420		IRF820		
	2.75	1.50		IRFF430			
	4	2.0	IRF432		IRF832		
	4.5	1.50	IRF430		IRF830		
	7	1.1	IRF442		IRF842		
	8	0.85	IRF440		IRF840		
	12	0.50	IRF452			IRFP452	
	13	0.40	IRF450			IRFP450	

JEDEC Types — N-Channel

Maximum Ratings N-Channel / Package				
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205
60	12	0.25	2N6755	
	30	0.08	2N6763	
100	3.50	0.60		2N6782*
	6	0.30		2N6788*
	8	0.18		2N6796*
	14	0.18	2N6756*	
	38	0.055	2N6764*	
150	8	0.60	2N6757	
	25	0.12	2N6765	

Maximum Ratings N-Channel / Package				
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205
200	2.25	1.50		2N6784*
	3.50	0.80		2N6790*
	5.50	0.40		2N6798*
	9	0.40	2N6758*	
	30	0.085	2N6766*	
350	4.50	1.50	2N6759	
	12	0.40	2N6767	
400	1.25	3.60		2N6786*
	2	1.80		2N6792*

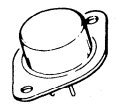
*QPL — Approved Types

Standard Power MOSFETs

JEDEC Types — N-Channel (Cont'd)

Maximum Ratings N-Channel / Package				
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205
400	3	1.00		2N6800*
	5.50	1.00	2N6760*	
	14	0.30	2N6768*	
450	4	2.00	2N6761	
	11	0.50	2N6769	

*QPL — Approved Types

Maximum Ratings N-Channel / Package				
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	TO-204	TO-205
500	1.50	3.00		2N6794*
	3.50	1.50		2N6802*
	4.50	1.50	2N6762*	
	12	0.40	2N6770*	

MegaFETs

The MEGAFET-Series of power MOSFETs represent an advancement in processing technology that achieves unmatched $r_{DS(ON)}$ performance per unit area of silicon. This application of VLSI IC dimensions and processing techniques allows for the integration of nearly 2 million cells per square inch of active silicon area. This represents a minimum twofold and, more typically, a four-fold increase in cell density.

The MEGAFET design achieves several important advantages. Among these are:

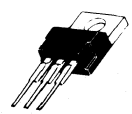
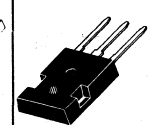
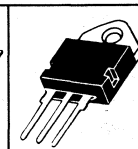
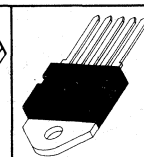
- More volt-ampere capability per unit cost
- Small die size for the same $r_{DS(ON)}$
- Lower $r_{DS(ON)}$ for the same die size
- 40% die size reduction at 50 V BV_{DSS}

The MEGAFET-series is also specified for avalanche energy capability.

Additional product introductions are anticipated. Among these are:

- N-channel 0.200, 0.100, 0.050 ohms $r_{DS(ON)}$ at BV_{DSS} = 100 V
- P-channel 0.300, 0.150, 0.070 ohms $r_{DS(ON)}$ at BV_{DSS} = 50 V

MegaFET Product Series — N-Channel

Maximum Ratings N-Channel / Package									
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	E_{AS} (mj)	TO-251	TO-252	TO-220	TO-247	TO-218	TO-218 5 Lead
50	10	0.10	100	RFD10N05	RFD10N05SM				
	14	0.10	100	RFD14N05	RFD14N05SM	RFP14N05			
	16	0.047	200	RFD16N05	RFD16N05SM				
	25	0.047	200			RFP25N05			
	50	0.022	400			RFP50N05	RFG50N05		
	75	0.010	800					RFH75N05	
	100	0.010	800						RFA100N05

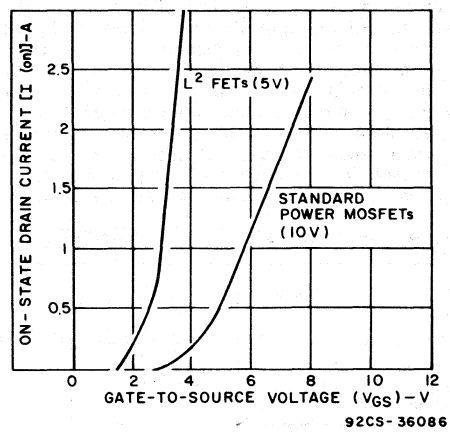
Logic Level Power MOSFETs

Logic-level power MOSFETs (L²FETs) feature a thinner gate-oxide separation layer that is typically one-half the industry standard for power MOSFETs. The surface inversion of the MOS channel is a direct function of this gate-oxide thickness; consequentially, the gate-to-source threshold voltage — i.e., the applied gate voltage required for uncompromised drain characteristics — on this series of devices is only half that of conventional power MOSFETs.

The reduced gate-drive requirement allows on-off switching of L²FETs directly from logic-level voltages of 5 volts, rather than the nominal 10 volts required for conventional power MOSFETs. The L²FETs feature the same low on-resistance characteristics, drain-current ratings, and blocking-voltage capability of corresponding types with the higher gate-drive requirements. In addition, the L²FETs offer twice the transconductance and half the threshold-voltage temperature coefficeint of conventional types having the same on-resistance and voltage ratings and demonstrate a comparable switching speed for the same gate drive power.

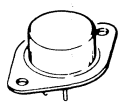
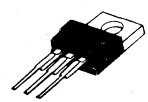
Special Features

- 5-Volt Gate Drive
- Compatible with CMOS, High-Speed CMOS, TTL, PMOS, and NMOS Logic Circuits
- Compatible with Automotive Drive Requirements



Comparison of standard power MOSFETs and L²FETs.

L²FETs — N-Channel Types

Maximum Ratings N-Channel / Package								
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	E_{AS} (mj)	TO-204	TO-205	TO-220	TO-251	TO-252
50	2	0.75	N.R.		RFL2N05L			
	4	0.60	N.R.			RFP4N05L		
	15	0.14	N.R.	RFM15N05L		RFP15N05L		
	14	0.100	100			RFP14N05L	RFD14N05L	RFD14N05LSM
	16	0.047	200				RFD16N05L	RFD16N05LSM
	25	0.047	200			RFP25N05L		
60	2	0.75	N.R.		RFL2N06L			
	4	0.60	N.R.			RFP4N06L		
	15	0.14	N.R.	RFM15N06L		RFP15N06L		
	17	0.100	N.R.			RFP17N06L		
	25	0.07	N.R.			RFP25N06L		
80	1	1.20	N.R.		RFL1N08L			
	2	1.05	N.R.			RFP2N08L		
	12	0.20	N.R.	RFM12N08L		RFP12N08L		
100	1	1.20	N.R.		RFL1N10L			
	1.50	1.40	N.R.		2N6901*			
	2	1.05	N.R.			RFP2N10L		
	12	0.20	N.R.	2N6902*				
	12	0.20	N.R.	RFM12N10L		RFP12N10L		
120	1	1.90	N.R.		RFL1N12L			
	2	1.75	N.R.			RFP2N12L		
	10	0.30	N.R.	RFM10N12L		RFP10N12L		
150	1	1.90	N.R.		RFL1N15L			
	2	1.75	N.R.			RFP2N15L		
	10	0.30	N.R.	RFM10N15L		RFP10N15L		
180	1	3.65	N.R.		RFL1N18L			
	2	3.50	N.R.			RFP2N18L		
	8	0.50	N.R.	RFM8N18L		RFP8N18L		
200	1	3.65	N.R.		RFL1N20L			
	1.5	3.65	N.R.		2N6903*			
	2	3.50	N.R.			RFP2N20L		
	8	0.65	N.R.	2N6904*				
	8	0.50	N.R.	RFM8N20L		RFP8N20L		

*QPL approved types N.R. NOT RATED

Rugged Power MOSFETs

The Rugged Series of Power MOSFETs are designed, tested and guaranteed to withstand a specified level of circuit-induced electrical stress in the breakdown avalanche mode of operation. These are n-channel enhancement-mode polysilicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor and relay drivers and drivers for high-power bipoler switching transistors requiring high speed and low gate-drive power.

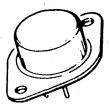
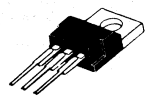
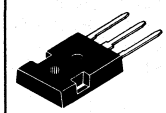
Using state-of-the-art integrated-circuit processing techniques these Rugged MOSFETs provide superior performance in inductive switching applications. The design is optimized to suppress the parasitic bipolar transistor and improve system reliability. These types can be driven directly from integrated circuits.

Rugged Series devices are identified by the suffix letter R following the type number.

Features:

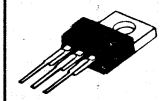
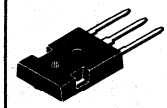
- Single pulse avalanche energy rated
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Allows reduced protection circuitry
- Reduced drive requirements
- Increased system reliability

Rugged-Series Power MOSFETs — N-Channel

Maximum Ratings N-Channel / Package								
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	E_{AS} (mj)	TO-204	TO-205	TO-220	TO-247	4-Pin DIP
60	0.80	0.80	19					IRFD113R
	1	0.60	19					IRFD111R
	1.1	0.40	36					IRFD123R
	1.3	0.30	36					IRFD121R
	3	0.80	19		IRFF113R			
	3.50	0.80	19		IRFF111R	IRF513R		
	4	0.60	19			IRF511R		
	5	0.40	36		IRFF123R			
	6	0.30	36		IRFF121R			
	7	0.25	69		IRFF133R			
	7	0.40	36			IRF523R		
	8	0.18	69		IRFF131R			
	8	0.30	36			IRF521R		
	12	0.25	69	IRF133R		IRF533R		
	14	0.18	69	IRF131R		IRF531R		
	24	0.11	100	IRF143R		IRF543R	IRFP143R	
	27	0.085	100	IRF141R		IRF541R	IRFP141R	
	33	0.080	150	IRF153R			IRFP153R	
	40	0.055	150	IRF151R			IRFP151R	
100	0.80	0.80	19					IRFD112R
	1	0.60	19					IRFD110R
	1.1	0.40	36					IRFD122R
	1.3	0.30	36					IRFD120R
	3	0.80	19		IRFF112R			
	3.5	0.60	19		IRFF110R			
	3.5	0.80	19			IRF512R		
	4	0.60	19			IRF510R		
	5	0.40	36		IRFF122R			
	6	0.30	36		IRFF120R			
	7	0.25	69		IRFF132R			
	7	0.40	36			IRF522R		
	8	0.18	69		IRFF130R			
	8	0.30	36			IRF520R		
	12	0.25	69	IRF132R		IRF532R		
	14	0.18	69	IRF130R		IRF530R		
	24	0.11	100	IRF142R		IRF542R	IRFP142R	
	27	0.085	100	IRF140R		IRF540R	IRFP140R	
	33	0.08	150	IRF152R			IRFP152R	
	40	0.055	150	IRF150R			IRFP150R	
150	0.45	2.40	30					IRFD213R
	0.60	1.50	30					IRFD211R
	0.70	1.20	85					IRFD223R
	0.80	0.80	85					IRFD221R
	1.80	2.40	30		IRFF213R			
	2	2.40	30			IRF613R		
	2.2	1.50	30		IRFF211R			
	2.5	1.50	30			IRF611R		

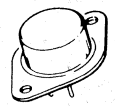
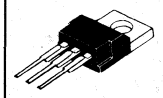
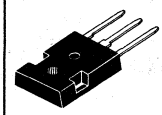
Rugged Power MOSFETs

Rugged-Series Power MOSFETs — N-Channel (Cont'd)

Maximum Ratings N-Channel / Package								
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	E_{AS} (mj)	TO-204	TO-205	TO-220	TO-247	4-Pin DIP
150	3	1.20	85		IRFF223R			
	3.5	0.80	85		IRFF221R			
	4	1.20	85			IRF623R		
	4.5	0.60	150		IRFF233R			
	5	0.80	85			IRF621R		
	5.5	0.40	150		IRFF231R			
	8	0.60	150	IRF233R		IRF633R		
	9	0.40	150	IRF231R		IRF631R		
	16	0.22	300	IRF243R		IRF643R	IRFP243R	
	18	0.18	300	IRF241R		IRF641R	IRFP241R	
	25	0.12	500	IRF253R			IRFP253R	
	30	0.085	500	IRF251R			IRFP251R	
200	0.45	2.40	30					IRFD212R
	0.60	1.50	30					IRFD210R
	0.70	1.20	85					IRFD222R
	0.80	0.80	85					IRFD220R
	1.80	2.40	30		IRFF212R			
	2	2.40	30			IRF612R		
	2.20	1.50	30		IRFF210R			
	2.50	1.50	30			IRF610R		
	3	1.20	85		IRFF222R			
	3.5	0.80	85		IRFF220R			
	4	1.20	85			IRF622R		
	4.5	0.60	150		IRFF232R			
	5	0.80	85			IRF620R		
	5.5	0.40	150		IRFF230R			
	8	0.60	150	IRF232R		IRF632R		
	9	0.40	150	IRF230R		IRF630R		
	16	0.22	300	IRF242R		IRF642R	IRFP242R	
	18	0.18	300	IRF240R		IRF640R	IRFP240R	
	25	0.12	500	IRF252R			IRFP252R	
	30	0.085	500	IRF250R			IRFP250R	
250	3.30	1.50	120			IRF625		
	3.80	1.10	120			IRF624		
	6.50	0.68	180	IRF235		IRF635	IRFP235	
	8.10	0.45	180	IRF234		IRF634	IRFP234	
	13	0.34	550	IRF245		IRF645	IRFP245	
	14	0.28	550	IRF244		IRF644	IRFP244	
	21	0.17	1000	IRF255			IRFP255	
	23	0.14	1000	IRF254			IRFP254	
275	3.30	1.50	120			IRF627		
	3.80	1.10	120			IRF626		
	6.50	0.68	180	IRF237		IRF637	IRFP237	
	8.10	0.45	180	IRF236		IRF636	IRFP236	
	13	0.34	550	IRF247		IRF647	IRFP247	
	14	0.28	550	IRF246		IRF646	IRFP246	
	21	0.17	1000	IRF257			IRFP257	
	23	0.14	1000	IRF256			IRFP256	
350	0.30	5.00	45					IRFD313R
	0.40	3.60	45					IRFD311R
	0.40	2.50	100					IRFD323R
	0.50	1.80	100					IRFD321R
	1.15	5.00	45		IRFF313R			
	1.30	5.00	45			IRF713R		
	1.35	3.60	45		IRFF311R			
	1.50	3.60	45			IRF711R		
	2	2.50	100		IRFF323R			
	2.50	1.80	100		IRFF321R			

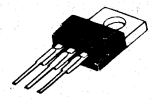
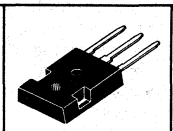
Rugged Power MOSFETs

Rugged-Series Power MOSFETs — N-Channel (Cont'd)

Maximum Ratings N-Channel / Package								
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	E_{AS} (mj)	TO-204	TO-205	TO-220	TO-247	4-Pin DIP
350	2.50	2.50	100			IRF723R		
	3	1.80	100			IRF721R		
	3	1.80	300		IRFF333R			
	3.50	1.00	300		IRFF331R			
	4.50	1.50	300	IRF333R		IRF733R		
	5.50	1.00	300	IRF331R		IRF731R		
	8	0.80	400	IRF343R		IRF743R	IRFP343R	
	10	0.55	400	IRF341R		IRF741R	IRFP341R	
	13	0.40	700	IRF353R			IRFP353R	
	15	0.30	700	IRF351R			IRFP351R	
400	0.30	5.00	45					IRFD312R
	0.40	3.60	45					IRFD310R
	0.40	2.50	100					IRFD322R
	0.50	1.80	100					IRFD320R
	1.15	5.00	45		IRFF312R			
	1.30	5.00	45			IRF712R		
	1.35	3.60	45		IRFF310R			
	1.50	3.60	45			IRF710R		
	2	2.50	100		IRFF322R			
	2.50	2.50	100			IRF722R		
	2.50	1.80	100		IRFF320R			
	3	1.50	300		IRFF332R			
	3	1.80	100			IRF720R		
	3.50	1.00	300		IRFF330R			
	4.50	1.50	300	IRF332R		IRF732R		
	5.50	1.00	300	IRF330R		IRF730R		
	8	0.80	400	IRF342R		IRF742R	IRFP342R	
	10	0.55	400	IRF340R		IRF740R	IRFP340R	
	13	0.40	700	IRF352R			IRFP352R	
	15	0.30	700	IRF350R			IRFP350R	
	22	0.25	980	IRF362			IRFP362	
	25	0.20	980	IRF360			IRFP360	
450	1.40	4.00	210		IRFF423R			
	1.60	3.00	210		IRFF421R			
	2	4.00	210			IRF823R		
	2.25	2.00	300		IRFF433R			
	2.50	3.00	210			IRF821R		
	2.75	1.50	300		IRFF431R			
	4	2.00	300	IRF433R		IRF833R		
	4.50	1.50	300	IRF431R		IRF831R		
	7	1.10	450	IRF443R		IRF843R	IRFP443R	
	8	0.85	450	IRF441R		IRF841R	IRFP441R	
	12	0.50	860	IRF453R			IRFP453R	
	13	0.40	860	IRF451R			IRFP451R	
500	1.40	4.00	210		IRFF422R			
	1.60	3.00	210		IRFF420R			
	2	4.00	210			IRF822R		
	2.25	2.00	300		IRFF432R			
	2.50	3.00	210			IRF820R		
	2.75	1.50	300		IRFF430R			
	4	2.00	300	IRF432R		IRF832R		
	4.50	1.50	300	IRF430R		IRF830R		
	7	1.10	450	IRF442R		IRF842R	IRFP442R	
	8	0.85	450	IRF440R		IRF840R	IRFP440R	
	12	0.50	860	IRF452R			IRFP452R	
	13	0.40	860	IRF450R			IRFP450R	
	17	0.35	960	IRF462			IRFP462	
	20	0.27	960	IRF460			IRFP460	
600	5.40	1.60	570	IRFAC42R		IRFBC42R		
	5.90	1.60	410				IRFPC42R	
	6.20	1.20	570	IRFAC40R		IRFBC40R		
	6.80	1.20	410				IRFPC40R	

Rugged Power MOSFETs

Rugged-Series Power MOSFETs — P-Channel

Maximum Ratings P-Channel / Package								
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ OHMS	E_{AS} (mj)	TO-204	TO-205	TO-220	TO-247	4-Pin DIP
60	0.6	1.6	170					IRFD9113
	0.8	0.8	370					IRFD9123
	2.5	1.6	170			IRF9513		
	3	1.2	170			IRF9511		
	3.5	0.8	370		IRFF9123			
	4	0.6	370		IRFF9121			
	5	0.8	370			IRF9523		
	5.5	0.4	500		IRFF9133			
	6	0.6	370			IRF9521		
	6.5	0.3	500		IRFF9131			
	10	0.4	500	IRF9133		IRF9533		
	12	0.3	500	IRF9131		IRF9531		
	19	0.2	960	IRF9141		IRF9541	IRFP9141	
	15	0.3	960	IRF9143		IRF9543	IRFP9143	
	25	0.15	1300	IRF9151			IRFP9151	
100	0.7	1.2	170					IRFD9110
	1	0.6	370					IRFD9120
	2.5	1.6	170			IRF9512		
	3	1.2	170			IRF9510		
	3.5	0.8	370		IRFF9122			
	4	0.6	370		IRFF9120			
	5	0.8	370			IRF9522		
	5.5	0.4	500		IRFF9132			
	6	0.6	370			IRF9520		
	6.5	0.3	500		IRFF9130			
	6.5	0.3	N.R.		2N6849*			
	10	0.4	500	IRF9132		IRF9532		
	12	0.3	500	IRF9130		IRF9530		
	12	0.3	N.R.	2N6804*				
	19	0.2	960	IRF9140		IRF9540	IRFP9140	
	15	0.3	960	IRF9142		IRF9542	IRFP9142	
	25	0.15	1300	IRF9150			IRFP9150	
150	0.5	2.4	290					IRFD9223
	2.0	2.4	290		IRFF9223			
	2.5	1.5	290		IRFF9221			
	3.0	2.4	290			IRF9623		
	3.5	1.2	500		IRFF9233			
	3.5	1.5	290			IRF9621		
	4.0	0.8	500		IRFF9231			
	5.5	1.2	500	IRF9233		IRF9633		
	6.5	0.8	500	IRF9231		IRF9631		
	9	0.7	790	IRF9243		IRF9643	IRFP9243	
	11	0.5	790	IRF9241		IRF9641	IRFP9241	
200	0.6	1.5	290					IRFD9220
	2.0	2.4	290		IRFF9222			
	2.5	1.5	290		IRFF9220			
	3.0	2.4	290			IRF9622		
	3.5	1.2	500		IRFF9232			
	3.5	1.5	290			IRF9620		
	4.0	0.8	500		IRFF9230			
	4.0	0.8	N.R.		2N6851*			
	5.5	1.2	500	IRF9232		IRF9632		
	6.5	0.8	500	IRF9230		IRF9630		
	9	0.7	790	IRF9242		IRF9642	IRFP9242	
	11	0.5	790	IRF9240		IRF9640	IRFP9240	

N.R. = not rated. *QPL — Approved Types

Insulated-Gate Bipolar Transistors (COMFETs and IGTs)

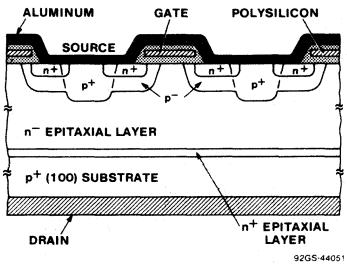
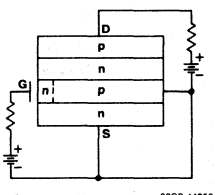
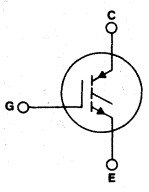
The COMFET, or Conductivity-Modulated Field-Effect Transistor, and the IGT, or Insulated-Gate Transistor, are discrete power switch devices that combine the characteristics of a power MOS transistor, a bipolar transistor, and a thyristor. As a result, they are cost-effective for many power switching and control applications. They feature an exceptionally low nonlinear on-resistance, $r_{DS(ON)}$, that is nearly independent of blocking-voltage level and temperature. In addition, their fast turn-on speed is very similar to that of standard power FETs, and their rise-time characteristics are easily controlled by the gate driving circuit. These characteristics enable the designer to control EMI and RFI generation more easily than with other power semiconductor devices, which may require elaborate circuit schemes to limit rapidly rising in-rush currents.*

There are twenty-four n-channel enhancement-mode conductivity-modulated power field-effect transistors (COMFETs) and sixteen n-channel insulated-gate transistors (IGTs) presently available. These types are designed for use in high-voltage, low on-dissipation applications such as switching regulators and motor drivers. They can be operated directly from low-power CMOS integrated circuits.

Features:

- **Voltage Gated** — Requires small gate power. Similar to standard power MOSFET.
- **Turn Off** — Turns off when gate drive is removed.
- **On-State Voltage Drop** — Nonlinear. Like that of an SCR. Temperature independent. Unlike the typical 2X variation of a power MOSFET.
- **Turn-On Speed** — Fast! Comparable to a standard power MOSFET.
- **Turn-Off Speed** — Comparable to a bipolar transistor.

COMFET (CONDUCTIVITY-MODULATED FIELD — EFFECT TRANSISTOR) OR IGT (INSULATED-GATE TRANSISTOR)

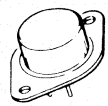
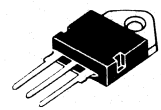
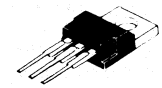
Cross section of chip structure	Junction diagram showing biasing arrangements	Schematic symbol
		

*These structures, however, trade off turn-off switching speed for this enhanced $r_{DS(ON)}$ performance. They have the small turn-off delay times of standard MOSFETs and fall times comparable to bipolar transistors.

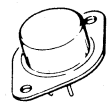
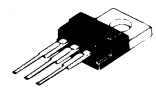
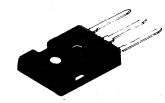
Insulated-Gate Bipolar Transistors (IGBTs)

N-Channel Enhancement-Mode Conductivity Modulated Power Field-Effect Transistors

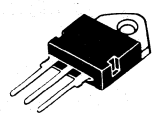
IGBT's Optimized for Switching Applications

Maximum Ratings N-Channel / Package						
BV_{CES} (V)	I_{CE} (A)	t_f (μs)	V_{CE} (v)	TO-204AA	TO-218AC	TO-220AB
400	5	1.0	2.0	2N6975		
	5	0.5	2.0	2N6977		
	10	1.0	2.5	IGTM10N40	IGTH10N40	IGTP10N40
	10	0.5	2.5	IGTM10N40A	IGTH10N40A	IGTP10N40A
	20	1.0	2.5	IGTM20N40	IGTH20N40	IGTP20N40
	20	0.5	2.5	IGTM20N40A	IGTH20N40A	IGTP20N40A
500	5	1.0	2.0	2N6976		
	5	0.5	2.0	2N6978		
	10	1.0	2.5	IGTM10N50	IGTH10N50	IGTP10N50
	10	0.5	2.5	IGTM10N50A	IGTH10N50A	IGTP10N50A
	20	1.0	2.5	IGTM20N50	IGTH20N50	IGTP20N50
	20	0.5	2.5	IGTM20N50A	IGTH20N50A	IGTP20N50A

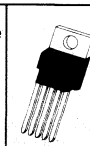
IGBT's Optimized for Motor Drive Applications

Maximum Ratings N-Channel / Package						
B_{CES} (V)	I_{CE} (A)	V_{CE} (V)	SOA I_{CE}	TO-204AA	TO-220AB	TO-247
400	18	2.5	30A	IGT6D10	IGT4D10	
	18	2.5	30A	IGT6D11	IGT4D11	
	32	2.2	50A	IGT6D20		IGT8D20
	32	2.5	50A	IGT6D21		IGT8D21
500	18	2.5	30A	IGT6E10	IGT4E10	
	18	2.5	30A	IGT6E11	IGT4E11	
	32	2.2	50A	IGT6E20		IGT8E20
	32	2.5	50A	IGT6E21		IGT8E21

IGBT's with Integral Reverse Diode

Maximum Ratings N-Channel / Package				
V_{CES} (V)	I_{CE} (A)	V_{CE} (V)	t_f (μs)	TO-218AC
400	10	2.5	1.0	IGTH10N40D
	10	2.5	0.5	IGTH10N40AD
	20	2.5	1.0	IGTH20N40D
	20	2.5	0.5	IGTH20N40AD
500	10	2.5	1.0	IGTH10N50D
	10	2.5	0.5	IGTH10N50AD
	20	2.5	1.0	IGTH20N50D
	20	2.5	0.5	IGTH20N50AD

IGBT's with Integral Current Sensing

Maximum Ratings N-Channel / Package					
V_{CES} (V)	I_{CE} (A)	V_{CE} (V)	t_f (μs)	TO-220 5-lead	TO-218 5-lead
500	10	2.3	1.2	GSI510	
	10	2.3	1.2	IGT5E10CS	
	25	2.6	1.2		GSI525
	25	2.6	1.2		IGT7E20CS

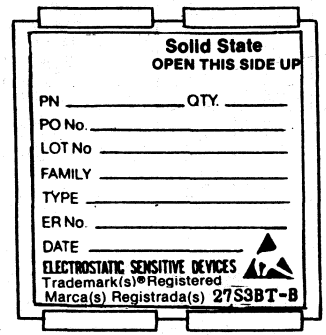
These devices provide thru a fourth terminal a non intrusive means of monitoring the collector to emitter current.

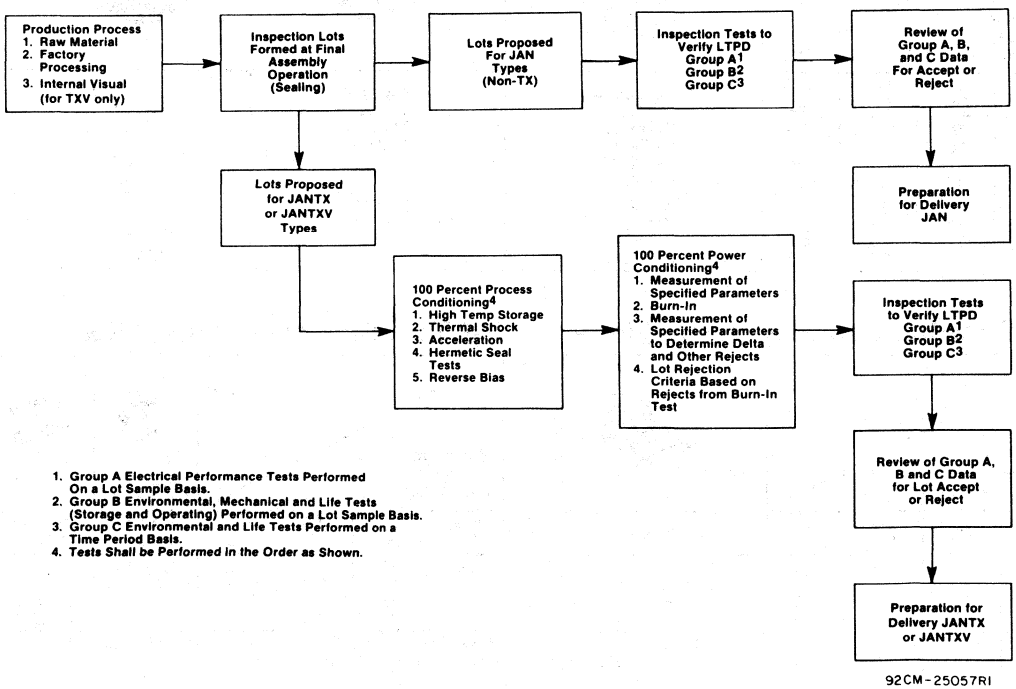
High-Reliability Power MOSFETs

Solid-state devices classified as high-reliability types have come to be primarily associated with military and aerospace applications. In many ways, this association is misleading because the commerical equipment market is probably the largest user of high-reliability products, but not necessarily by that label. Military and aerospace agencies, however, have been largely responsible for establishment of comprehensive published reliability specifications and standards which have been accepted by the solid-state industry. MIL standards dominate the procedures used to specify high-reliability solid-state devices and represent a common reference point frequently used by commerical users to define their requirements.

Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured: rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed those required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment. These standards also cover a wide range of requirements for the manufacturer on such things as:

(a) The procedure and requirements for a manufacturer to become certified to manufacture MIL-spec parts.
(b) The requirements for qualifying parts.
(c) Product-assurance provisions in such areas as quality control, inspection procedures, personnel training, cleanliness, failure analysis, and documentation.
(d) Test methods and procedures.
(e) Marking and identification of product.
(f) Preservation and packing.





Order of procedure diagram for JAN, JANTX, and JANTXV solid-state devices.

Radiation-Resistant Power MOSFETs

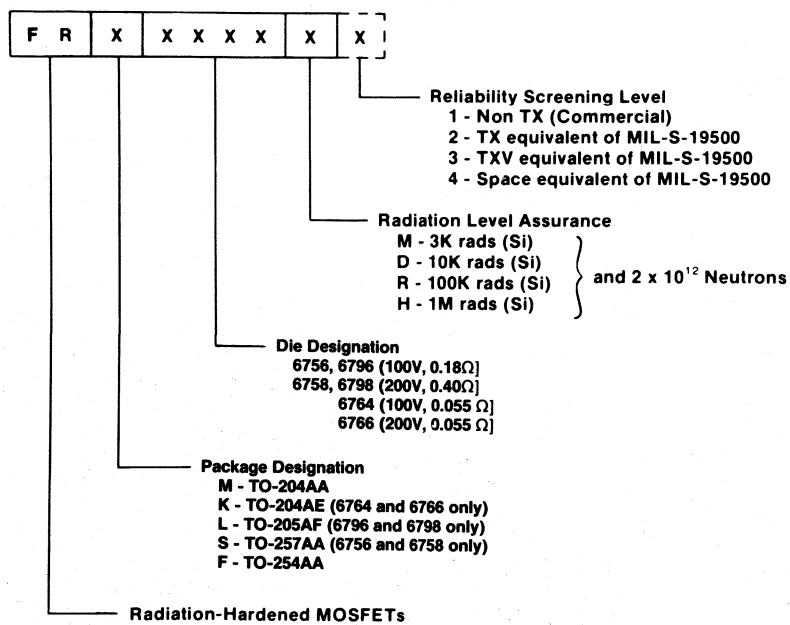
The following Harris power MOSFETs are manufactured using special design and processing techniques to assure continued functional performance after exposure to specified dosages of neutron and gamma radiation.

The following types are recommended for those applications where radiation tolerance is a critical factor. Radiation tolerance is not covered by present slash (/) specifications.

Rad-Hard Power MOSFET Specifications

Types	Pre-Rad Look Alike	Rating or Characteristic	Pre-Rad		Post-Radiation Electrical Characteristics								Units
					3K Rad(Si)[1]		10K Rad(Si)[2]		100K Rad(Si)[3]		1M Rad(Si)[4]		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
FRM6756	2N6756 IRF130	I_D	14		14		14		14		8		Amps
		BV_{DSS}	100		100		100		100		100		Volts
		$R_{DS(ON)}$		0.18		0.18		0.18		0.20		0.30	Ohms
		V_{th}	2.0	4.0	2.0	4.0	1.5	4.2	1.0	4.5	0.5	5.00	Volts
FRM6758	2N6758 IRF230	I_D	9		9		9		8		5		Amps
		BV_{DSS}	200		180		180		180		180		Volts
		$R_{DS(ON)}$		0.4		0.4		0.4		0.5		0.75	Ohms
		V_{th}	2.0	4.0	2.0	4.0	1.5	4.2	1.0	4.5	0.5	5.0	Volts
FRK6764 FRF6764	2N6764 IRF150	I_D	38		38		38		38		16		Amps
		BV_{DSS}	100		100		100		100		100		Volts
		$R_{DS(ON)}$		.055		.055		.055		.060		0.125	Ohms
		V_{th}	2.0	4.0	2.0	4.0	1.5	4.2	1.0	4.5	0.5	5.0	Volts
FRK6766 FRF6766	2N6766 IRF250	I_D	30		30		30		25		8		Amps
		BV_{DSS}	200		180		180		180		180		Volts
		$R_{DS(ON)}$		.085		.085		0.100		0.125		0.250	Ohms
		V_{th}	2.0	4.0	2.0	4.0	1.5	4.2	1.0	4.5	0.5	5.00	Volts
FRL6796	2N6796 IRFF130	I_D	8		8		8		8		6		Amps
		BV_{DSS}	100		100		100		100		100		Volts
		$R_{DS(ON)}$		0.18		0.18		0.18		0.20		0.30	Ohms
		V_{th}	2.0	4.0	2.0	4.0	1.5	4.2	1.0	4.5	0.5	5.00	Volts
FRL6798	2N6798 IRFF230	I_D	5.5		5.5		5.5		5.5		5		Amps
		BV_{DSS}	200		180		180		180		180		Volts
		$R_{DS(ON)}$		0.4		0.4		0.4		0.5		0.75	Ohms
		V_{th}	2.0	4.0	2.0	4.0	1.5	4.2	1.0	4.5	0.5	5.00	Volts

Radiation-Hardened MOSFET Nomenclature System



Handling Precautions for Power MOSFETs

Insulated-Gate Field-Effect Transistors (MOSFETs) are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling a MOSFET, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no damage problems due to electrostatic discharge.

MOSFETs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive materials such as "ECCOSORB* LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hands being used should be grounded by any suitable means — for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating — Never exceed the gate-voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.
7. Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. If gate protection is required an external zener is recommended.

*Trademark Emerson and Cumming, Inc.

Standard Power MOSFETs

BUZ Series N-Channel 3-2
IRF Series N-Channel 3-54
RF Series N-Channel 3-324
RF Series P-Channel 3-440
JEDEC Types N-Channel 3-472

BUZ 11

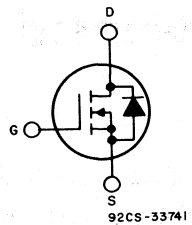
File Number **2253**

N-Channel Enhancement-Mode Power Field-Effect Transistors

30 A, 50 V
$r_{DS(on)}$ = 0.04 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



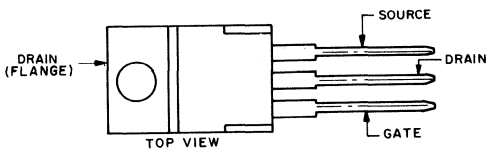
92CS-33741

TERMINAL DIAGRAM

The BUZ 11 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 11 is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	50	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	50	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 30 °C	I_D	30	A
Pulsed T_C = 25 °C	I_{DM}	120	A
POWER DISSIPATION @ T_C = 25 °C	P_T	75	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	50	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 50$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 15$ A	—	0.03	0.04	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 15$ A	4.0	8.0	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V $f = 1$ MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	750	1100	
Reverse Transfer Capacitance	C_{rss}		—	250	400	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 3$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	30 70	45 110	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$ t_f		— —	180 130	230 170	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	30	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	120	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.7	2.6	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$	—	200	—	ns
Reverse Recovered Charge	Q_{RR}	$dI_F/dt = 100$ A/μs, $V_R = 30$ V	—	0.25	—	μC

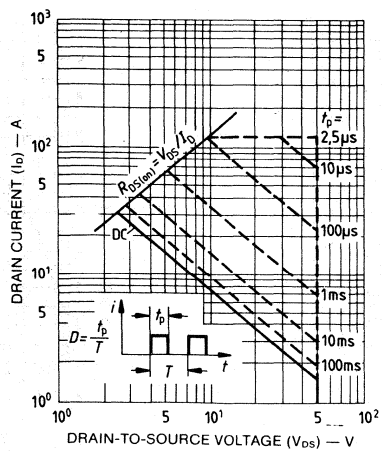


Fig. 1 - Maximum safe operating areas for all types.

BUZ 11

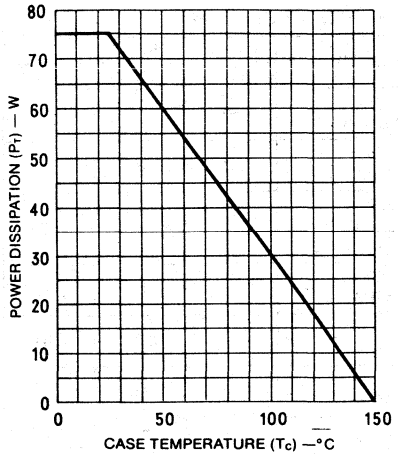


Fig. 2 - Power vs. temperature derating curve for all types.

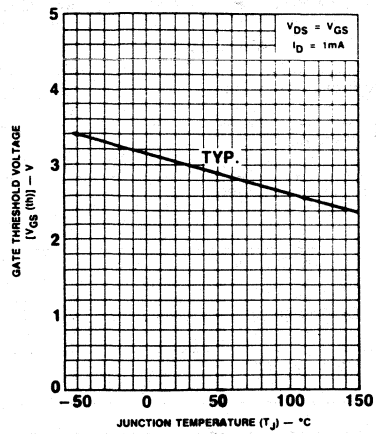


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

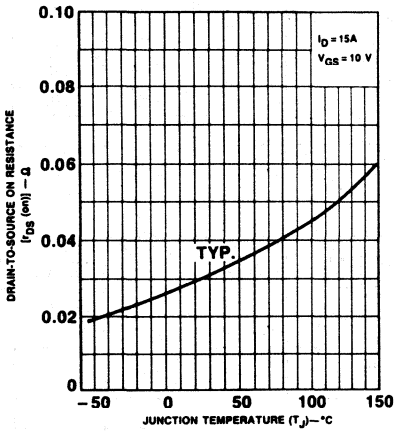


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

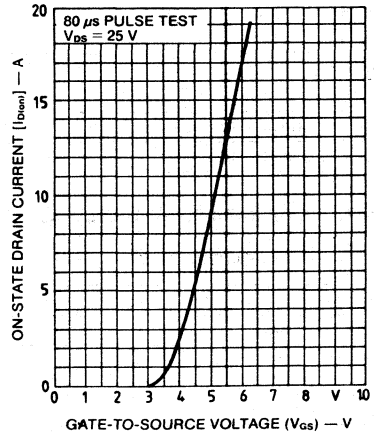


Fig. 5 - Typical transfer characteristics for all types.

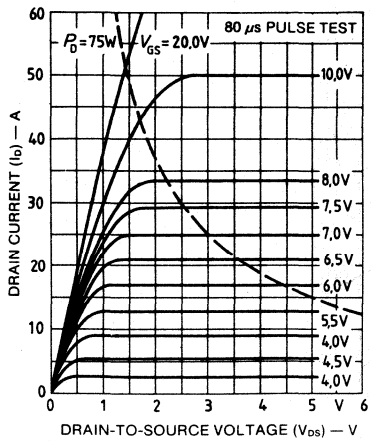


Fig. 6 - Typical output characteristics.

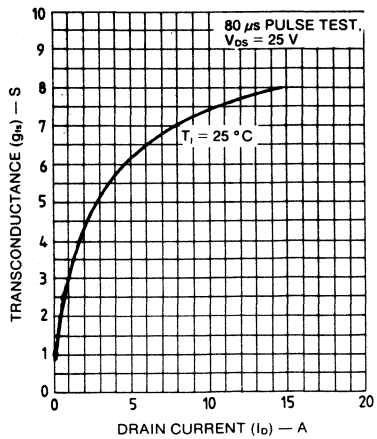


Fig. 7 - Typical transconductance vs. drain current.

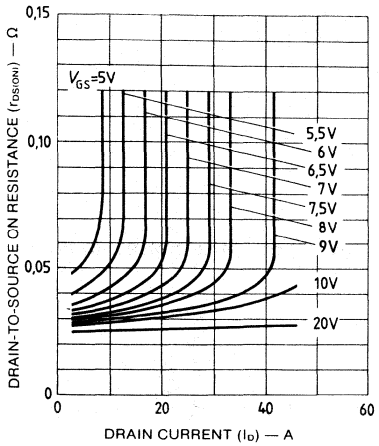


Fig. 8 - Typical on-resistance vs. drain current.

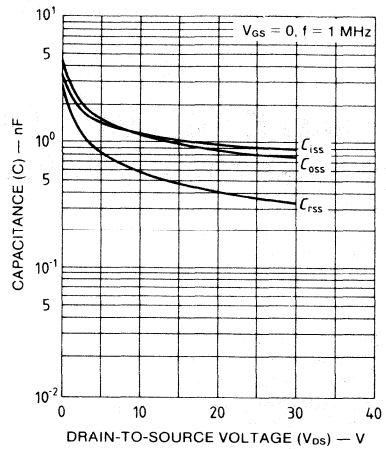


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

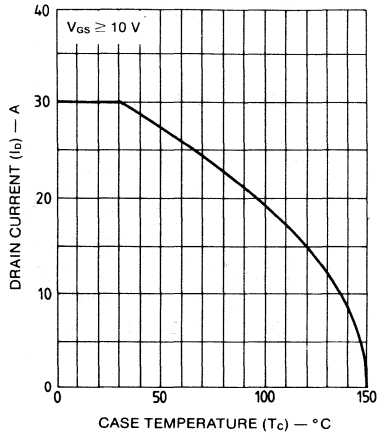


Fig. 10 - Maximum drain current vs. case temperature.

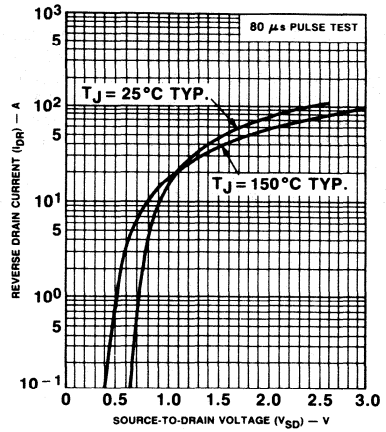


Fig. 11 - Typical source-drain diode forward voltage.

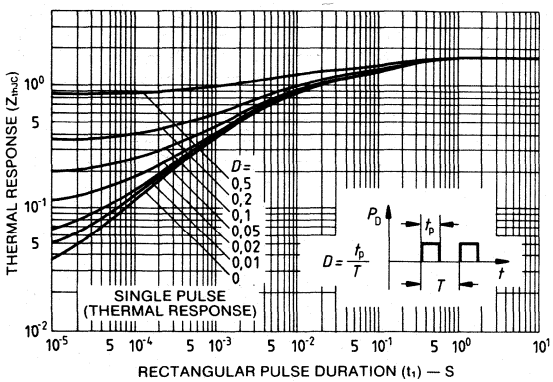


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

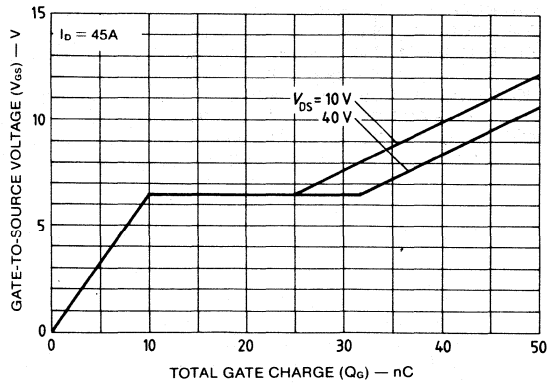


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 20

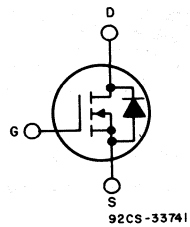
File Number **2254**

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 100 V
$r_{DS(on)}$ = 0.2 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

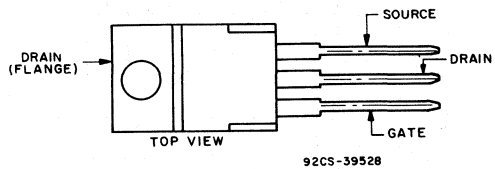


TERMINAL DIAGRAM

The BUZ 20 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 20 is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	100	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 55 °C	I_D	12	A
Pulsed T_C = 25 °C	I_{DM}	48	A
POWER DISSIPATION @ T_C = 25 °C	P_T	75	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 100$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 6$ A	—	0.15	0.2	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 6$ A	2.7	4.0	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V $f = 1$ MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	300	500	
Reverse Transfer Capacitance	C_{rss}		—	80	140	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.9$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	30 50	45 75	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	110 60	140 80	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	12	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	48	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.4	1.8	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$ $dI_F/dt = 100$ A/μs, $V_R = 30$ V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	1.6	—	μC

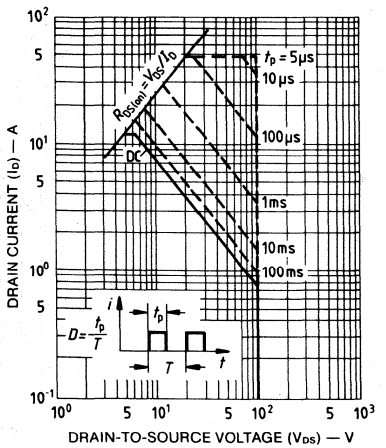


Fig. 1 - Maximum safe operating areas for all types.

BUZ 20

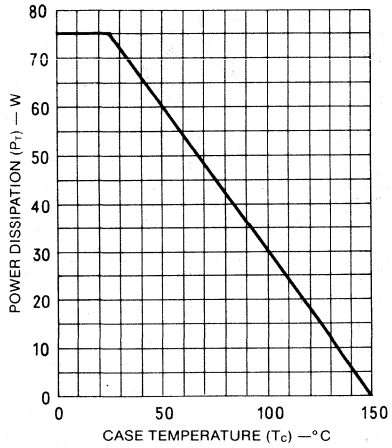


Fig. 2 - Power vs. temperature derating curve for all types.

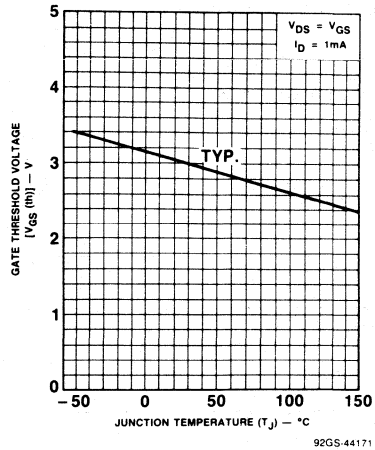


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

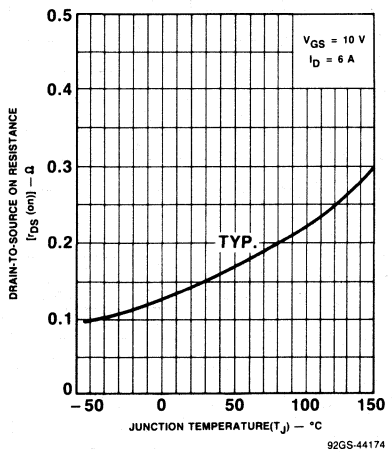


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

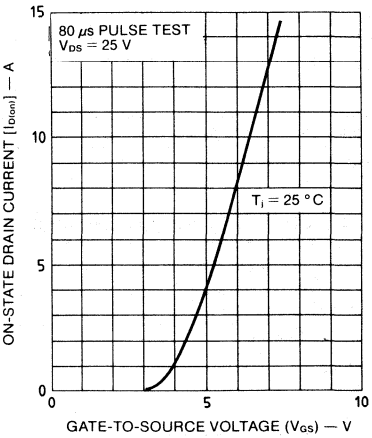


Fig. 5 - Typical transfer characteristics for all types.

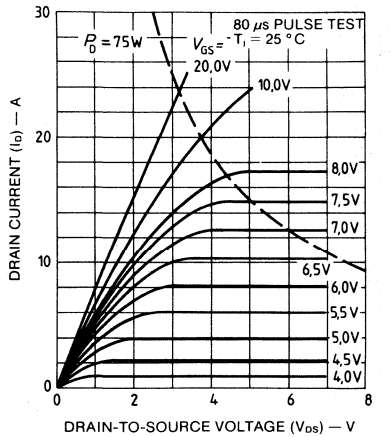


Fig. 6 - Typical output characteristics.

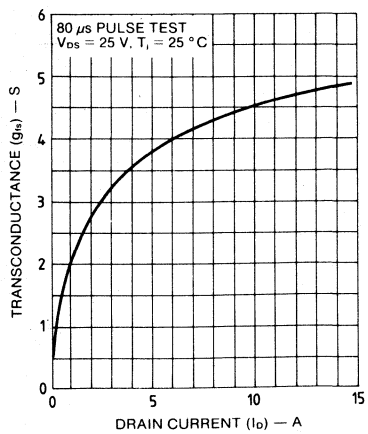


Fig. 7 - Typical transconductance vs. drain current.

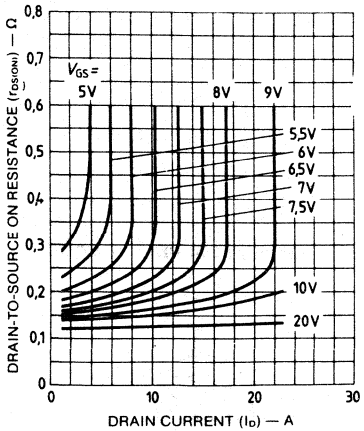


Fig. 8 - Typical on-resistance vs. drain current.

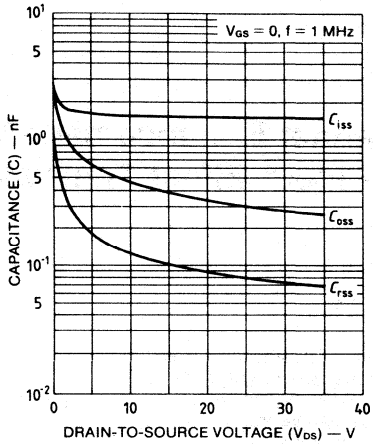


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

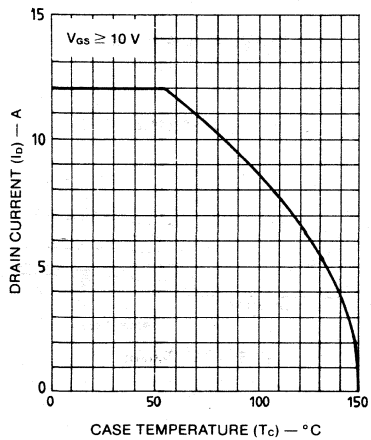


Fig. 10 - Maximum drain current vs. case temperature.

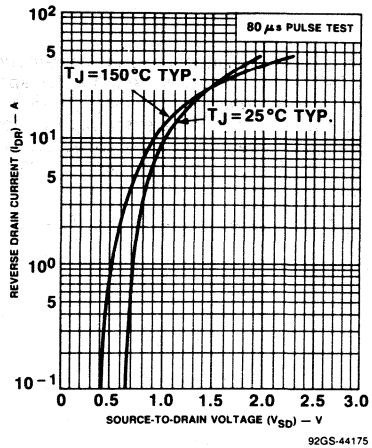


Fig. 11 - Typical source-drain diode forward voltage.

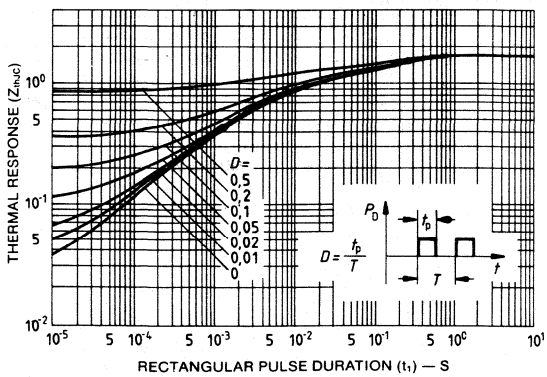


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

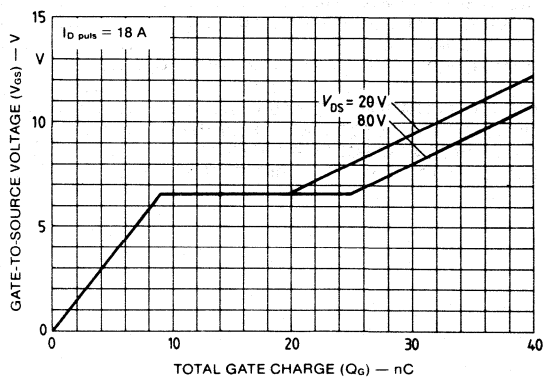


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 41 A

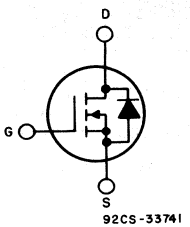
File Number **2256**

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5 A, 500 V
$r_{DS(on)}$ = 1.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

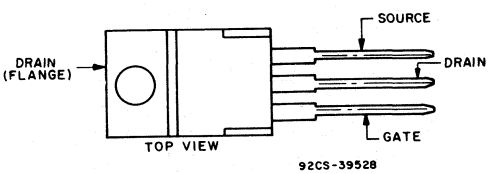


TERMINAL DIAGRAM

The BUZ 41 A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 41 A is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	500	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 35 °C	I_D	4.5	A
Pulsed T_C = 25 °C	I_{DM}	18	A
POWER DISSIPATION @ T_C = 25°C	P_T	75	W
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 500$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 2.5$ A	—	1.4	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 2.5$ A	1.5	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V $f = 1$ MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	110	170	
Reverse Transfer Capacitance	C_{rss}		—	40	70	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.6$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	30 40	45 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	110 50	140 65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	4.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	18	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.1	1.5	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}	$dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	6	—	μC

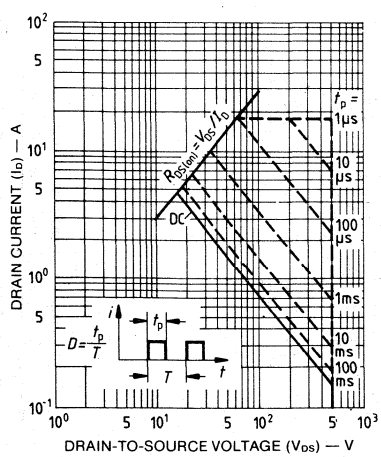


Fig. 1 - Maximum safe operating areas for all types.

BUZ 41 A

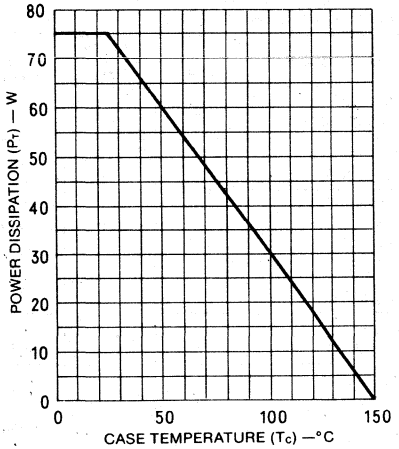


Fig. 2 - Power vs. temperature derating curve for all types.

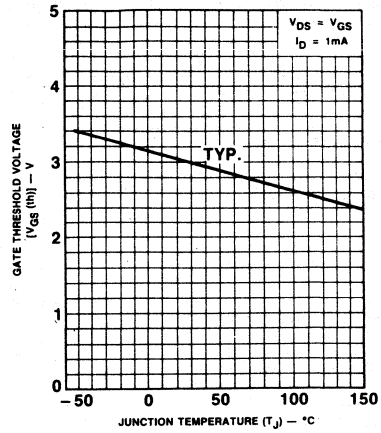


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

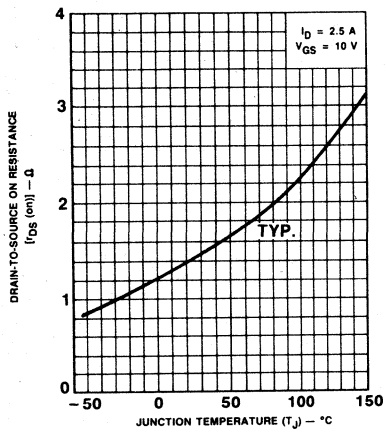


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

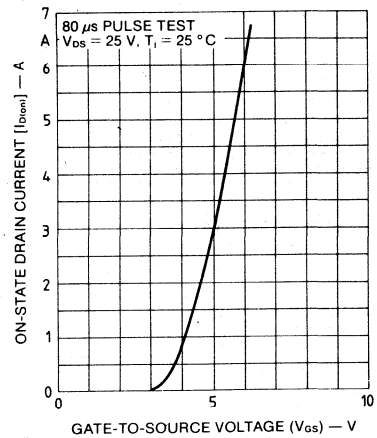


Fig. 5 - Typical transfer characteristics for all types.

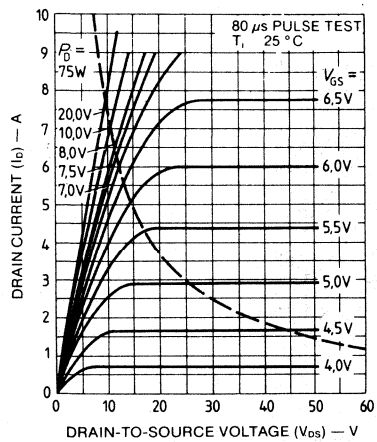


Fig. 6 - Typical output characteristics.

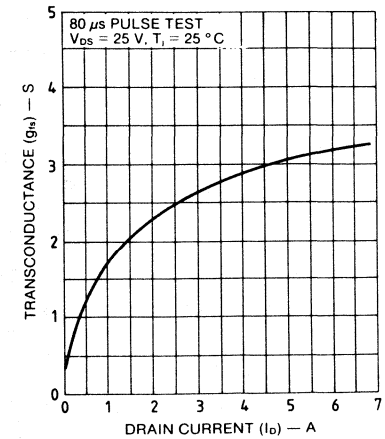


Fig. 7 - Typical transconductance vs. drain current.

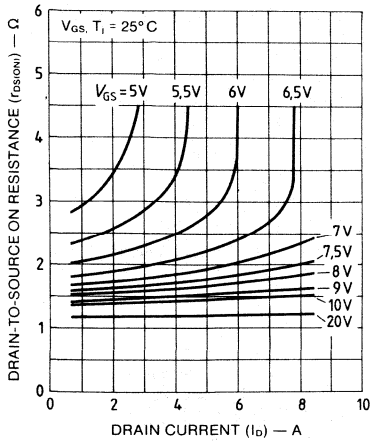


Fig. 8 - Typical on-resistance vs. drain current.

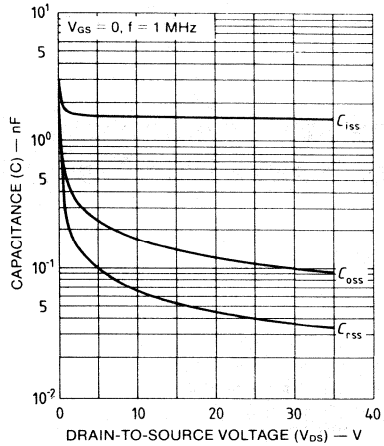


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

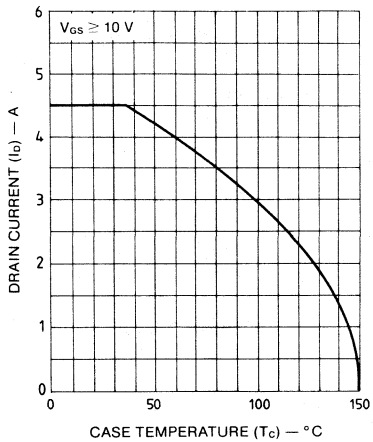


Fig. 10 - Maximum drain current vs. case temperature.

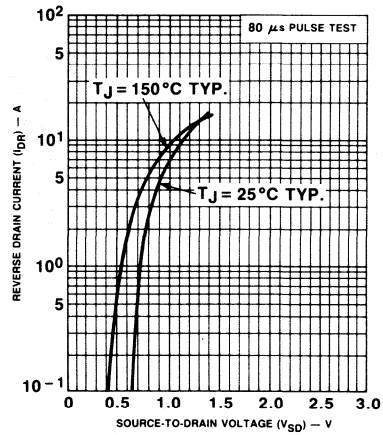


Fig. 11 - Typical source-drain diode forward voltage.

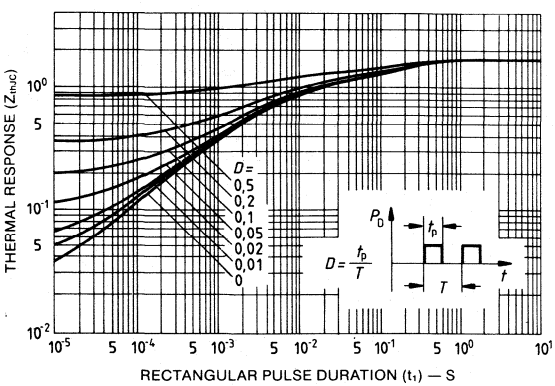


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

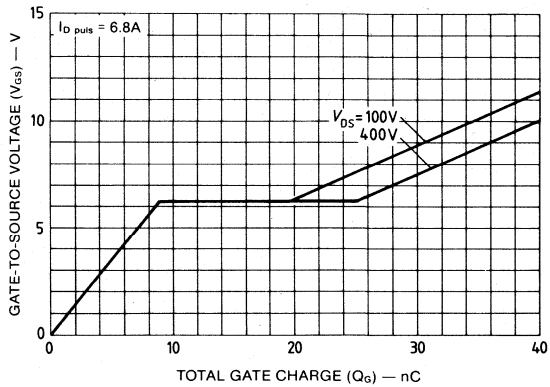


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 45

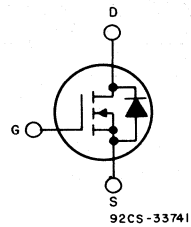
File No. 2257

N-Channel Enhancement-Mode Power Field-Effect Transistors

9.6 A, 500 V
$r_{DS(on)}$ = 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

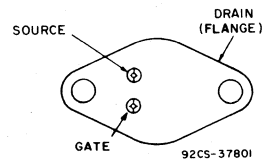


TERMINAL DIAGRAM

The BUZ 45 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 45 is supplied in the JEDEC TO-204AA plastic package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	500	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 25 °C	I_D	9.6	A
Pulsed T_C = 25 °C	I_{DM}	38	A
POWER DISSIPATION @ T_C = 25 °C	P_T	125	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 500$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 5$ A	—	0.55	0.6	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 5$ A	2.7	5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	
Reverse Transfer Capacitance	C_{rss}		—	100	170	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.8$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	50 80	75 120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	330 110	430 140	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 35			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	9.6	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	38	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}	$dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	12	—	μC

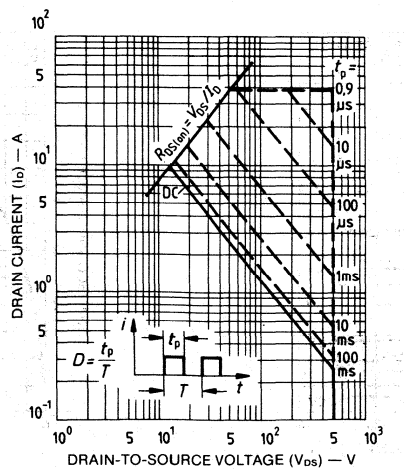


Fig. 1 - Maximum safe operating areas for all types.

BUZ 45

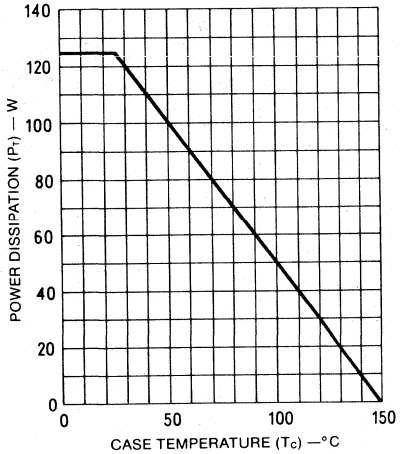


Fig. 2 - Power vs. temperature derating curve for all types.

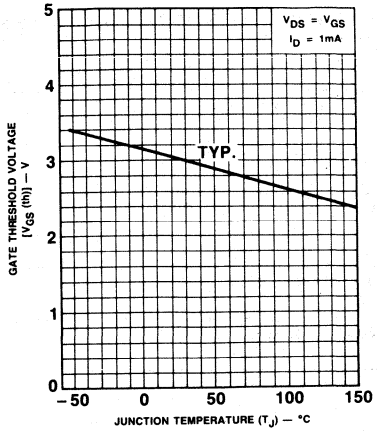


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

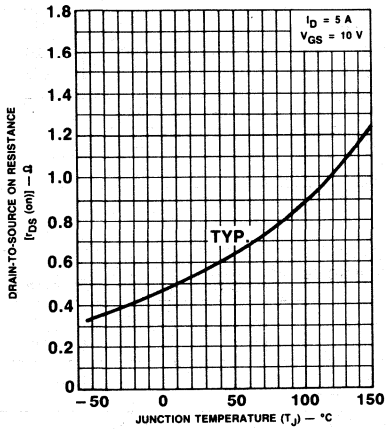


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

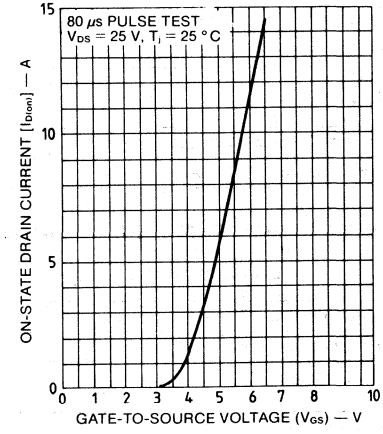


Fig. 5 - Typical transfer characteristics for all types.

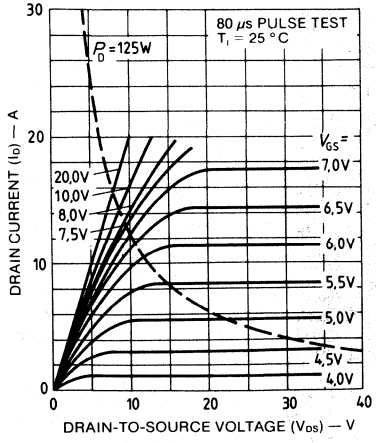


Fig. 6 - Typical output characteristics.

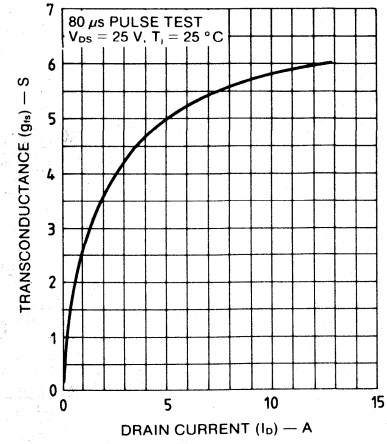


Fig. 7 - Typical transconductance vs. drain current.

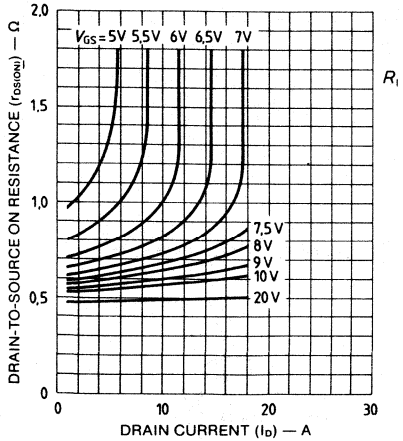


Fig. 8 - Typical on-resistance vs. drain current.

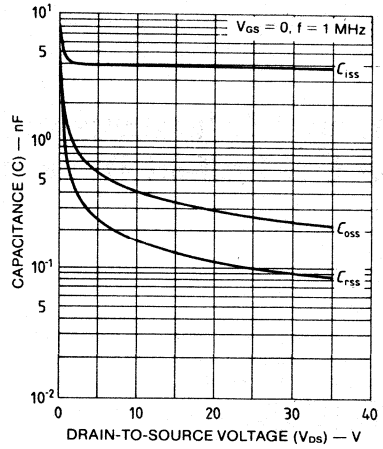


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

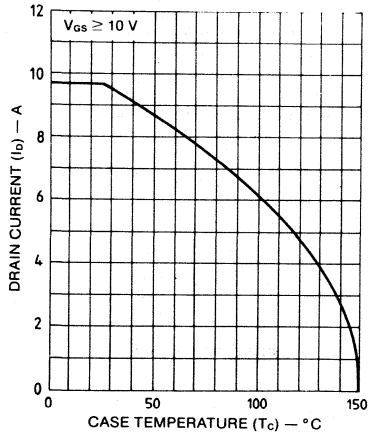


Fig. 10 - Maximum drain current vs. case temperature.

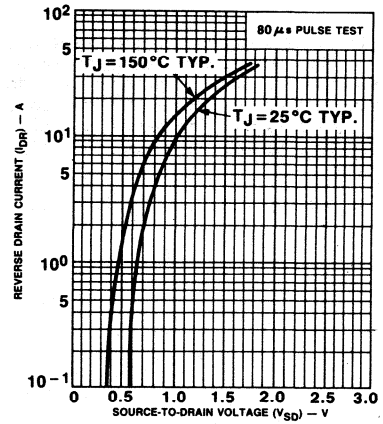


Fig. 11 - Typical source-drain diode forward voltage.

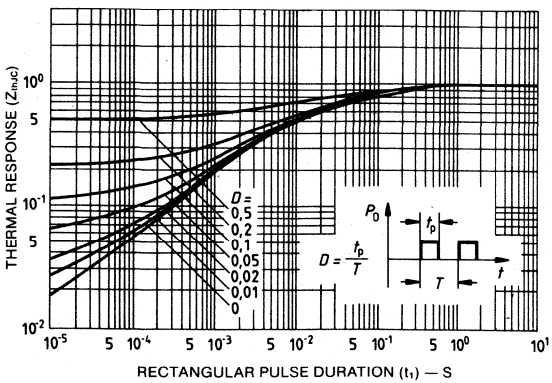


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

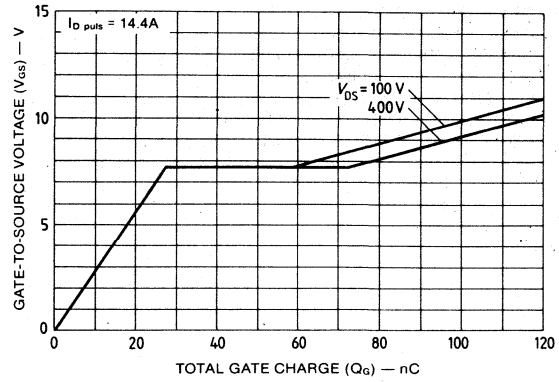


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 45 A

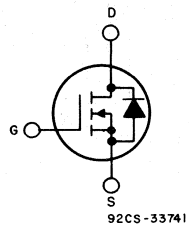
File Number **2258**

N-Channel Enhancement-Mode Power Field-Effect Transistors

8.3 A, 500 V
$r_{DS(on)}$ = 0.8 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

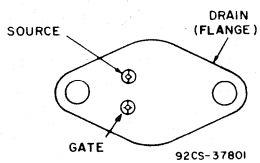


TERMINAL DIAGRAM

The BUZ 45 A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 45 A is supplied in the JEDEC TO-204AA plastic package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	500	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 25 °C	I_D	8.3	A
Pulsed T_C = 25 °C	I_{DM}	33	A
POWER DISSIPATION @ T_C = 25° C	P_T	125	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	—	0.7	0.8	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	pF
Reverse Transfer Capacitance	C_{rss}		—	100	170	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.8 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	50	75	ns
	t_r		—	80	120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	330	430	ns
	t_r		—	110	140	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 35		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	8.3	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	33	A
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.6	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}, dI_F/dt = 100 A/μs, V_R = 100 V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	12	—	μC

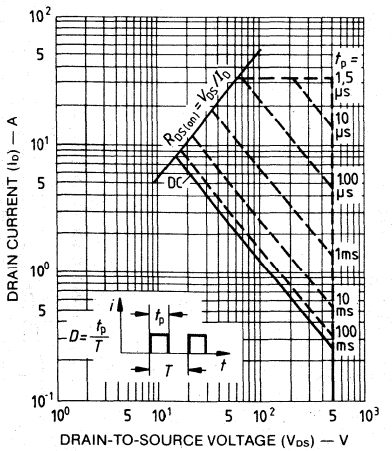


Fig. 1 - Maximum safe operating areas for all types.

BUZ 45 A

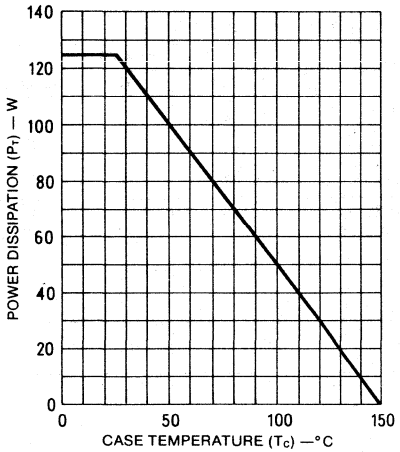


Fig. 2 - Power vs. temperature derating curve for all types.

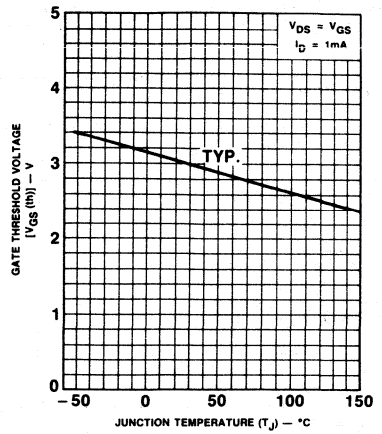


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

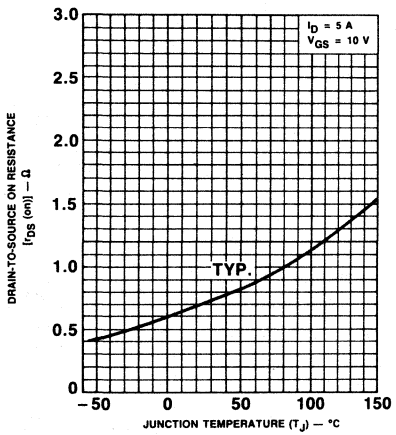


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

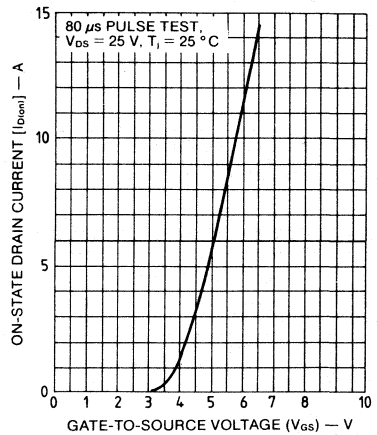


Fig. 5 - Typical transfer characteristics for all types.

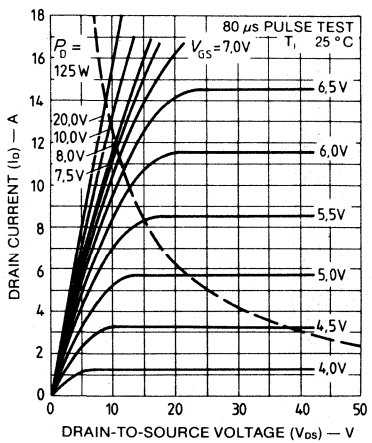


Fig. 6 - Typical output characteristics.

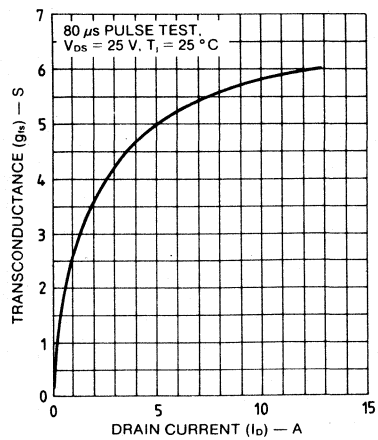


Fig. 7 - Typical transconductance vs. drain current.

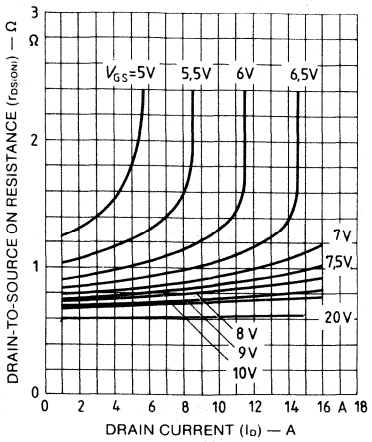


Fig. 8 - Typical on-resistance vs. drain current.

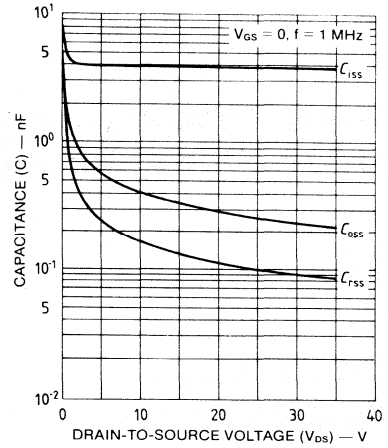


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

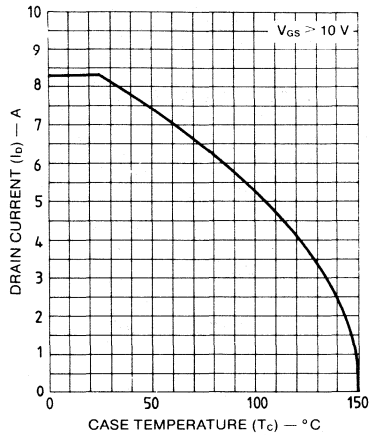


Fig. 10 - Maximum drain current vs. case temperature.

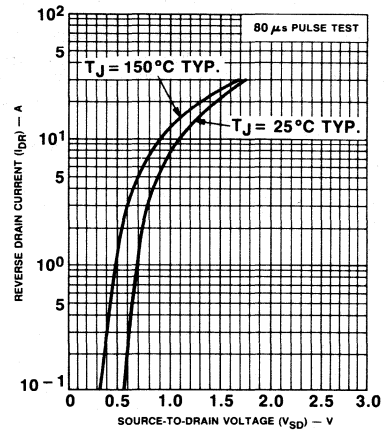


Fig. 11 - Typical source-drain diode forward voltage.

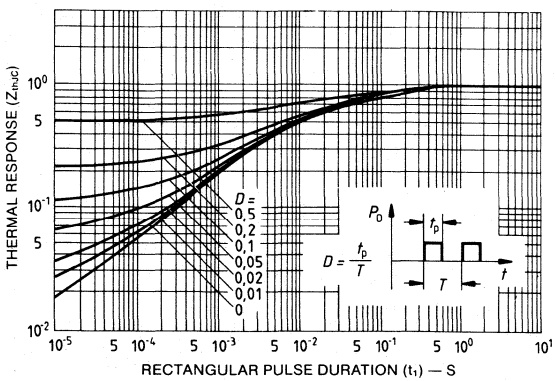


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

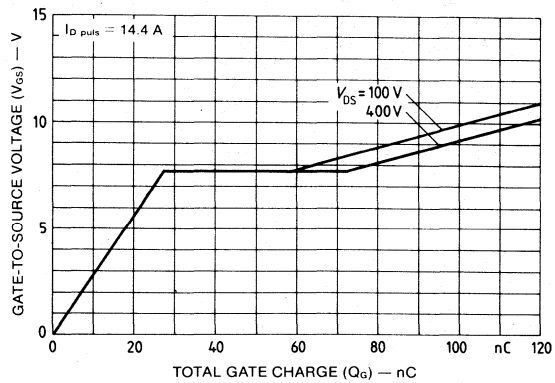


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 45 B

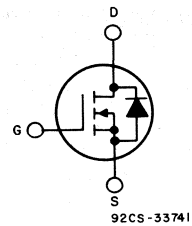
File Number **2259**

N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 500 V
$r_{DS(on)}$ = 0.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

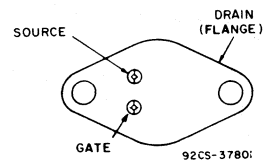


TERMINAL DIAGRAM

The BUZ 45 B is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 45 B is supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	500	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 35 °C	I_D	10	A
Pulsed T_C = 25 °C	I_{DM}	40	A
POWER DISSIPATION @ T_C = 25 °C	P_T	125	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	—	0.49	0.50	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	pF
Reverse Transfer Capacitance	C_{rss}		—	100	170	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.9 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	50	75	ns
	t_r		—	80	120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	330	430	ns
	t_f		—	110	140	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 35		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	10	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	40	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, $I_F = I_{DR}$, dI_F/dt = 100 A/μs, V_R = 100 V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	12	—	μC

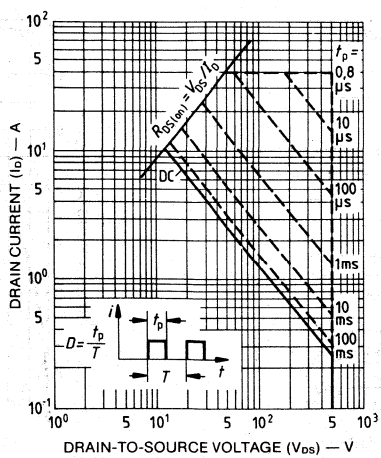


Fig. 1 - Maximum safe operating areas for all types.

BUZ 45 B

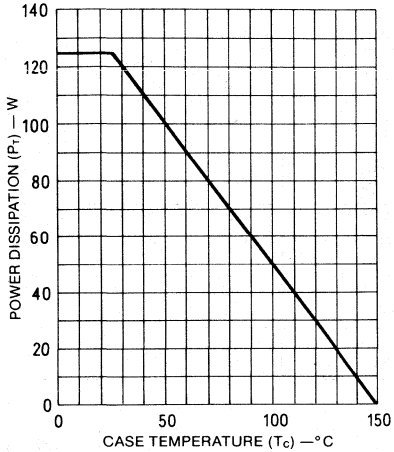


Fig. 2 - Power vs. temperature derating curve for all types.

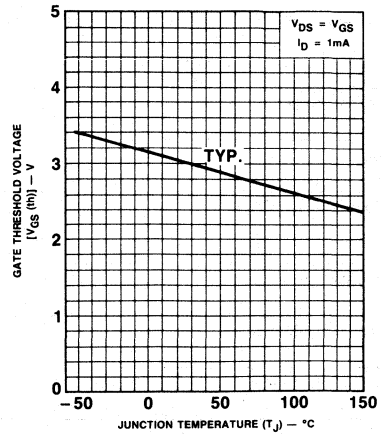


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

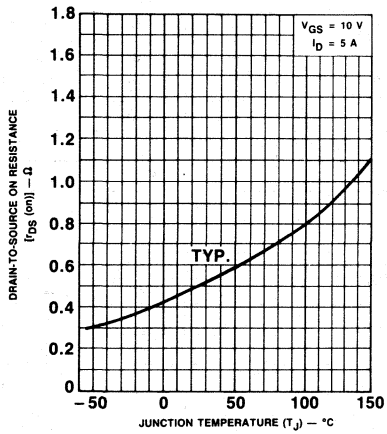


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

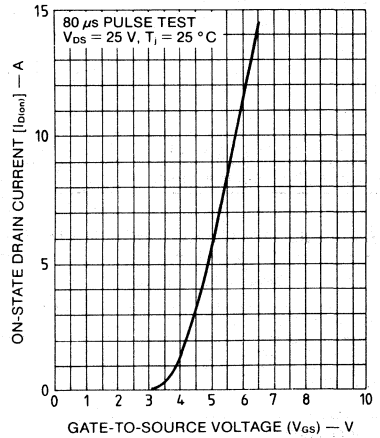


Fig. 5 - Typical transfer characteristics for all types.

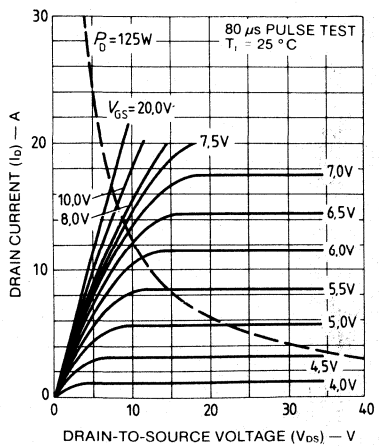


Fig. 6 - Typical output characteristics.

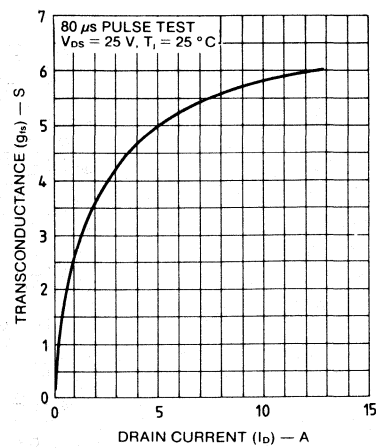


Fig. 7 - Typical transconductance vs. drain current.

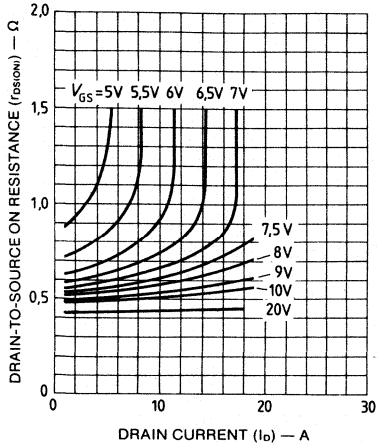


Fig. 8 - Typical on-resistance vs. drain current.

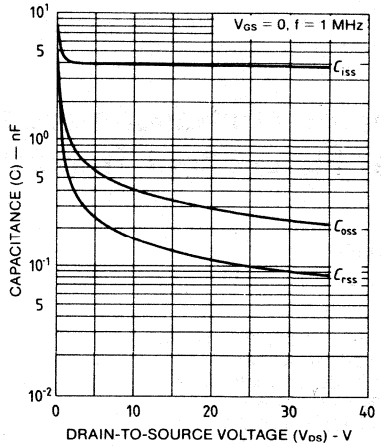


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

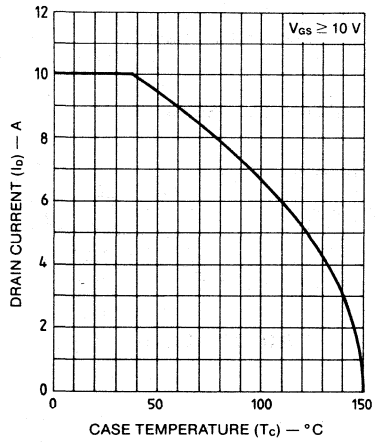


Fig. 10 - Maximum drain current vs. case temperature.

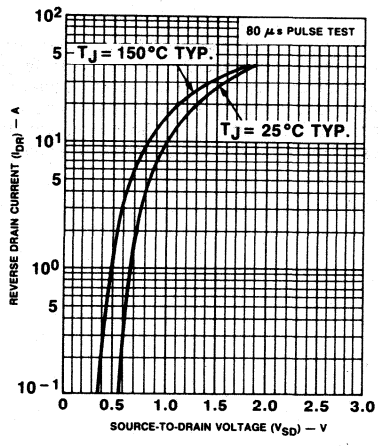


Fig. 11 - Typical source-drain diode forward voltage.

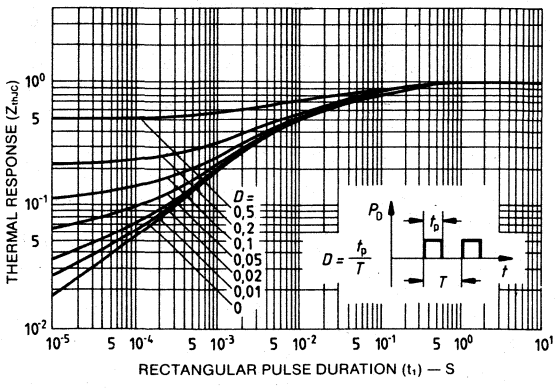


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

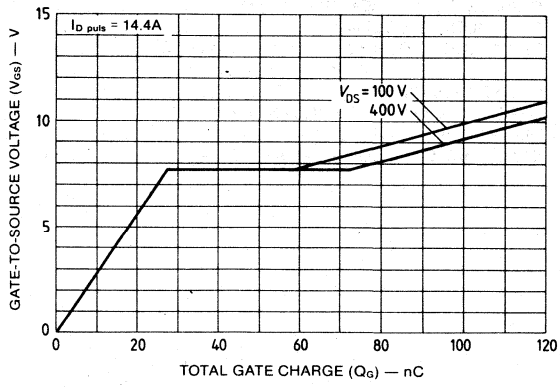


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 60

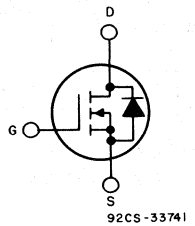
File Number **2260**

N-Channel Enhancement-Mode Power Field-Effect Transistors

5.5 A, 400 V
$r_{DS(on)}$ = 1.0 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

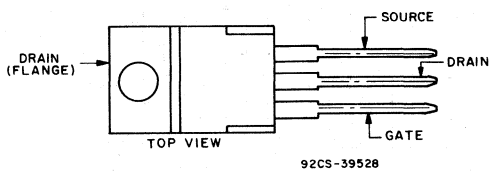


TERMINAL DIAGRAM

The BUZ 60 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 60 is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	400	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 35 °C	I_D	5.5	A
Pulsed T_C = 25 °C	I_{DM}	22	A
POWER DISSIPATION @ T_C = 25 °C	P_T	75	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 400 V, V_{GS} = 0 V	—	20	250	µA
		T_j = 125 °C, V_{DS} = 400 V, V_{GS} = 0 V	—	100	1000	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A	—	0.9	1	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 2.5 A	1.7	2.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	1.5	2	pF
Output Capacitance	C_{oss}		—	120	180	pF
Reverse Transfer Capacitance	C_{rss}		—	35	60	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.7 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	30	45	ns
	t_r		—	40	60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	110	140	ns
	t_r		—	50	65	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	5.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	22	A
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.15	1.6	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}, dI_F/dt = 100 A/µs, V_R = 100 V	—	1000	—	ns
Reverse Recovered Charge	Q_{RR}		—	5	—	µC

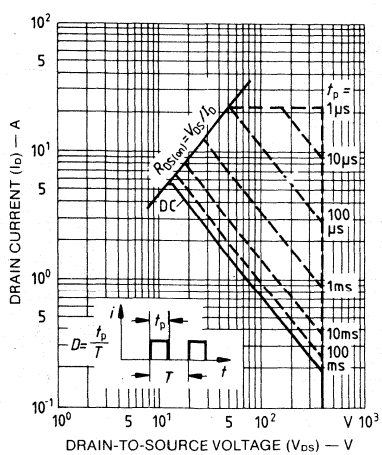


Fig. 1 - Maximum safe operating areas for all types.

BUZ 60

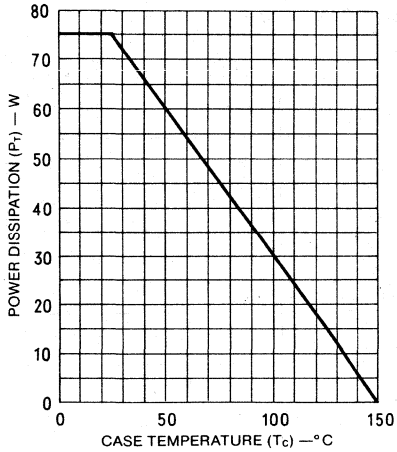


Fig. 2 - Power vs. temperature derating curve for all types.

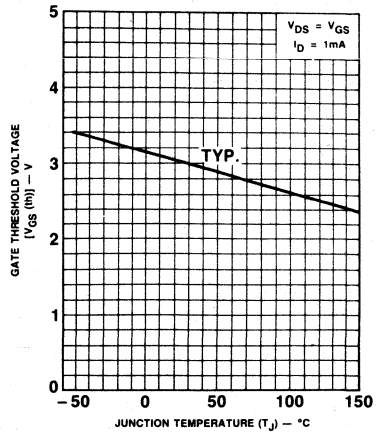


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

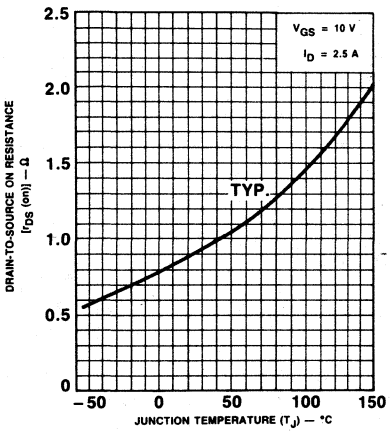


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

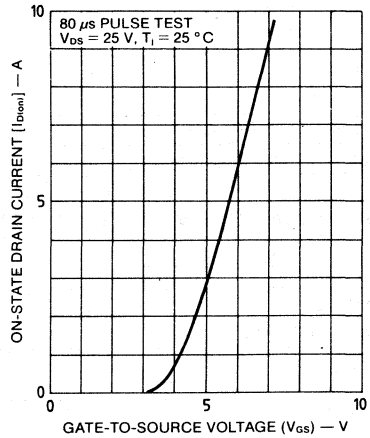


Fig. 5 - Typical transfer characteristics for all types.

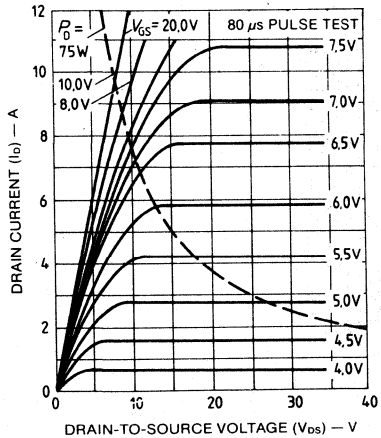


Fig. 6 - Typical output characteristics.

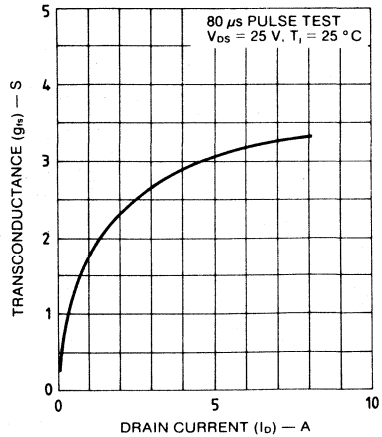


Fig. 7 - Typical transconductance vs. drain current.

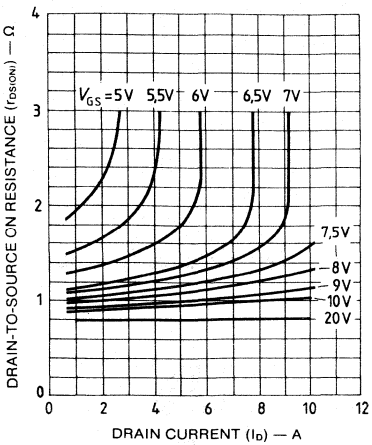


Fig. 8 - Typical on-resistance vs. drain current.

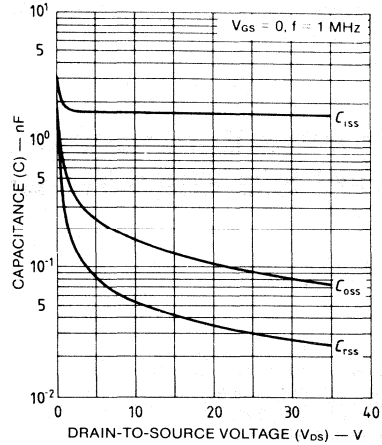


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

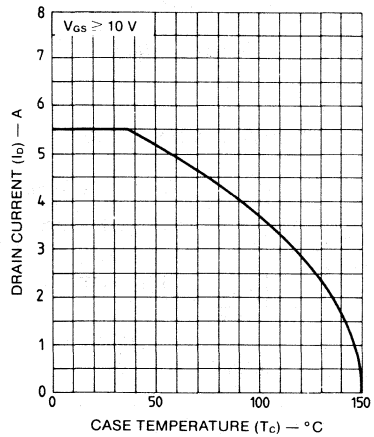


Fig. 10 - Maximum drain current vs. case temperature.

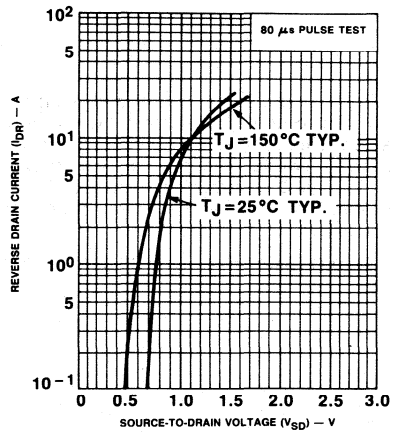


Fig. 11 - Typical source-drain diode forward voltage.

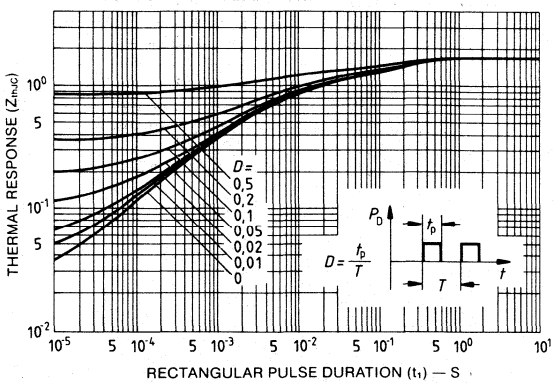


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

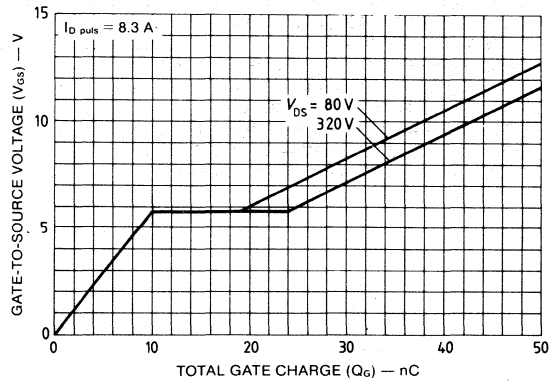


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 60 B

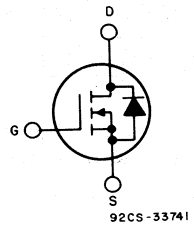
File Number **2261**

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5 A, 400 V
$r_{DS(on)}$ = 1.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

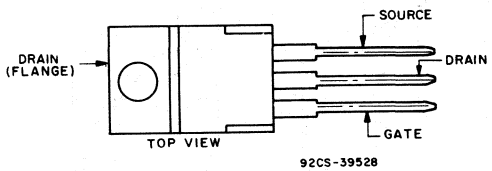


TERMINAL DIAGRAM

The BUZ 60 B is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 60 B is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	400	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 35 °C	I_D	4.5	A
Pulsed T_C = 25 °C	I_{DM}	18	A
POWER DISSIPATION @ T_C = 25 °C	P_T	75	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 400$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 2.5$ A	—	1.2	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 2.5$ A	1.7	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V f = 1 MHz	—	1.5	2	pF
Output Capacitance	C_{oss}		—	120	180	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.6$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	30 40	45 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$ t_f		— —	110 50	140 65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	1.7	4.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	18	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.15	1.50	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$ $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	1000	—	ns
Reverse Recovered Charge	Q_{RR}		—	5	—	μC

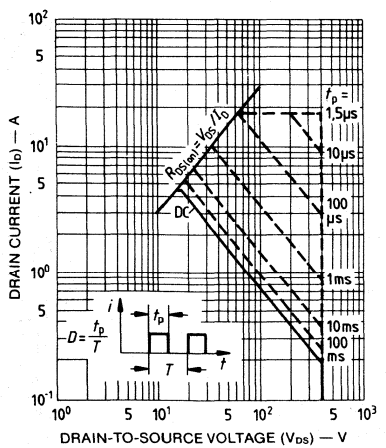


Fig. 1 - Maximum safe operating areas for all types.

BUZ 60

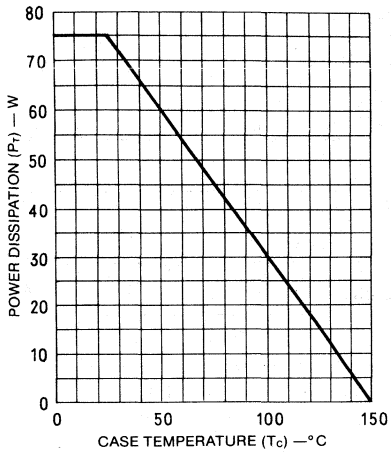


Fig. 2 - Power vs. temperature derating curve for all types.

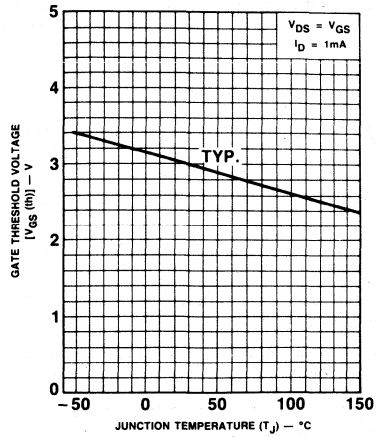


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

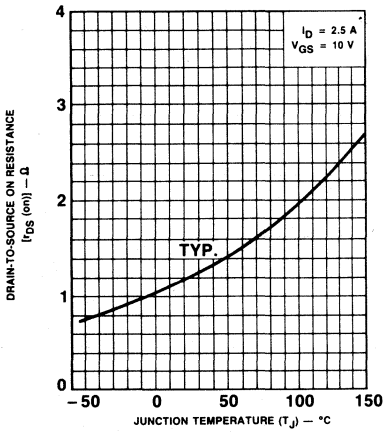


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

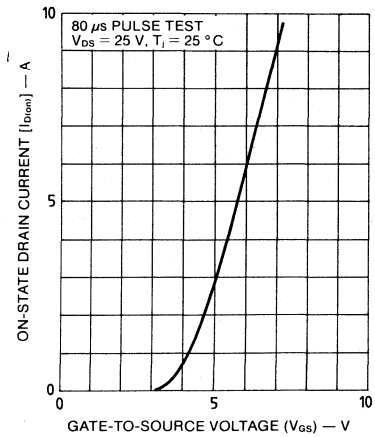


Fig. 5 - Typical transfer characteristics for all types.

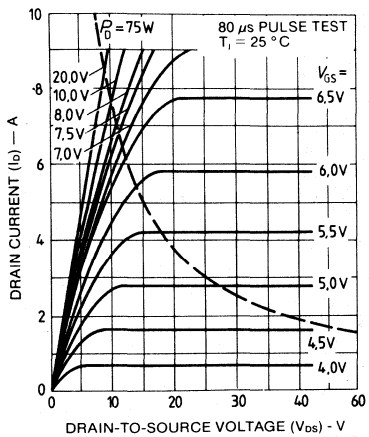


Fig. 6 - Typical output characteristics.

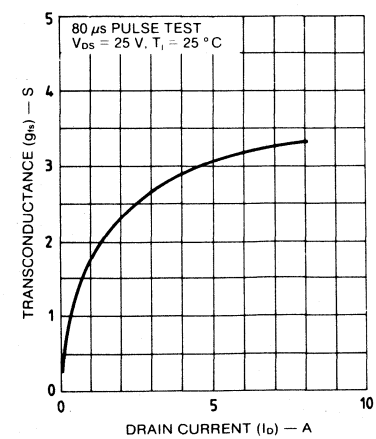


Fig. 7 - Typical transconductance vs. drain current.

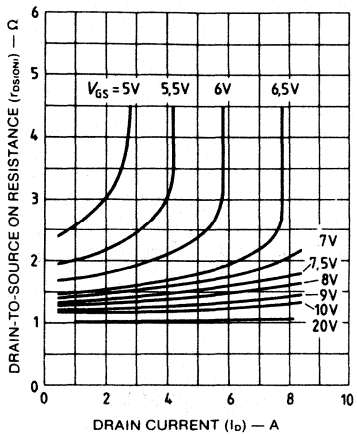


Fig. 8 - Typical on-resistance vs. drain current.

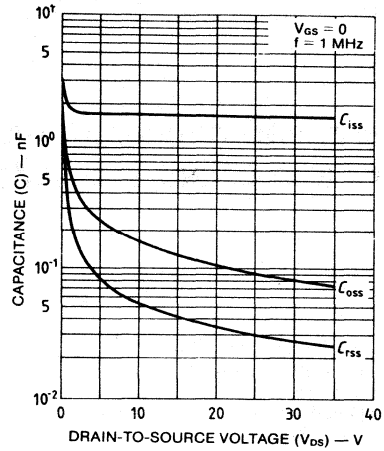


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

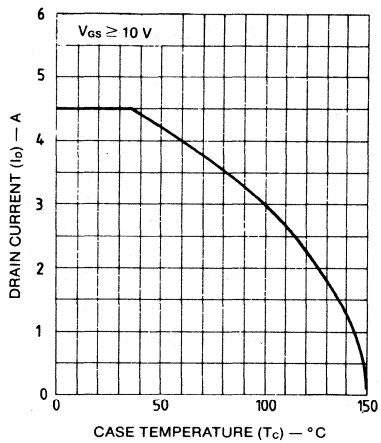


Fig. 10 - Maximum drain current vs. case temperature.

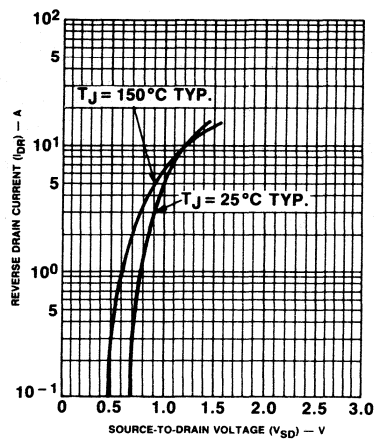


Fig. 11 - Typical source-drain diode forward voltage.

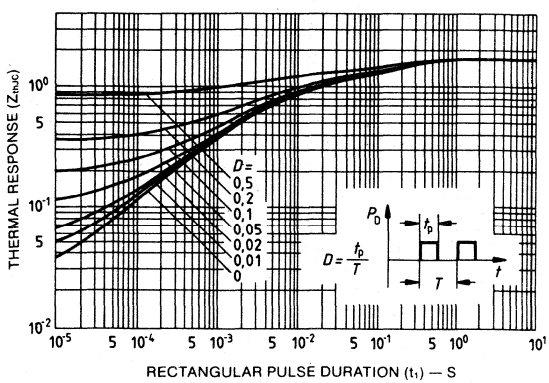


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

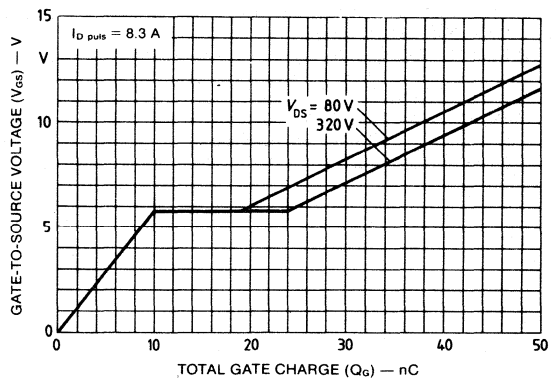


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 72 A

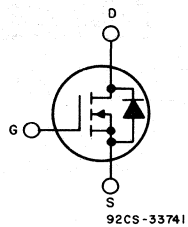
File Number **2262**

N-Channel Enhancement-Mode Power Field-Effect Transistors

9 A, 100 V
$r_{DS(on)}$ = 0.25 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

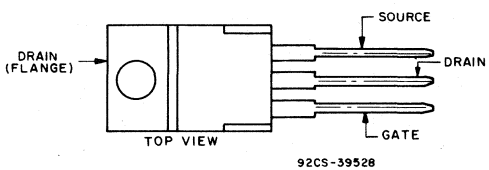


TERMINAL DIAGRAM

The BUZ 72 A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 72 A is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	100	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 25 °C	I_D	9	A
Pulsed T_C = 25 °C	I_{DM}	36	A
POWER DISSIPATION @ T_C = 25 °C	P_T	40	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 100$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 5$ A	—	0.23	0.25	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 5$ A	2.7	3.8	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V f = 1 MHz	—	450	600	pF
Output Capacitance	C_{oss}		—	150	240	
Reverse Transfer Capacitance	C_{rss}		—	80	130	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.9$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	20 45	30 70	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	70 55	90 70	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 3.1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	9	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	36	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.5	2	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$	—	170	—	ns
Reverse Recovered Charge	Q_{RR}	$dI_F/dt = 100$ A/μs, $V_R = 30$ V	—	0.30	—	μC

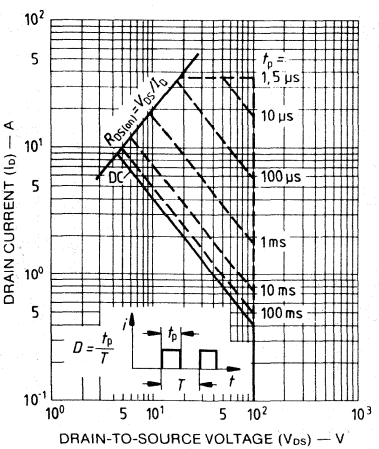


Fig. 1 - Maximum safe operating areas for all types.

BUZ 72 A

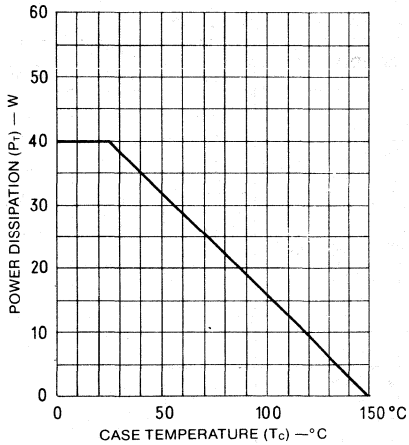


Fig. 2 - Power vs. temperature derating curve for all types.

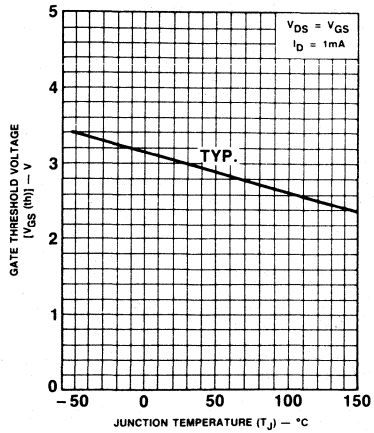


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

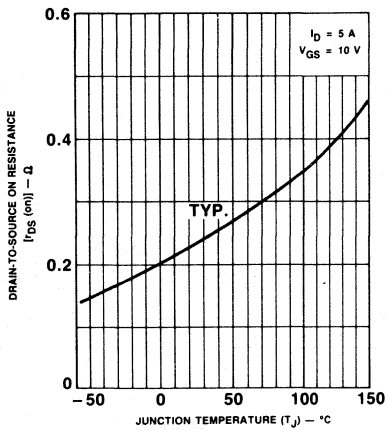


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

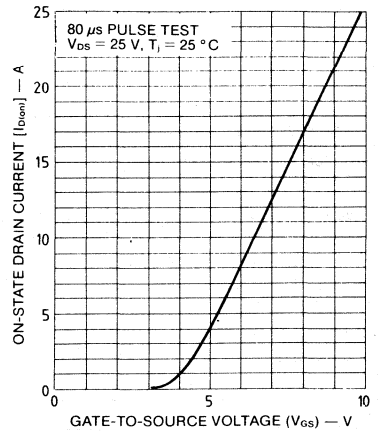


Fig. 5 - Typical transfer characteristics for all types.

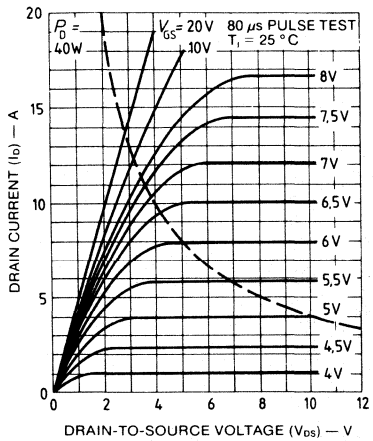


Fig. 6 - Typical output characteristics.

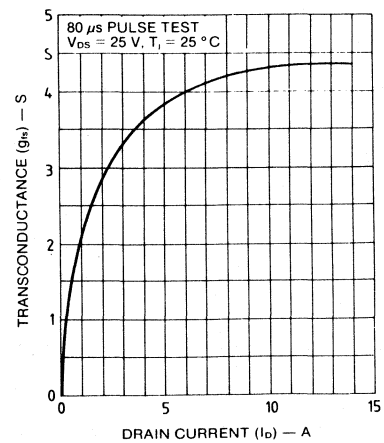


Fig. 7 - Typical transconductance vs. drain current.

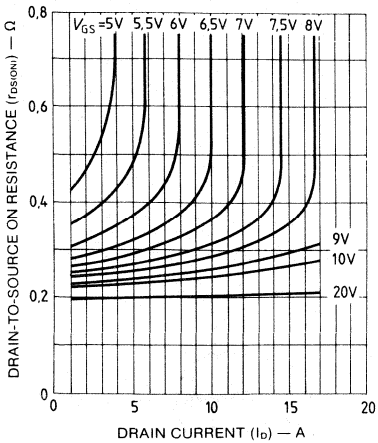


Fig. 8 - Typical on-resistance vs. drain current.

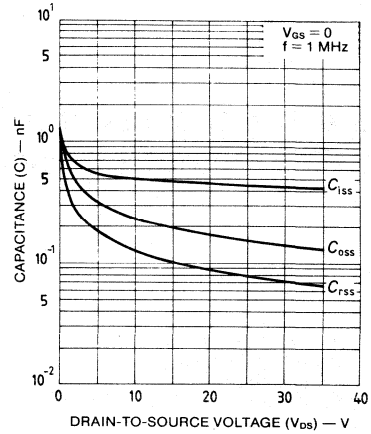


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

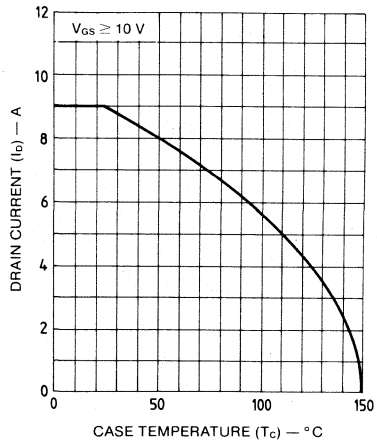


Fig. 10 - Maximum drain current vs. case temperature.

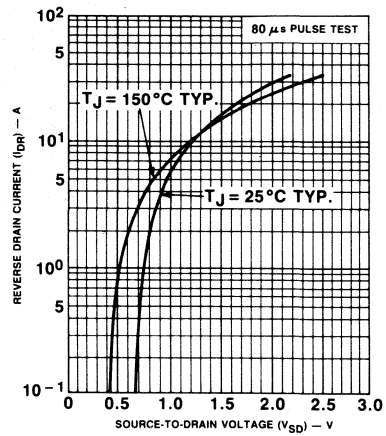


Fig. 11 - Typical source-drain diode forward voltage.

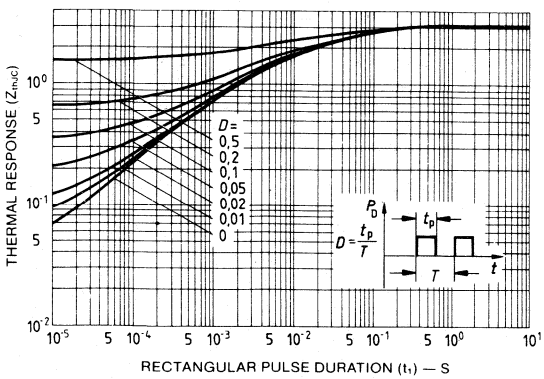


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

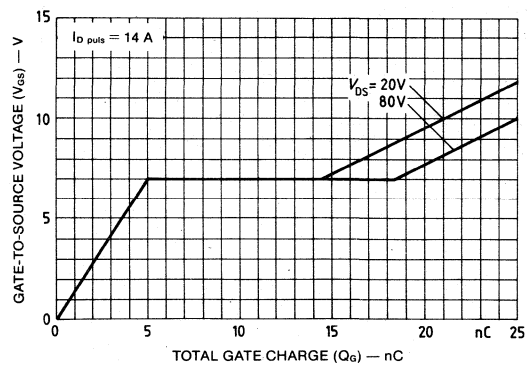


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 73 A

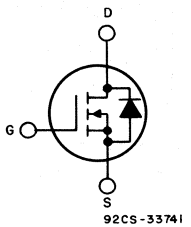
File Number **2263**

N-Channel Enhancement-Mode Power Field-Effect Transistors

5.8 A, 200 V
$r_{DS(on)}$ = 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

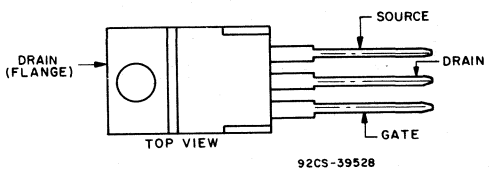


TERMINAL DIAGRAM

The BUZ 73 A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 73 A is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	200	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 25 °C	I_D	5.8	A
Pulsed T_C = 25 °C	I_{DM}	23	A
POWER DISSIPATION @ T_C = 25 °C	P_T	40	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V, $I_D = 0.25$ mA	200	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C, $V_{DS} = 200$ V, $V_{GS} = 0$ V	—	20	250	μA
		$T_j = 125$ °C, $V_{DS} = 200$ V, $V_{GS} = 0$ V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V, $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 3.5$ A	—	0.5	0.6	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V, $I_D = 3.5$ A	2.2	3.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	—	450	600	pF
Output Capacitance	C_{oss}		—	100	160	pF
Reverse Transfer Capacitance	C_{rss}		—	50	80	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	$V_{CC} = 30$ V, $I_D = 2.8$ A, $V_{GS} = 10$ V, $R_{GS} = 50$ Ω	—	15	20	ns
	t_r		—	40	60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	70	90	ns
	t_f		—	40	55	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 3.1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	5.8	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	23	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.4	1.7	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$, $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	0.6	—	μC

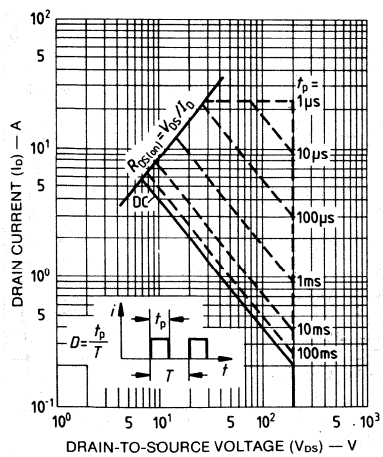


Fig. 1 - Maximum safe operating areas for all types.

BUZ 73 A

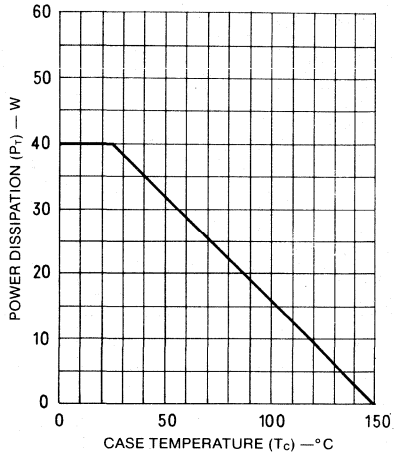


Fig. 2 - Power vs. temperature derating curve for all types.

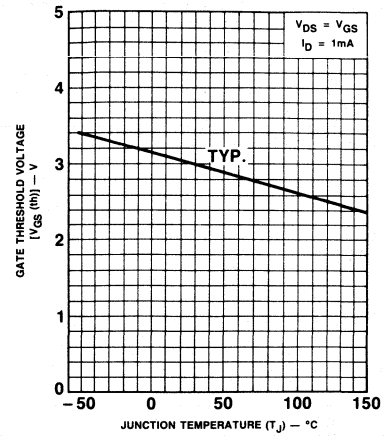


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

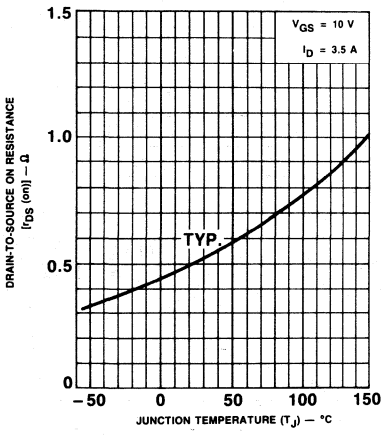


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

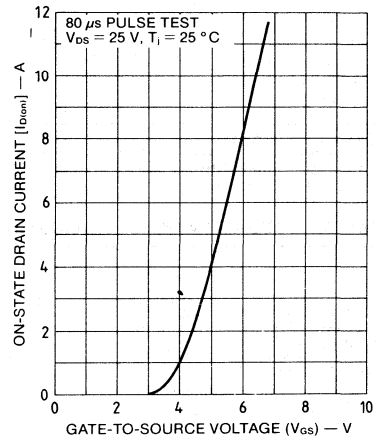


Fig. 5 - Typical transfer characteristics for all types.

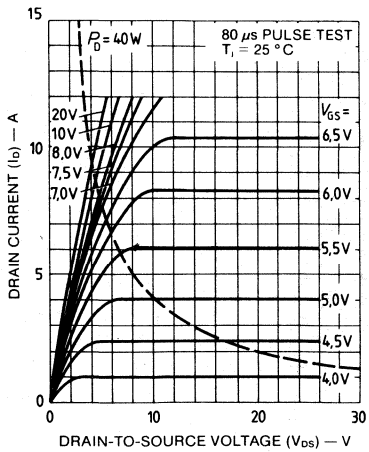


Fig. 6 - Typical output characteristics.

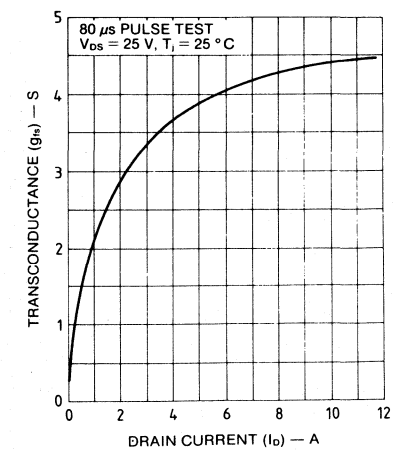


Fig. 7 - Typical transconductance vs. drain current.

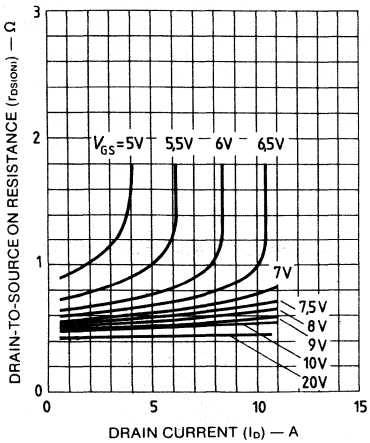


Fig. 8 - Typical on-resistance vs. drain current.

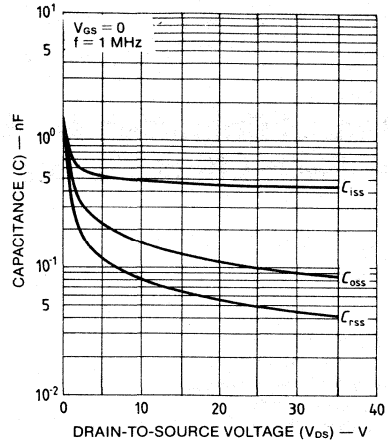


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

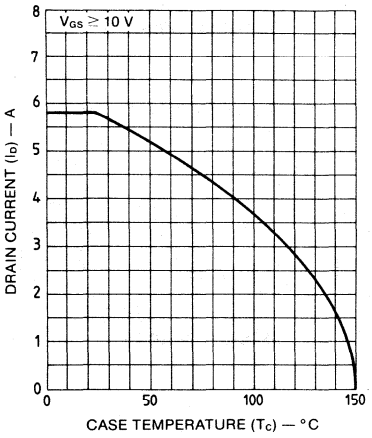


Fig. 10 - Maximum drain current vs. case temperature.

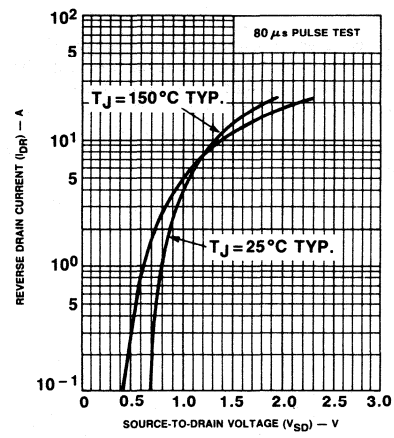


Fig. 11 - Typical source-drain diode forward voltage.

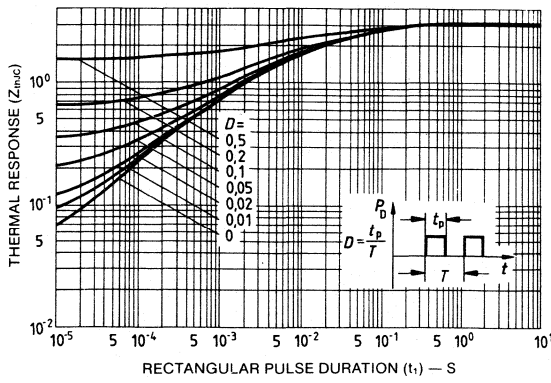


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

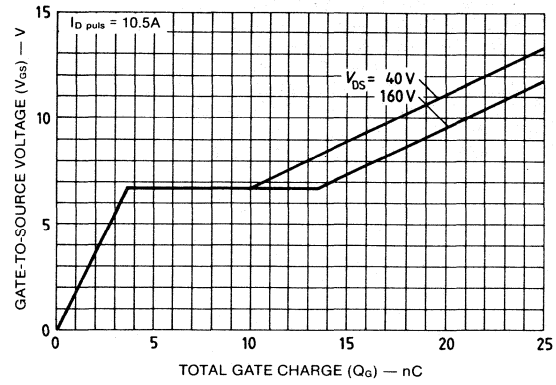


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 76

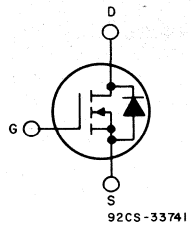
File Number **2264**

N-Channel Enhancement-Mode Power Field-Effect Transistors

3 A, 400 V
$r_{DS(on)}$ = 1.8 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

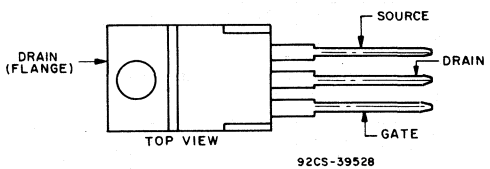


TERMINAL DIAGRAM

The BUZ 76 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 76 is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	400	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 35 °C	I_D	3	A
Pulsed T_C = 25 °C	I_{DM}	12	A
POWER DISSIPATION @ T_C = 25 °C	P_T	40	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 400$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 1.5$ A	—	1.65	1.8	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 1.5$ A	2.1	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V f = 1 MHz	—	300	500	pF
Output Capacitance	C_{oss}		—	50	80	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.5$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	15 40	20 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$ t_f		— —	50 30	65 40	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 3.1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	3	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	12	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.1	1.4	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$	—	300	—	ns
Reverse Recovered Charge	Q_{RR}	$dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	2.5	—	μC

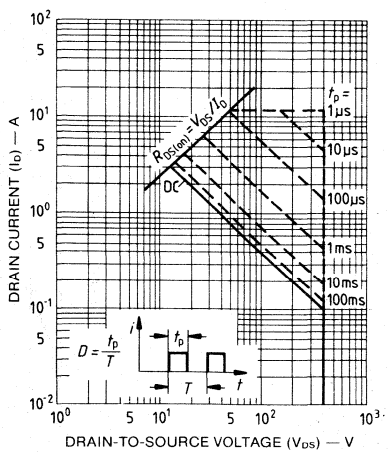


Fig. 1 - Maximum safe operating areas for all types.

BUZ 76

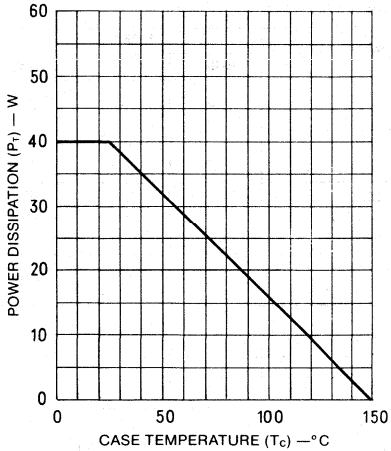


Fig. 2 - Power vs. temperature derating curve for all types.

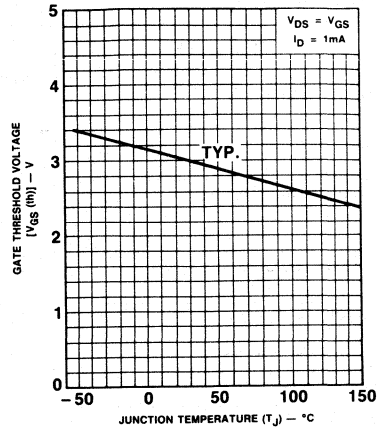


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

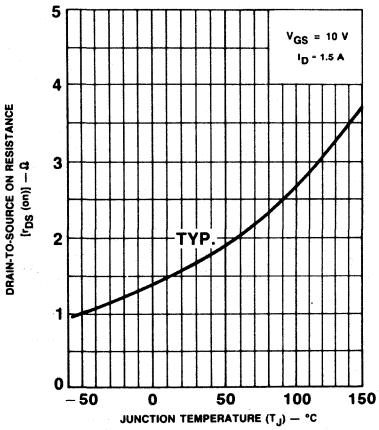


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

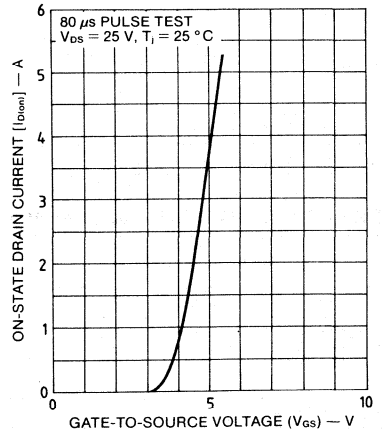


Fig. 5 - Typical transfer characteristics for all types.

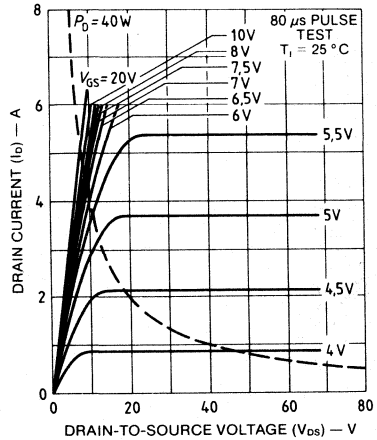


Fig. 6 - Typical output characteristics.

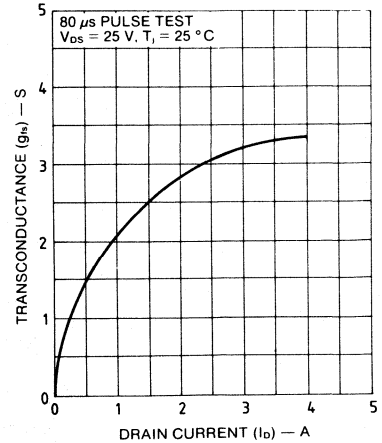


Fig. 7 - Typical transconductance vs. drain current.

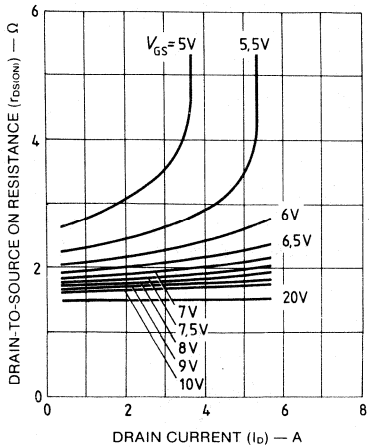


Fig. 8 - Typical on-resistance vs. drain current.

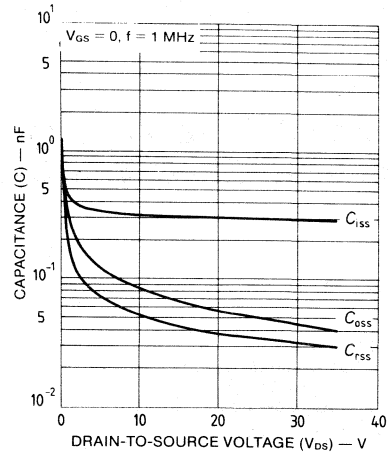


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

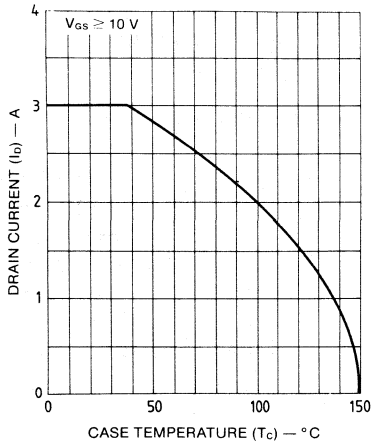


Fig. 10 - Maximum drain current vs. case temperature.

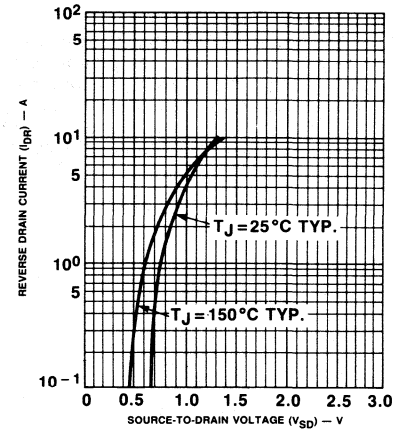


Fig. 11 - Typical source-drain diode forward voltage.

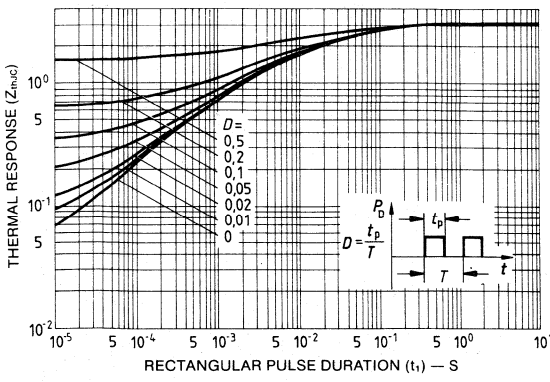


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

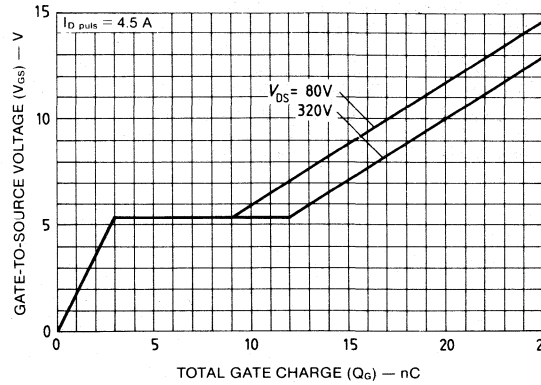


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

BUZ 76 A

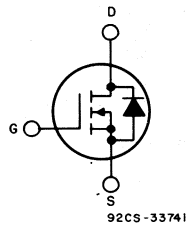
File No. 2265

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.6 A, 400 V
$r_{DS(on)}$ = 2.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

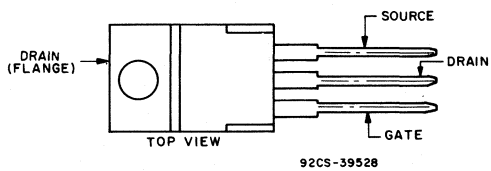


TERMINAL DIAGRAM

The BUZ 76 A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 76 A is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	400	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 30 °C	I_D	2.6	A
Pulsed T_C = 25 °C	I_{DM}	10	A
POWER DISSIPATION @ T_C = 25 °C	P_T	40	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 400$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 1.5$ A	—	2.2	2.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 1.5$ A	2.1	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V $f = 1$ MHz	—	300	500	pF
Output Capacitance	C_{oss}		—	50	80	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.4$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	15 40	20 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	50 30	65 40	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 3.1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	2.6	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	10	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.1	1.4	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$ $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	300	—	ns
Reverse Recovered Charge	Q_{RR}		—	2.5	—	μC

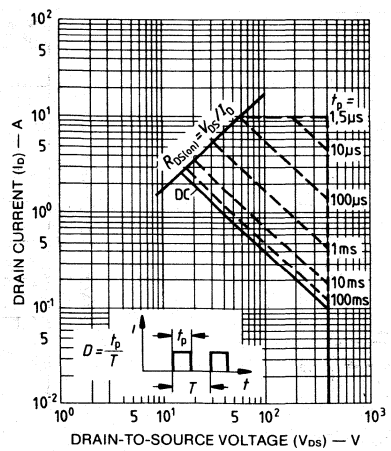


Fig. 1 - Maximum safe operating areas for all types.

BUZ 76 A

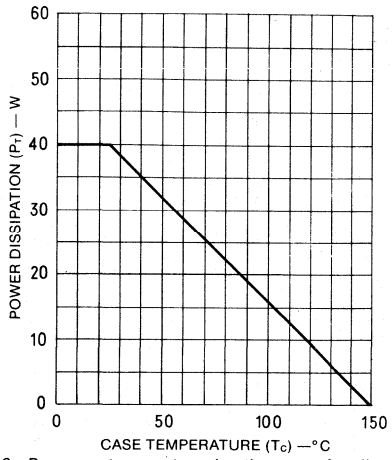


Fig. 2 - Power vs. temperature derating curve for all types.

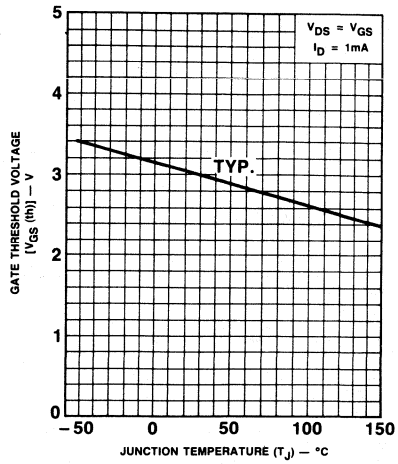


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

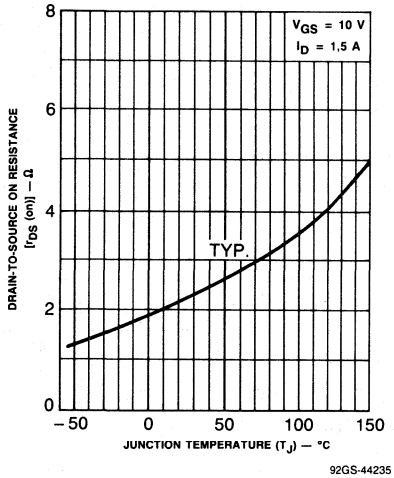


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

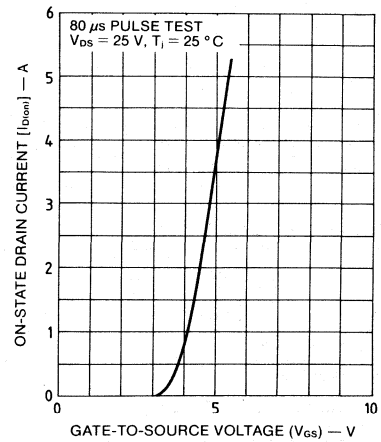


Fig. 5 - Typical transfer characteristics for all types.

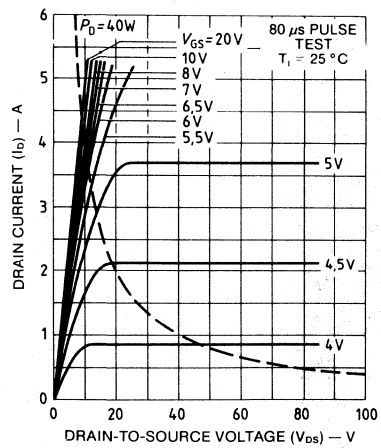


Fig. 6 - Typical output characteristics.

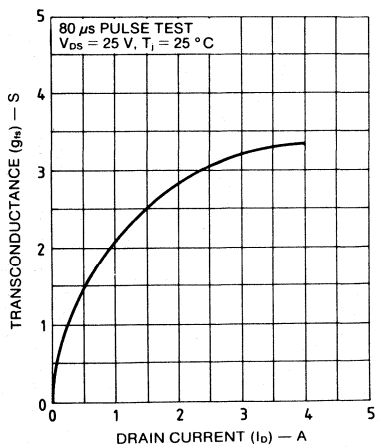


Fig. 7 - Typical transconductance vs. drain current.

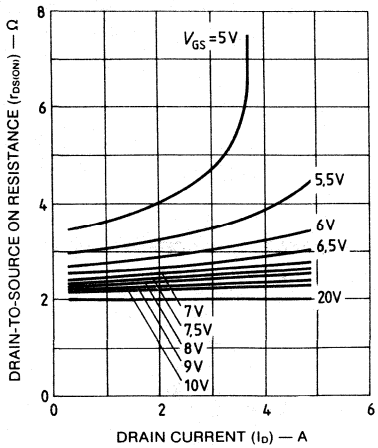


Fig. 8 - Typical on-resistance vs. drain current.

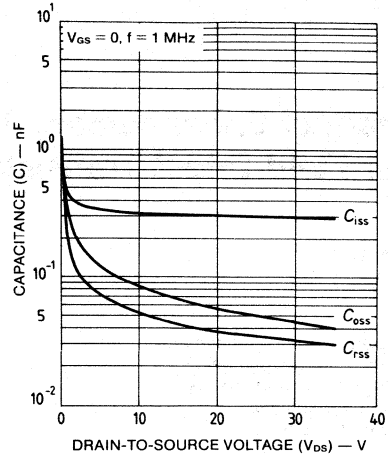


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

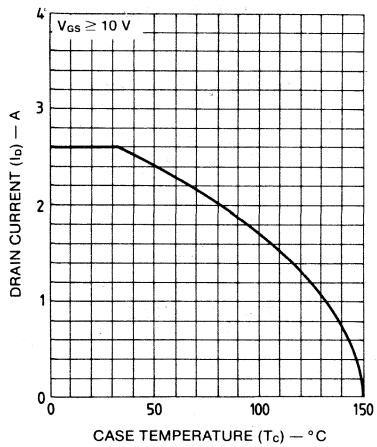


Fig. 10 - Maximum drain current vs. case temperature.

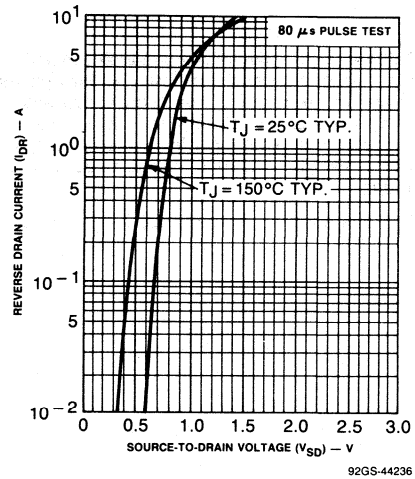


Fig. 11 - Typical source-drain diode forward voltage.

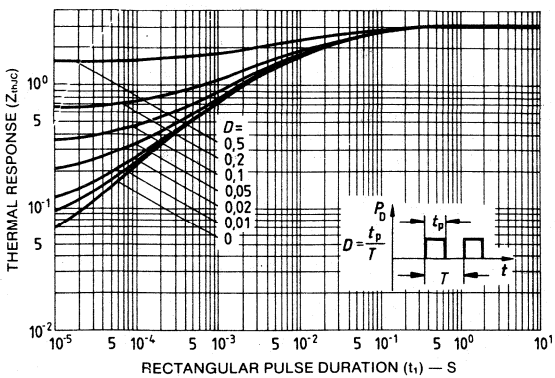


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

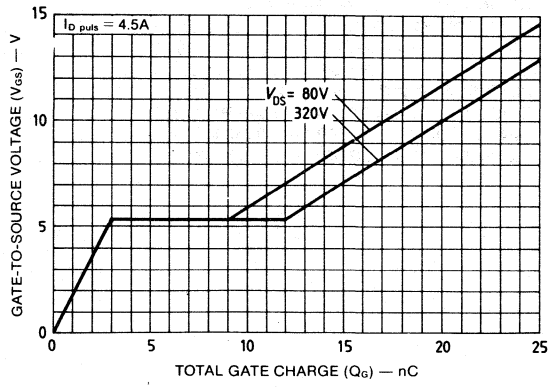


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

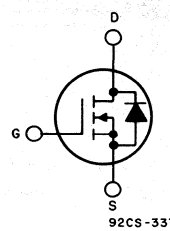
BUZ 351 **File No. 2266**

N-Channel Enhancement-Mode Power Field-Effect Transistors

11.5 A, 400 V
$r_{DS(on)}$ = 0.4 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

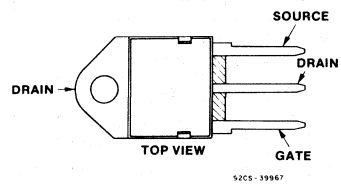


TERMINAL DIAGRAM

The BUZ 351 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 351 is supplied in the JEDEC TO-218AC plastic package.

TERMINAL DESIGNATION



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	400	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 30 °C	I_D	11.5	A
Pulsed T_C = 25 °C	I_{DM}	46	A
POWER DISSIPATION @ T_C = 25 °C	P_T	125	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 400 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 5.5 A	—	0.35	0.4	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 5.5 A	3.3	4.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	3.8	4.9	nF
Output Capacitance	C_{oss}		—	300	500	pF
Reverse Transfer Capacitance	C_{rss}		—	120	200	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.9 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	50 80	75 120	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_f)	$t_{d(off)}$ t_f		— —	330 110	430 140	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 45			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	11.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	46	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, I_F = I_{DR} dI_F/dt = 100 A/μs, V_R = 100 V	—	1	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

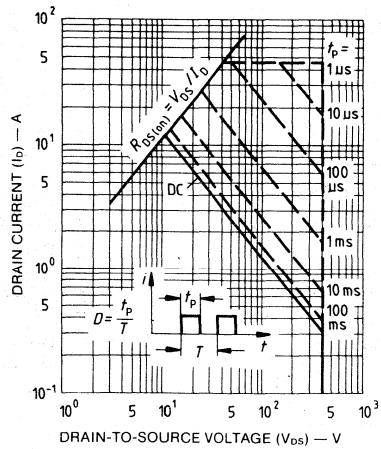


Fig. 1 - Maximum safe operating areas for all types.

BUZ 351

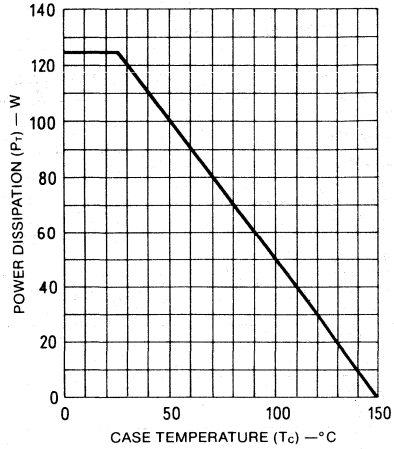


Fig. 2 - Power vs. temperature derating curve for all types.

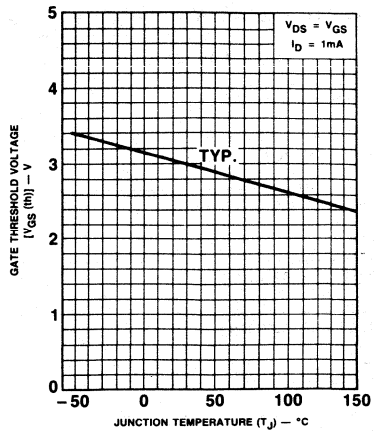


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

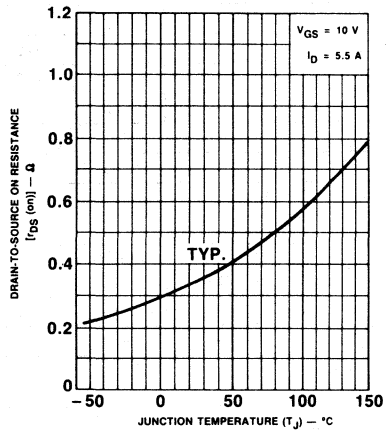


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

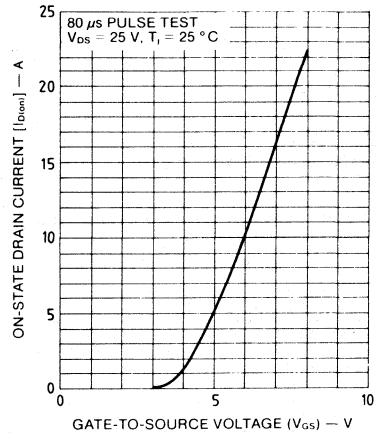


Fig. 5 - Typical transfer characteristics for all types.

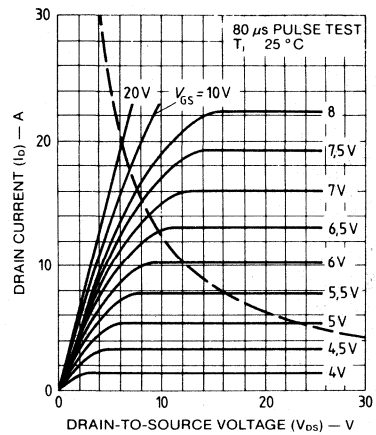


Fig. 6 - Typical output characteristics.

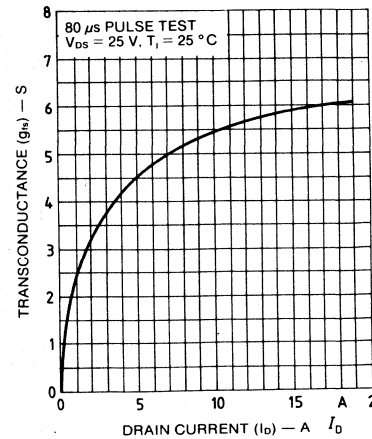


Fig. 7 - Typical transconductance vs. drain current.

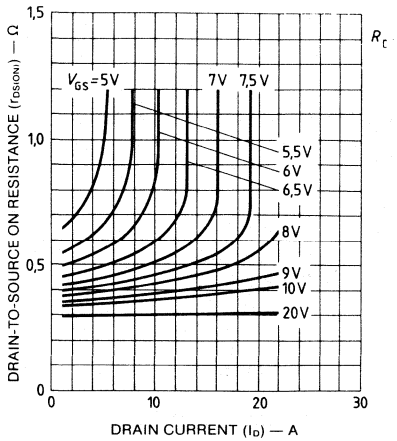


Fig. 8 - Typical on-resistance vs. drain current.

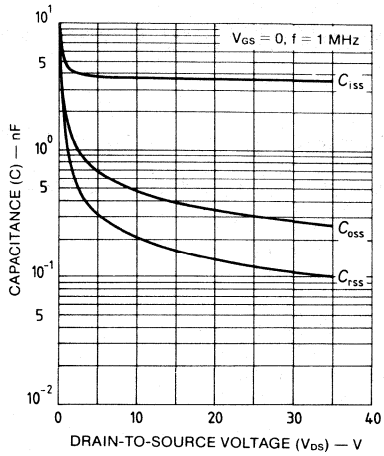


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

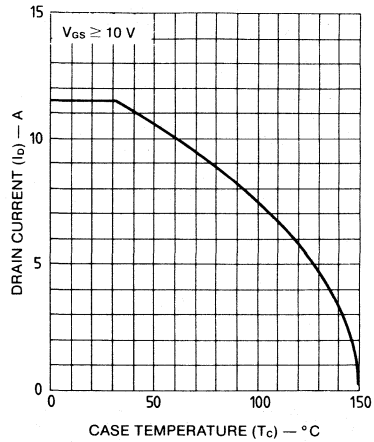


Fig. 10 - Maximum drain current vs. case temperature.

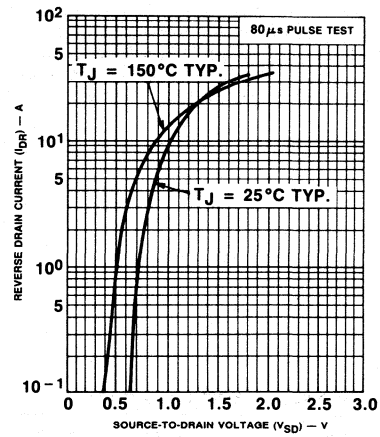


Fig. 11 - Typical source-drain diode forward voltage.

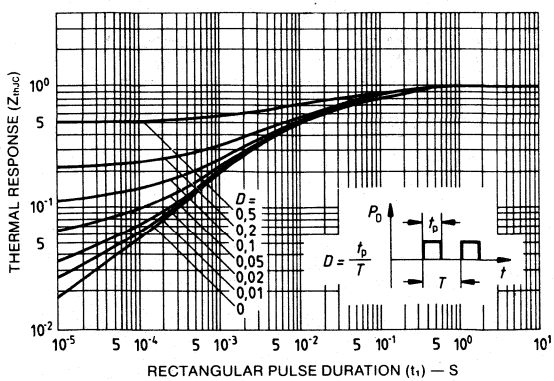


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

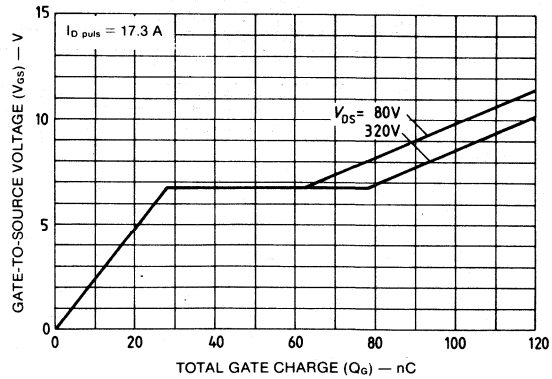


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

IRF120, IRF121, IRF122, IRF123

File Number **1565**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

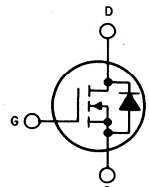
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF120, IRF121, IRF122 and IRF123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

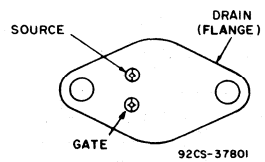
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

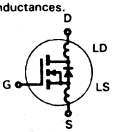
Absolute Maximum Ratings

Parameter		IRF120	IRF121	IRF122	IRF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF120 IRF122	100	–	–	V	V_{GS} = 0V
		IRF121 IRF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF120 IRF121	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF122 IRF123	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF120 IRF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF122 IRF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	6.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF120 IRF121	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF122 IRF123	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF120 IRF121	–	–	32	A	
		IRF122 IRF123	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF120 IRF121	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF122 IRF123	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF120, IRF121, IRF122, IRF123

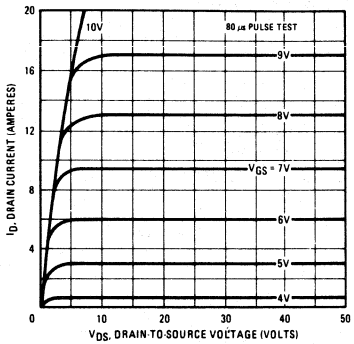


Fig. 1 — Typical Output Characteristics

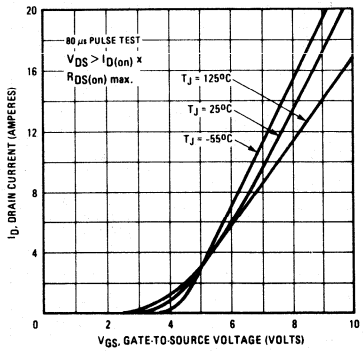


Fig. 2 — Typical Transfer Characteristics

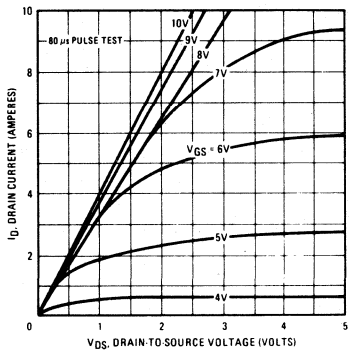


Fig. 3 — Typical Saturation Characteristics

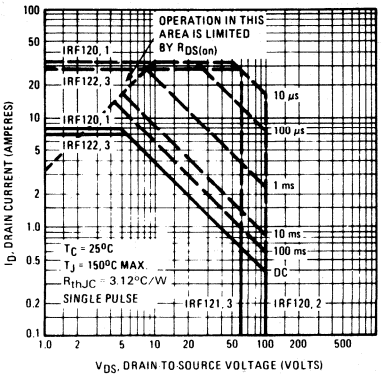


Fig. 4 — Maximum Safe Operating Area

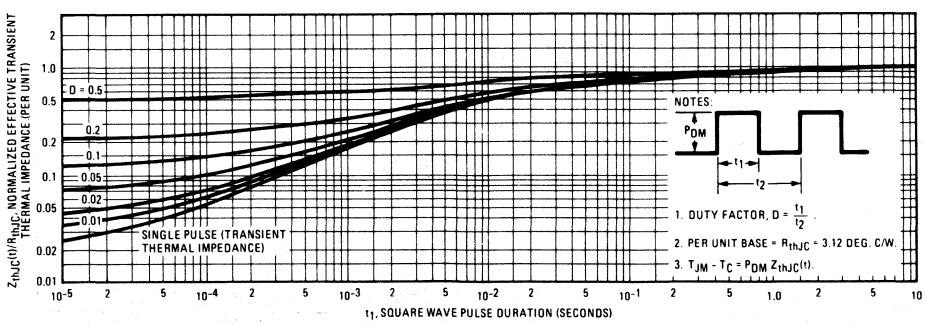


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

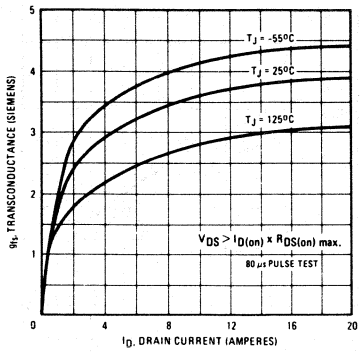


Fig. 6 – Typical Transconductance Vs. Drain Current

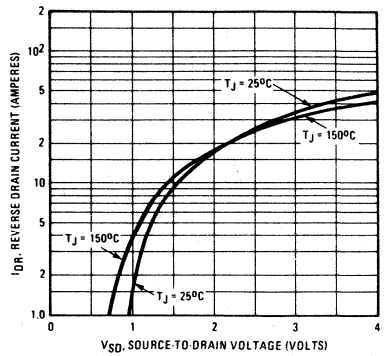


Fig. 7 – Typical Source-Drain Diode Forward Voltage

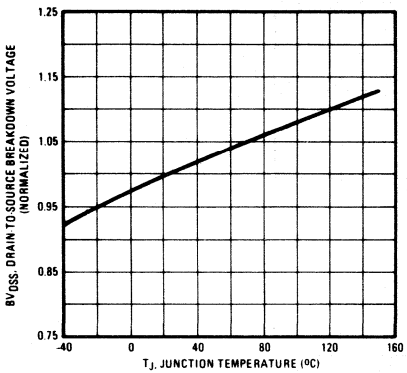


Fig. 8 – Breakdown Voltage Vs. Temperature

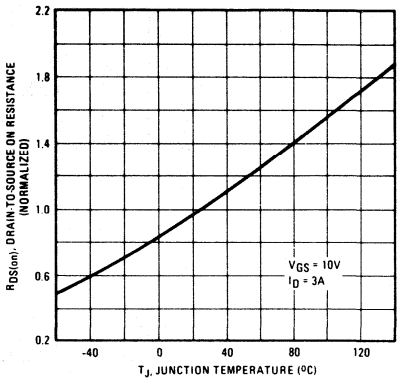


Fig. 9 – Normalized On-Resistance Vs. Temperature

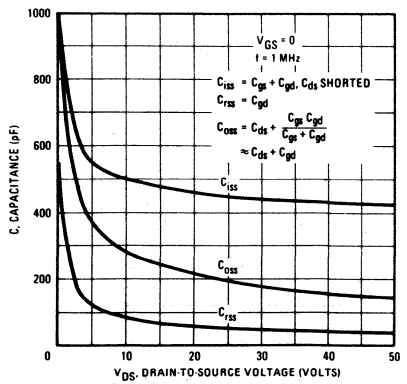


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

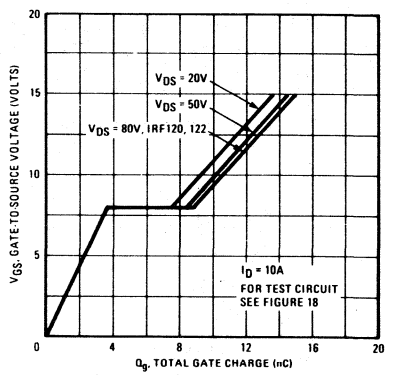


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF120, IRF121, IRF122, IRF123

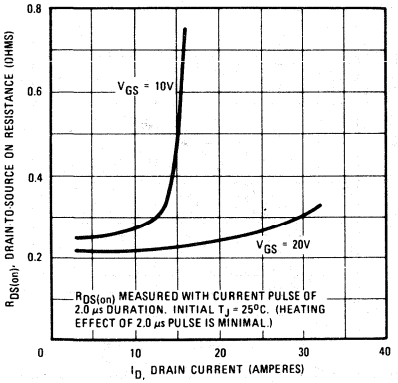


Fig. 12 – Typical On-Resistance Vs. Drain Current

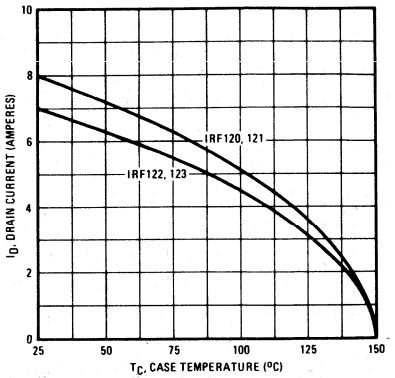


Fig. 13 – Maximum Drain Current Vs. Case Temperature

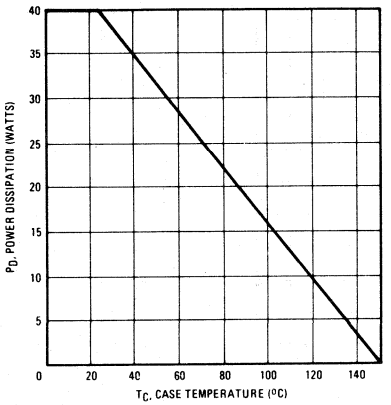


Fig. 14 – Power Vs. Temperature Derating Curve

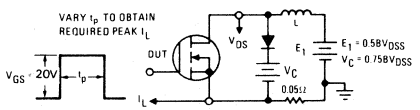


Fig. 15 – Clamped Inductive Test Circuit

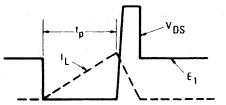


Fig. 16 – Clamped Inductive Waveforms

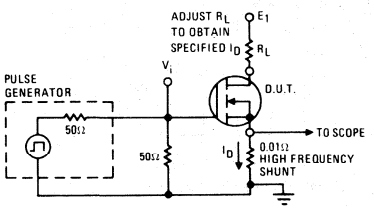


Fig. 17 – Switching Time Test Circuit

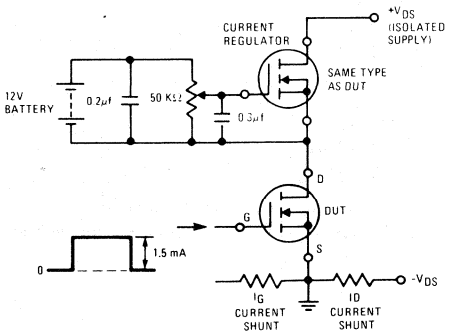


Fig. 18 – Gate Charge Test Circuit

File Number **1566**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

12A and 14A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

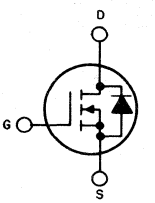
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF130, IRF131, IRF132 and IRF133 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

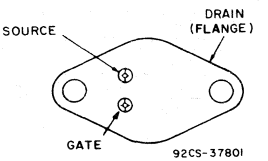
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

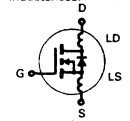
Parameter		IRF130	IRF131	IRF132	IRF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		56	56	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF130, IRF131, IRF132, IRF133

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF130 IRF132	100	–	–	V	V_{GS} = 0V
		IRF131 IRF133	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF130 IRF131	14	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF132 IRF133	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF130 IRF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF132 IRF133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40	ns	
t_f	Fall Time	ALL	–	–	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} ≈ 10V, I_D = 18A, V_{DS} ≈ 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	14	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	14	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF130 IRF131	–	–	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF132 IRF133	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF130 IRF131	–	–	56	A	
		IRF132 IRF133	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF130 IRF131	–	–	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF132 IRF133	–	–	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	360	–	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.1	–	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

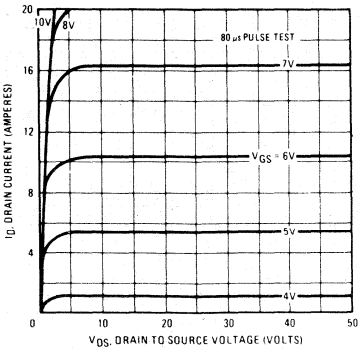


Fig. 1 – Typical Output Characteristics

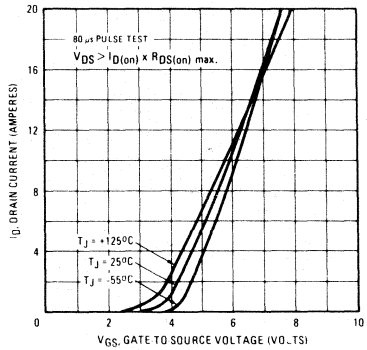


Fig. 2 – Typical Transfer Characteristics

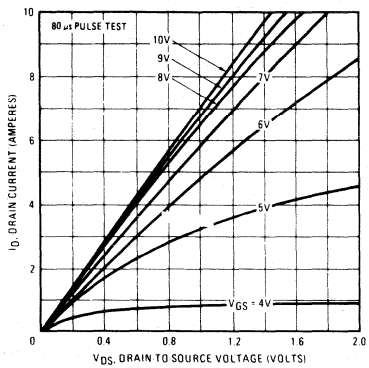


Fig. 3 – Typical Saturation Characteristics

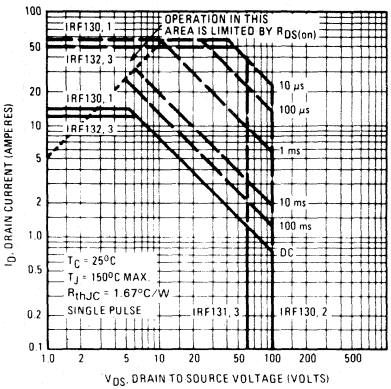


Fig. 4 – Maximum Safe Operating Area

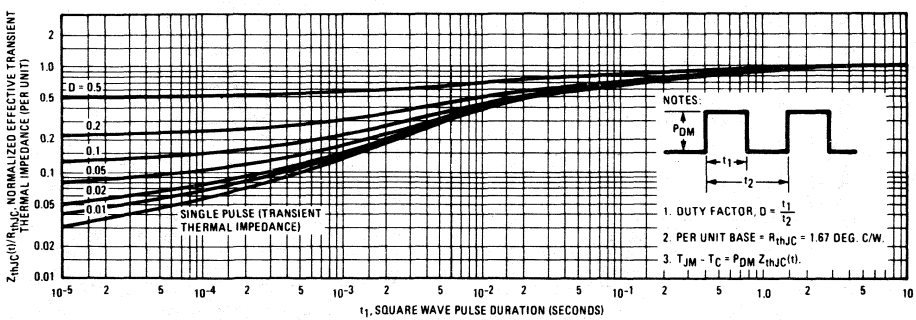


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF130, IRF131, IRF132, IRF133

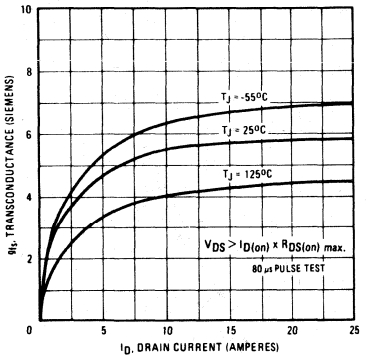


Fig. 6 – Typical Transconductance Vs. Drain Current

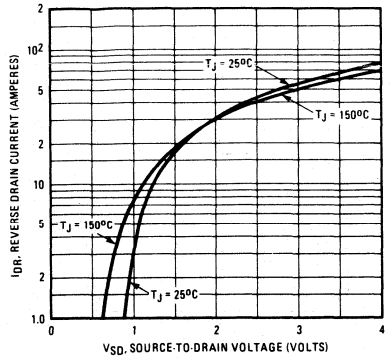


Fig. 7 – Typical Source-Drain Diode Forward Voltage

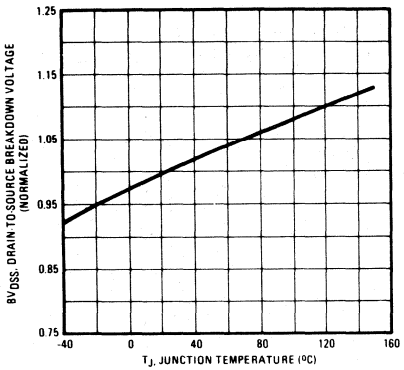


Fig. 8 – Breakdown Voltage Vs. Temperature

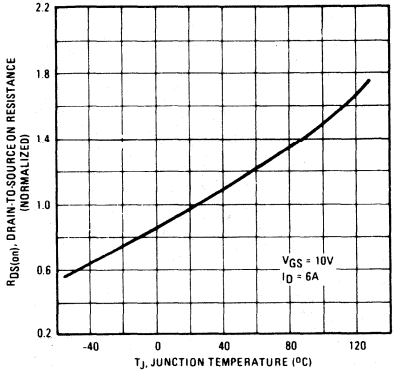


Fig. 9 – Normalized On-Resistance Vs. Temperature

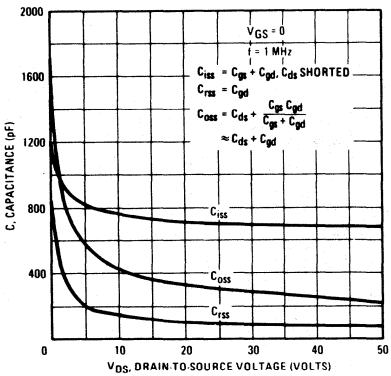


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

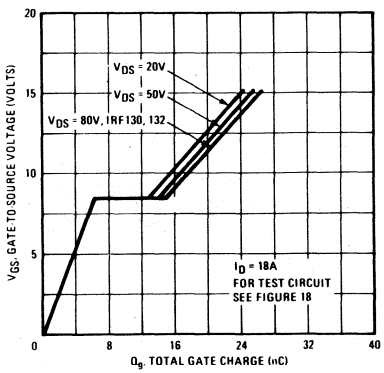


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

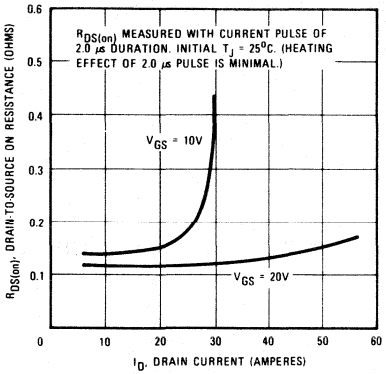


Fig. 12 – Typical On-Resistance Vs. Drain Current

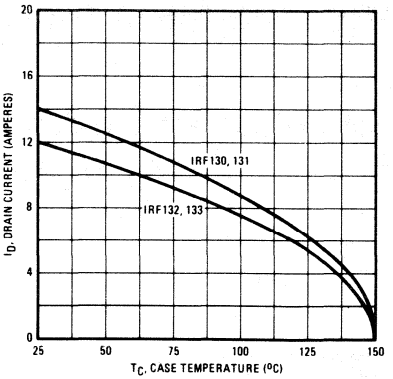


Fig. 13 – Maximum Drain Current Vs. Case Temperature

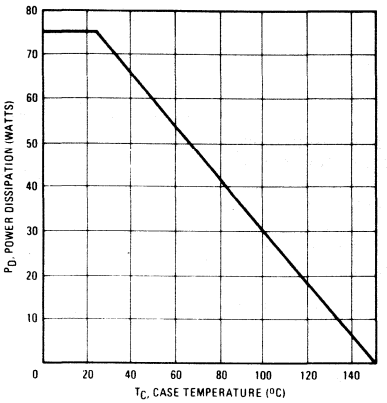


Fig. 14 – Power Vs. Temperature Derating Curve

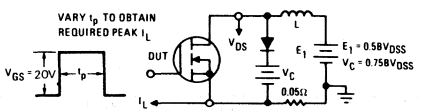


Fig. 15 – Clamped Inductive Test Circuit

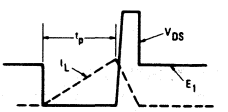


Fig. 16 – Clamped Inductive Waveforms

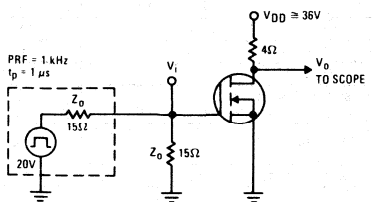


Fig. 17 – Switching Time Test Circuit

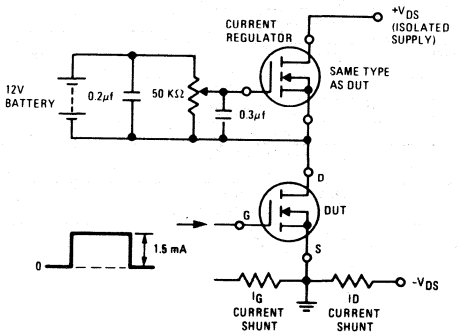


Fig. 18 – Gate Charge Test Circuit

IRF140, IRF141, IRF142, IRF143

File Number **2306**

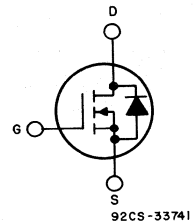
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

24 A and 27 A, 60 V – 100 V
$r_{DS(on)}$ = 0.085 Ω and 0.11 Ω

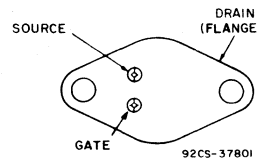
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AE

The IRF140, IRF141, IRF142, and IRF143 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

Absolute Maximum Ratings

	Parameter	IRF140	IRF141	IRF142	IRF143	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	27	27	24	24	A
I_D @ T_C = 100°C	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		108	108	96	96	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF140, IRF142	100	–	–	V	V_{GS} = 0V
		IRF141, IRF143	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF140, IRF141	27	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF142, IRF143	24	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF140, IRF141	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		IRF142, IRF143	–	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 15A
C_{iss}	Input Capacitance	ALL	–	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	550	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≈ 30V, I_D = 15A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	38	80	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	17	26	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	21	32	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF140, IRF141	–	–	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF142, IRF143	–	–	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF140, IRF141	–	–	108	A	
		IRF142, IRF143	–	–	96	A	
V_{SD}	Diode Forward Voltage ②	IRF140, IRF141	–	–	2.5	V	T_C = 25°C, I_S = 27A, V_{GS} = 0V
		IRF142, IRF143	–	–	2.3	V	T_C = 25°C, I_S = 24A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.9	–	μC	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF140, IRF141, IRF142, IRF143

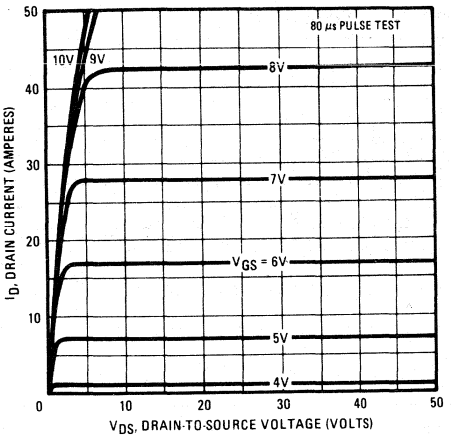


Fig. 1 – Typical Output Characteristics

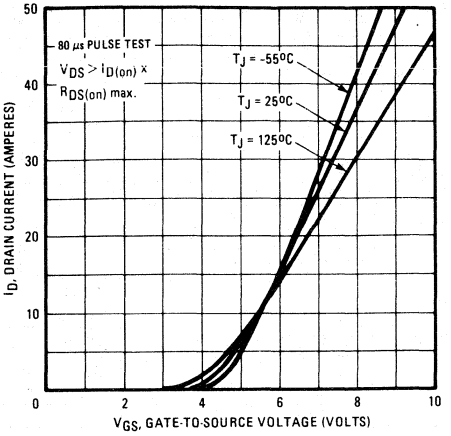


Fig. 2 – Typical Transfer Characteristics

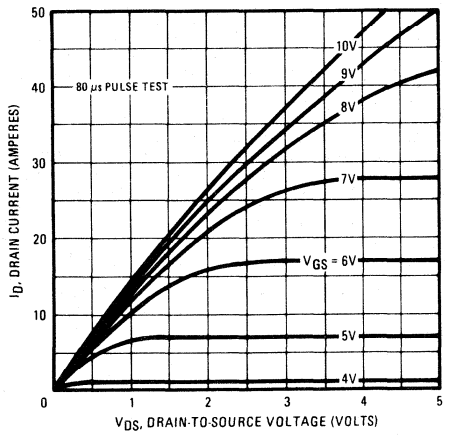


Fig. 3 – Typical Saturation Characteristics

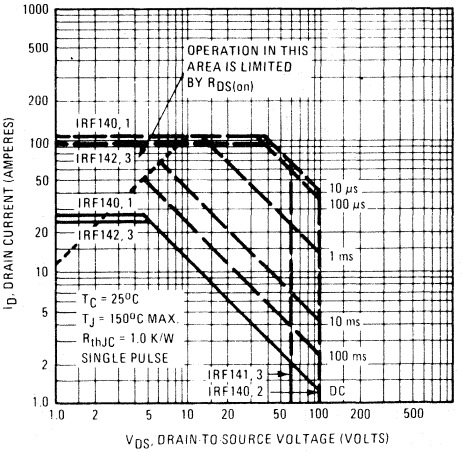


Fig. 4 – Maximum Safe Operating Area

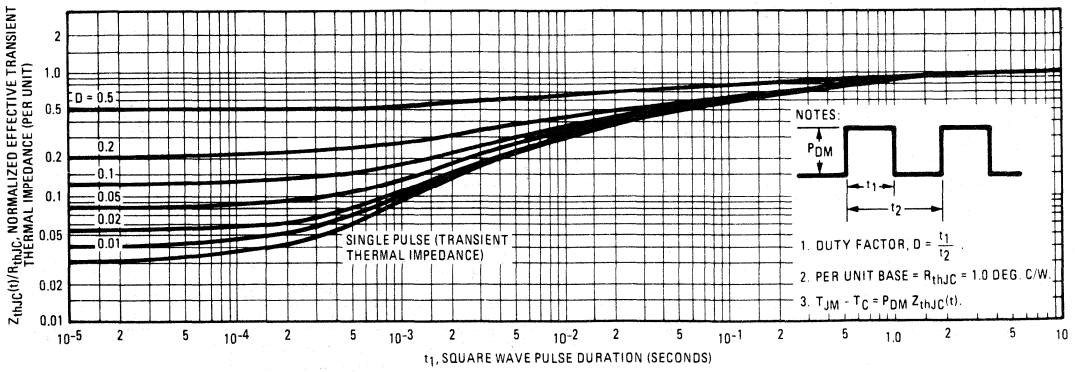


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

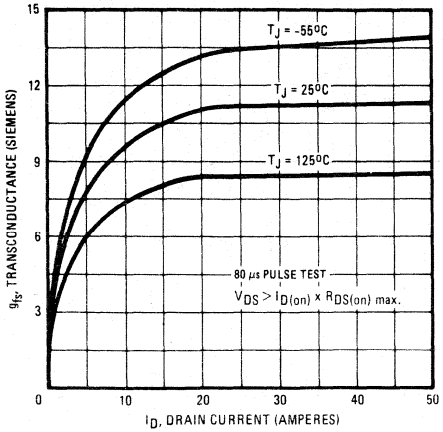


Fig. 6 – Typical Transconductance Vs. Drain Current

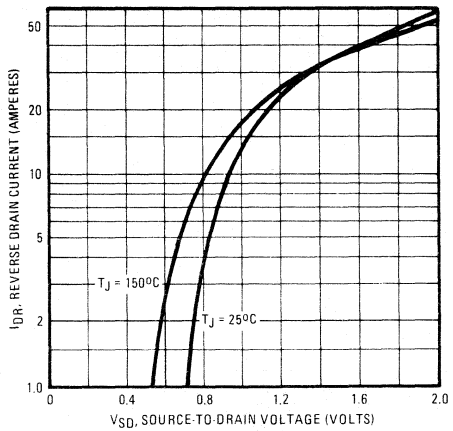


Fig. 7 – Typical Source-Drain Diode Forward Voltage

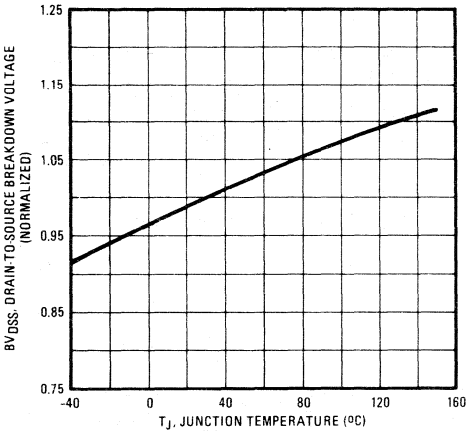


Fig. 8 – Breakdown Voltage Vs. Temperature

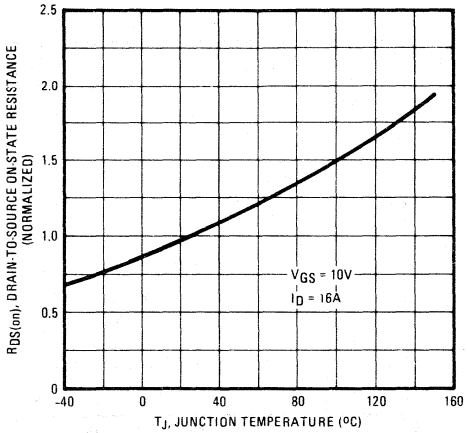


Fig. 9 – Normalized On-Resistance Vs. Temperature

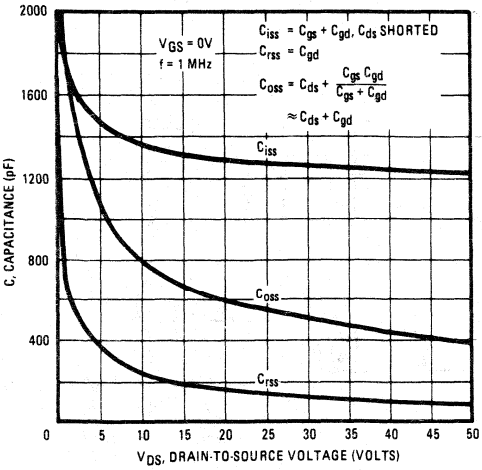


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

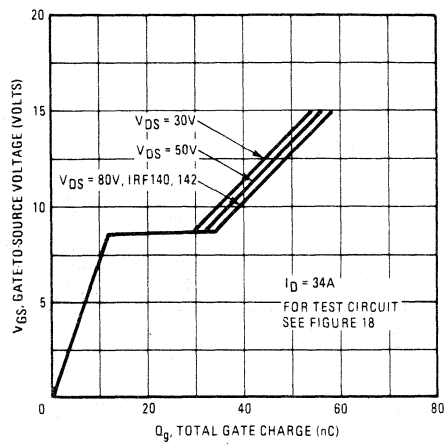


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF140, IRF141, IRF142, IRF143

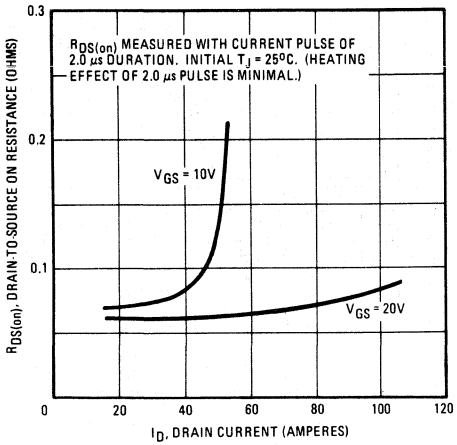


Fig. 12 – Typical On-Resistance Vs. Drain Current

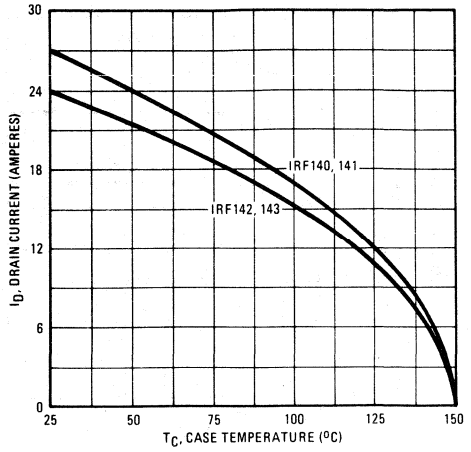


Fig. 13 – Maximum Drain Current Vs. Case Temperature

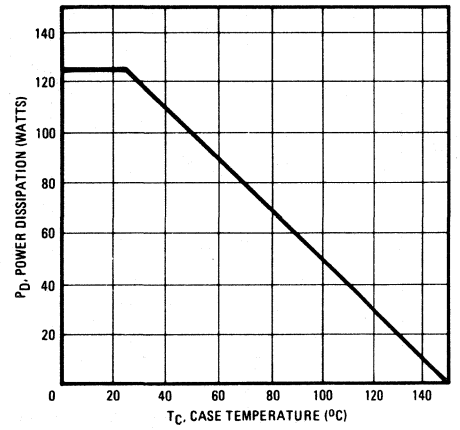


Fig. 14 – Power Vs. Temperature Derating Curve

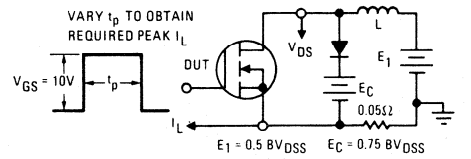


Fig. 15 – Clamped Inductive Test Circuit

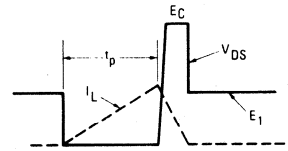


Fig. 16 – Clamped Inductive Waveforms

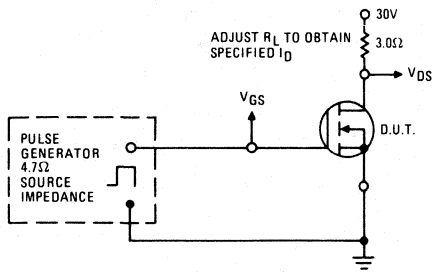


Fig. 17 – Switching Time Test Circuit

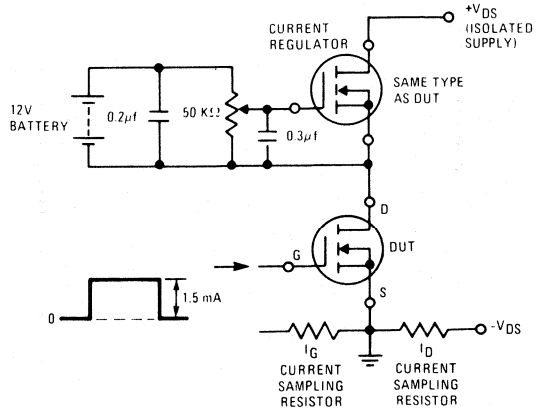


Fig. 18 – Gate Charge Test Circuit

File Number **1824**

IRF150, IRF151, IRF152, IRF153

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

33 A and 40 A, 60 V - 100 V
$r_{DS}(on)$ = 0.055 Ω and 0.08 Ω

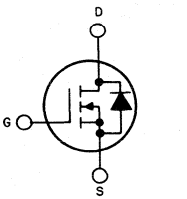
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF150, IRF151, IRF152 and IRF153 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

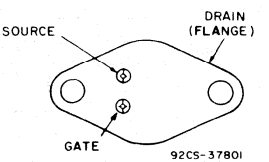
The IRF-types are supplied in the JEDEC TO-204AE metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AE

Absolute Maximum Ratings

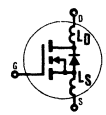
Parameter		IRF150	IRF151	IRF152	IRF153	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	40	40	33	33	A
I_D @ T_C = 100°C	Continuous Drain Current	25	25	20	20	A
I_{DM}	Pulsed Drain Current ③	160	160	132	132	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	160	(See Fig. 15 and 16) L = 100μH 160	132	132	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF150, IRF151, IRF152, IRF153

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF150 IRF152	100	–	–	V	V_{GS} = 0V
		IRF151 IRF153	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF150 IRF151	40	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF152 IRF153	33	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF150 IRF151	–	0.045	0.055	Ω	V_{GS} = 10V, I_D = 20A
		IRF152 IRF153	–	0.06	0.08	Ω	
g_{fs}	Forward Transconductance ②	ALL	9.0	11	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 20A
C_{iss}	Input Capacitance	ALL	–	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	1000	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	350	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 24V, I_D = 20A, Z_o = 4.7Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	63	120	nC	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	27	41	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	36	54	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF150 IRF151	–	–	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF152 IRF153	–	–	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF150 IRF151	–	–	160	A	
		IRF152 IRF153	–	–	132	A	
V_{SD}	Diode Forward Voltage ②	IRF150 IRF151	–	–	2.5	V	T_C = 25°C, I_S = 40A, V_{GS} = 0V
		IRF152 IRF153	–	–	2.3	V	T_C = 25°C, I_S = 33A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.3	–	μC	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

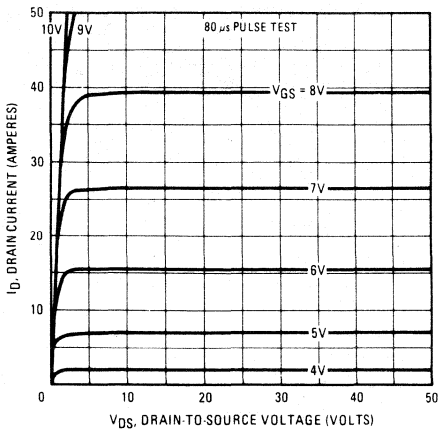


Fig. 1 — Typical Output Characteristics

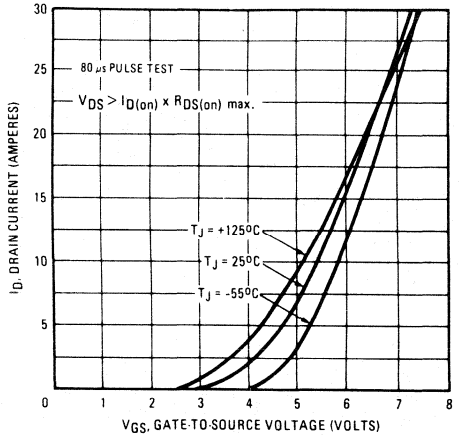


Fig. 2 — Typical Transfer Characteristics

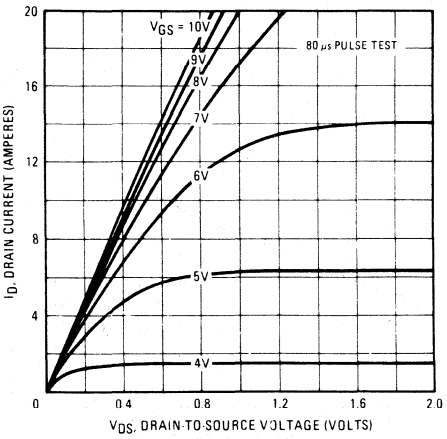


Fig. 3 — Typical Saturation Characteristics

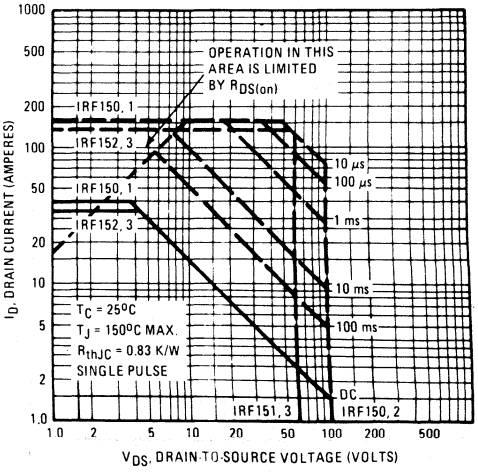


Fig. 4 — Maximum Safe Operating Area

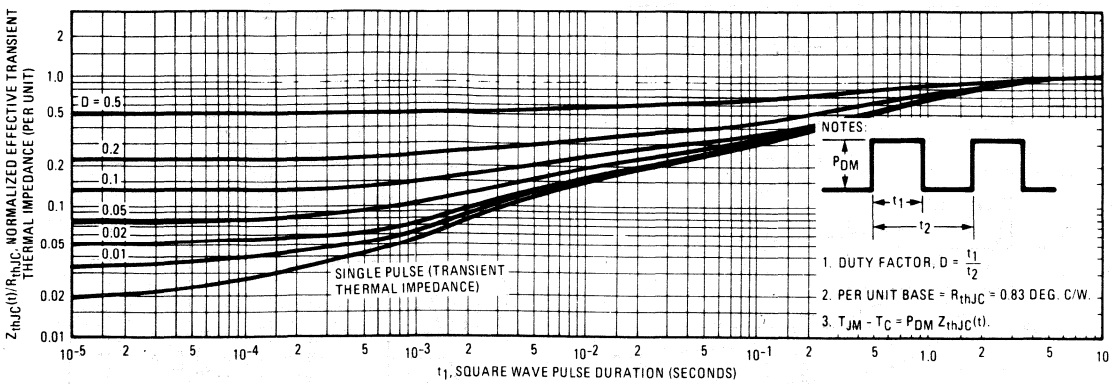


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF150, IRF151, IRF152, IRF153

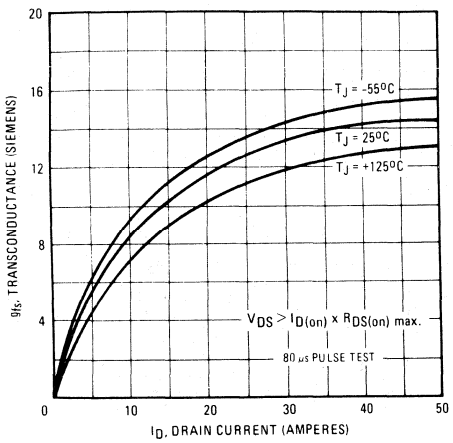


Fig. 6 — Typical Transconductance Vs. Drain Current

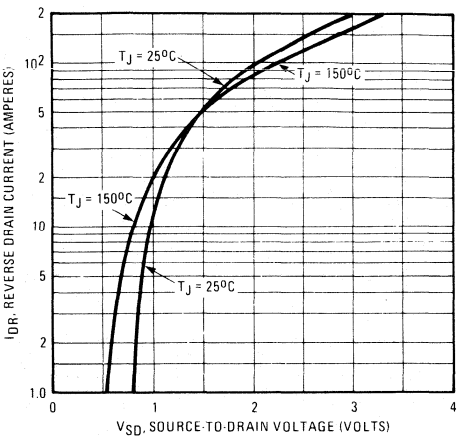


Fig. 7 — Typical Source-Drain Diode Forward Voltage

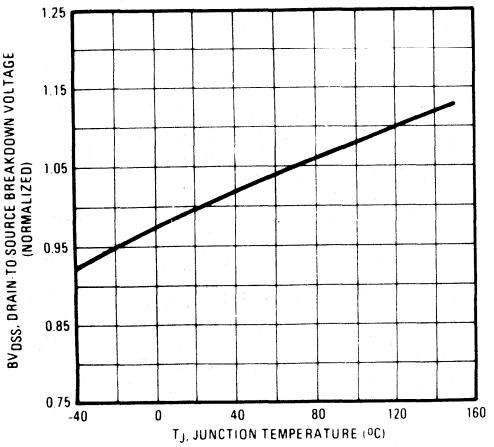


Fig. 8 — Breakdown Voltage Vs. Temperature

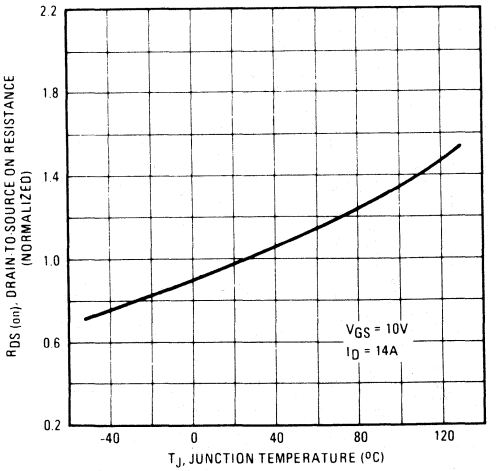


Fig. 9 — Normalized On-Resistance Vs. Temperature

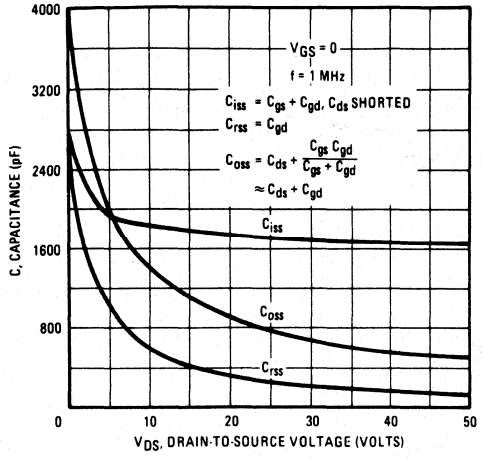


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

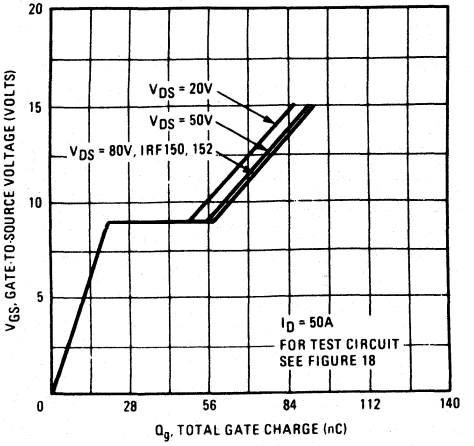


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

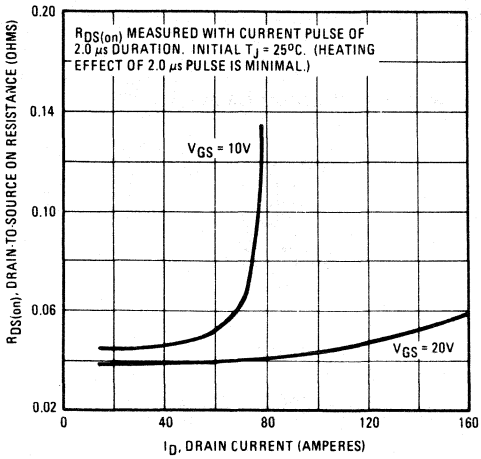


Fig. 12 – Typical On-Resistance Vs. Drain Current

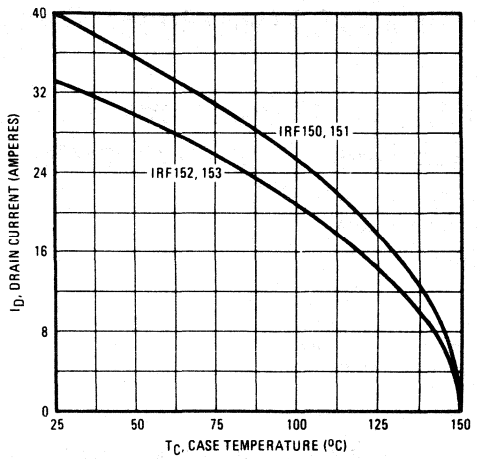


Fig. 13 – Maximum Drain Current Vs. Case Temperature

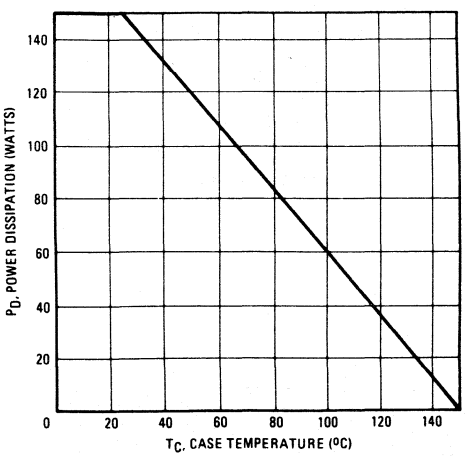


Fig. 14 – Power Vs. Temperature Derating Curve

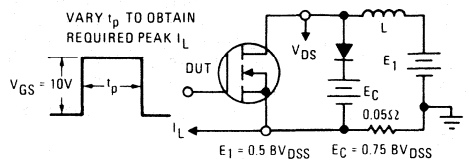


Fig. 15 – Clamped Inductive Test Circuit

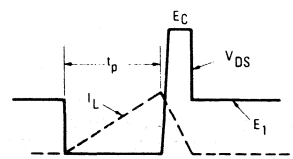


Fig. 16 – Clamped Inductive Waveforms

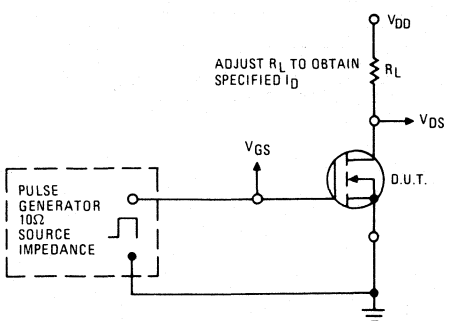


Fig. 17 – Switching Time Test Circuit

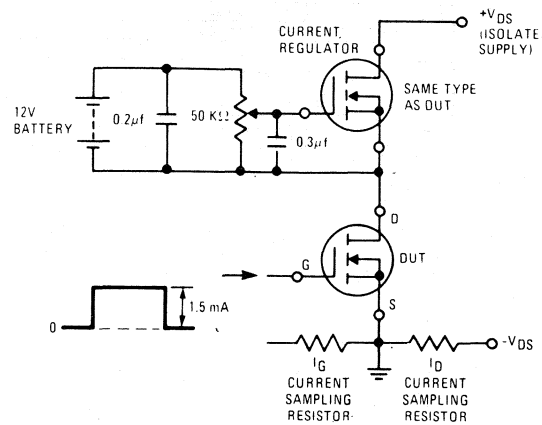


Fig. 18 – Gate Charge Test Circuit

IRF220, IRF221, IRF222, IRF223

File Number **1567**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 5.0A, 150V-200V

$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

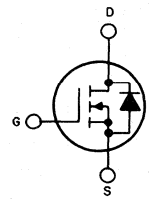
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF220, IRF221, IRF222 and IRF223 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

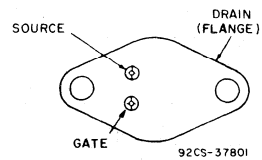
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

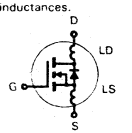
Absolute Maximum Ratings

Parameter		IRF220	IRF221	IRF222	IRF223	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		20	20	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-50 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF220 IRF222	200	–	–	V	V_{GS} = 0V
		IRF221 IRF223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF220 IRF221	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF222 IRF223	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF220 IRF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF222 IRF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	7.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

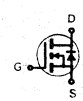


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF220 IRF221	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF222 IRF223	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF220 IRF221	–	–	20	A	
		IRF222 IRF223	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF220 IRF221	–	–	2.0	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF222 IRF223	–	–	1.8	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF220, IRF221, IRF222, IRF223

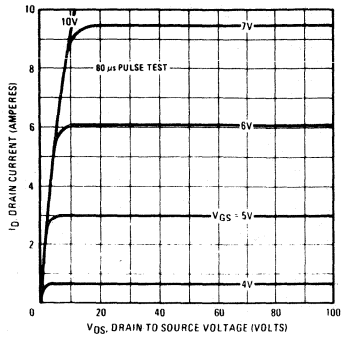


Fig. 1 – Typical Output Characteristics

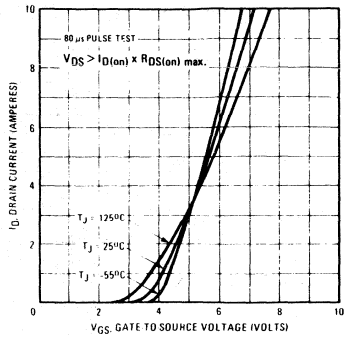


Fig. 2 – Typical Transfer Characteristics

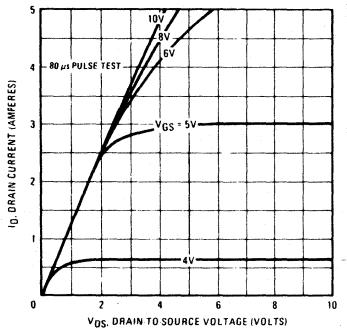


Fig. 3 – Typical Saturation Characteristics

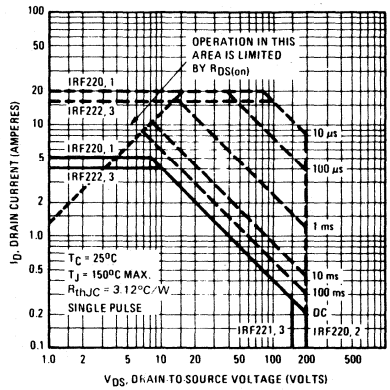


Fig. 4 – Maximum Safe Operating Area

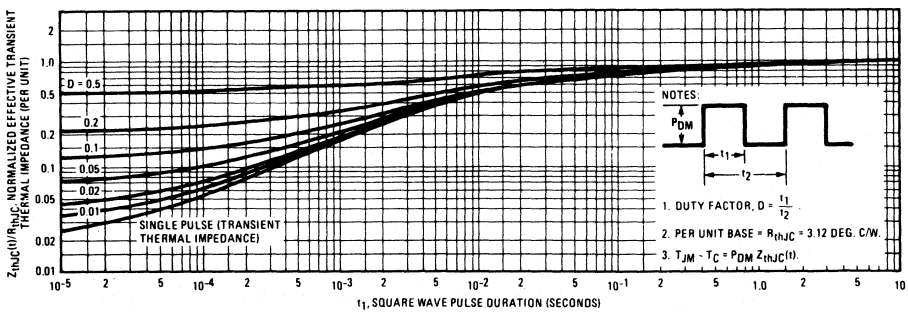


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

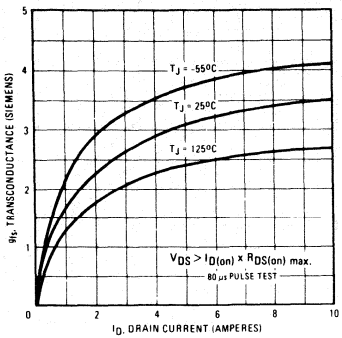


Fig. 6 – Typical Transconductance Vs. Drain Current

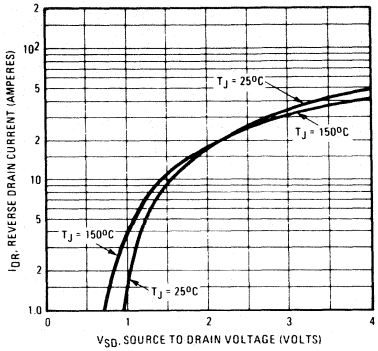


Fig. 7 – Typical Source-Drain Diode Forward Voltage

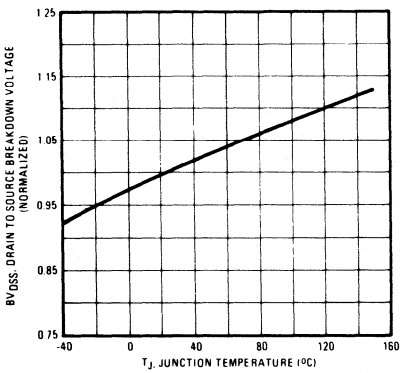


Fig. 8 – Breakdown Voltage Vs. Temperature

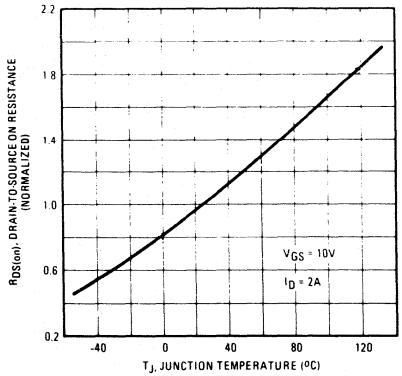


Fig. 9 – Normalized On-Resistance Vs. Temperature

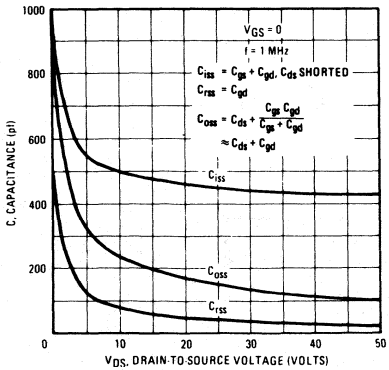


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

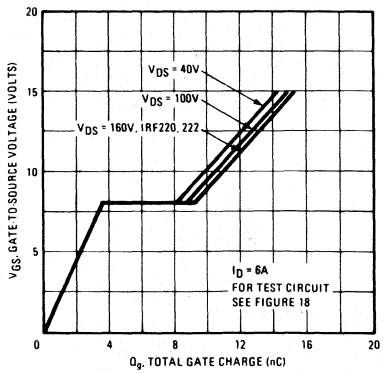


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF220, IRF221, IRF222, IRF223

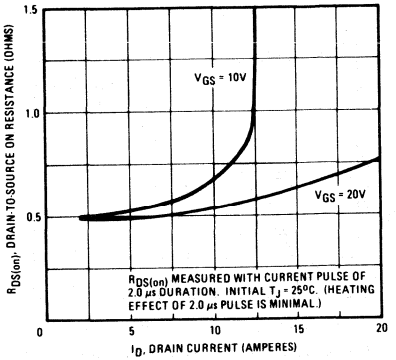


Fig. 12 – Typical On-Resistance Vs. Drain Current

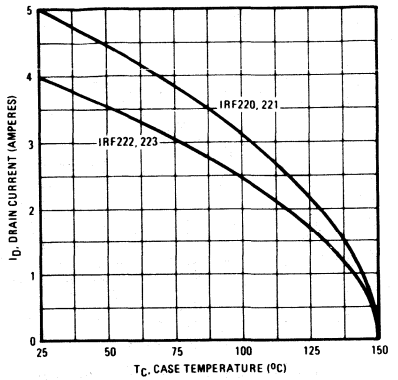


Fig. 13 – Maximum Drain Current Vs. Case Temperature

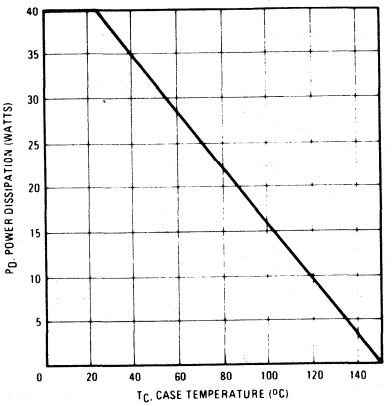


Fig. 14 – Power Vs. Temperature Derating Curve

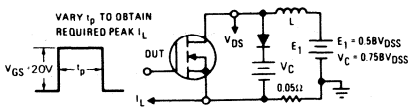


Fig. 15 – Clamped Inductive Test Circuit

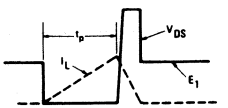


Fig. 16 – Clamped Inductive Waveforms

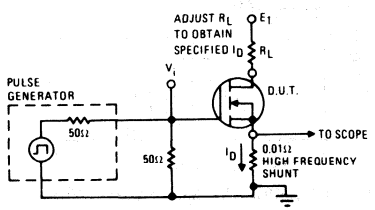


Fig. 17 – Switching Time Test Circuit

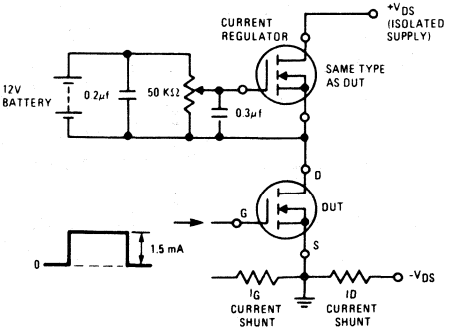


Fig. 18 – Gate Charge Test Circuit

File Number **1568**

IRF230, IRF231, IRF232, IRF233

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8.0A and 9.0A, 150V-200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

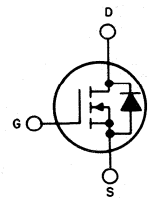
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF230, IRF231, IRF232 and IRF233 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

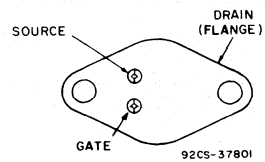
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

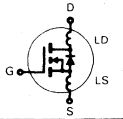
Parameter		IRF230	IRF231	IRF232	IRF233	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		36	36	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF230, IRF231, IRF232, IRF233

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF230 IRF232	200	–	–	V	V_{GS} = 0V
		IRF231 IRF233	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF230 IRF231	9.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF232 IRF233	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF230 IRF231	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF232 IRF233	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	15	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	15	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF230 IRF231	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF232 IRF233	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF230 IRF231	–	–	36	A	
		IRF232 IRF233	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF230 IRF231	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF232 IRF233	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 9.0A, di_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 9.0A, di_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

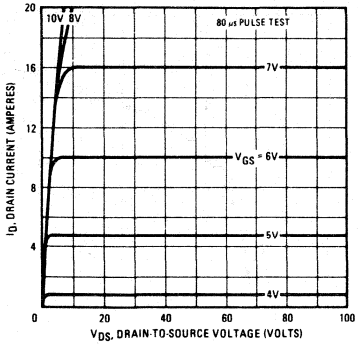


Fig. 1 – Typical Output Characteristics

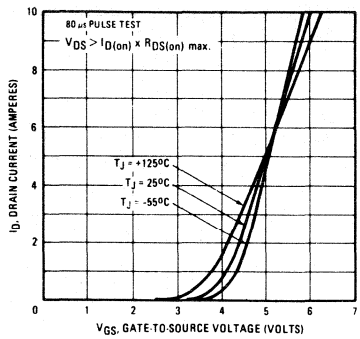


Fig. 2 – Typical Transfer Characteristics

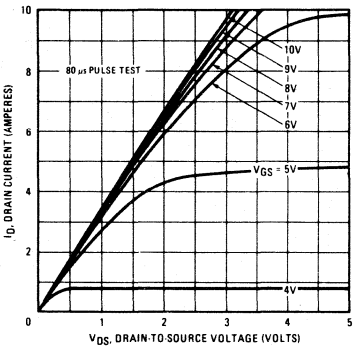


Fig. 3 – Typical Saturation Characteristics

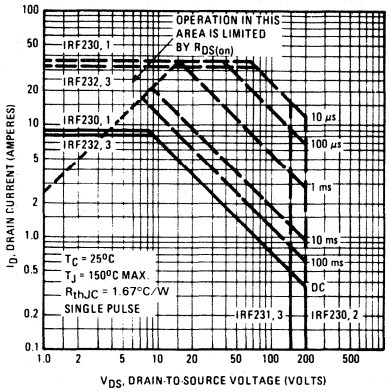


Fig. 4 – Maximum Safe Operating Area

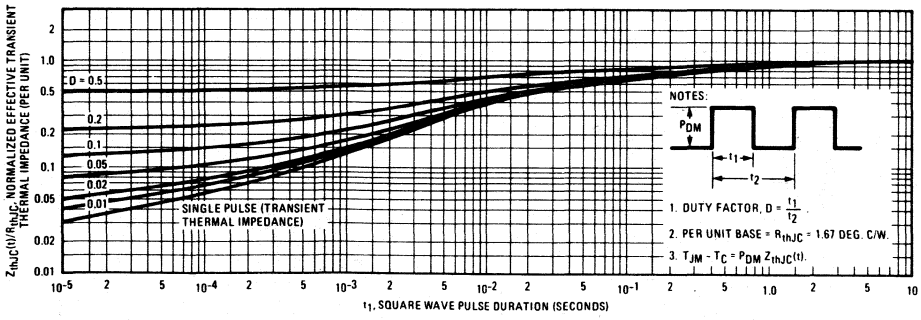


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF230, IRF231, IRF232, IRF233

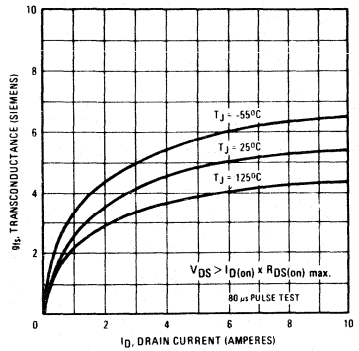


Fig. 6 – Typical Transconductance Vs. Drain Current

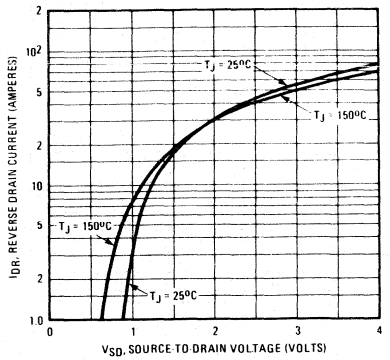
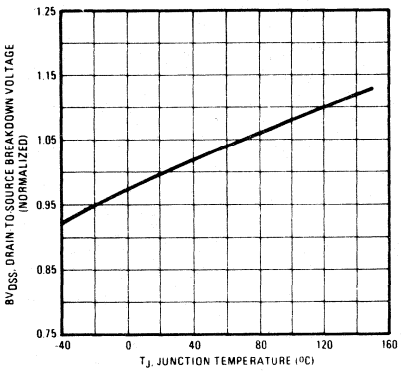


Fig. 7 – Typical Source-Drain Diode Forward Voltage



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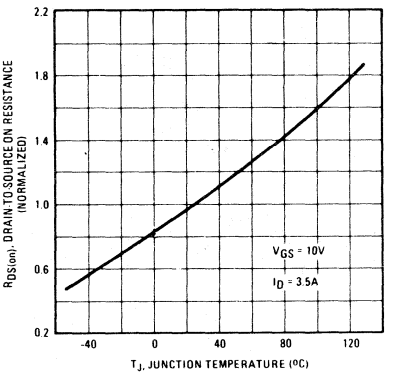


Fig. 9 – Normalized On-Resistance Vs. Temperature

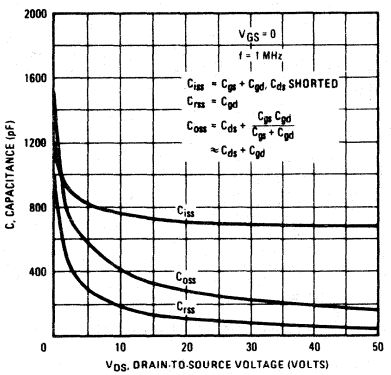


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

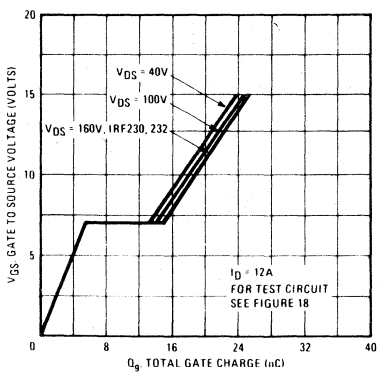


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

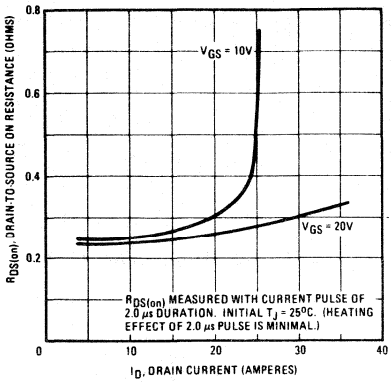


Fig. 12 – Typical On-Resistance Vs. Drain Current

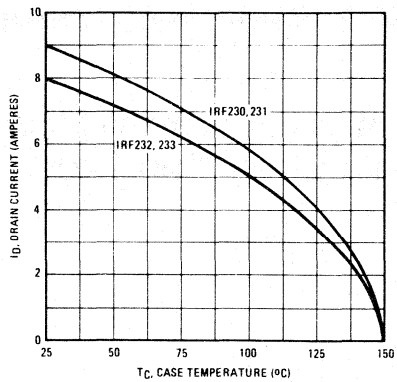


Fig. 13 – Maximum Drain Current Vs. Case Temperature

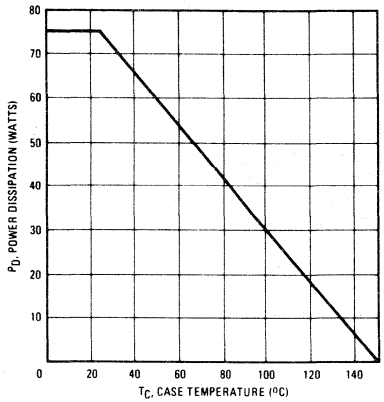


Fig. 14 – Power Vs. Temperature Derating Curve

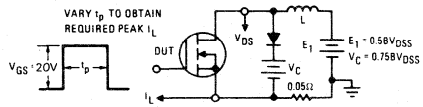


Fig. 15 – Clamped Inductive Test Circuit

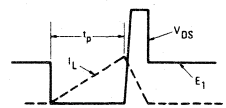


Fig. 16 – Clamped Inductive Waveforms

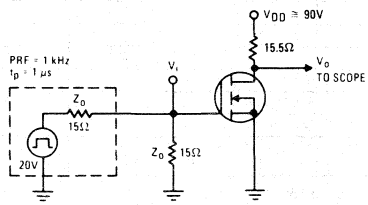


Fig. 17 – Switching Time Test Circuit

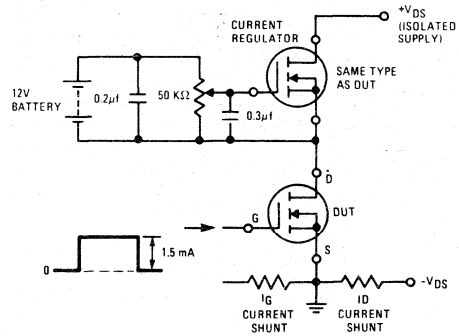


Fig. 18 – Gate Charge Test Circuit

IRF240, IRF241, IRF242, IRF243

File Number **1584**

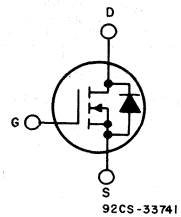
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

16 A and 18 A, 150 V - 200 V
$r_{DS(on)}$ = 0.18 Ω and 0.22 Ω

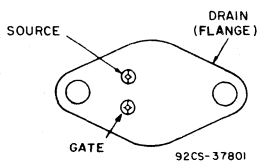
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AE

The IRF240, IRF241, IRF242, and IRF243 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

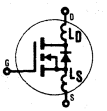
Absolute Maximum Ratings

	Parameter	IRF240	IRF241	IRF242	IRF243	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		72	72	64	64	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF240 IRF242	200	—	—	V	V_{GS} = 0V
		IRF241 IRF243	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF240 IRF241	18	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF242 IRF243	16	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF240 IRF241	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRF242 IRF243	—	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	9.0	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, I_D = 10A
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	500	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	V_{DD} ≈ 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	40	80	ns	
t_f	Fall Time	ALL	—	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	16	24	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	27	41	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF240 IRF241	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF242 IRF243	—	—	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF240 IRF241	—	—	72	A	
		IRF242 IRF243	—	—	64	A	
V_{SD}	Diode Forward Voltage ②	IRF240 IRF241	—	—	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRF242 IRF243	—	—	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.1	—	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF240, IRF241, IRF242, IRF243

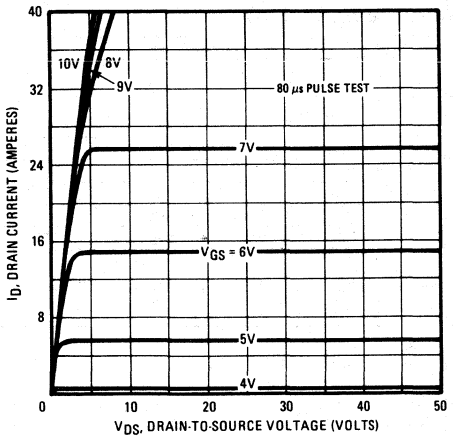


Fig. 1 — Typical Output Characteristics

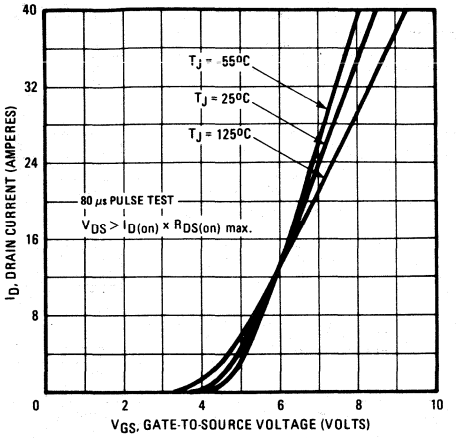


Fig. 2 — Typical Transfer Characteristics

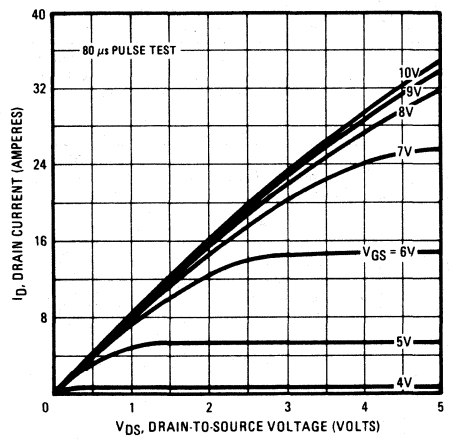


Fig. 3 — Typical Saturation Characteristics

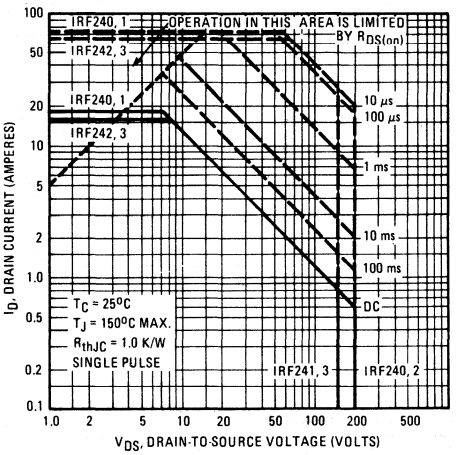


Fig. 4 — Maximum Safe Operating Area

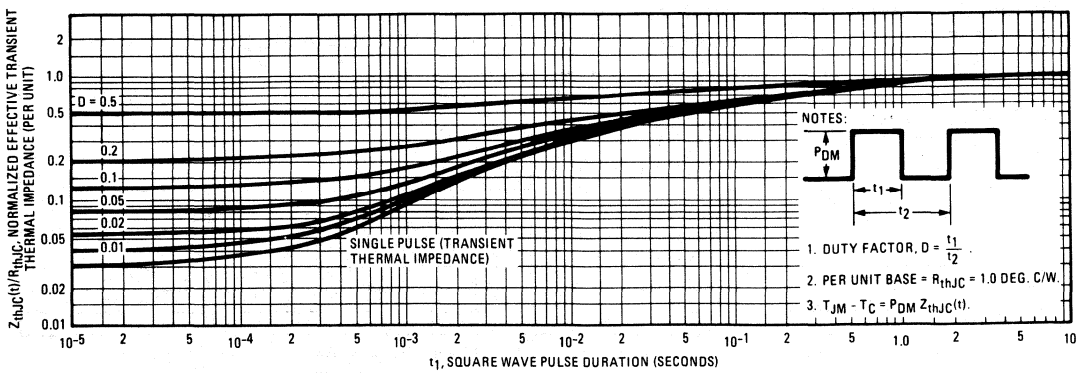


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

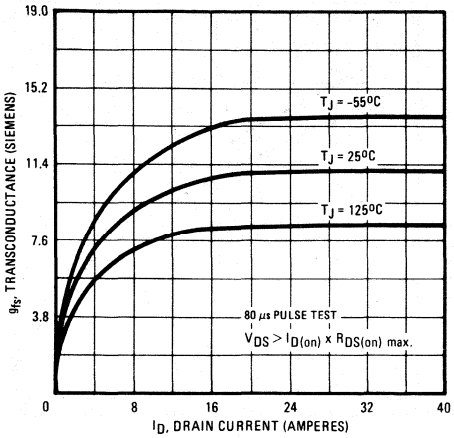


Fig. 6 — Typical Transconductance Vs. Drain Current

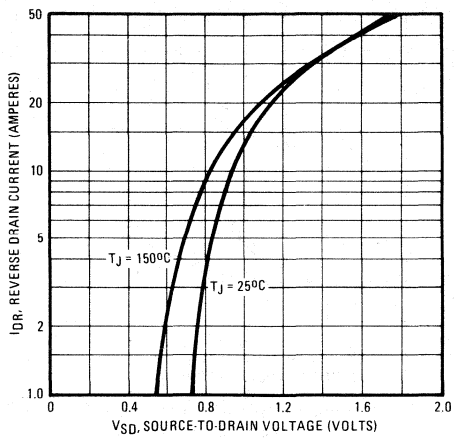


Fig. 7 — Typical Source-Drain Diode Forward Voltage

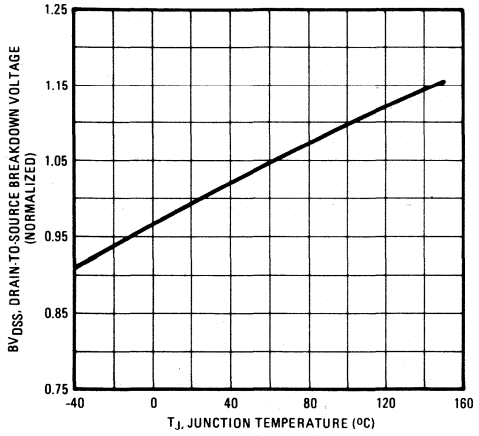


Fig. 8 — Breakdown Voltage Vs. Temperature

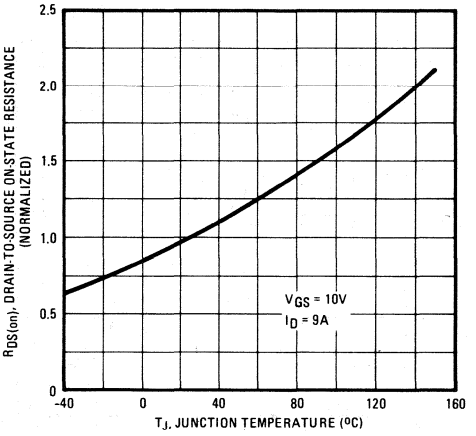


Fig. 9 — Normalized On-Resistance Vs. Temperature

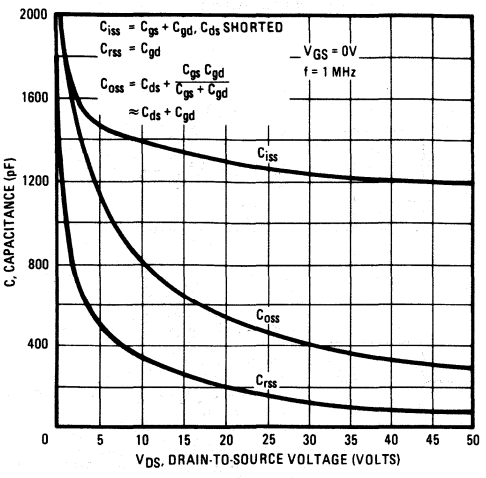


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

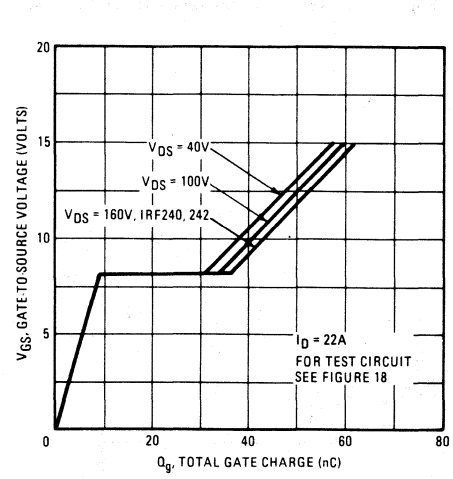


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

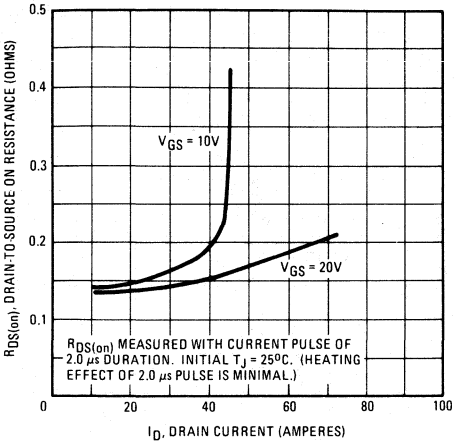


Fig. 12 – Typical On-Resistance Vs. Drain Current

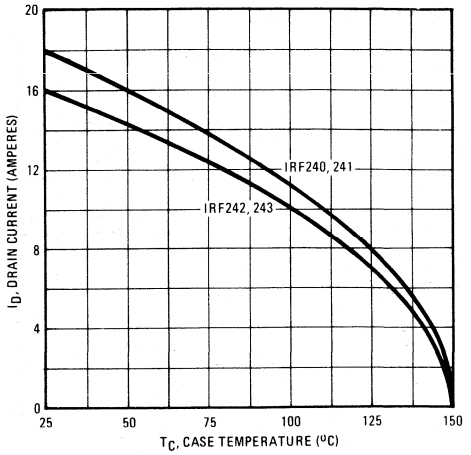


Fig. 13 – Maximum Drain Current Vs. Case Temperature

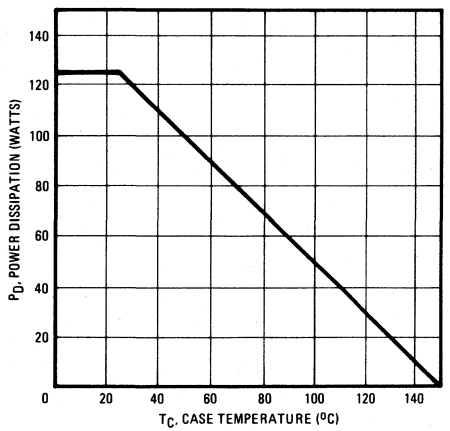


Fig. 14 – Power Vs. Temperature Derating Curve

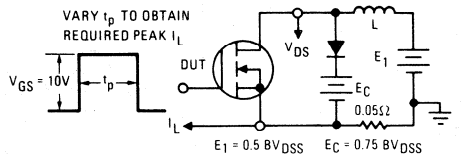


Fig. 15 – Clamped Inductive Test Circuit

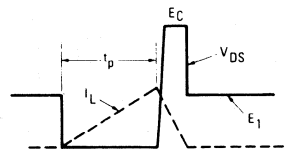


Fig. 16 – Clamped Inductive Waveforms

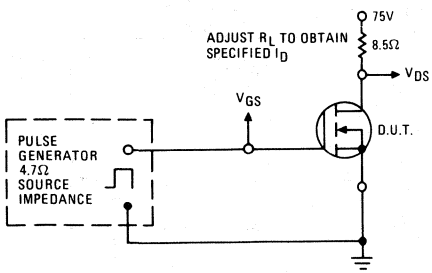


Fig. 17 – Switching Time Test Circuit

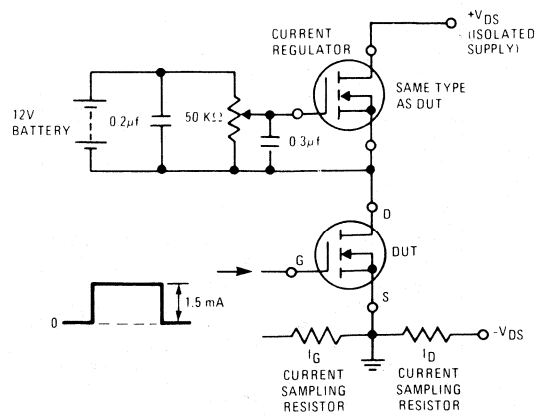


Fig. 18 – Gate Charge Test Circuit

File Number **1825**

IRF250, IRF251, IRF252, IRF253

Power MOS Field-Effect Transistors

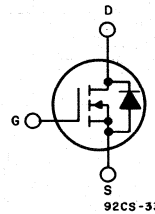
N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A and 30 A, 150 V - 200 V
$r_{DS}(on)$ = 0.085 Ω and 0.120 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

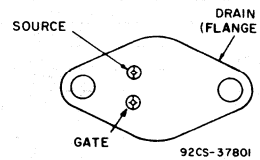


TERMINAL DIAGRAM

The IRF250, IRF251, IRF252 and IRF253 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

TERMINAL DESIGNATION



JEDEC TO-204AE

Absolute Maximum Ratings

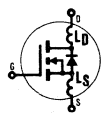
Parameter		IRF250	IRF251	IRF252	IRF253	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	30	30	25	25	A
I_D @ T_C = 100°C	Continuous Drain Current	19	19	16	16	A
I_{DM}	Pulsed Drain Current ③	120	120	100	100	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		120	120	100	100	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF250, IRF251, IRF252, IRF253

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF250 IRF252	200	–	–	V	V_{GS} = 0V
		IRF251 IRF253	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF250 IRF251	30	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF252 IRF253	25	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF250 IRF251	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 16A
		IRF252 IRF253	–	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 16A
C_{iss}	Input Capacitance	ALL	–	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	800	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	300	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≈ 95V, I_D = 16A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	37	56	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	63	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF250 IRF251	–	–	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF252 IRF253	–	–	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF250 IRF251	–	–	120	A	
		IRF252 IRF253	–	–	100	A	
V_{SD}	Diode Forward Voltage ②	IRF250 IRF251	–	–	2.0	V	T_C = 25°C, I_S = 30A, V_{GS} = 0V
		IRF252 IRF253	–	–	1.8	V	T_C = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	750	–	ns	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.7	–	μC	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

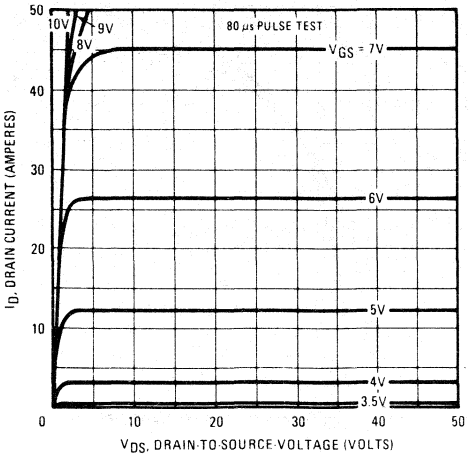


Fig. 1 — Typical Output Characteristics

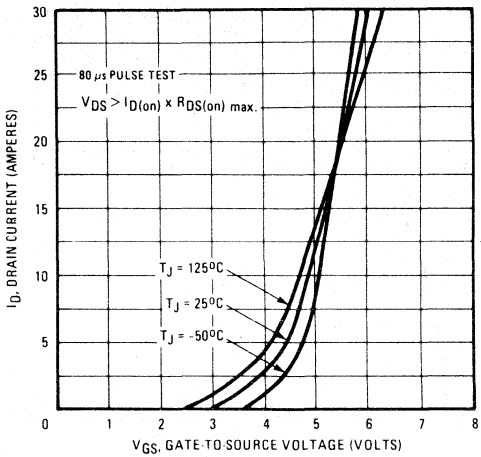


Fig. 2 — Typical Transfer Characteristics

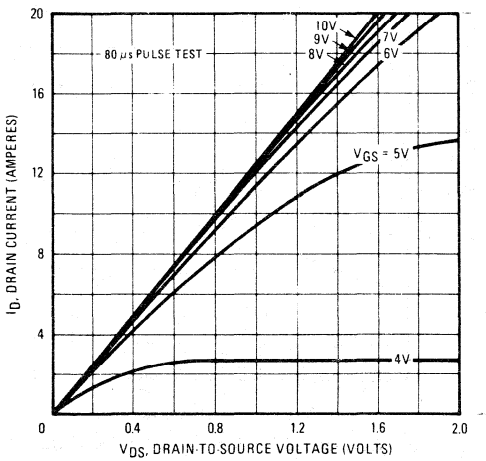


Fig. 3 — Typical Saturation Characteristics

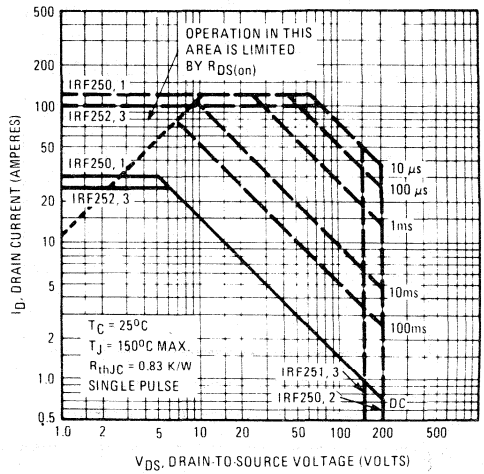


Fig. 4 — Maximum Safe Operating Area

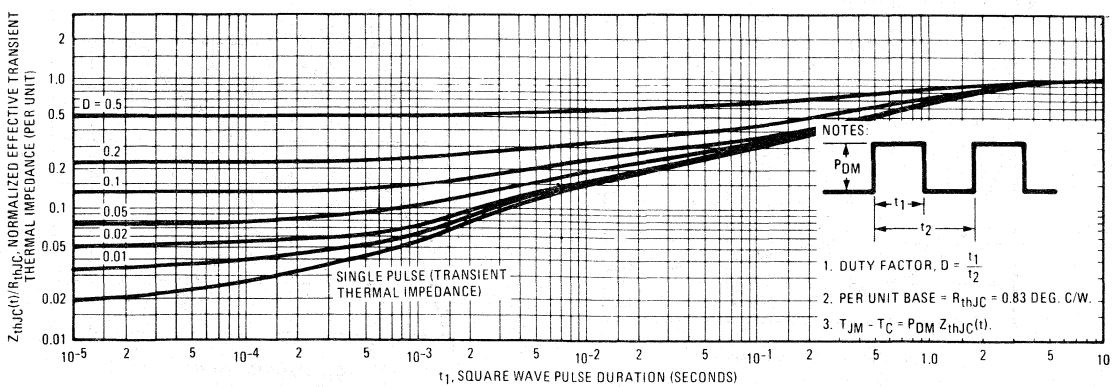


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF250, IRF251, IRF252, IRF253

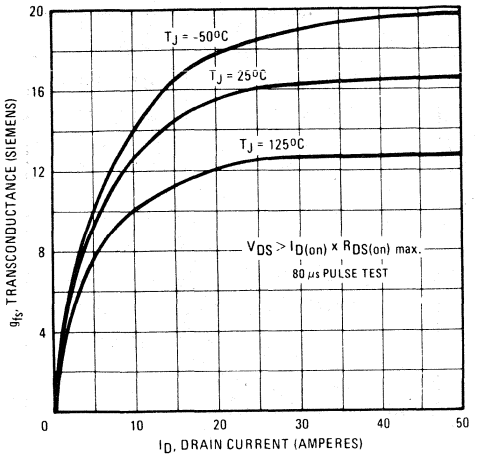


Fig. 6 — Typical Transconductance Vs. Drain Current

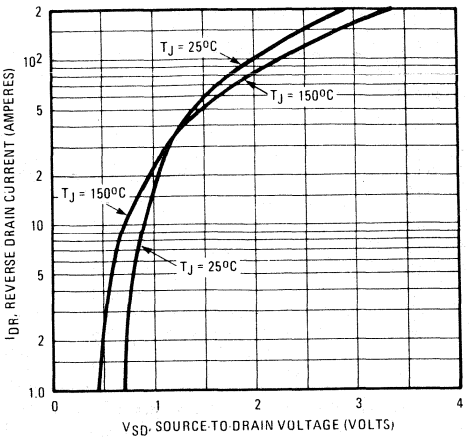


Fig. 7 — Typical Source-Drain Diode Forward Voltage

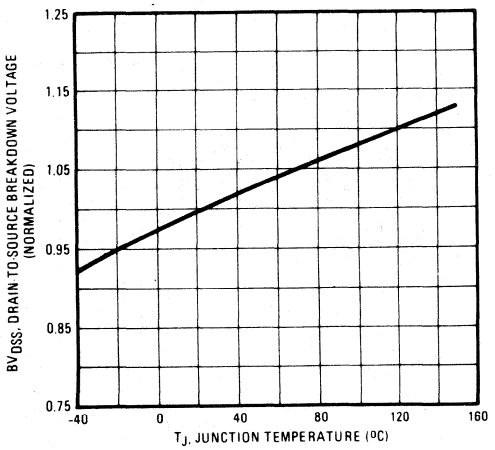


Fig. 8 — Breakdown Voltage Vs. Temperature

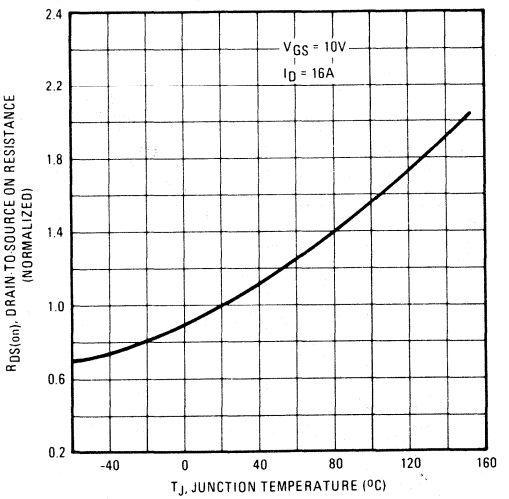


Fig. 9 — Normalized On-Resistance Vs. Temperature

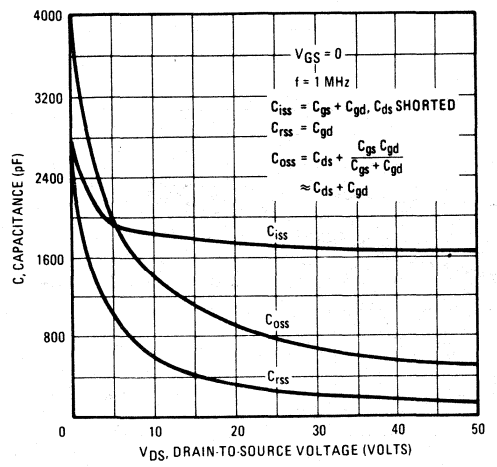


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

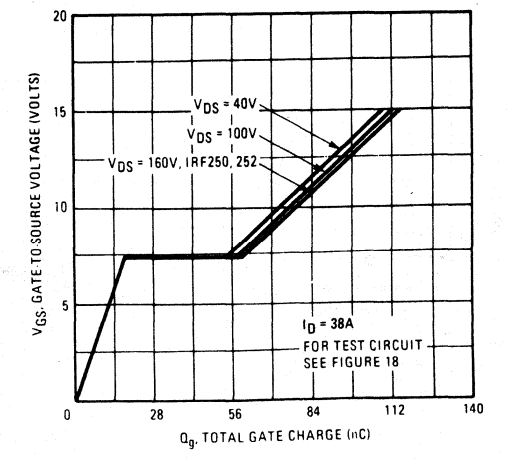


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

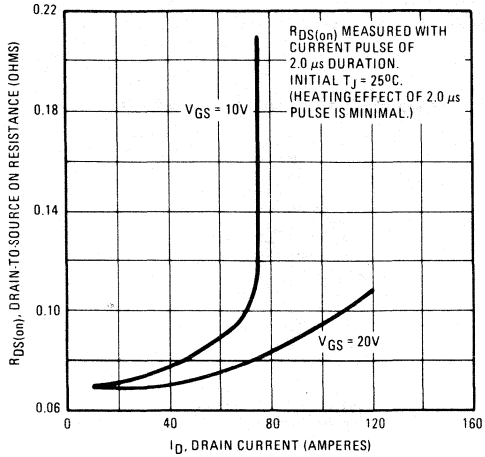


Fig. 12 – Typical On-Resistance Vs. Drain Current

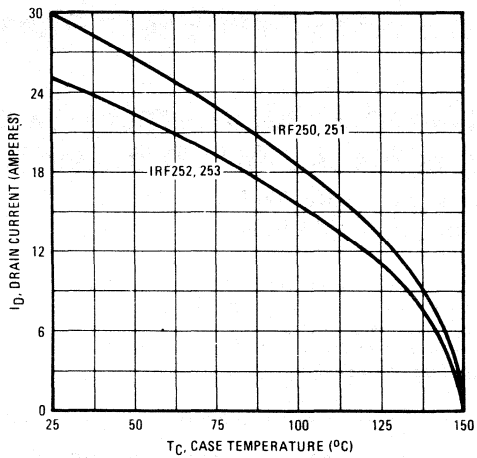


Fig. 13 – Maximum Drain Current Vs. Case Temperature

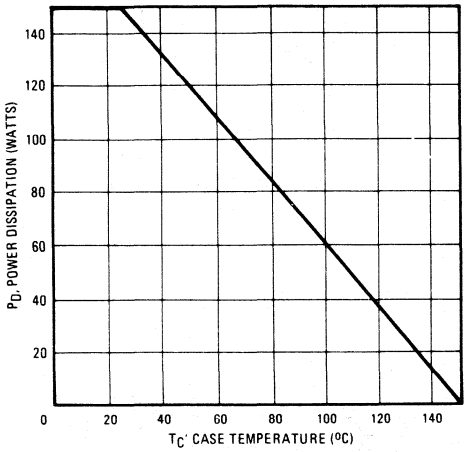


Fig. 14 – Power Vs. Temperature Derating Curve

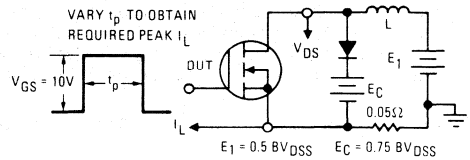


Fig. 15 – Clamped Inductive Test Circuit

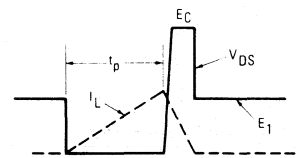


Fig. 16 – Clamped Inductive Waveforms

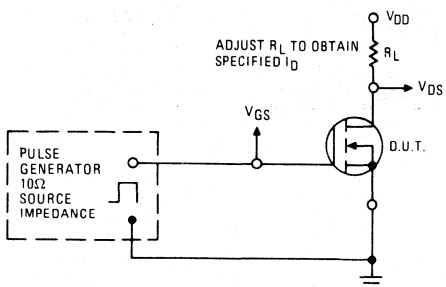


Fig. 17 – Switching Time Test Circuit

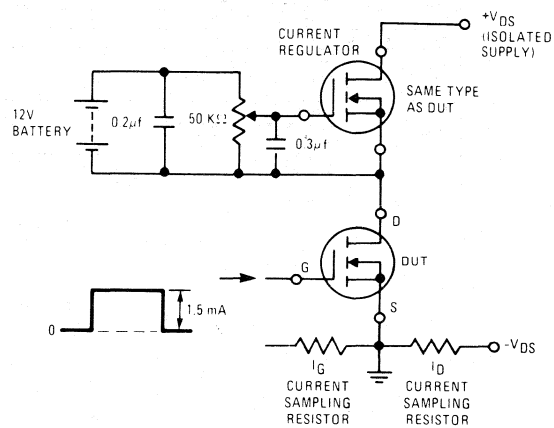


Fig. 18 – Gate Charge Test Circuit

IRF320, IRF321, IRF322, IRF323

File Number **1569**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.5A and 3.0A, 350V-400V

$r_{DS}(on)$ = 1.8 Ω and 2.5 Ω

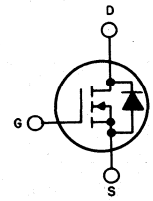
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF320, IRF321, IRF322 and IRF323 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

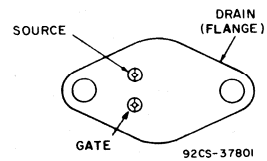
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

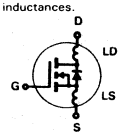
Parameter		IRF320	IRF321	IRF322	IRF323	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		12	12	10	10	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF320, IRF321, IRF322, IRF323

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF320 IRF322	400	–	–	V	V_{GS} = 0V
		IRF321 IRF323	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF320 IRF321	3.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF322 IRF323	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF320 IRF321	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF322 IRF323	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

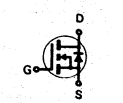


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF320 IRF321	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF322 IRF323	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF320 IRF321	–	–	12	A	
		IRF322 IRF323	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	IRF320 IRF321	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		IRF322 IRF323	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2% ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF320, IRF321, IRF322, IRF323

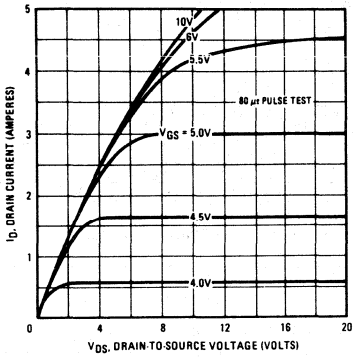


Fig. 1 – Typical Output Characteristics

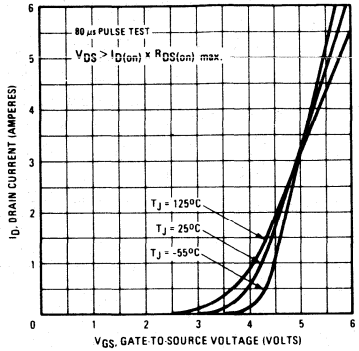


Fig. 2 – Typical Transfer Characteristics

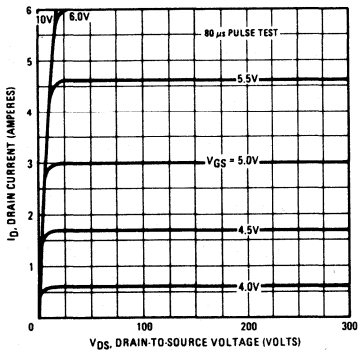


Fig. 3 – Typical Saturation Characteristics

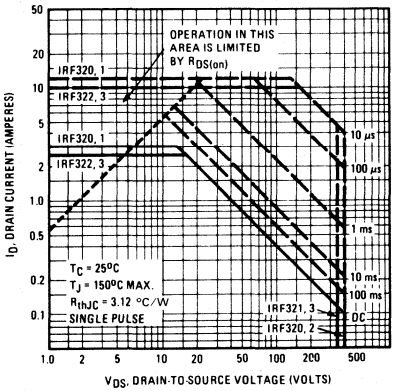


Fig. 4 – Maximum Safe Operating Area

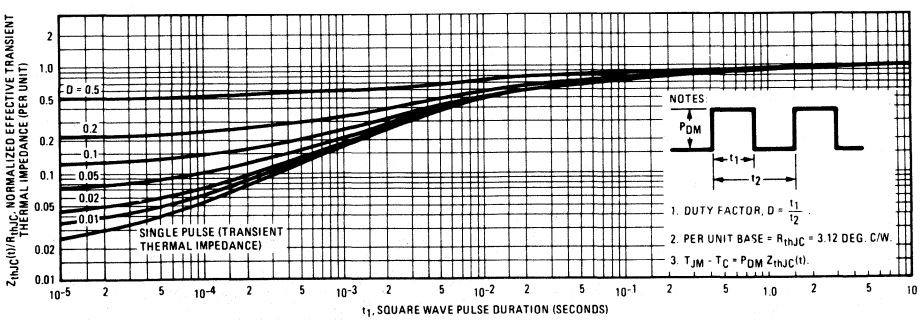


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

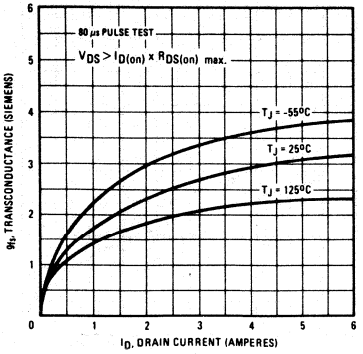


Fig. 6 – Typical Transconductance Vs. Drain Current

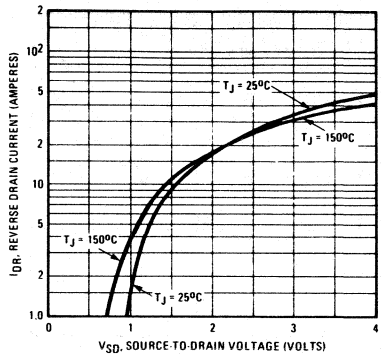


Fig. 7 – Typical Source-Drain Diode Forward Voltage

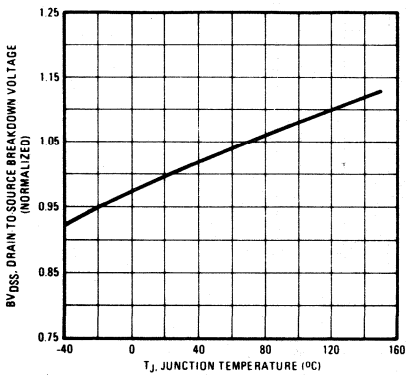


Fig. 8 – Breakdown Voltage Vs. Temperature

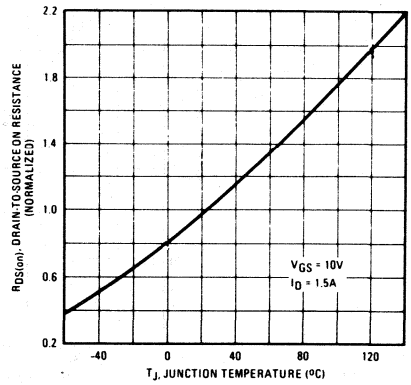


Fig. 9 – Normalized On-Resistance Vs. Temperature

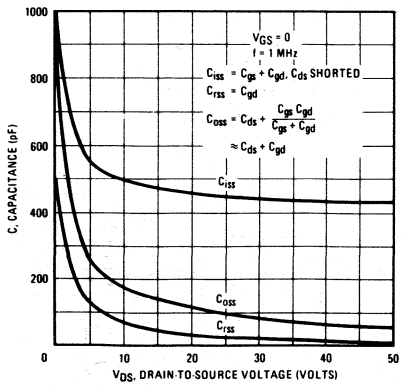


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

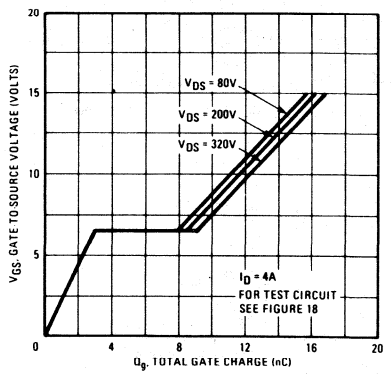


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF320, IRF321, IRF322, IRF323

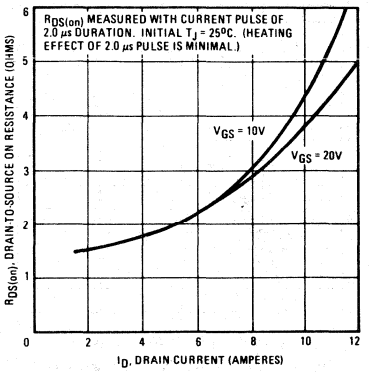


Fig. 12 – Typical On-Resistance Vs. Drain Current

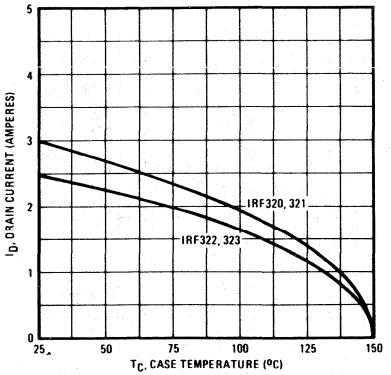


Fig. 13 – Maximum Drain Current Vs. Case Temperature

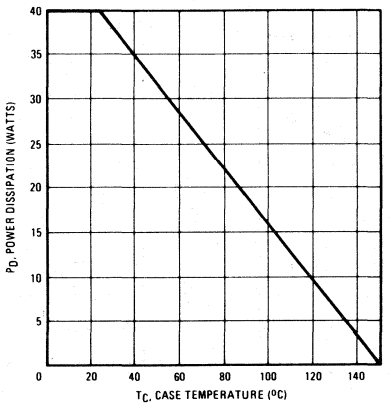


Fig. 14 – Power Vs. Temperature Derating Curve

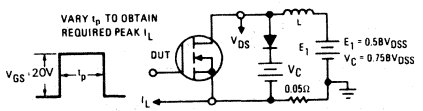


Fig. 15 – Clamped Inductive Test Circuit

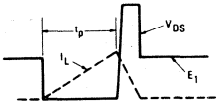


Fig. 16 – Clamped Inductive Waveforms

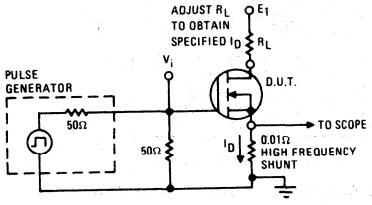


Fig. 17 – Switching Time Test Circuit

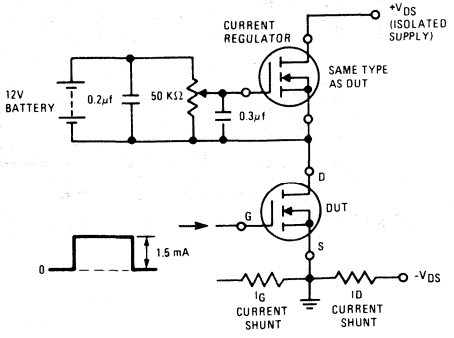


Fig. 18 – Gate Charge Test Circuit

File Number **1570**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5A and 5.5A, 350V-400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

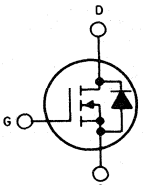
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF330, IRF331, IRF332 and IRF333 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

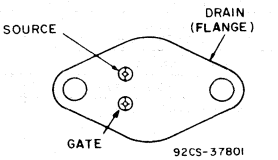
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

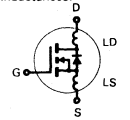
	Parameter	IRF330	IRF331	IRF332	IRF333	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF330, IRF331, IRF332, IRF333

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF330 IRF332	400	–	–	V	V_{GS} = 0V
		IRF331 IRF333	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF330 IRF331	5.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF332 IRF333	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF330 IRF331	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF332 IRF333	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	700	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	17	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	11	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

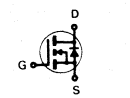


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF330 IRF331	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF332 IRF333	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF330 IRF331	–	–	22	A	
		IRF332 IRF333	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	IRF330 IRF331	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF332 IRF333	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

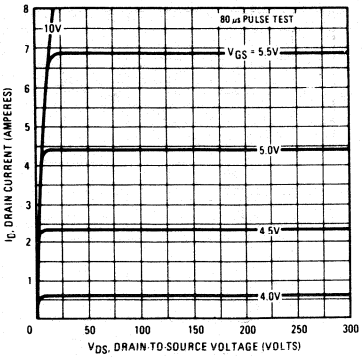


Fig. 1 — Typical Output Characteristics

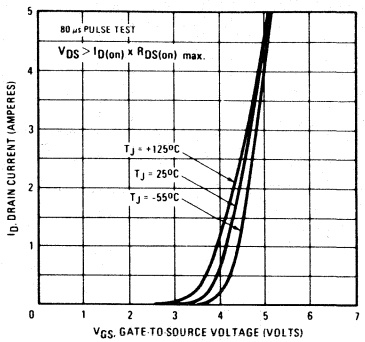


Fig. 2 — Typical Transfer Characteristics

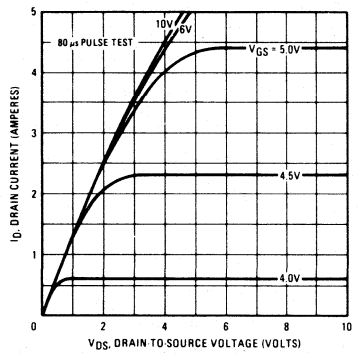


Fig. 3 — Typical Saturation Characteristics

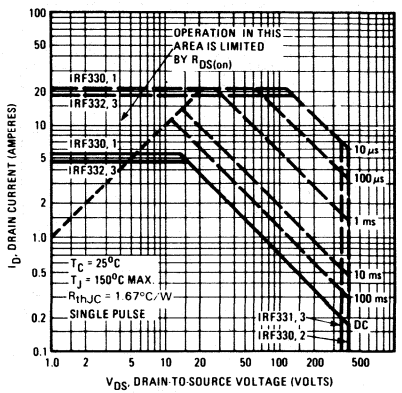


Fig. 4 — Maximum Safe Operating Area

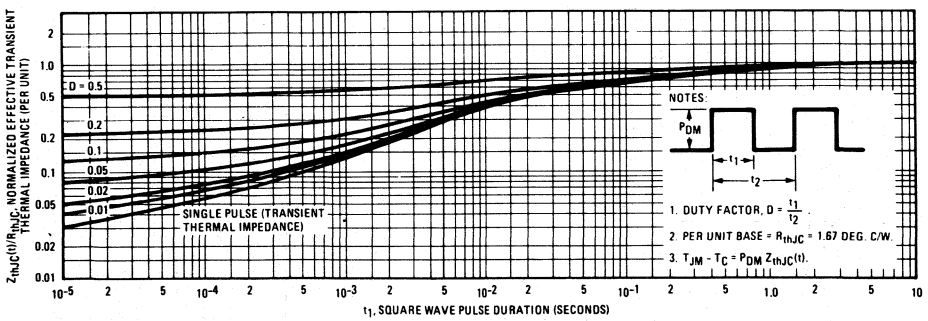


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

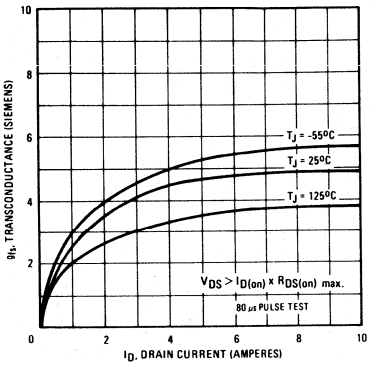


Fig. 6 – Typical Transconductance Vs. Drain Current

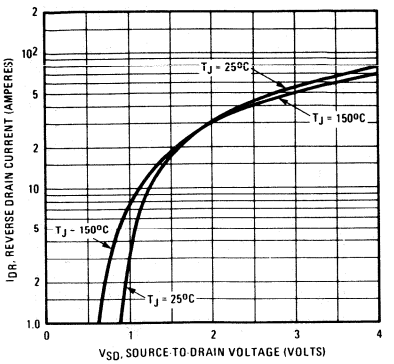


Fig. 7 – Typical Source-Drain Diode Forward Voltage

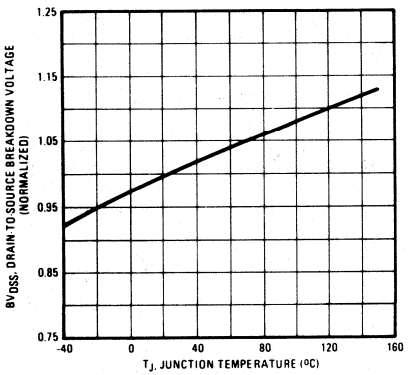


Fig. 8 – Breakdown Voltage Vs. Temperature

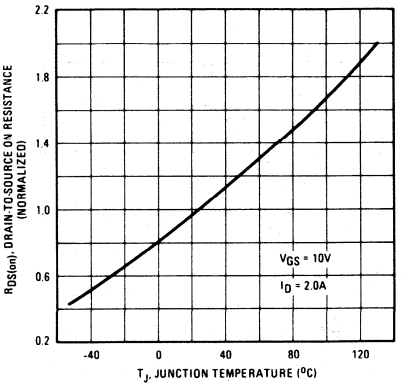


Fig. 9 – Normalized On-Resistance Vs. Temperature

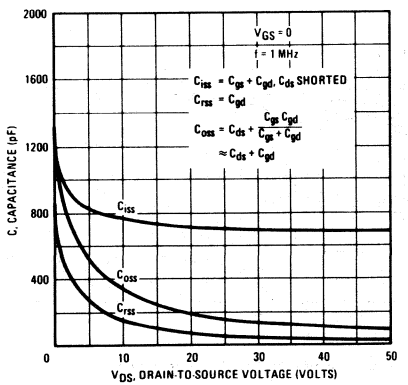


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

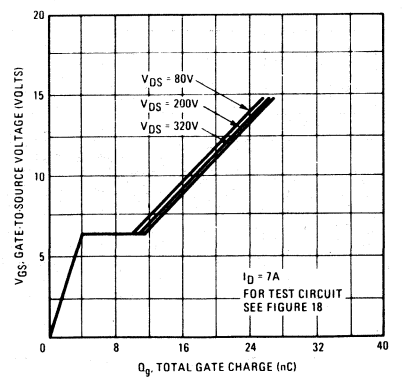


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

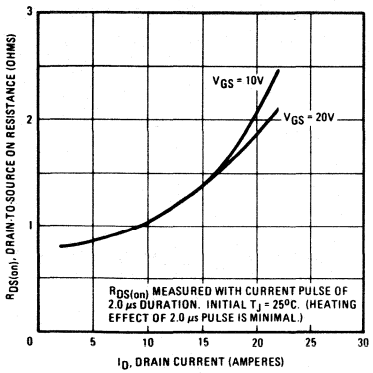


Fig. 12 – Typical On-Resistance Vs. Drain Current

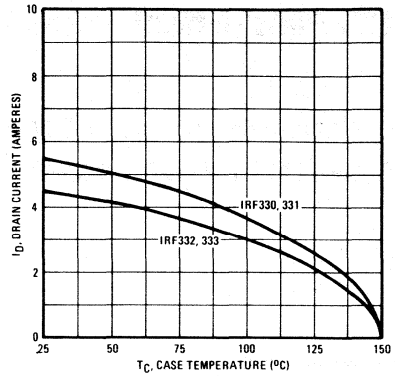


Fig. 13 – Maximum Drain Current Vs. Case Temperature

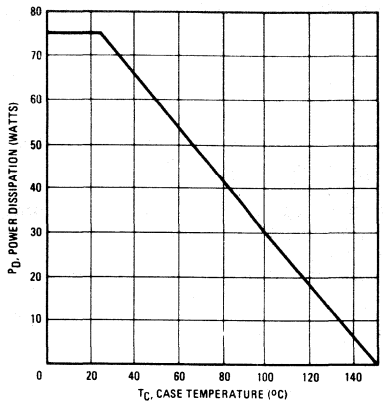


Fig. 14 – Power Vs. Temperature Derating Curve

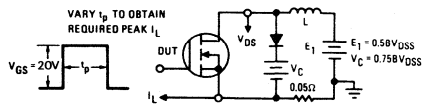


Fig. 15 – Clamped Inductive Test Circuit

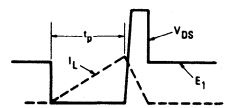


Fig. 16 – Clamped Inductive Waveforms

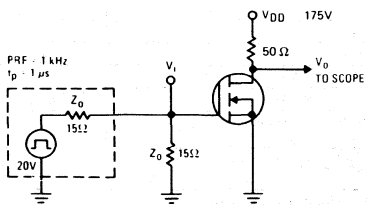


Fig. 17 – Switching Time Test Circuit

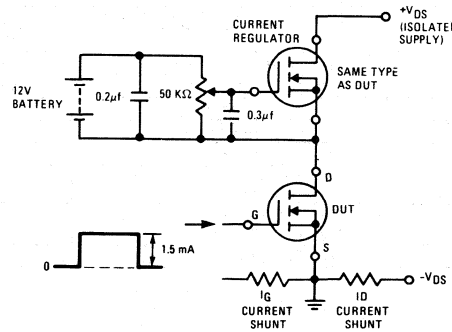


Fig. 18 – Gate Charge Test Circuit

IRF340, IRF341, IRF342, IRF343

File Number **2307**

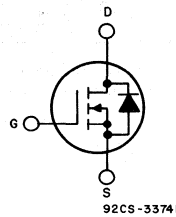
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8 A and 10 A, 350 V - 400 V
$r_{DS(on)}$ = 0.55 Ω and 0.8 Ω

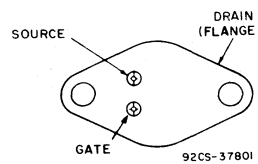
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

The IRF340, IRF341, IRF342, and IRF343 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA metal package.

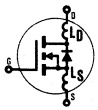
Absolute Maximum Ratings

	Parameter	IRF340	IRF341	IRF342	IRF343	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		40	40	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF340 IRF342	400	–	–	V	V_{GS} = 0V
		IRF341 IRF343	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF340 IRF341	10	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF342 IRF343	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF340 IRF341	–	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF342 IRF343	–	0.68	0.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	1250	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5.0	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	45	90	ns	
t_f	Fall Time	ALL	–	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	18	27	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	23	35	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF340 IRF341	–	–	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF342 IRF343	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF340 IRF341	–	–	40	A	
		IRF342 IRF343	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF340 IRF341	–	–	2.0	V	T_C = 25°C, I_S = 10A, V_{GS} = 0V
		IRF342 IRF343	–	–	1.9	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	5.7	–	μC	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF340, IRF341, IRF342, IRF343

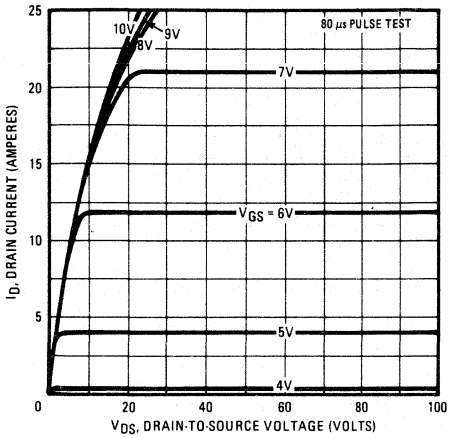


Fig. 1 — Typical Output Characteristics

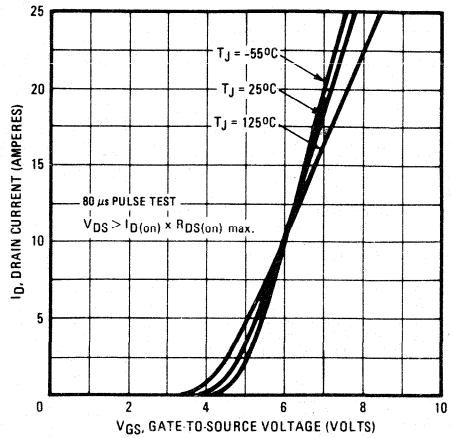


Fig. 2 — Typical Transfer Characteristics

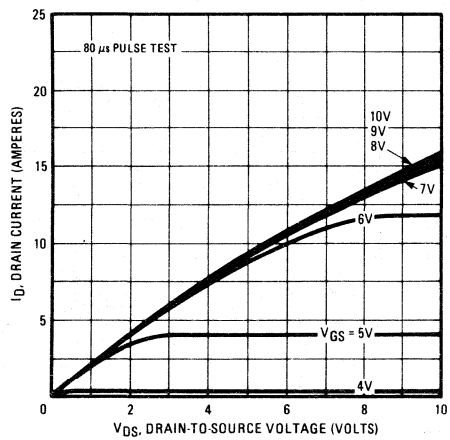


Fig. 3 — Typical Saturation Characteristics

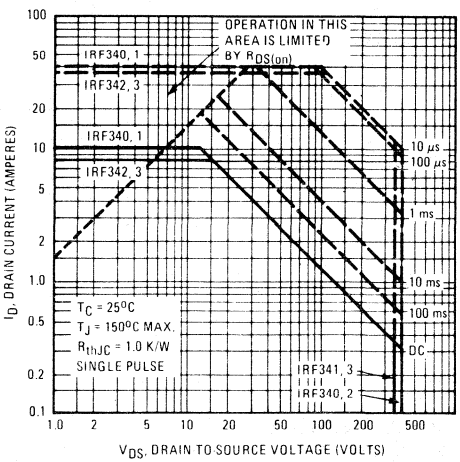


Fig. 4 — Maximum Safe Operating Area

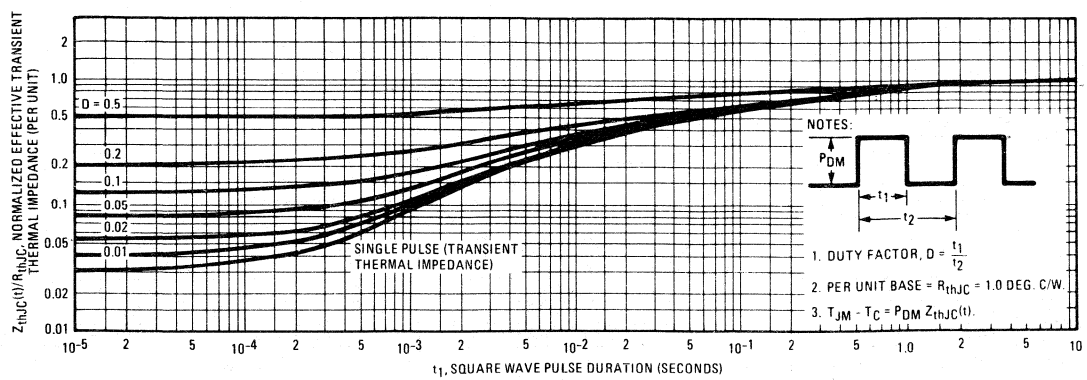


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

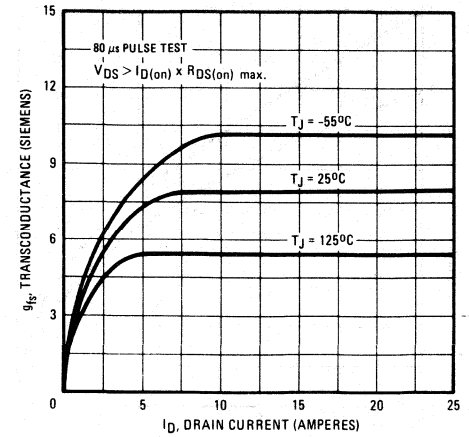


Fig. 6 – Typical Transconductance Vs. Drain Current

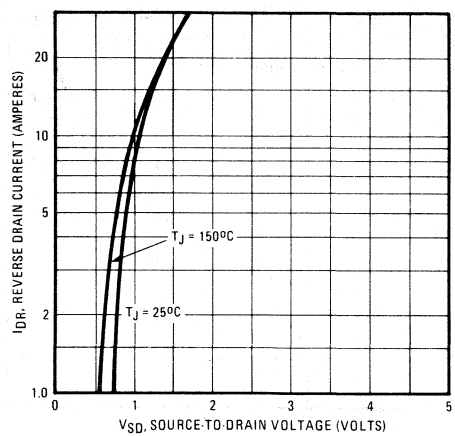


Fig. 7 – Typical Source-Drain Diode Forward Voltage

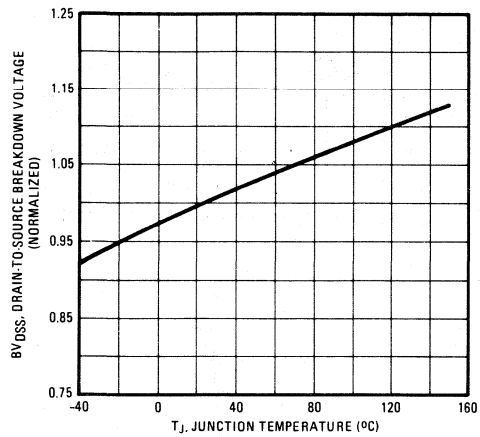


Fig. 8 – Breakdown Voltage Vs. Temperature

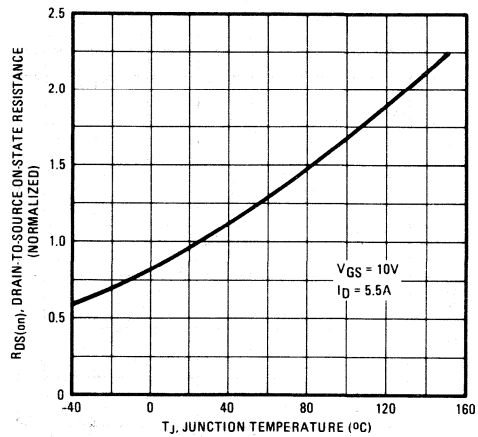


Fig. 9 – Normalized On-Resistance Vs. Temperature

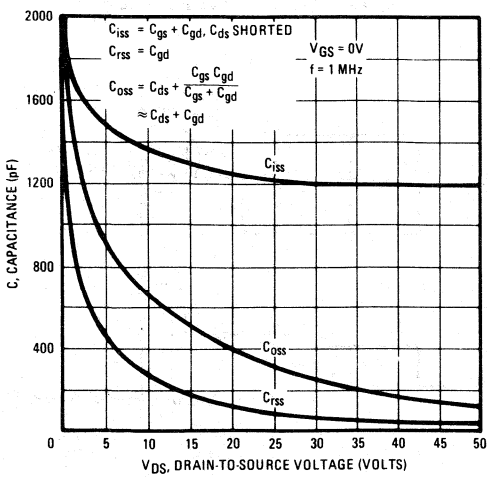


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

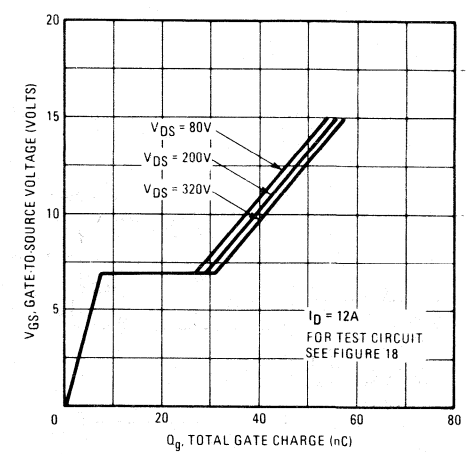


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF340, IRF341, IRF342, IRF343

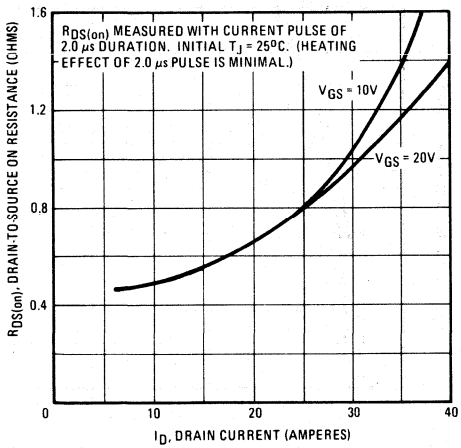


Fig. 12 – Typical On-Resistance Vs. Drain Current

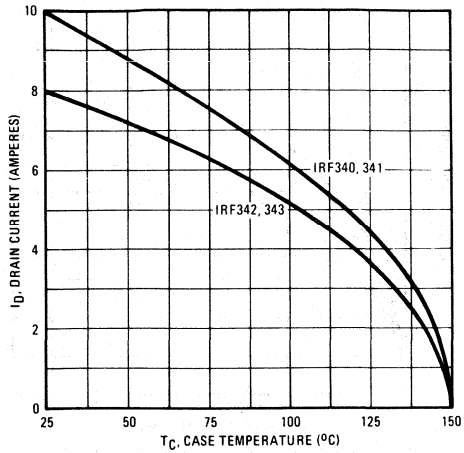


Fig. 13 – Maximum Drain Current Vs. Case Temperature

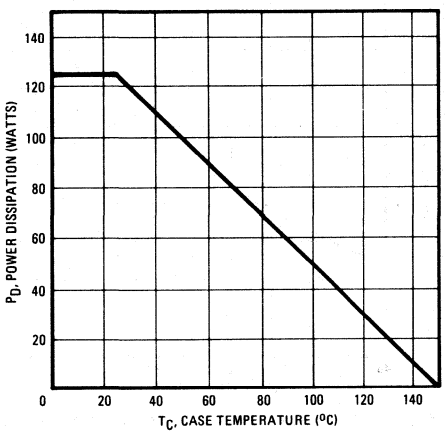


Fig. 14 – Power Vs. Temperature Derating Curve

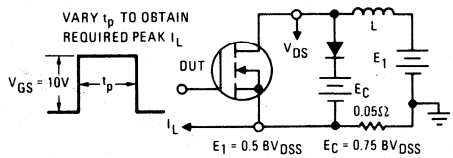


Fig. 15 – Clamped Inductive Test Circuit

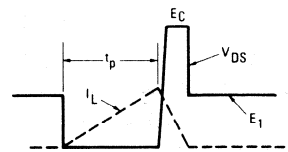


Fig. 16 – Clamped Inductive Waveforms

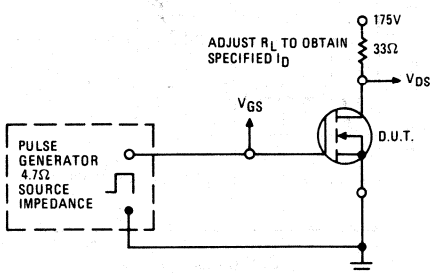


Fig. 17 – Switching Time Test Circuit

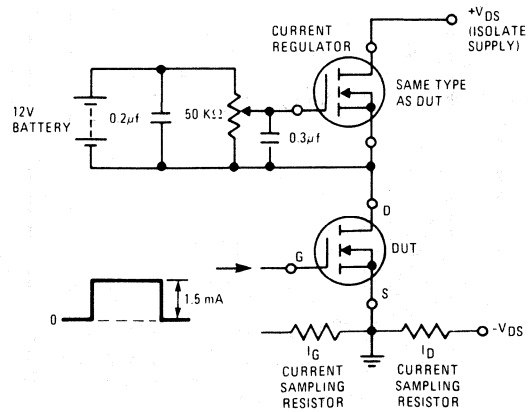


Fig. 18 – Gate Charge Test Circuit

File Number **1826**

IRF350, IRF351, IRF352, IRF353

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

13 A and 15 A, 350 V - 400 V
$r_{DS}(on)$ = 0.3 Ω and 0.4 Ω

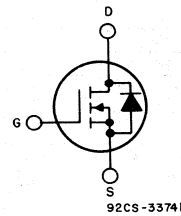
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF350, IRF351, IRF352 and IRF353 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

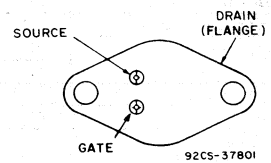
The IRF-types are supplied in the JEDEC TO-204AA metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

Absolute Maximum Ratings

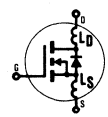
	Parameter	IRF350	IRF351	IRF352	IRF353	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	15	15	13	13	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	60	60	52	52	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		60	60	52	52	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF350, IRF351, IRF352, IRF353

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF350 IRF352	400	–	–	V	V_{GS} = 0V
		IRF351 IRF353	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF350 IRF351	15	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF352 IRF353	13	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF350 IRF351	–	0.25	0.3	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF352 IRF353	–	0.3	0.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≈ 180V, I_D = 8.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	65	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	75	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	38	57	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	41	62	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF350 IRF351	–	–	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF352 IRF353	–	–	13	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF350 IRF351	–	–	60	A	
		IRF352 IRF353	–	–	52	A	
V_{SD}	Diode Forward Voltage ②	IRF350 IRF351	–	–	1.6	V	T_C = 25°C, I_S = 15A, V_{GS} = 0V
		IRF352 IRF353	–	–	1.5	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.6	–	μC	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

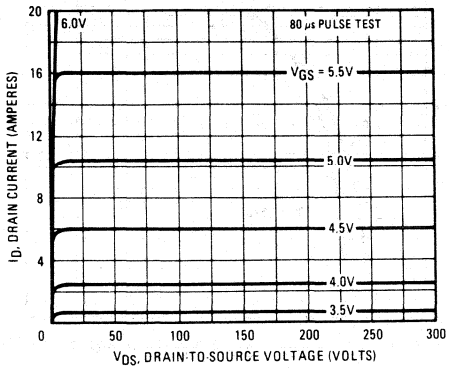


Fig. 1 — Typical Output Characteristics

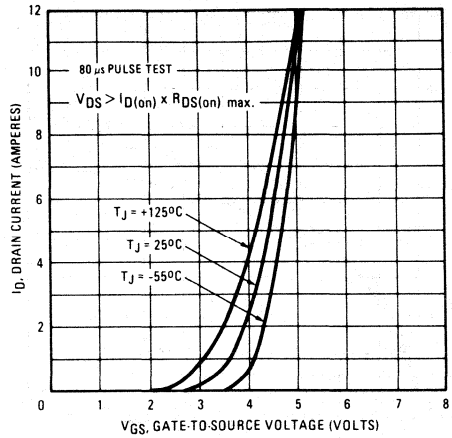


Fig. 2 — Typical Transfer Characteristics

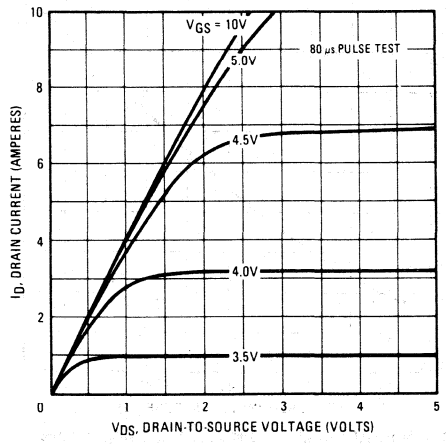


Fig. 3 — Typical Saturation Characteristics

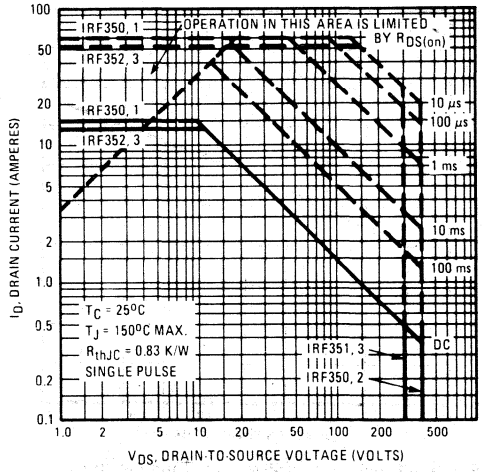


Fig. 4 — Maximum Safe Operating Area

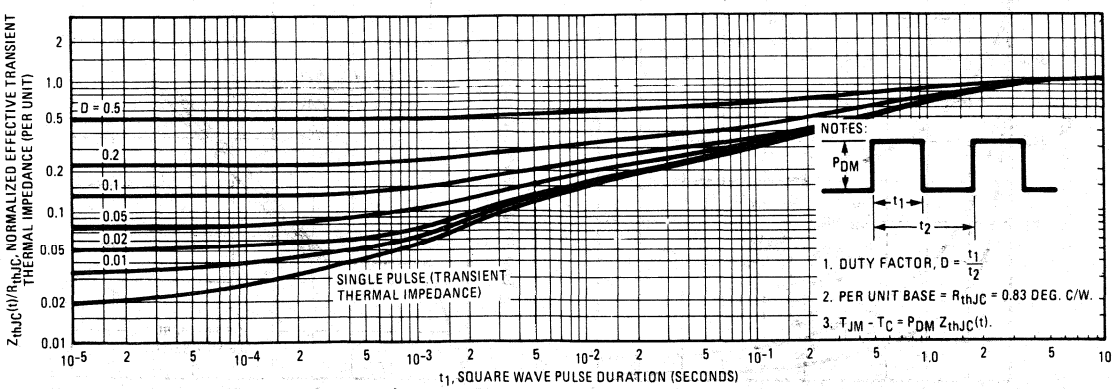


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

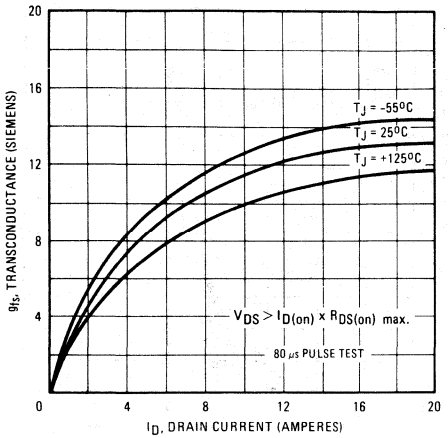


Fig. 6 — Typical Transconductance Vs. Drain Current

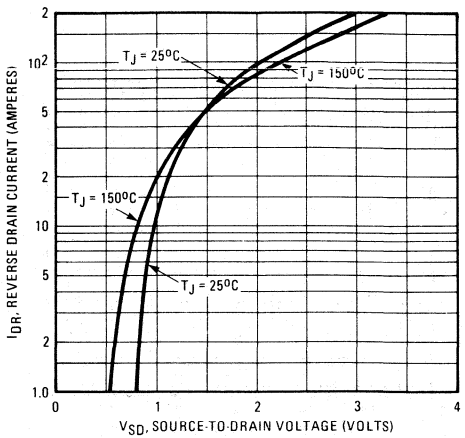


Fig. 7 — Typical Source-Drain Diode Forward Voltage

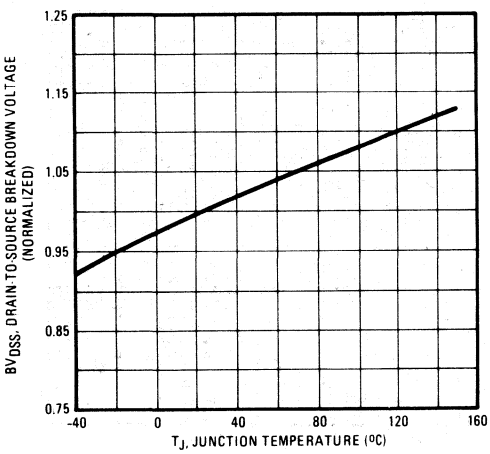


Fig. 8 — Breakdown Voltage Vs. Temperature

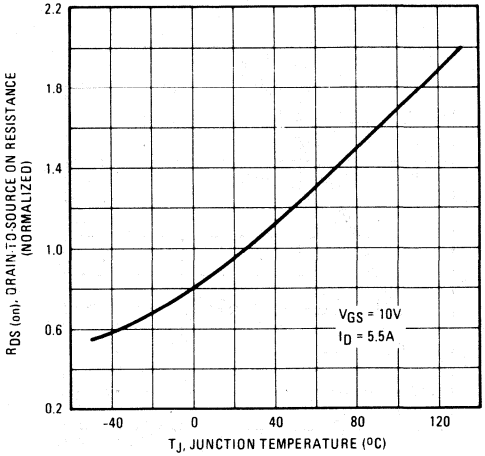


Fig. 9 — Normalized On-Resistance Vs. Temperature

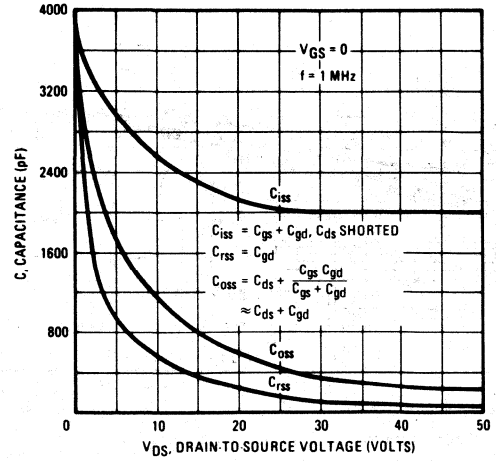


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

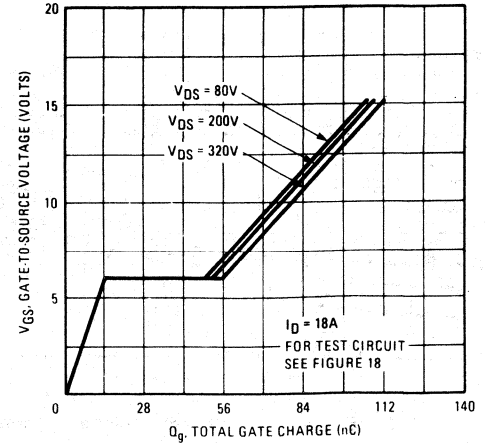


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

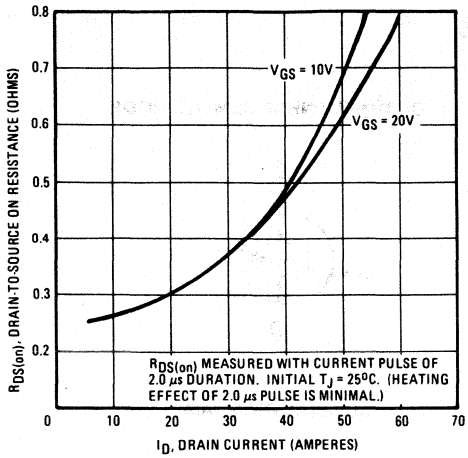


Fig. 12 – Typical On-Resistance Vs. Drain Current

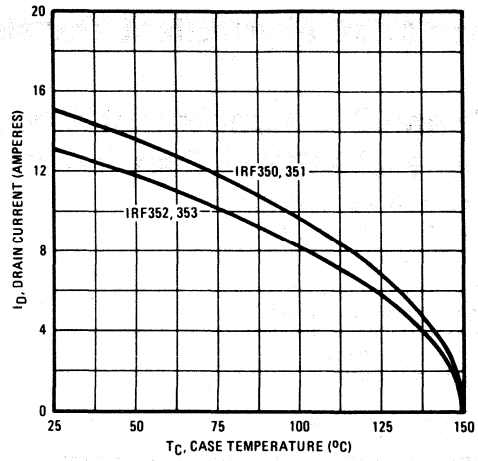


Fig. 13 – Maximum Drain Current Vs. Case Temperature

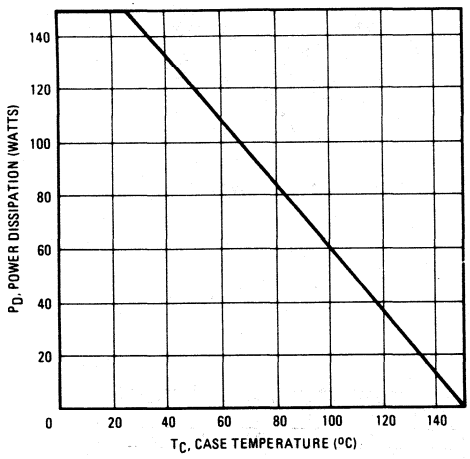


Fig. 14 – Power Vs. Temperature Derating Curve

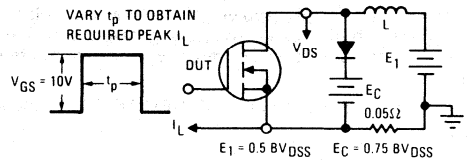


Fig. 15 – Clamped Inductive Test Circuit

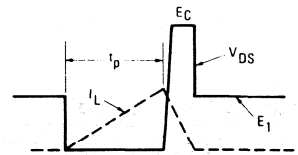


Fig. 16 – Clamped Inductive Waveforms

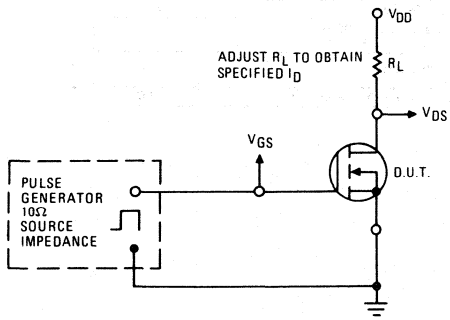


Fig. 17 – Switching Time Test Circuit

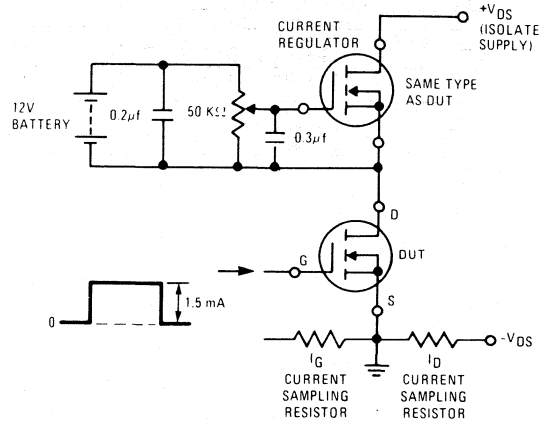


Fig. 18 – Gate Charge Test Circuit

IRF420, IRF421, IRF422, IRF423

File Number **1571**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.0A and 2.5A, 450V-500V

$r_{DS}(on)$ = 3.0 Ω and 4.0 Ω

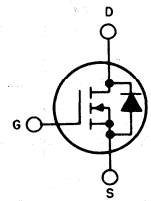
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF420, IRF421, IRF422 and IRF423 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

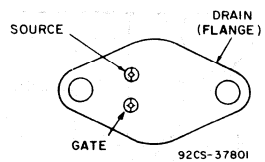
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

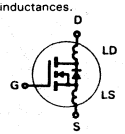
Absolute Maximum Ratings

Parameter		IRF420	IRF421	IRF422	IRF423	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF420, IRF422	500	–	–	V	V_{GS} = 0V
		IRF421, IRF423	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF420, IRF421	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF422, IRF423	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF420, IRF421	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF422, IRF423	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	7.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

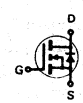


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF420, IRF421	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF422, IRF423	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF420, IRF421	–	–	10	A	
		IRF422, IRF423	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF420, IRF421	–	–	1.4	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF422, IRF423	–	–	1.3	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF420, IRF421, IRF422, IRF423

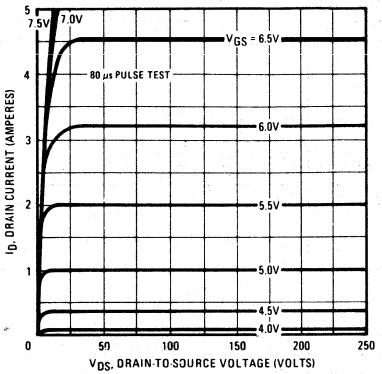


Fig. 1 — Typical Output Characteristics

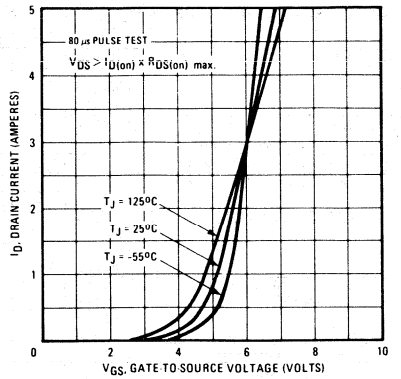


Fig. 2 — Typical Transfer Characteristics

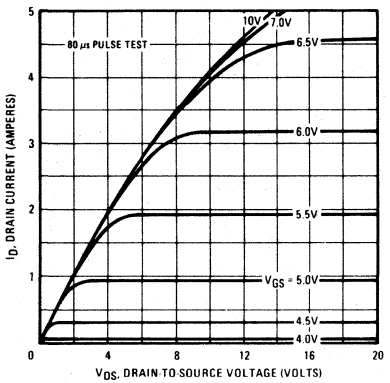


Fig. 3 — Typical Saturation Characteristics

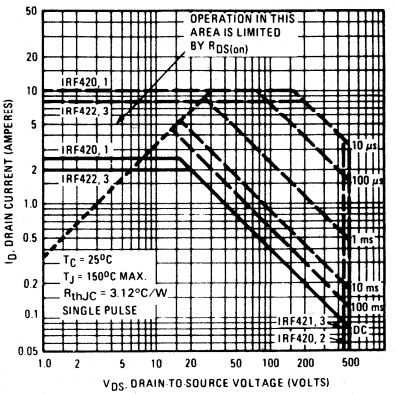


Fig. 4 — Maximum Safe Operating Area

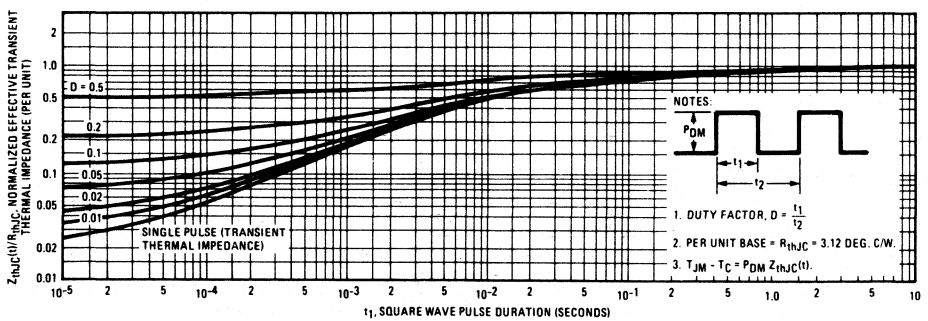


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

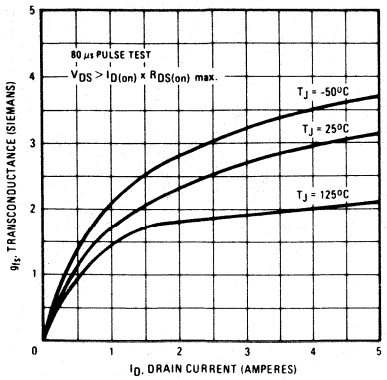


Fig. 6 – Typical Transconductance Vs. Drain Current

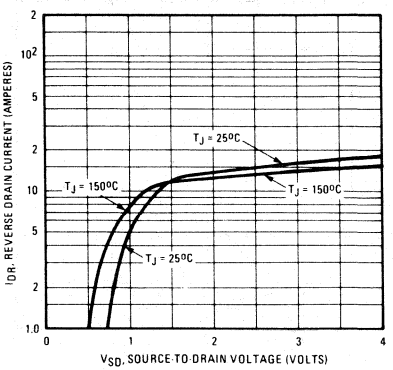


Fig. 7 – Typical Source-Drain Diode Forward Voltage

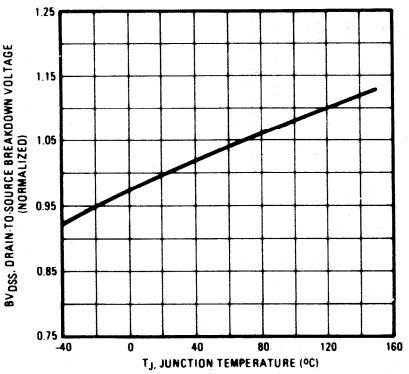


Fig. 8 – Breakdown Voltage Vs. Temperature

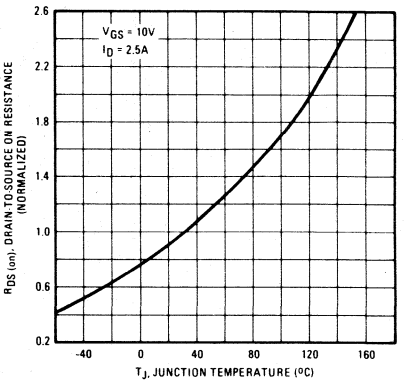


Fig. 9 – Normalized On-Resistance Vs. Temperature

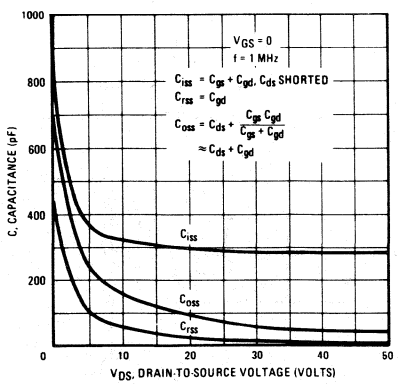


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

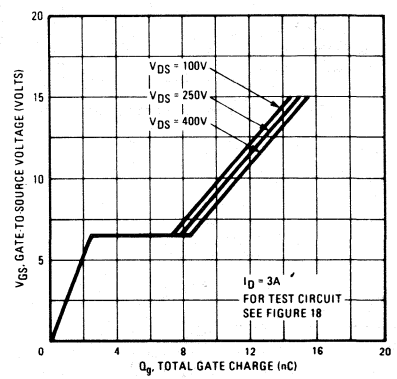


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF420, IRF421, IRF422, IRF423

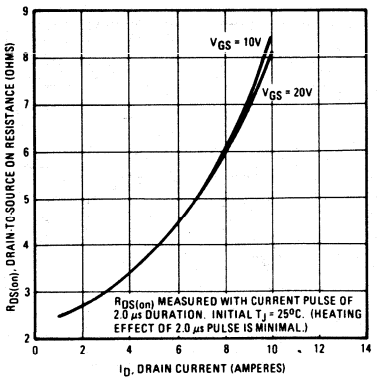


Fig. 12 – Typical On-Resistance Vs. Drain Current

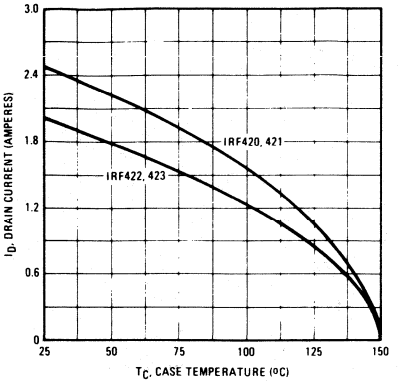


Fig. 13 – Maximum Drain Current Vs. Case Temperature

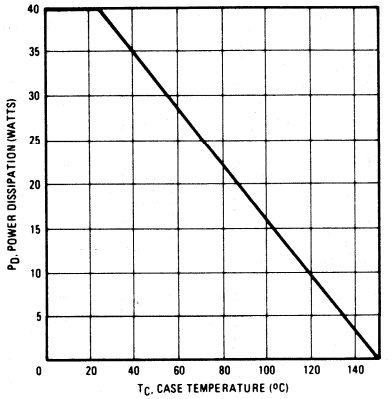


Fig. 14 – Power Vs. Temperature Derating Curve

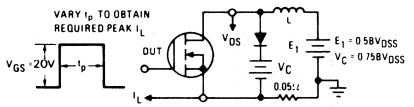


Fig. 15 – Clamped Inductive Test Circuit

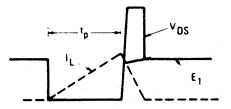


Fig. 16 – Clamped Inductive Waveforms

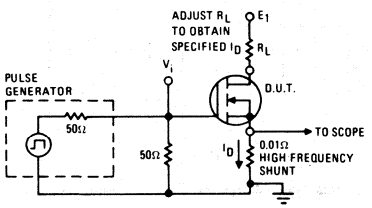


Fig. 17 – Switching Time Test Circuit

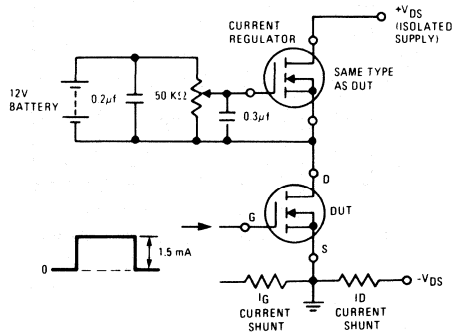


Fig. 18 – Gate Charge Test Circuit

File Number **1572**

IRF430, IRF431, IRF432, IRF433

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

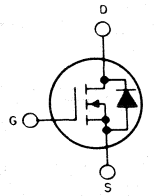
4.0A and 4.5A, 450V-500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

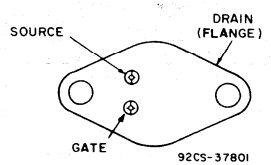
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

The IRF430, IRF431, IRF432 and IRF433 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

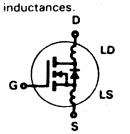
Parameter		IRF430	IRF431	IRF432	IRF433	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		18	18	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF430, IRF431, IRF432, IRF433

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF430 IRF432	500	–	–	V	V_{GS} = 0V
		IRF431 IRF433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF430 IRF431	4.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF432 IRF433	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF430 IRF431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF432 IRF433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 225V, I_D = 2.5A, Z_O = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	17	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	17	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF430 IRF431	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF432 IRF433	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF430 IRF431	–	–	18	A	
		IRF432 IRF433	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF430 IRF431	–	–	1.4	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF432 IRF433	–	–	1.3	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

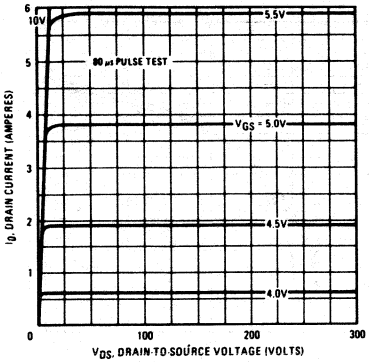


Fig. 1 – Typical Output Characteristics

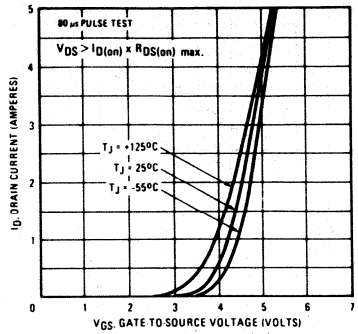


Fig. 2 – Typical Transfer Characteristics

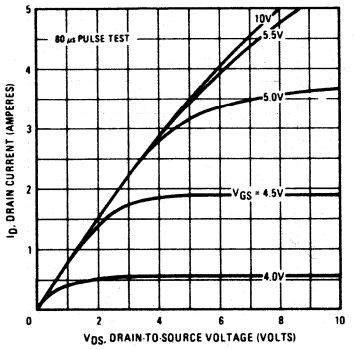


Fig. 3 – Typical Saturation Characteristics

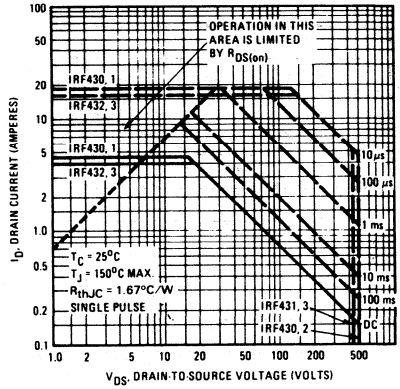


Fig. 4 – Maximum Safe Operating Area

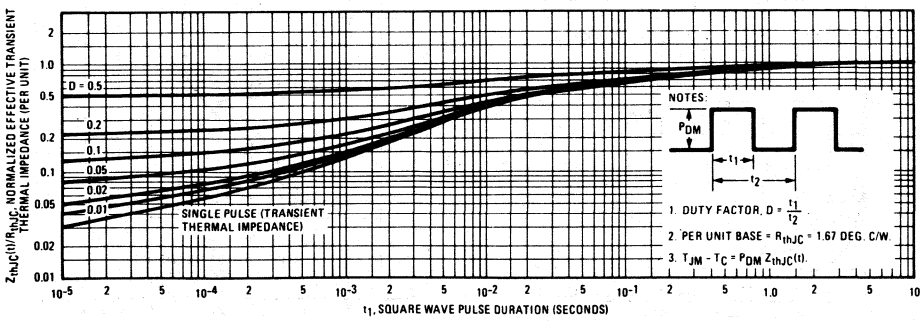


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF430, IRF431, IRF432, IRF433

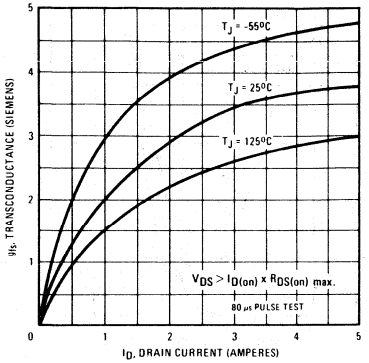


Fig. 6 – Typical Transconductance Vs. Drain Current

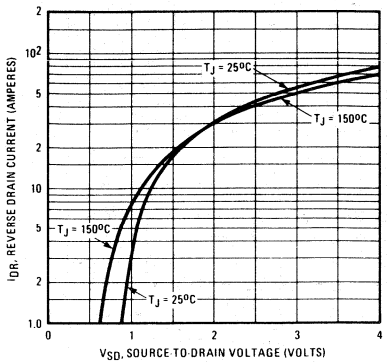


Fig. 7 – Typical Source-Drain Diode Forward Voltage

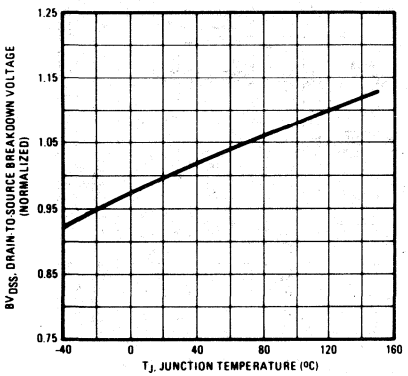


Fig. 8 – Breakdown Voltage Vs. Temperature

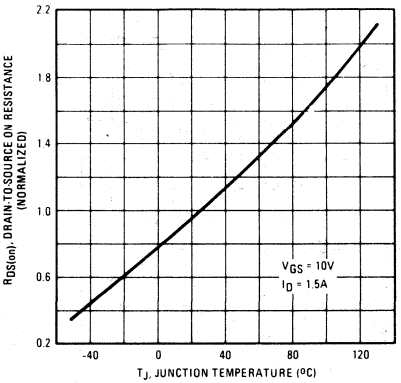


Fig. 9 – Normalized On-Resistance Vs. Temperature

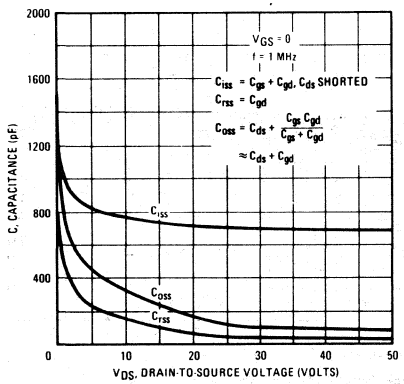


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

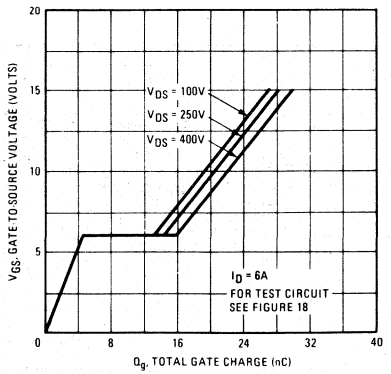


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

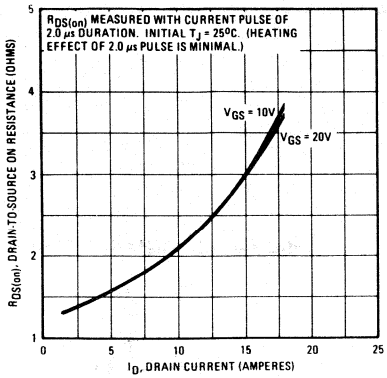


Fig. 12 – Typical On-Resistance Vs. Drain Current

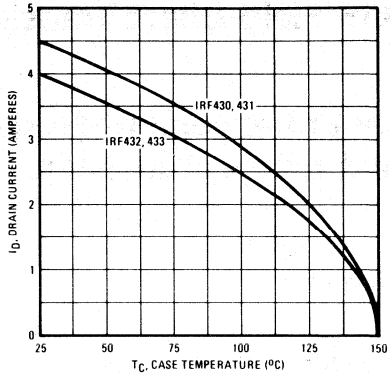


Fig. 13 – Maximum Drain Current Vs. Case Temperature

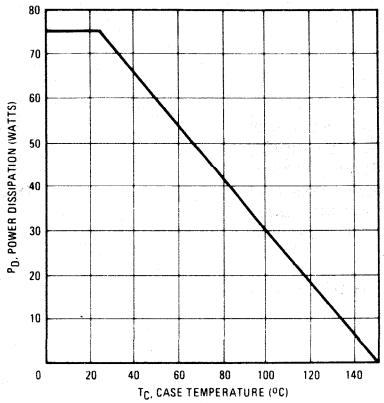


Fig. 14 – Power Vs. Temperature Derating Curve

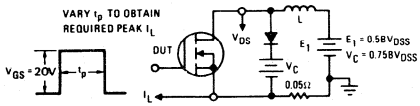


Fig. 15 – Clamped Inductive Test Circuit

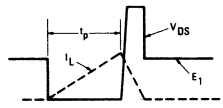


Fig. 16 – Clamped Inductive Waveforms

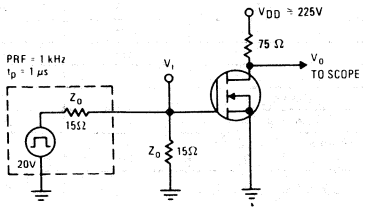


Fig. 17 – Switching Time Test Circuit

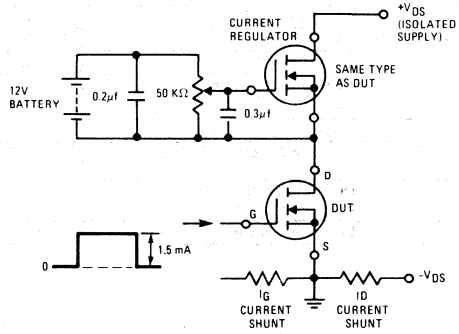


Fig. 18 – Gate Charge Test Circuit

IRF440, IRF441, IRF442, IRF443

File Number **2308**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

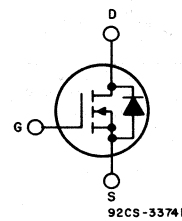
7 A and 8 A, 450 V - 500 V
$r_{DS(on)}$ = 0.85 Ω and 1.1 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF440, IRF441, IRF442, and IRF443 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

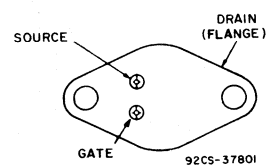
The IRF-types are supplied in the JEDEC TO-204AA steel package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

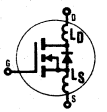
Absolute Maximum Ratings

	Parameter	IRF440	IRF441	IRF442	IRF443	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF440 IRF442	500	–	–	V	V_{GS} = 0V
		IRF441 IRF443	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF440 IRF441	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF442 IRF443	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF440 IRF441	–	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF442 IRF443	–	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	1225	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	85	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 200V, I_D = 4.0A, Z_O = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	42	90	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	20	30	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	22	33	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF440 IRF441	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF442 IRF443	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF440 IRF441	–	–	32	A	
		IRF442 IRF443	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF440 IRF441	–	–	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF442 IRF443	–	–	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1100	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.4	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF440, IRF441, IRF442, IRF443

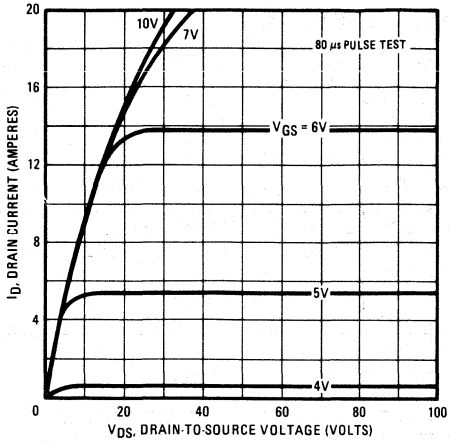


Fig. 1 — Typical Output Characteristics

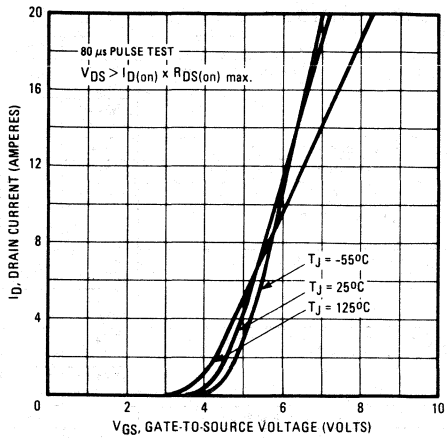


Fig. 2 — Typical Transfer Characteristics

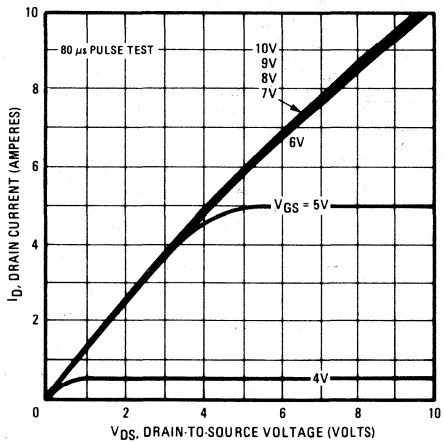


Fig. 3 — Typical Saturation Characteristics

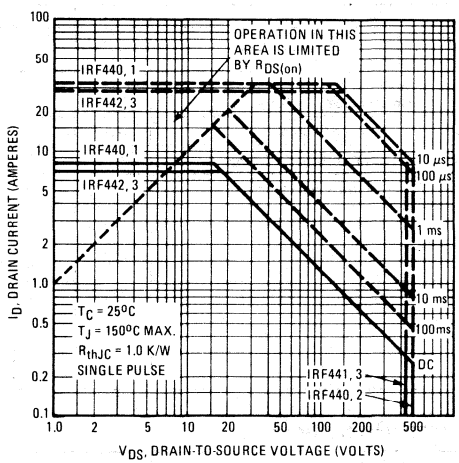


Fig. 4 — Maximum Safe Operating Area

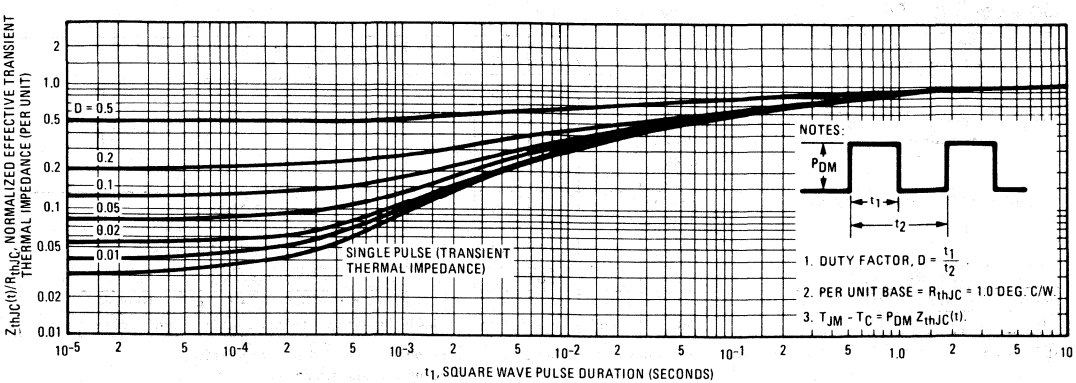


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

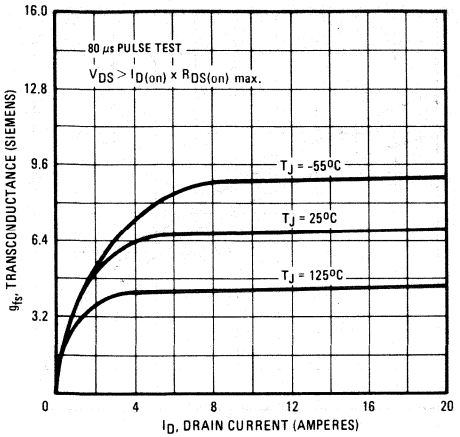


Fig. 6 — Typical Transconductance Vs. Drain Current

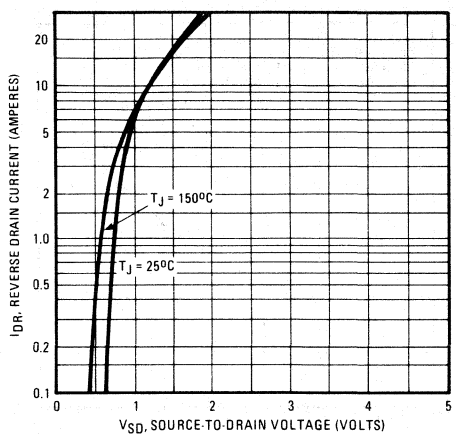


Fig. 7 — Typical Source-Drain Diode Forward Voltage

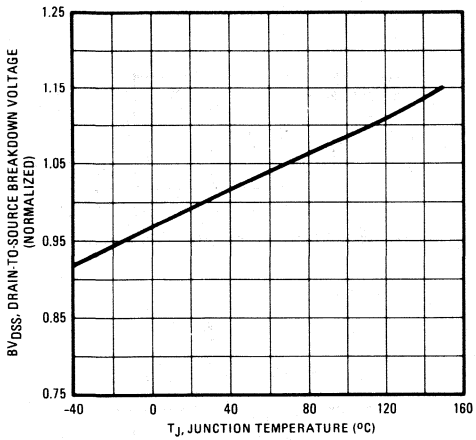


Fig. 8 — Breakdown Voltage Vs. Temperature

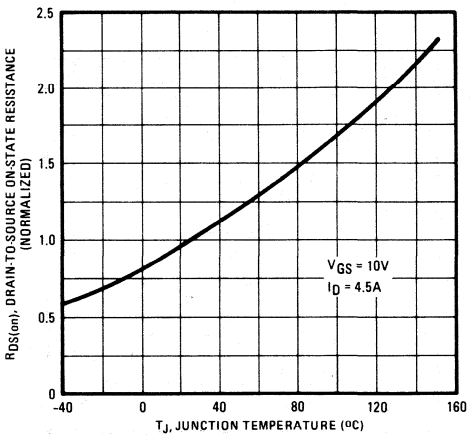


Fig. 9 — Normalized On-Resistance Vs. Temperature

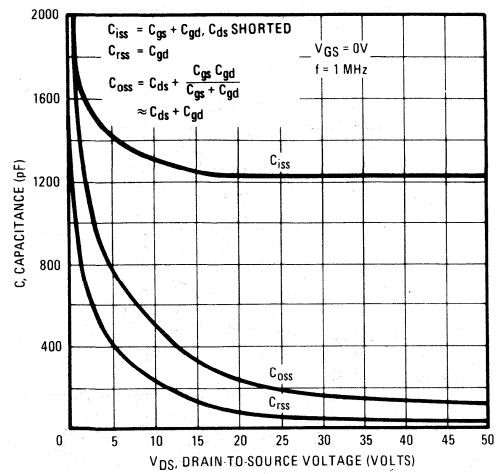


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

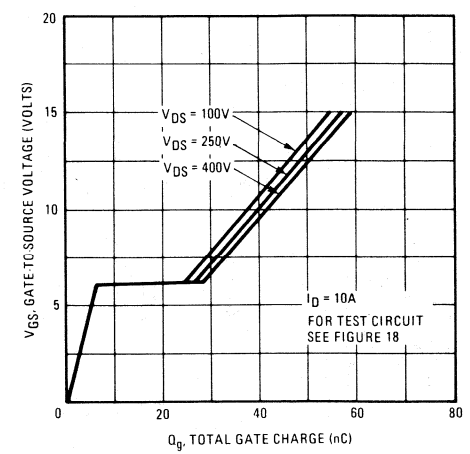


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

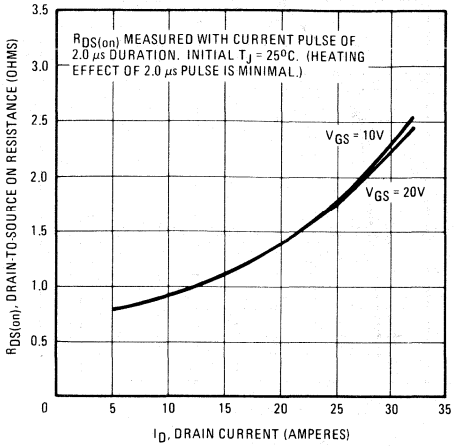


Fig. 12 – Typical On-Resistance Vs. Drain Current

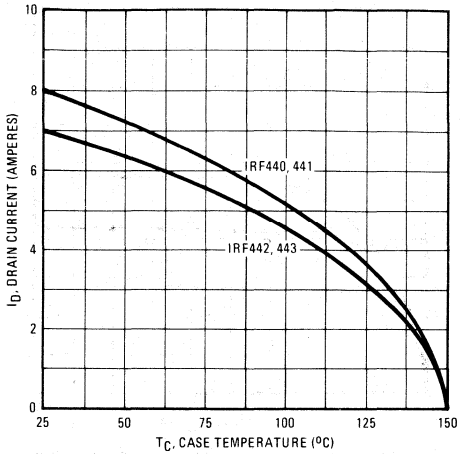


Fig. 13 – Maximum Drain Current Vs. Case Temperature

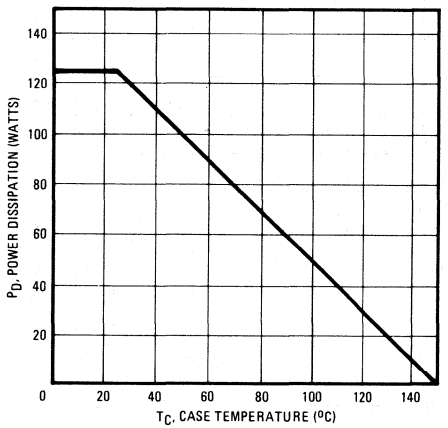


Fig. 14 – Power Vs. Temperature Derating Curve

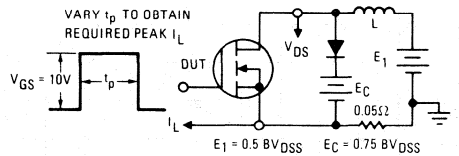


Fig. 15 – Clamped Inductive Test Circuit

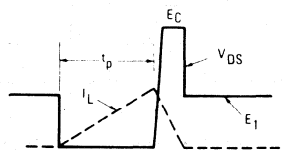


Fig. 16 – Clamped Inductive Waveforms

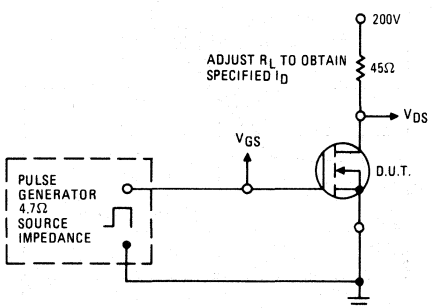


Fig. 17 – Switching Time Test Circuit

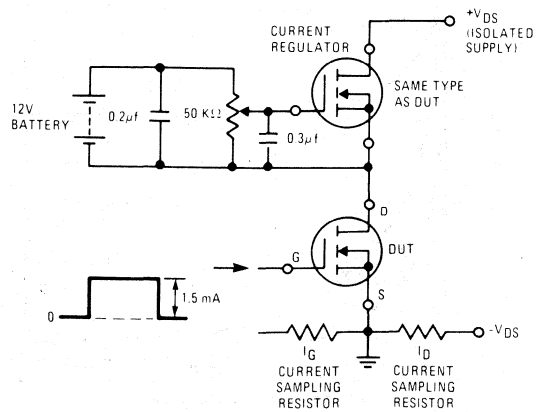


Fig. 18 – Gate Charge Test Circuit

File Number **1827**

IRF450, IRF451, IRF452, IRF453

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A and 13 A, 450 V - 500 V
$r_{DS}(on)$ = 0.4 Ω and 0.5 Ω

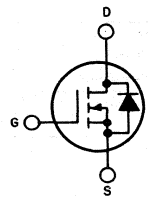
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF450, IRF451, IRF452 and IRF453 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

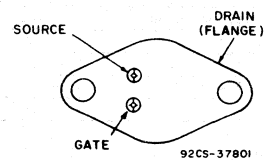
The IRF-types are supplied in the JEDEC TO-204AA metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

Absolute Maximum Ratings

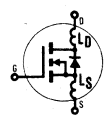
	Parameter	IRF450	IRF451	IRF452	IRF453	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	13	13	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
		52	52	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF450, IRF451, IRF452, IRF453

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF450 IRF452	500	–	–	V	V_{GS} = 0V
		IRF451 IRF453	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF450 IRF451	13	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF452 IRF453	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF450 IRF451	–	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		IRF452 IRF453	–	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	–	S(℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 7.0A
C_{iss}	Input Capacitance	ALL	–	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≈ 210V, I_D ≈ 7.0A, Z_O = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	82	120	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentialiv independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	40	60	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	63	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF450 IRF451	–	–	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF452 IRF453	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF450 IRF451	–	–	52	A	
		IRF452 IRF453	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF450 IRF451	–	–	1.4	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
		IRF452 IRF453	–	–	1.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1300	–	ns	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.4	–	μC	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

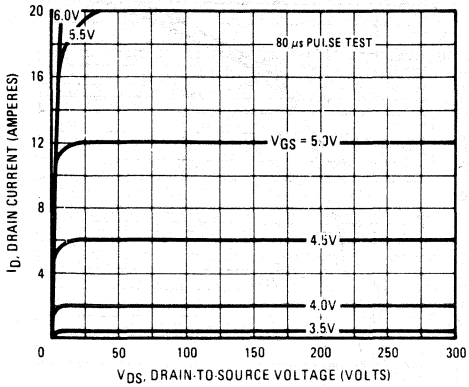


Fig. 1 — Typical Output Characteristics

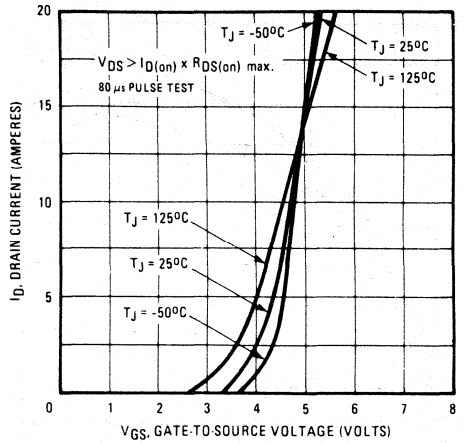


Fig. 2 — Typical Transfer Characteristics

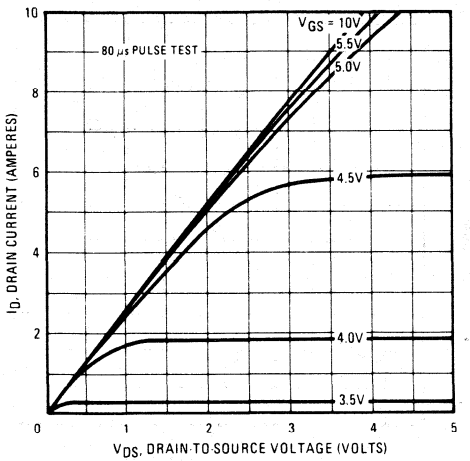


Fig. 3 — Typical Saturation Characteristics

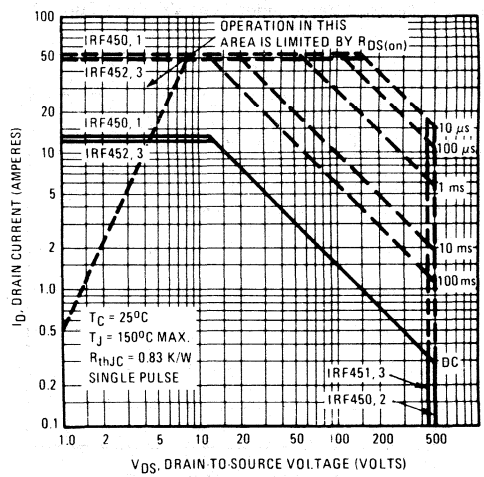


Fig. 4 — Maximum Safe Operating Area

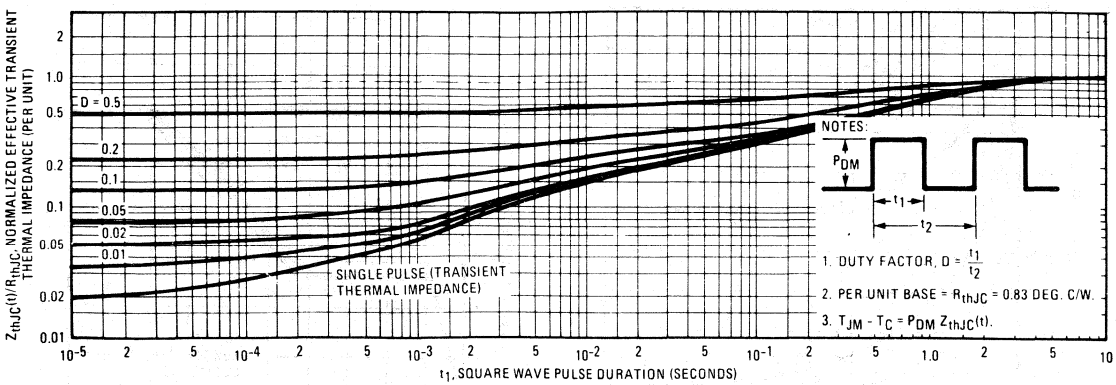


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF450, IRF451, IRF452, IRF453

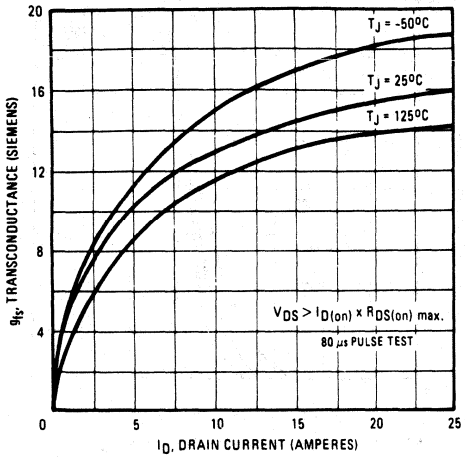


Fig. 6 — Typical Transconductance Vs. Drain Current

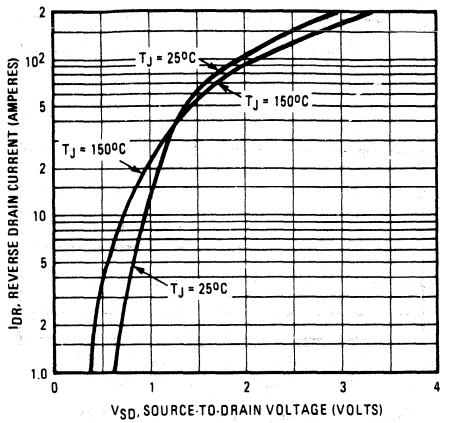


Fig. 7 — Typical Source-Drain Diode Forward Voltage

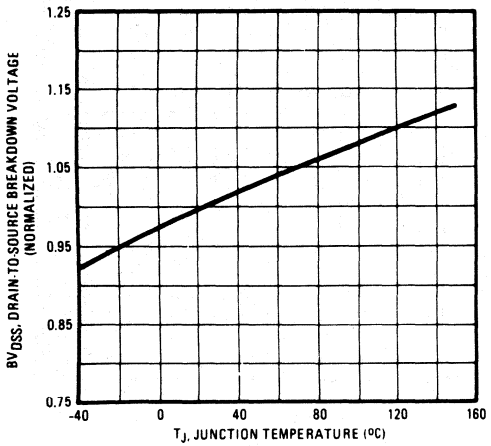


Fig. 8 — Breakdown Voltage Vs. Temperature

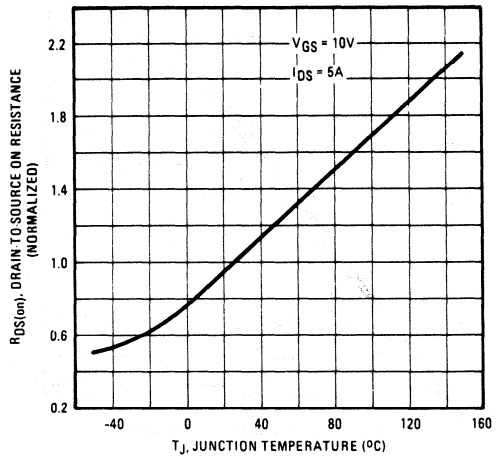


Fig. 9 — Normalized On-Resistance Vs. Temperature

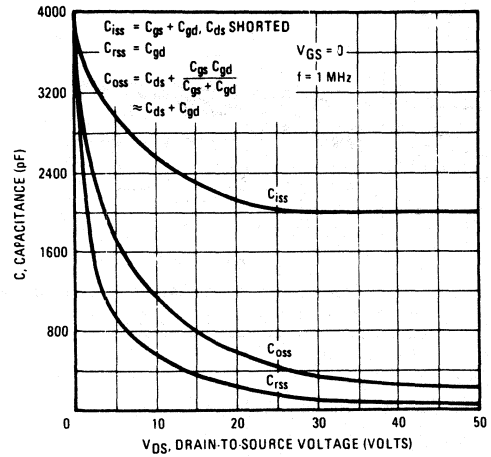


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

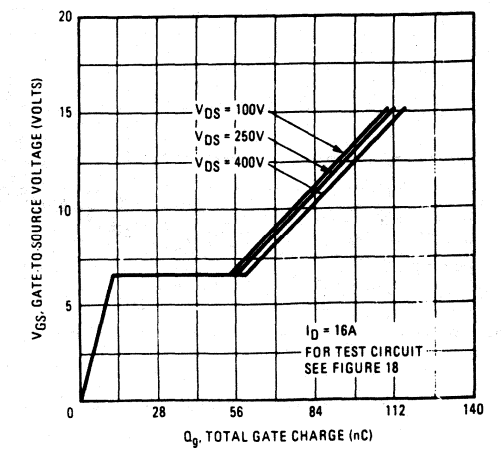


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

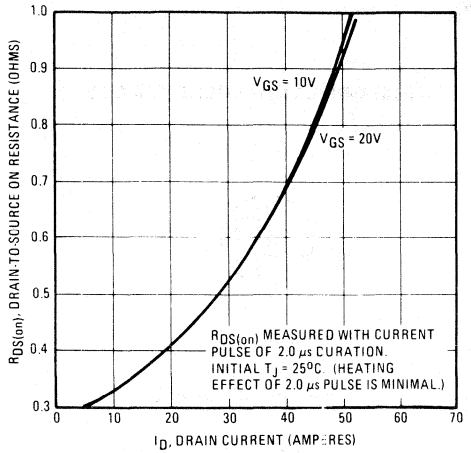


Fig. 12 – Typical On-Resistance Vs. Drain Current

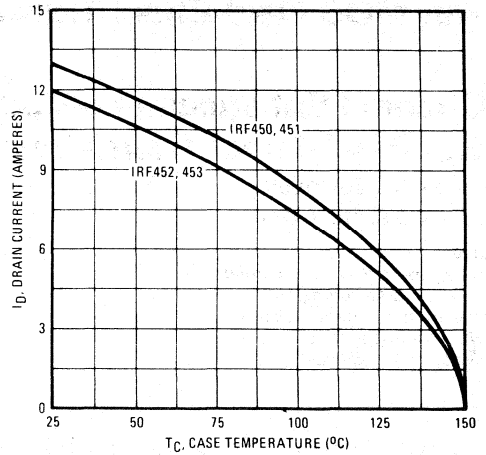


Fig. 13 – Maximum Drain Current Vs. Case Temperature

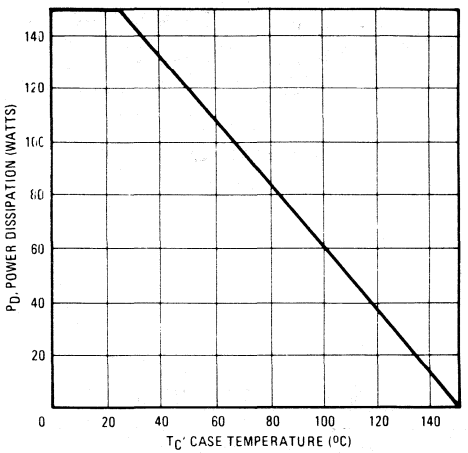


Fig. 14 – Power Vs. Temperature Derating Curve

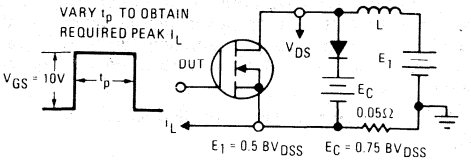


Fig. 15 – Clamped Inductive Test Circuit

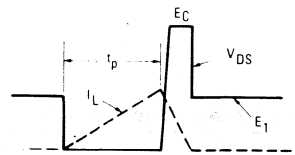


Fig. 16 – Clamped Inductive Waveforms

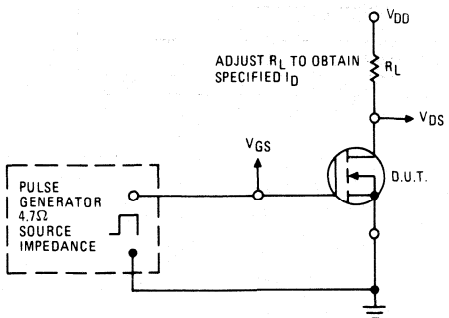


Fig. 17 – Switching Time Test Circuit

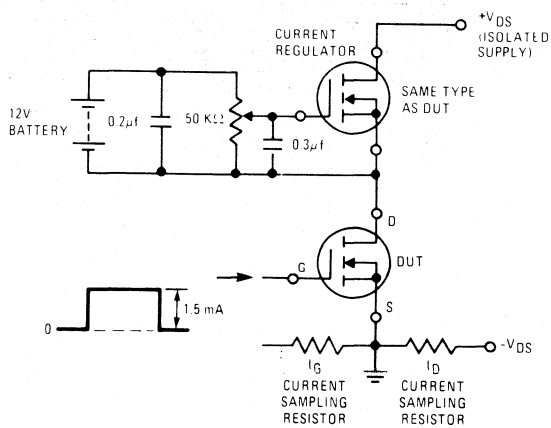


Fig. 18 – Gate Charge Test Circuit

IRF510, IRF511, IRF512, IRF513

File Number **1573**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

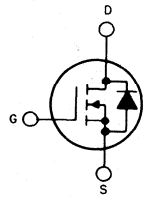
3.5A and 4.0A, 60V-100V

$r_{DS}(on)$ = 0.6 Ω and 0.8 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

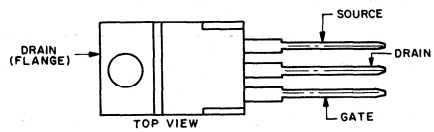
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF510, IRF511, IRF512 and IRF513 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

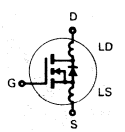
Absolute Maximum Ratings

Parameter		IRF510	IRF511	IRF512	IRF513	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0	4.0	3.5	3.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	16	16	14	14	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		16	16	14	14	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF510 IRF512	100	–	–	V	V_{GS} = 0V
		IRF511 IRF513	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF510 IRF511	4.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF512 IRF513	3.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF510 IRF511	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF512 IRF513	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.0A
C_{iss}	Input Capacitance	ALL	–	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	3.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

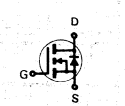


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF510 IRF511	–	–	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF512 IRF513	–	–	3.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF510 IRF511	–	–	16	A	
		IRF512 IRF513	–	–	14	A	
V_{SD}	Diode Forward Voltage ②	IRF510 IRF511	–	–	2.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
		IRF512 IRF513	–	–	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.4	–	μC	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF510, IRF511, IRF512, IRF513

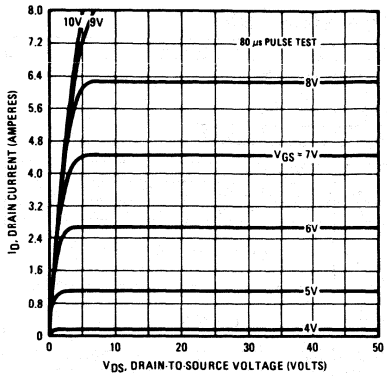


Fig. 1 – Typical Output Characteristics

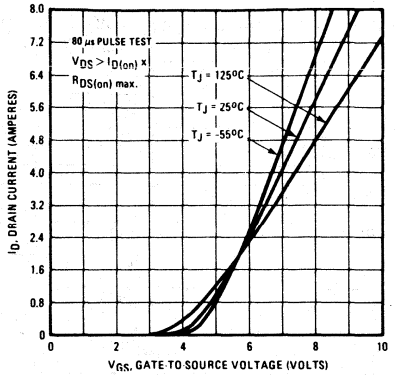


Fig. 2 – Typical Transfer Characteristics

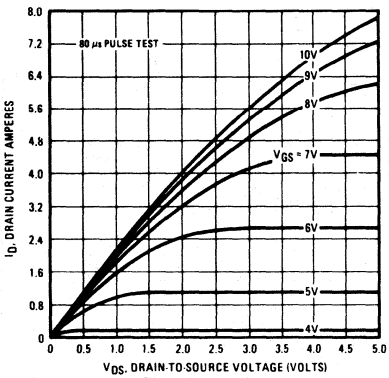


Fig. 3 – Typical Saturation Characteristics

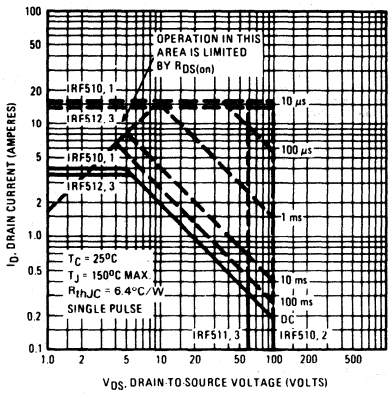


Fig. 4 – Maximum Safe Operating Area

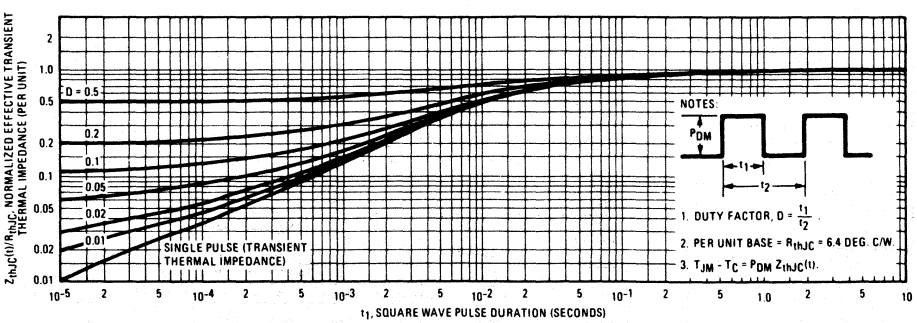


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

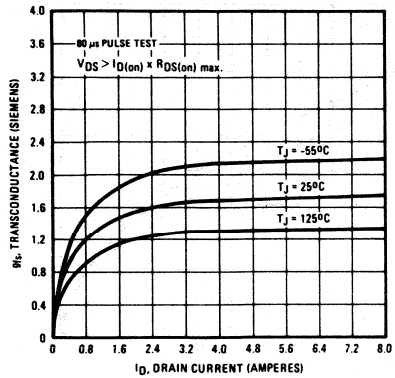


Fig. 6 — Typical Transconductance Vs. Drain Current

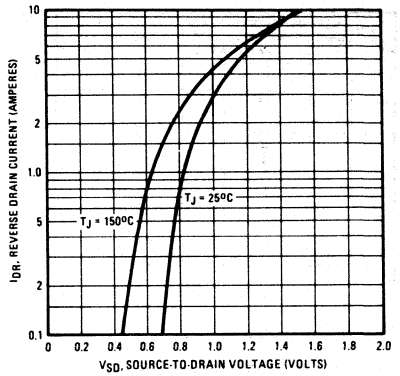


Fig. 7 — Typical Source-Drain Diode Forward Voltage

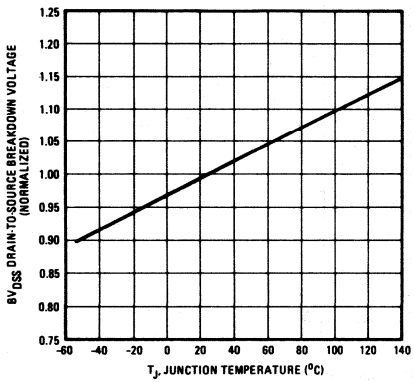


Fig. 8 — Breakdown Voltage Vs. Temperature

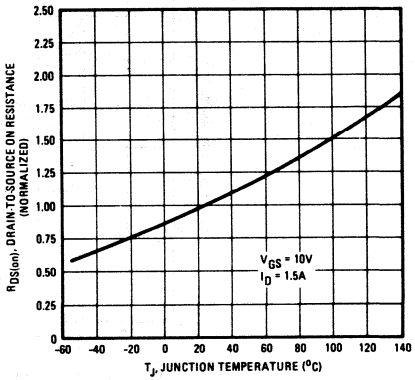


Fig. 9 — Normalized On-Resistance Vs. Temperature

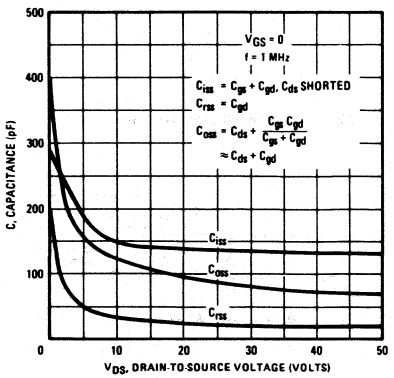


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

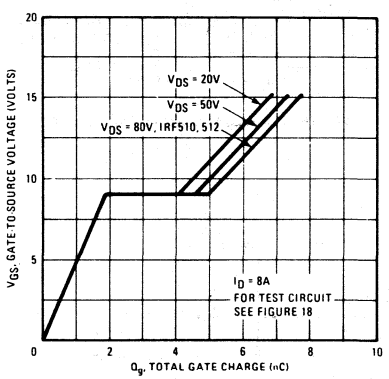


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF510, IRF511, IRF512, IRF513

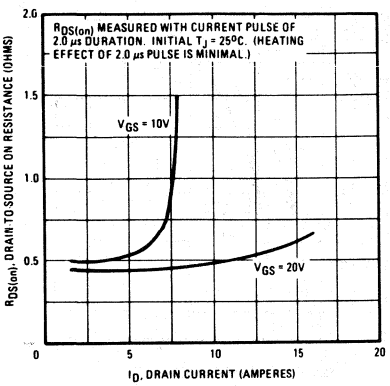


Fig. 12 – Typical On-Resistance Vs. Drain Current

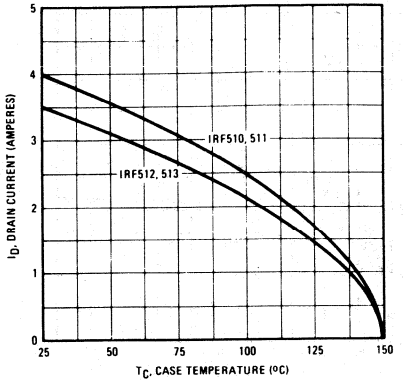


Fig. 13 – Maximum Drain Current Vs. Case Temperature

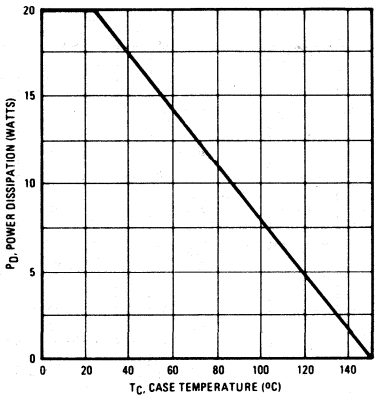


Fig. 14 – Power Vs. Temperature Derating Curve

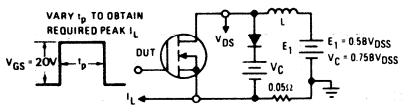


Fig. 15 – Clamped Inductive Test Circuit

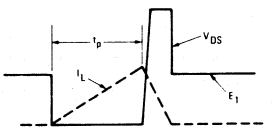


Fig. 16 – Clamped Inductive Waveforms

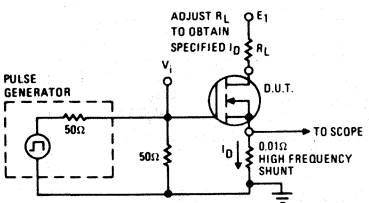


Fig. 17 – Switching Time Test Circuit

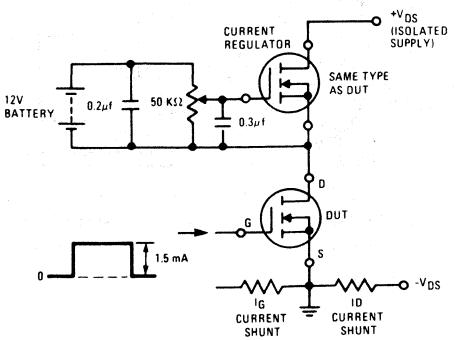


Fig. 18 – Gate Charge Test Circuit

File Number **1574**

IRF520, IRF521, IRF522, IRF523

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

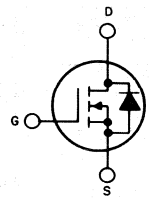
7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



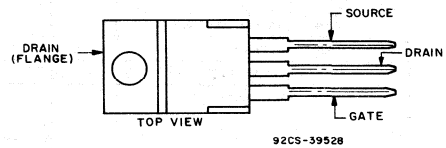
92CS-33741

TERMINAL DIAGRAM

The IRF520, IRF521, IRF522 and IRF523 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

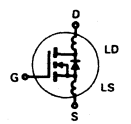
Parameter		IRF520	IRF521	IRF522	IRF523	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF520, IRF521, IRF522, IRF523

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF520 IRF522	100	–	–	V	V_{GS} = 0V
		IRF521 IRF523	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF520 IRF521	8.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF522 IRF523	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF520 IRF521	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF522 IRF523	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 15V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	6.0	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

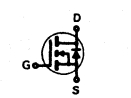


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF520 IRF521	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF522 IRF523	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF520 IRF521	–	–	32	A	
		IRF522 IRF523	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF520 IRF521	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF522 IRF523	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

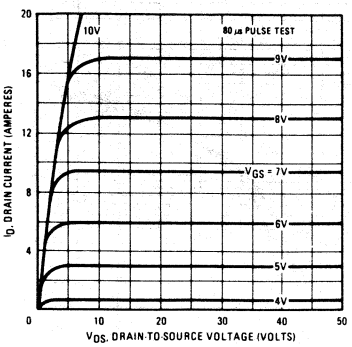


Fig. 1 – Typical Output Characteristics

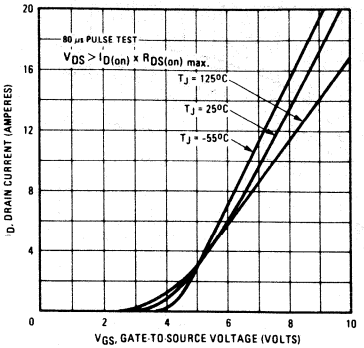


Fig. 2 – Typical Transfer Characteristics

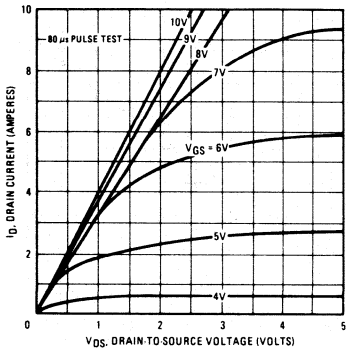


Fig. 3 – Typical Saturation Characteristics

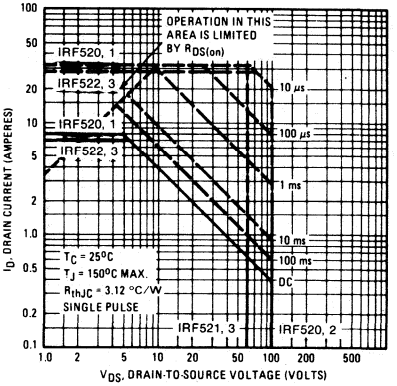


Fig. 4 – Maximum Safe Operating Area

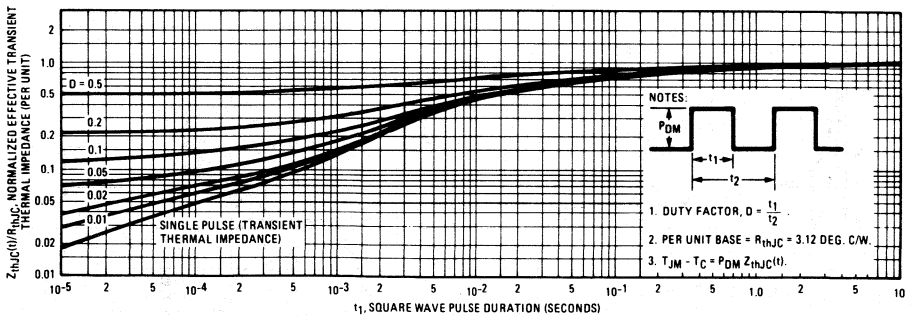


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF520, IRF521, IRF522, IRF523

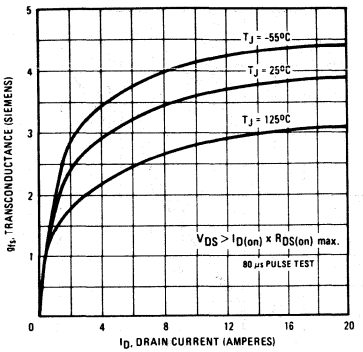


Fig. 6 – Typical Transconductance Vs. Drain Current

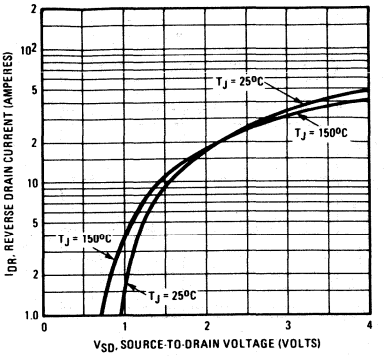


Fig. 7 – Typical Source-Drain Diode Forward Voltage

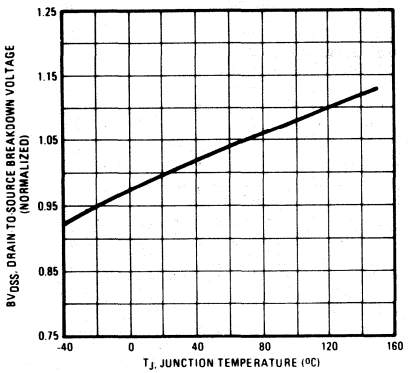


Fig. 8 – Breakdown Voltage Vs. Temperature

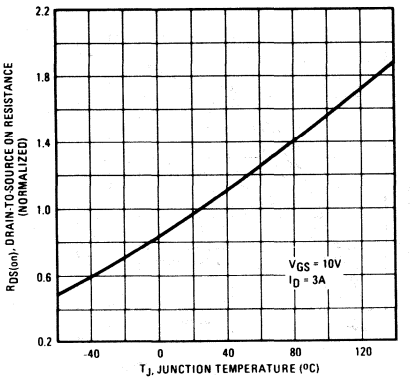


Fig. 9 – Normalized On-Resistance Vs. Temperature

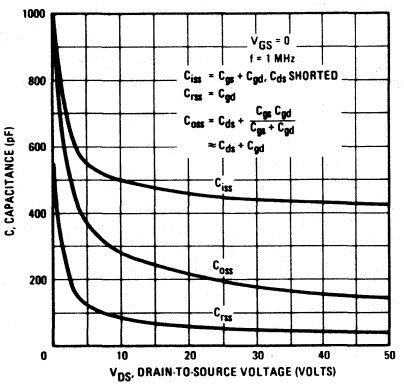


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

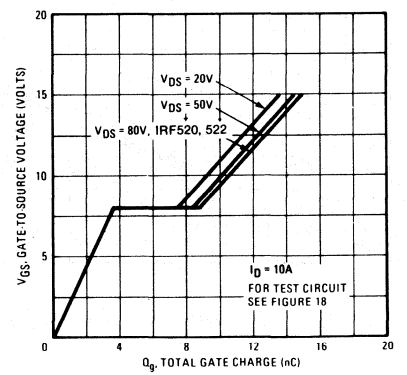


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

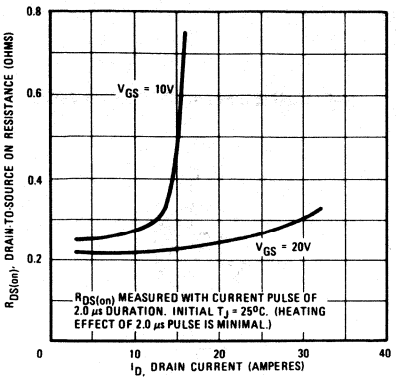


Fig. 12 – Typical On-Resistance Vs. Drain Current

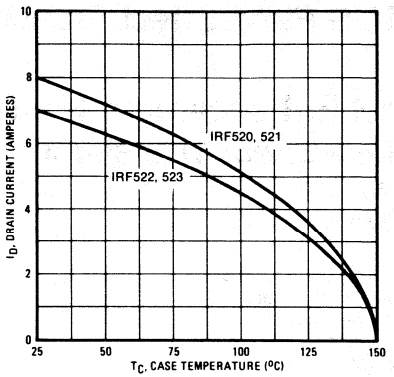


Fig. 13 – Maximum Drain Current Vs. Case Temperature

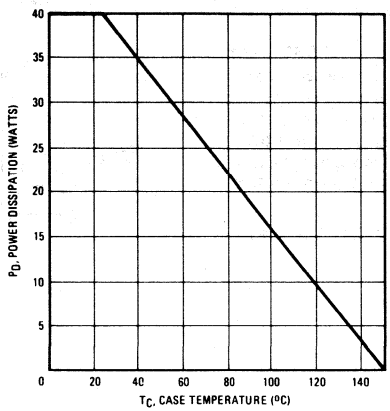


Fig. 14 – Power Vs. Temperature Derating Curve

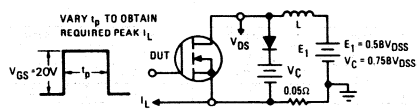


Fig. 15 – Clamped Inductive Test Circuit

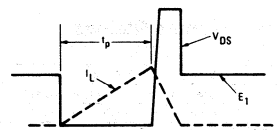


Fig. 16 – Clamped Inductive Waveforms

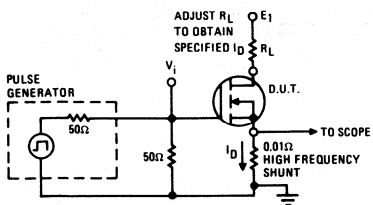


Fig. 17 – Switching Time Test Circuit

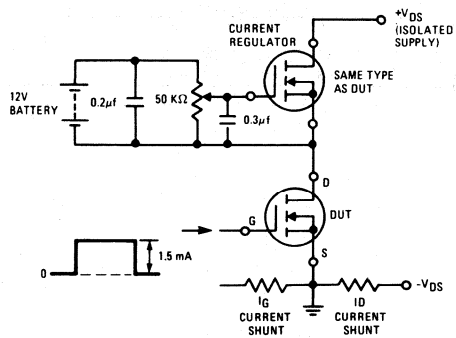


Fig. 18 – Gate Charge Test Circuit

IRF530, IRF531, IRF532, IRF533

File Number **1575**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

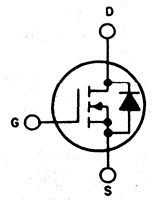
12A and 14A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

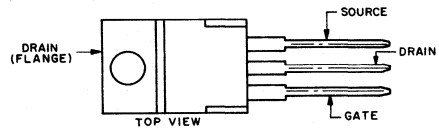
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF530, IRF531, IRF532 and IRF533 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

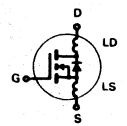
Absolute Maximum Ratings

Parameter		IRF530	IRF531	IRF532	IRF533	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		56	56	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF530 IRF532	100	–	–	V	V_{GS} = 0V
		IRF531 IRF533	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF530 IRF531	14	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF532 IRF533	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF530 IRF531	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF532 IRF533	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40	ns	
t_f	Fall Time	ALL	–	–	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	14	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	14	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF530 IRF531	–	–	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF532 IRF533	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF530 IRF531	–	–	56	A	
		IRF532 IRF533	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF530 IRF531	–	–	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF532 IRF533	–	–	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	360	–	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.1	–	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF530, IRF531, IRF532, IRF533

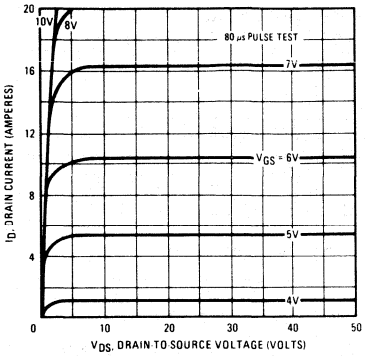


Fig. 1 — Typical Output Characteristics

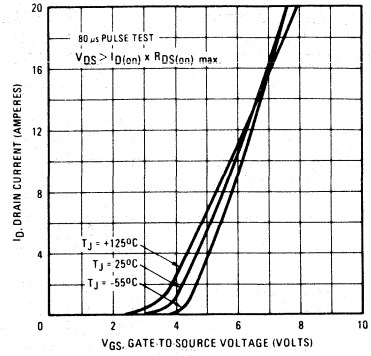


Fig. 2 — Typical Transfer Characteristics

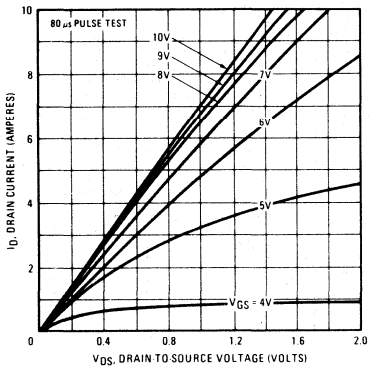


Fig. 3 — Typical Saturation Characteristics

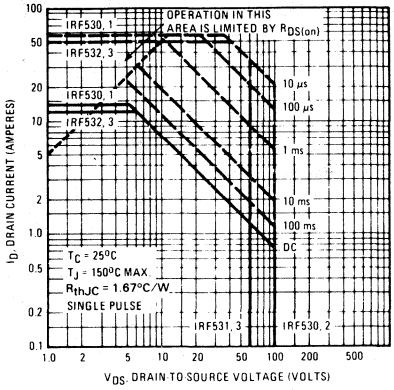


Fig. 4 — Maximum Safe Operating Area

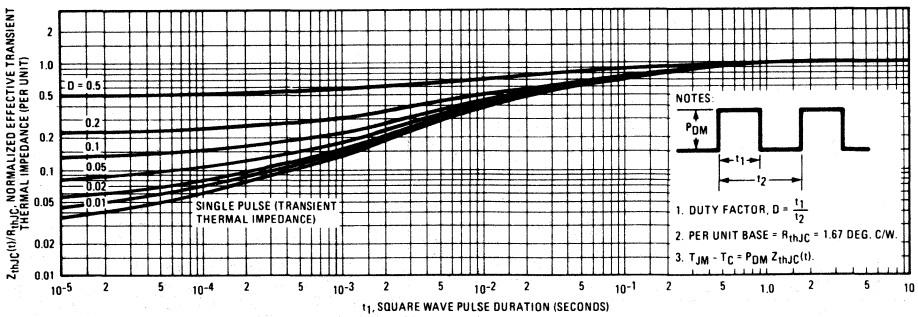


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

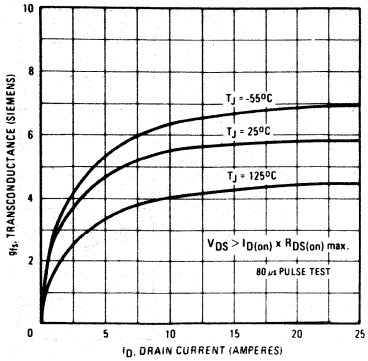


Fig. 6 – Typical Transconductance Vs. Drain Current

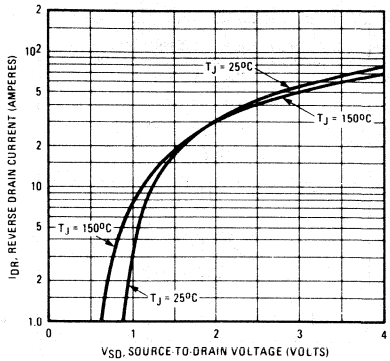


Fig. 7 – Typical Source-Drain Diode Forward Voltage

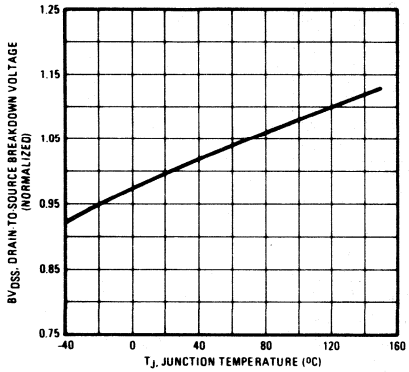


Fig. 8 – Breakdown Voltage Vs. Temperature

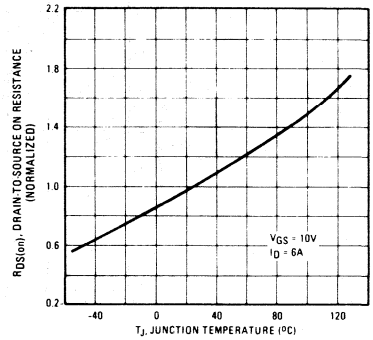


Fig. 9 – Normalized On-Resistance Vs. Temperature

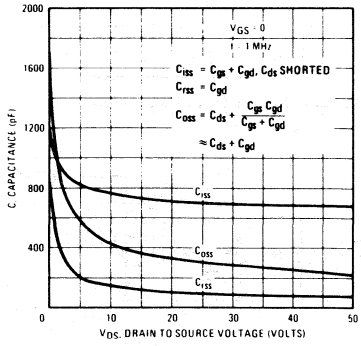


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

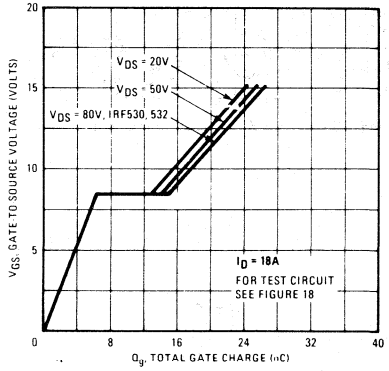


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF530, IRF531, IRF532, IRF533

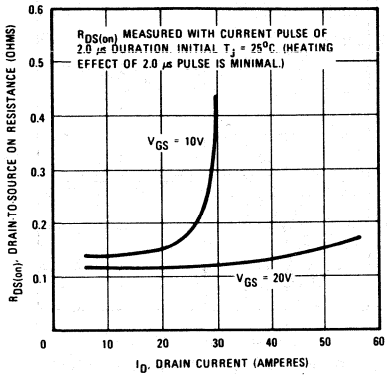


Fig. 12 – Typical On-Resistance Vs. Drain Current

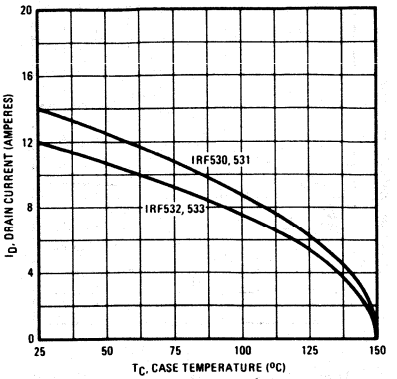


Fig. 13 – Maximum Drain Current Vs. Case Temperature

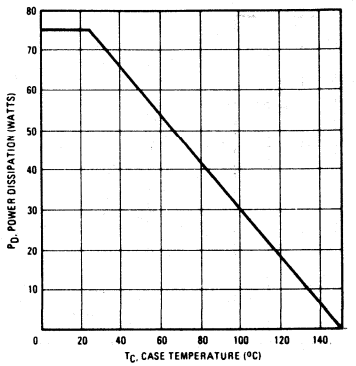


Fig. 14 – Power Vs. Temperature Derating Curve

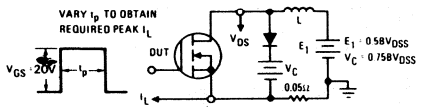


Fig. 15 – Clamped Inductive Test Circuit

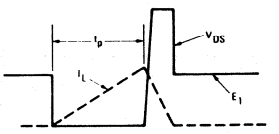


Fig. 16 – Clamped Inductive Waveforms

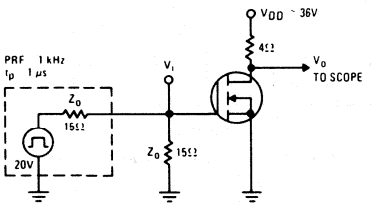


Fig. 17 – Switching Time Test Circuit

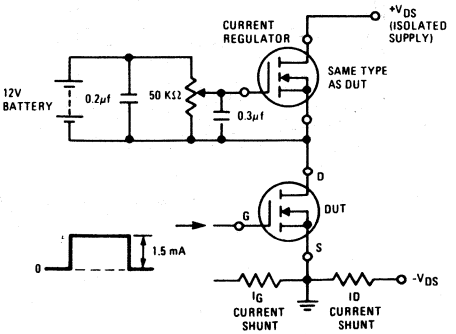


Fig. 18 – Gate Charge Test Circuit

File Number **2309**

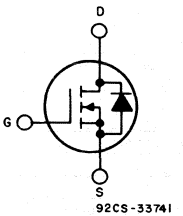
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

24 A and 27 A, 60 V - 100 V
$r_{DS(on)}$ = 0.085 Ω and 0.11 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

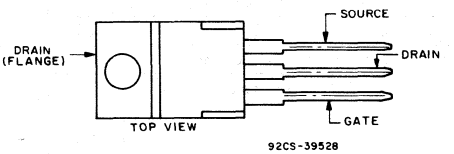


TERMINAL DIAGRAM

The IRF540, IRF541, IRF542, and IRF543 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

Absolute Maximum Ratings

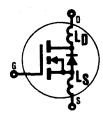
	Parameter	IRF540	IRF541	IRF542	IRF543	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	27	27	24	24	A
I_D @ T_C = 100°C	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		108	108	96	96	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF540, IRF541, IRF542, IRF543

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF540 IRF542	100	–	–	V	V_{GS} = 0V
		IRF541 IRF543	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF540 IRF541	27	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF542 IRF543	24	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF540 IRF541	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		IRF542 IRF543	–	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 15A
C_{iss}	Input Capacitance	ALL	–	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	550	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≈ 30V, I_D = 15A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	38	80	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	17	26	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	21	32	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF540 IRF541	–	–	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF542 IRF543	–	–	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF540 IRF541	–	–	108	A	
		IRF542 IRF543	–	–	96	A	
V_{SD}	Diode Forward Voltage ②	IRF540 IRF541	–	–	2.5	V	T_C = 25°C, I_S = 27A, V_{GS} = 0V
		IRF542 IRF543	–	–	2.3	V	T_C = 25°C, I_S = 24A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.9	–	μC	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

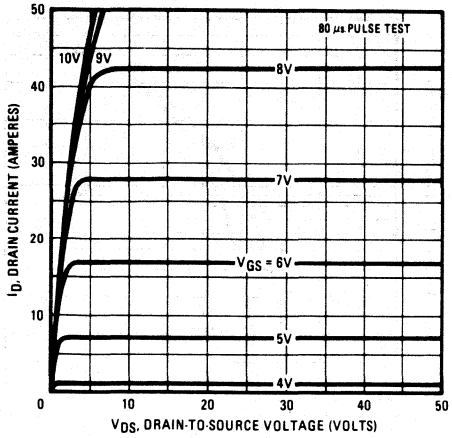


Fig. 1 – Typical Output Characteristics

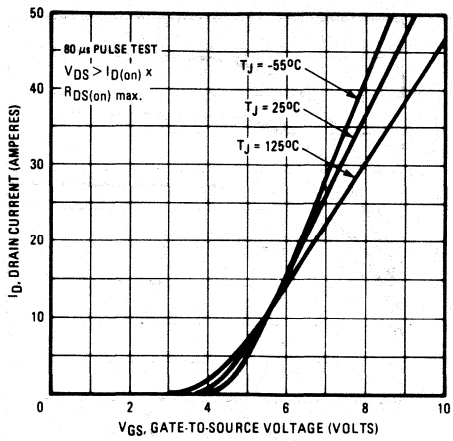


Fig. 2 – Typical Transfer Characteristics

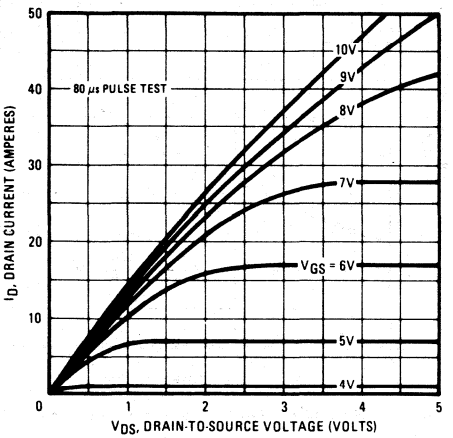


Fig. 3 – Typical Saturation Characteristics

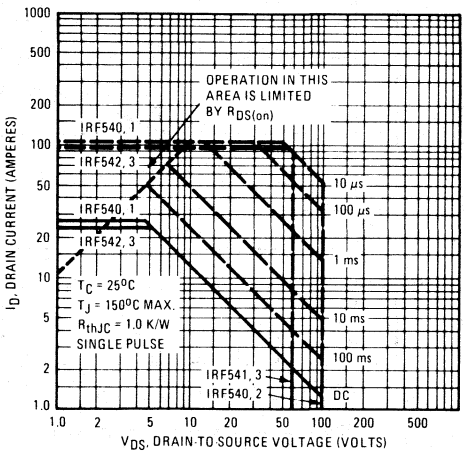


Fig. 4 – Maximum Safe Operating Area

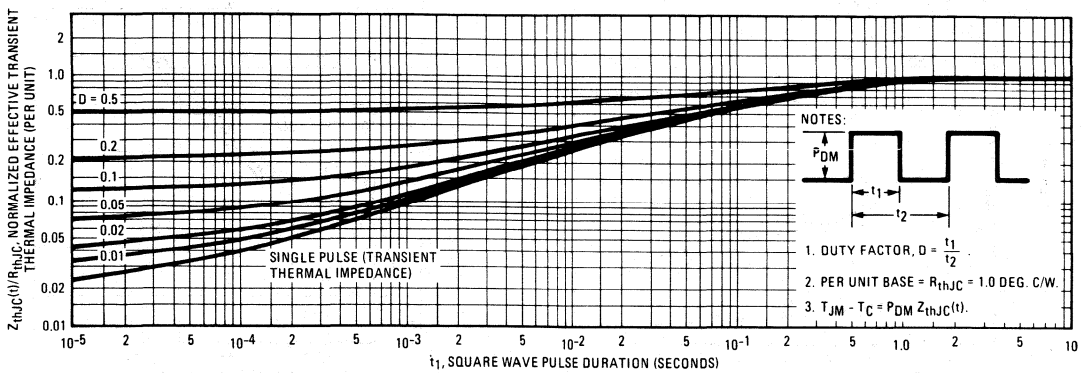


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF540, IRF541, IRF542, IRF543

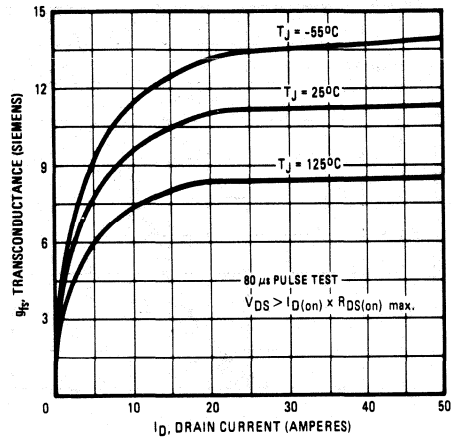


Fig. 6 — Typical Transconductance Vs. Drain Current

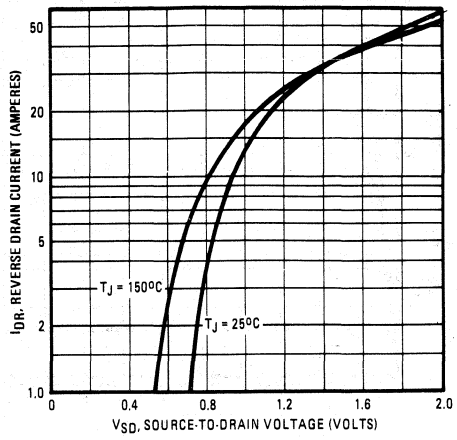


Fig. 7 — Typical Source-Drain Diode Forward Voltage

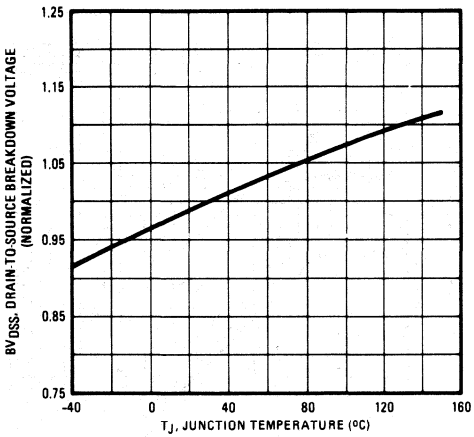


Fig. 8 — Breakdown Voltage Vs. Temperature

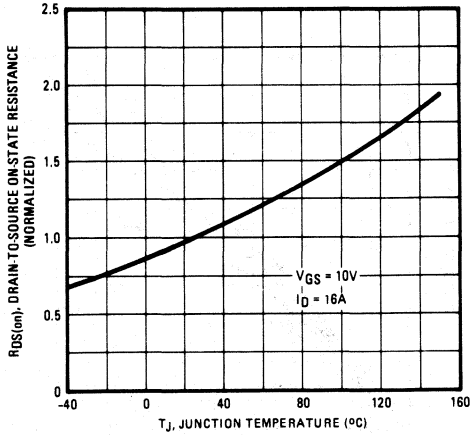


Fig. 9 — Normalized On-Resistance Vs. Temperature

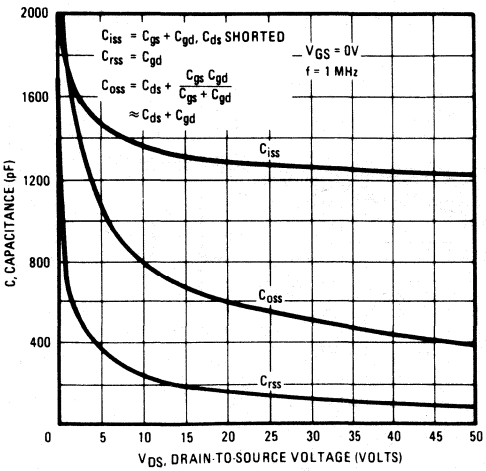


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

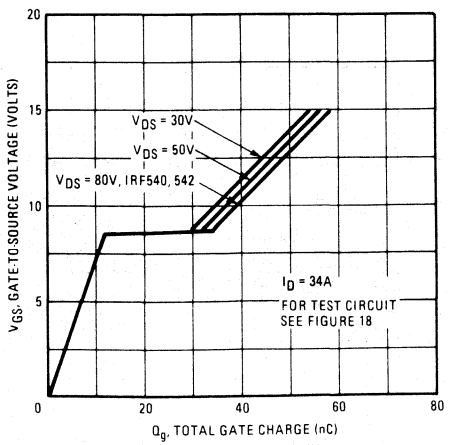


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

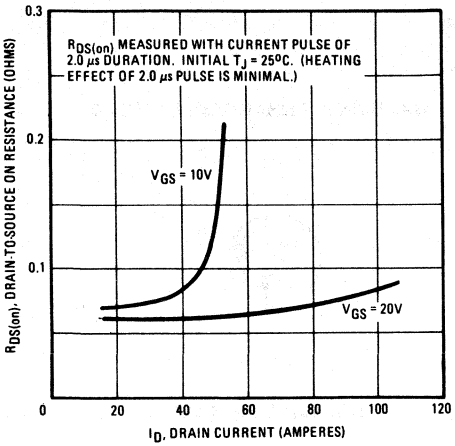


Fig. 12 – Typical On-Resistance Vs. Drain Current

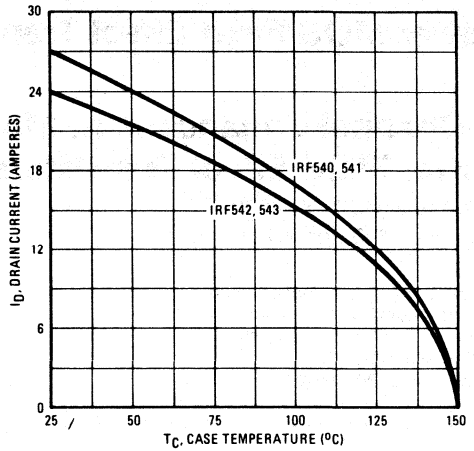


Fig. 13 – Maximum Drain Current Vs. Case Temperature

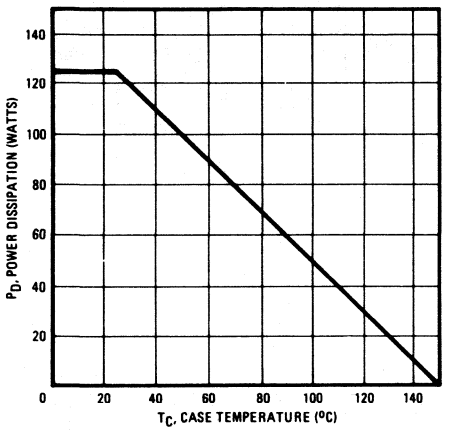


Fig. 14 – Power Vs. Temperature Derating Curve

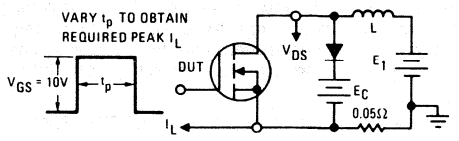


Fig. 15 – Clamped Inductive Test Circuit

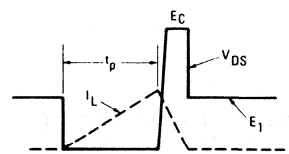


Fig. 16 – Clamped Inductive Waveforms

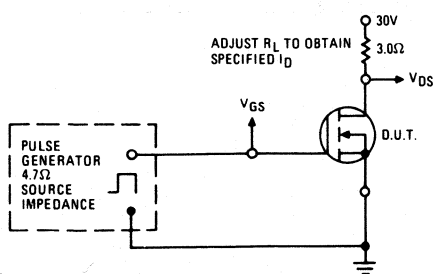


Fig. 17 – Switching Time Test Circuit

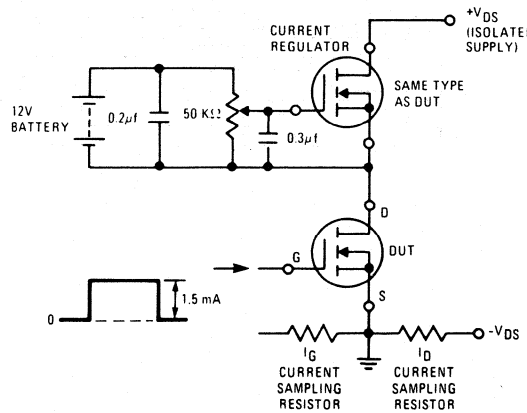


Fig. 18 – Gate Charge Test Circuit

IRF610, IRF611, IRF612, IRF613

File Number **1576**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

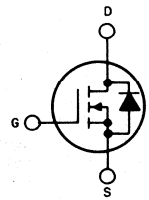
2.0A and 2.5A, 150V-200V

$r_{DS}(on)$ = 1.5 Ω and 2.4 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

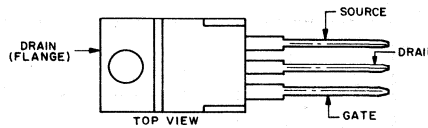
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF610, IRF611, IRF612 and IRF613 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

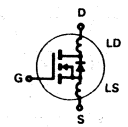
Absolute Maximum Ratings

Parameter		IRF610	IRF611	IRF612	IRF613	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C 100°C	Continuous Drain Current	1.5	1.5	1.25	1.25	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF610 IRF612	200	–	–	V	V_{GS} = 0V
		IRF611 IRF613	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF610 IRF611	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF612 IRF613	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF610 IRF611	–	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		IRF612 IRF613		1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3		S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	–	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	60	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	16	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	8.0	15	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	10	15	ns	
t_f	Fall Time	ALL		8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL		5.0	7.5	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL		2.0	3.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL		3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL		3.5		nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF610 IRF611			2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF612 IRF613			2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF610 IRF611			10	A	
		IRF612 IRF613			8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF610 IRF611			2.0	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF612 IRF613			1.8	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL		290		ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.0	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF610, IRF611, IRF612, IRF613

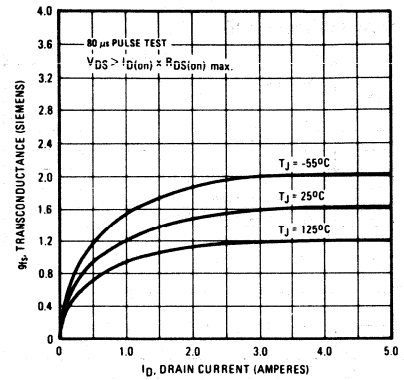


Fig. 6 – Typical Transconductance Vs. Drain Current

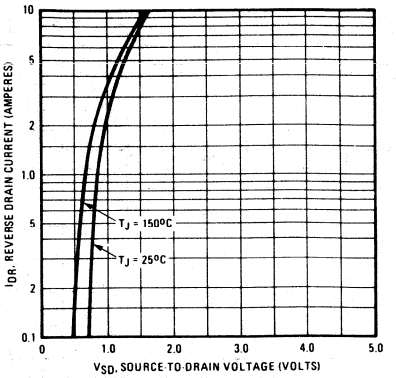


Fig. 7 – Typical Source-Drain Diode Forward Voltage

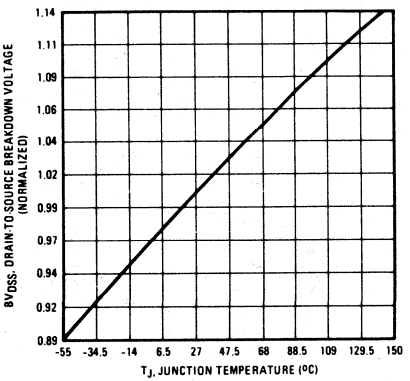


Fig. 8 – Breakdown Voltage Vs. Temperature

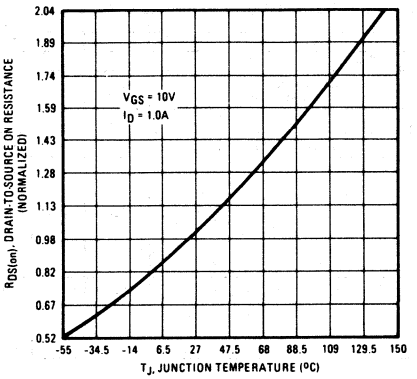


Fig. 9 – Normalized On-Resistance Vs. Temperature

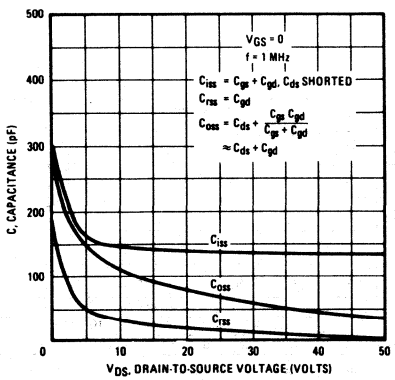


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

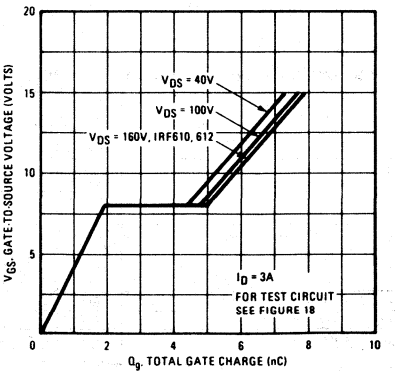


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

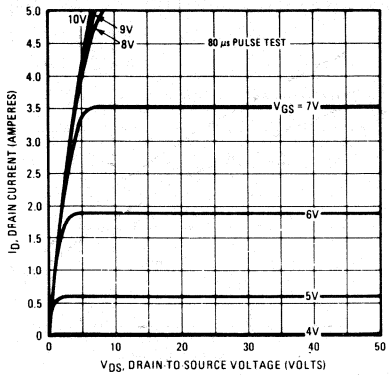


Fig. 1 – Typical Output Characteristics

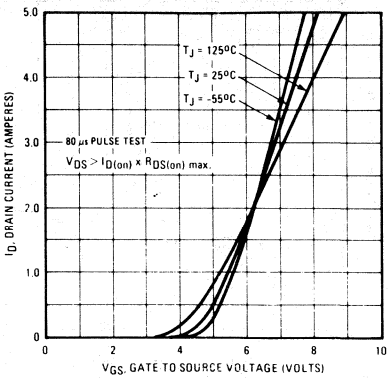


Fig. 2 – Typical Transfer Characteristics

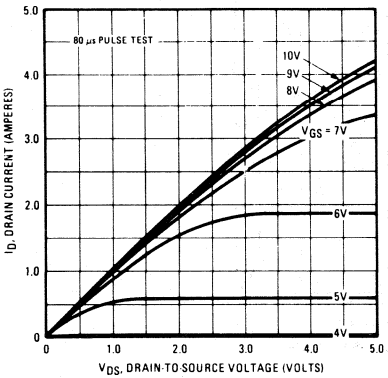


Fig. 3 – Typical Saturation Characteristics

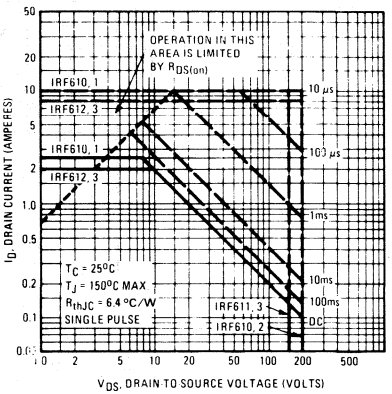


Fig. 4 – Maximum Safe Operating Area

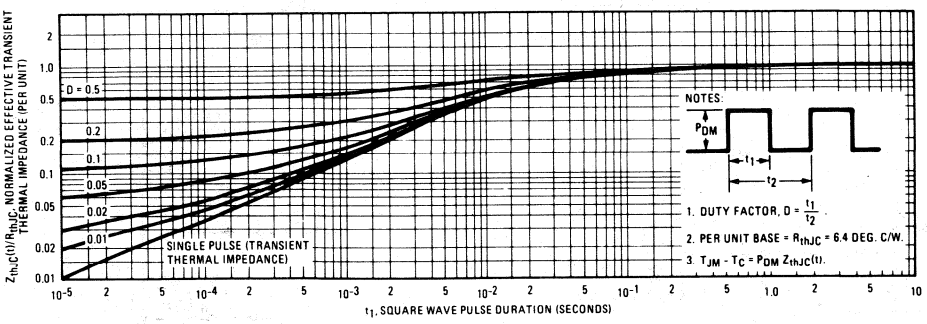


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF610, IRF611, IRF612, IRF613

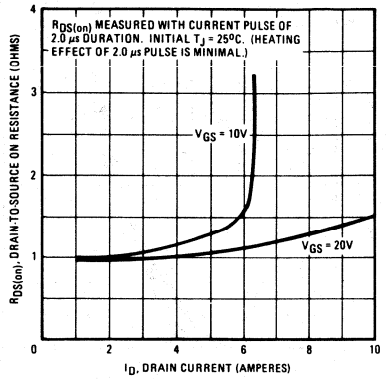


Fig. 12 – Typical On-Resistance Vs. Drain Current

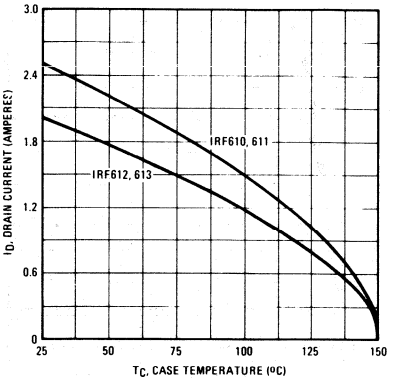


Fig. 13 – Maximum Drain Current Vs. Case Temperature

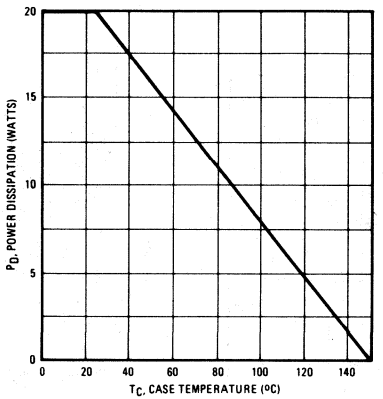


Fig. 14 – Power Vs. Temperature Derating Curve

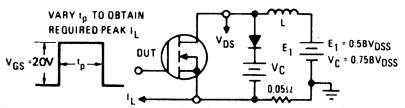


Fig. 15 – Clamped Inductive Test Circuit

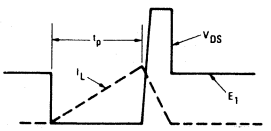


Fig. 16 – Clamped Inductive Waveforms

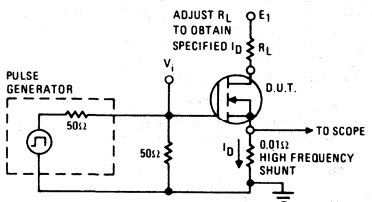


Fig. 17 – Switching Time Test Circuit

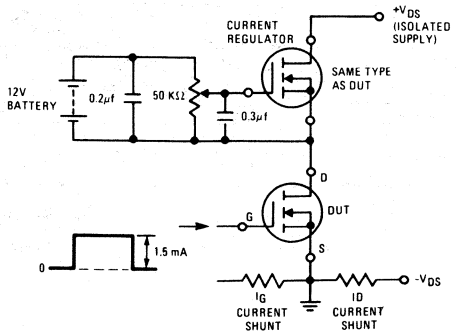


Fig. 18 – Gate Charge Test Circuit

File Number **1577**

IRF620, IRF621, IRF622, IRF623

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 5.0A, 150V-200V

$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

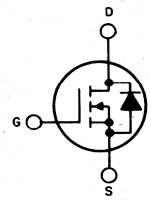
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF620, IRF621, IRF622 and IRF623 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

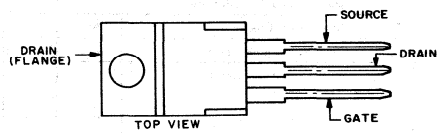
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

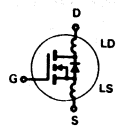
Parameter		IRF620	IRF621	IRF622	IRF623	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		20	20	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF620, IRF621, IRF622, IRF623

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF620 IRF622	200	–	–	V	V_{GS} = 0V
		IRF621 IRF623	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF620 IRF621	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF622 IRF623	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF620 IRF621	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF622 IRF623	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 2.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 50V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	7.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF620 IRF621	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF622 IRF623	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF620 IRF621	–	–	20	A	
		IRF622 IRF623	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF620 IRF621	–	–	1.8	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF622 IRF623	–	–	1.4	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

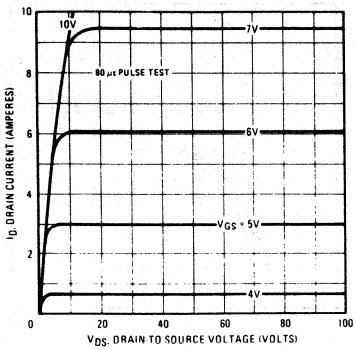


Fig. 1 – Typical Output Characteristics

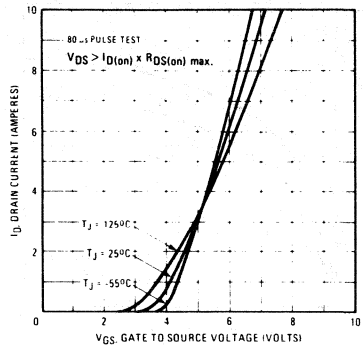


Fig. 2 – Typical Transfer Characteristics

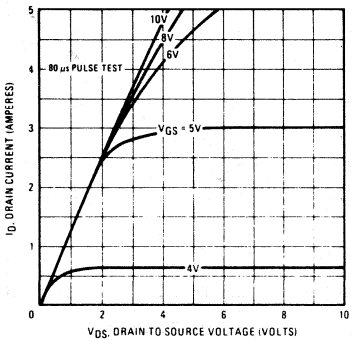


Fig. 3 – Typical Saturation Characteristics

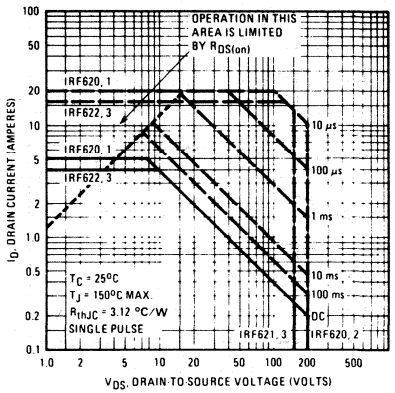


Fig. 4 – Maximum Safe Operating Area

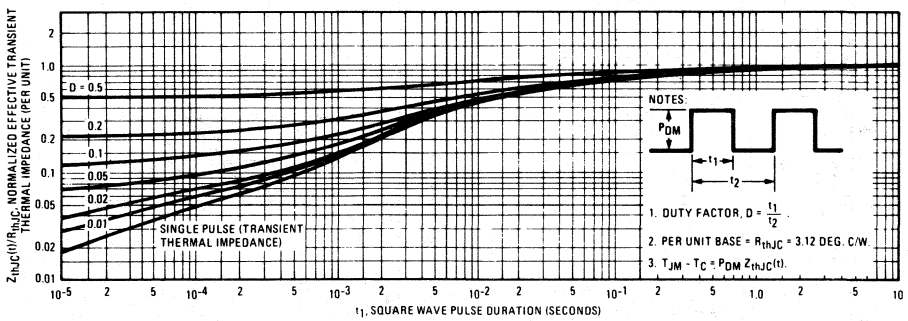


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF620, IRF621, IRF622, IRF623

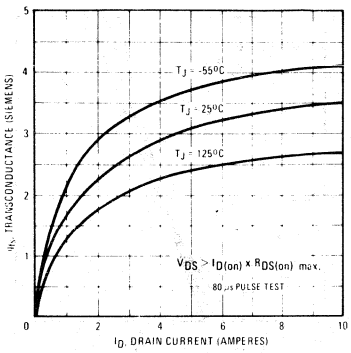


Fig. 6 — Typical Transconductance Vs. Drain Current

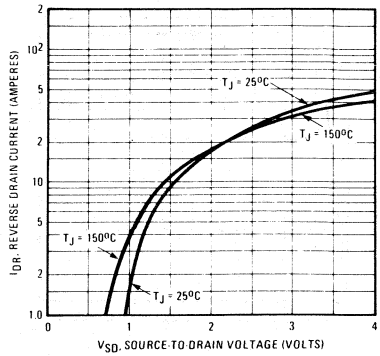


Fig. 7 — Typical Source-Drain Diode Forward Voltage

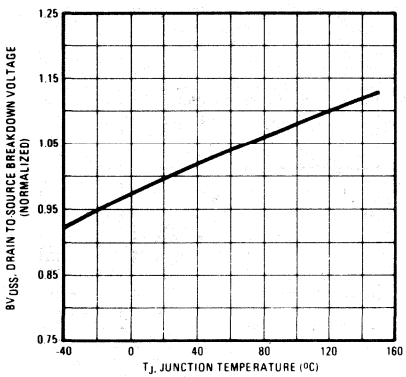


Fig. 8 — Breakdown Voltage Vs. Temperature

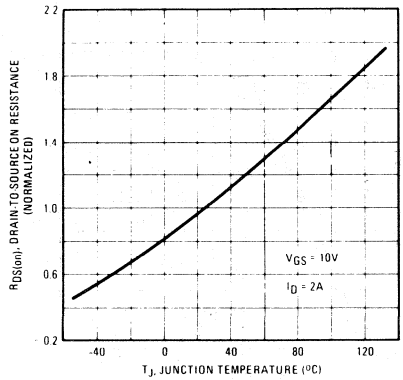


Fig. 9 — Normalized On-Resistance Vs. Temperature

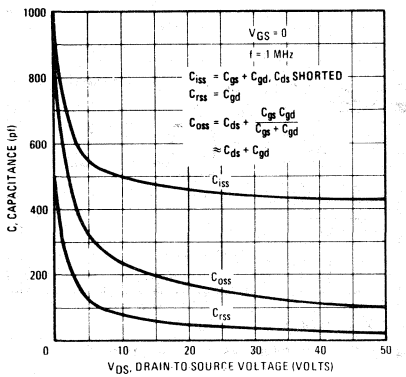


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

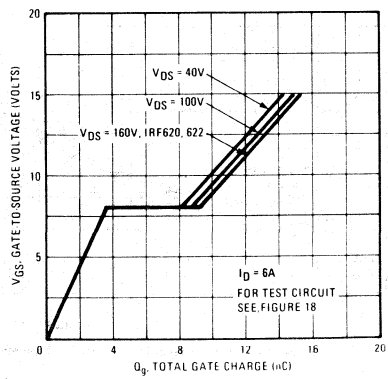


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

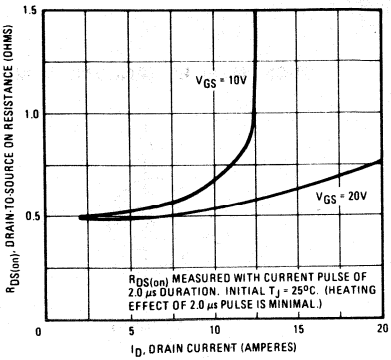


Fig. 12 – Typical On-Resistance Vs. Drain Current

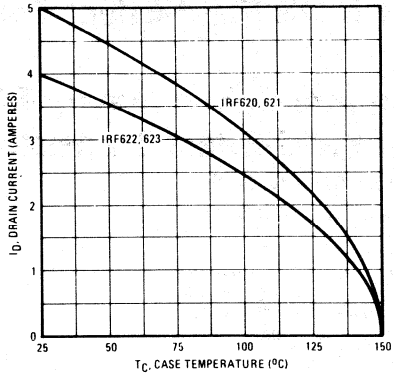


Fig. 13 – Maximum Drain Current Vs. Case Temperature

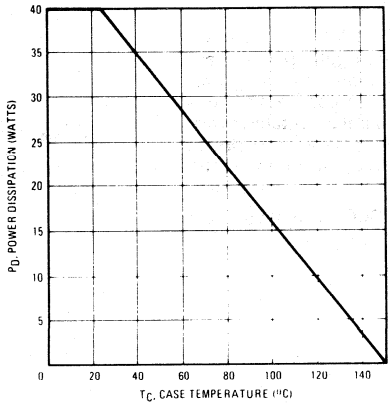


Fig. 14 – Power Vs. Temperature Derating Curve

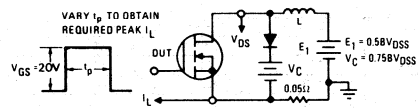


Fig. 15 – Clamped Inductive Test Circuit

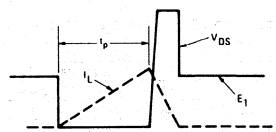


Fig. 16 – Clamped Inductive Waveforms

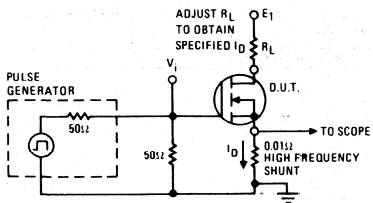


Fig. 17 – Switching Time Test Circuit

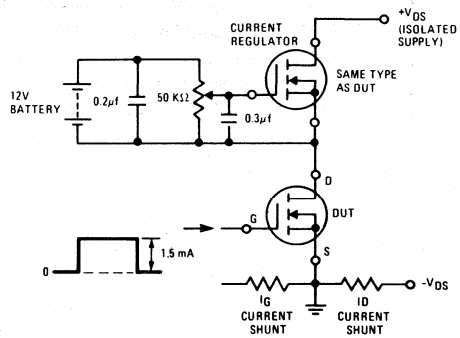


Fig. 18 – Gate Charge Test Circuit

IRF630, IRF631, IRF632, IRF633

File Number **1578**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8.0A and 9.0A, 150V-200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

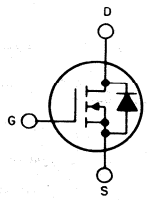
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF630, IRF631, IRF632 and IRF633 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

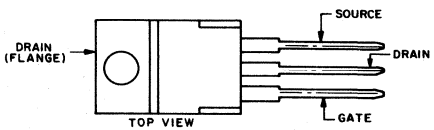
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

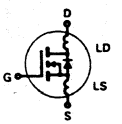
Absolute Maximum Ratings

Parameter		IRF630	IRF631	IRF632	IRF633	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		36	36	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF630 IRF632	200	–	–	V	V_{GS} = 0V
		IRF631 IRF633	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF630 IRF631	9.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF632 IRF633	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF630 IRF631	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF632 IRF633	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8		S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	15	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	14	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF630 IRF631	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF632 IRF633	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF630 IRF631	–	–	36	A	
		IRF632 IRF633	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF630 IRF631	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF632 IRF633	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F ≈ 9.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F ≈ 9.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF630, IRF631, IRF632, IRF633

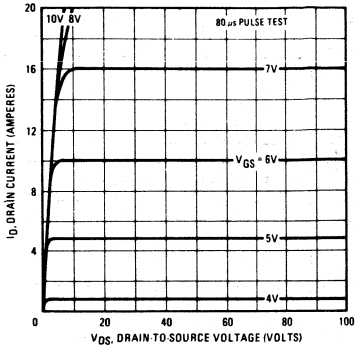


Fig. 1 – Typical Output Characteristics

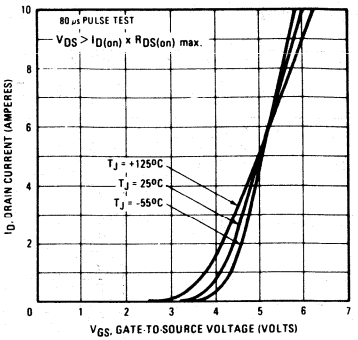


Fig. 2 – Typical Transfer Characteristics

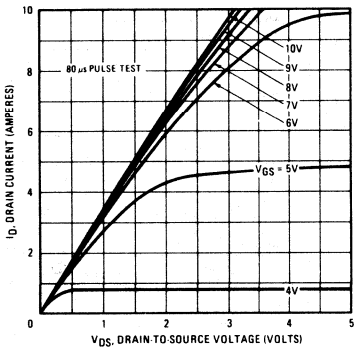


Fig. 3 – Typical Saturation Characteristics

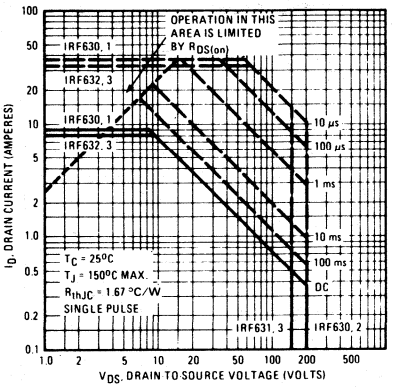


Fig. 4 – Maximum Safe Operating Area

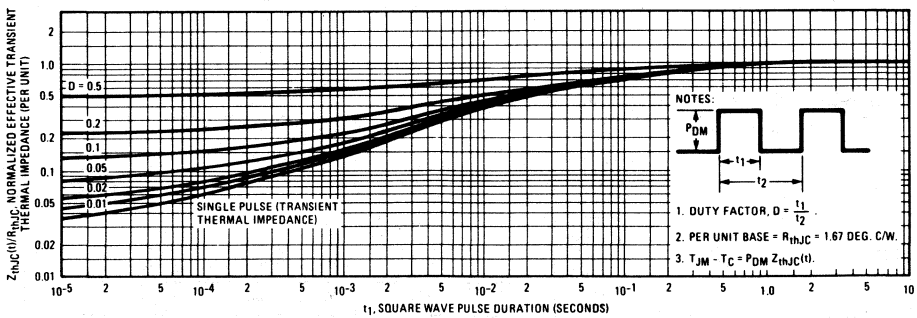


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

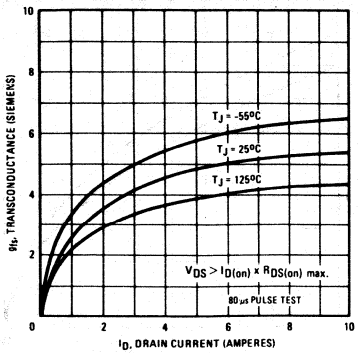


Fig. 6 – Typical Transconductance Vs. Drain Current

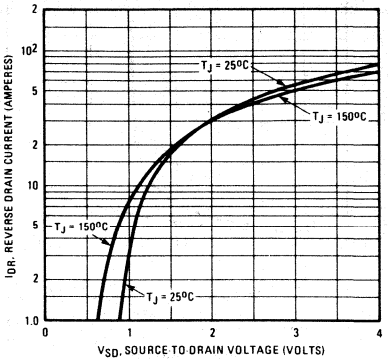


Fig. 7 – Typical Source-Drain Diode Forward Voltage

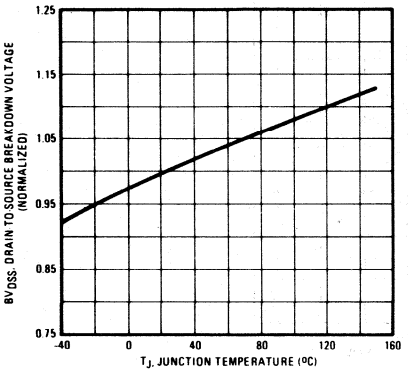


Fig. 8 – Breakdown Voltage Vs. Temperature

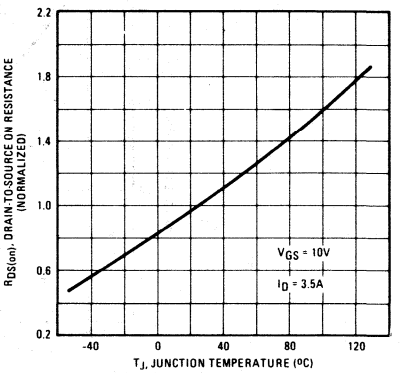


Fig. 9 – Normalized On-Resistance Vs. Temperature

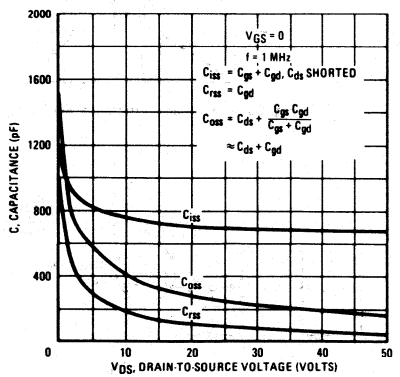


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

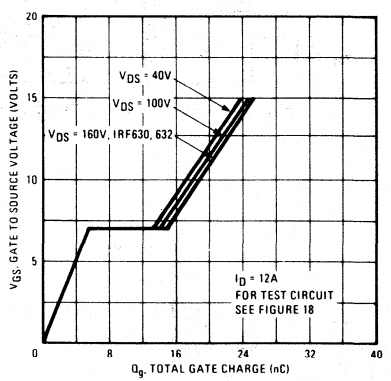


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

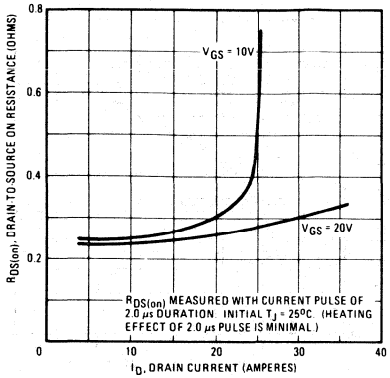


Fig. 12 – Typical On-Resistance Vs. Drain Current

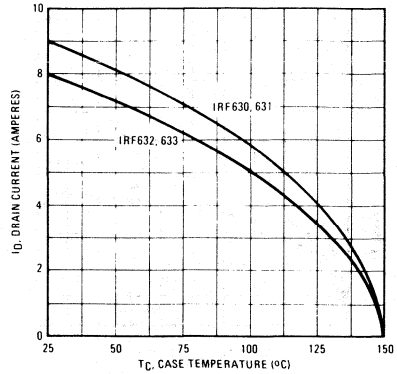


Fig. 13 – Maximum Drain Current Vs. Case Temperature

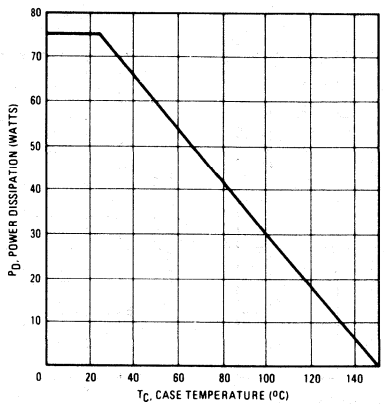


Fig. 14 – Power Vs. Temperature Derating Curve

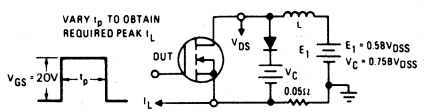


Fig. 15 – Clamped Inductive Test Circuit

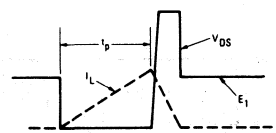


Fig. 16 – Clamped Inductive Waveforms

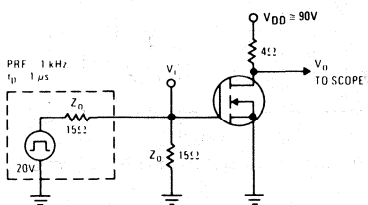


Fig. 17 – Switching Time Test Circuit

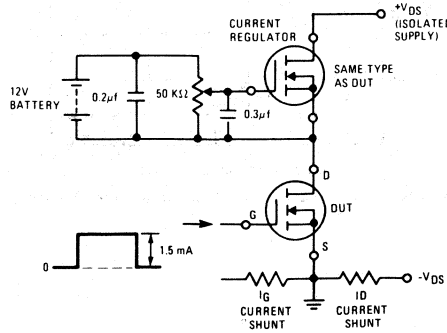


Fig. 18 – Gate Charge Test Circuit

File Number **1585**

IRF640, IRF641, IRF642, IRF643

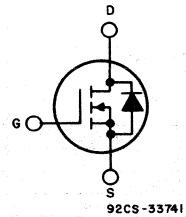
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

16 A and 18 A, 150 V - 200 V
$r_{DS(on)}$ = 0.18 Ω and 0.22 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

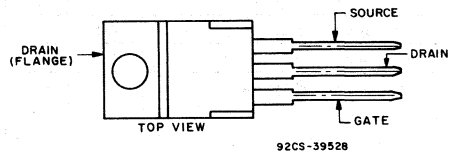


TERMINAL DIAGRAM

The IRF640, IRF641, IRF642, and IRF643 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

Absolute Maximum Ratings

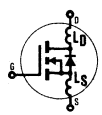
Parameter		IRF640	IRF641	IRF642	IRF643	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		72	72	64	64	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.064 in. (1.6mm) from case for 10s)				°C

IRF640, IRF641, IRF642, IRF643

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF640 IRF642	200	–	–	V	V_{GS} = 0V
		IRF641 IRF643	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF640 IRF641	18	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF642 IRF643	16	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF640 IRF641	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRF642 IRF643	–	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	–	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	500	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≈ 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	40	80	ns	
t_f	Fall Time	ALL	–	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	16	24	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	41	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF640 IRF641	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF642 IRF643	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF640 IRF641	–	–	72	A	
		IRF642 IRF643	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	IRF640 IRF641	–	–	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRF642 IRF643	–	–	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

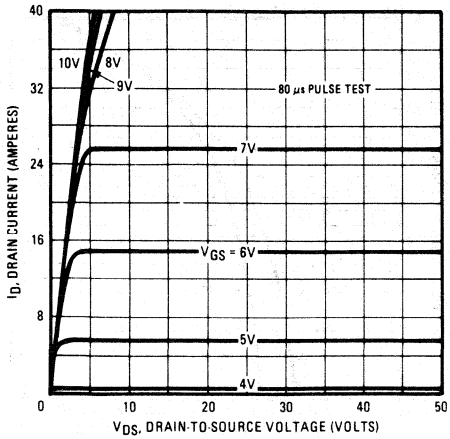


Fig. 1 — Typical Output Characteristics

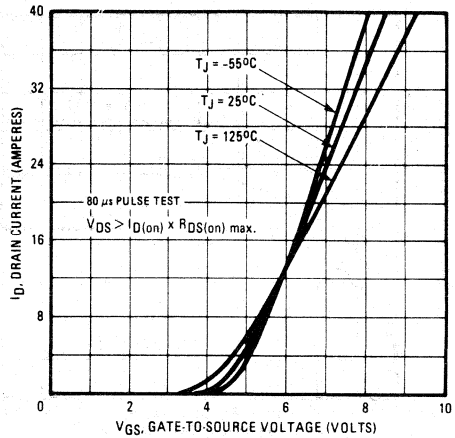


Fig. 2 — Typical Transfer Characteristics

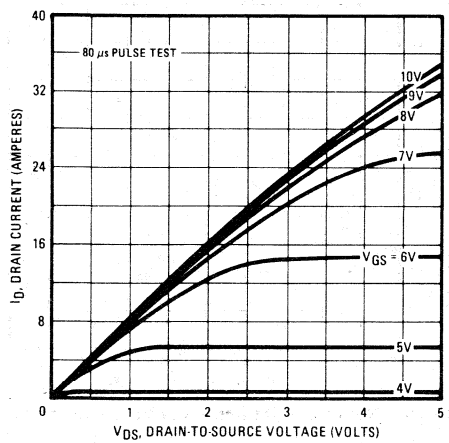


Fig. 3 — Typical Saturation Characteristics

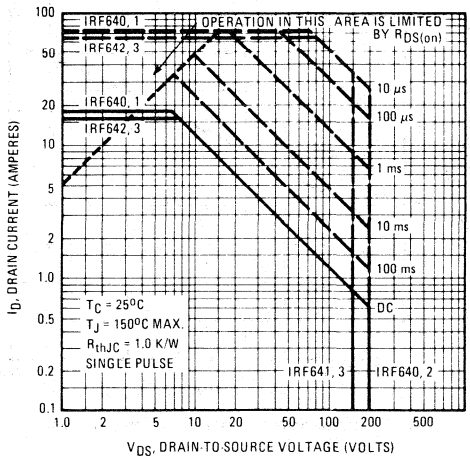


Fig. 4 — Maximum Safe Operating Area

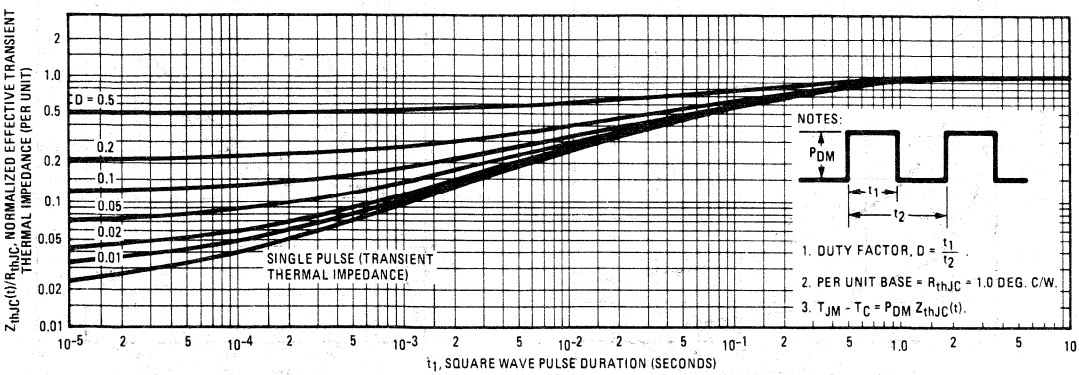


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF640, IRF641, IRF642, IRF643

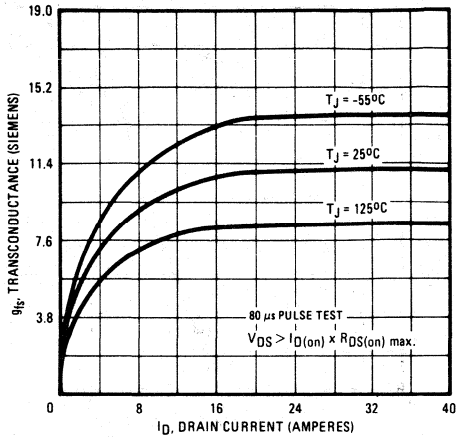


Fig. 6 — Typical Transconductance Vs. Drain Current

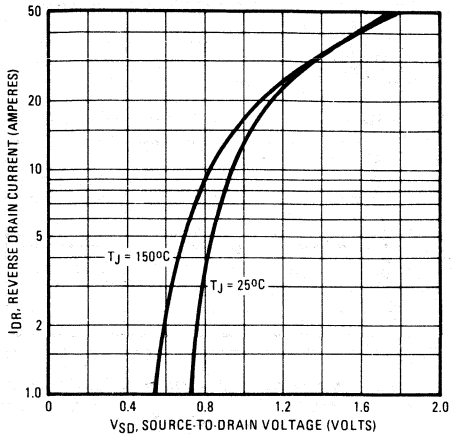


Fig. 7 — Typical Source-Drain Diode Forward Voltage

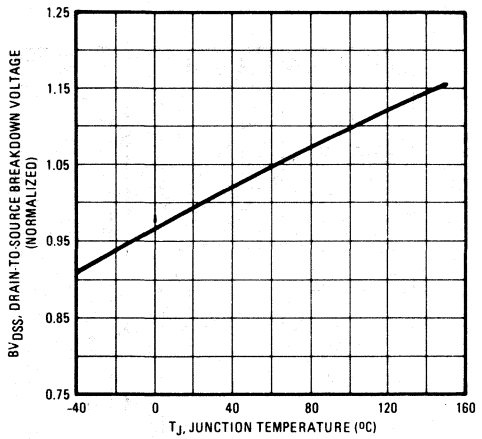


Fig. 8 — Breakdown Voltage Vs. Temperature

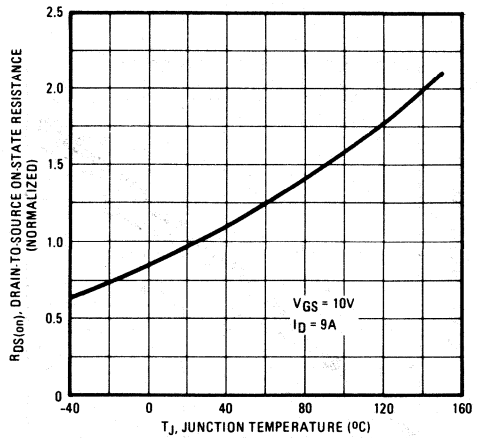


Fig. 9 — Normalized On-Resistance Vs. Temperature

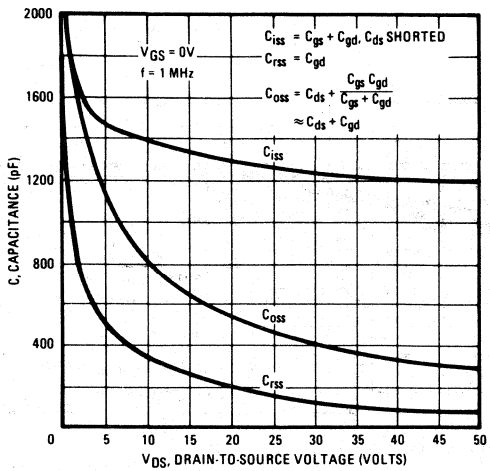


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

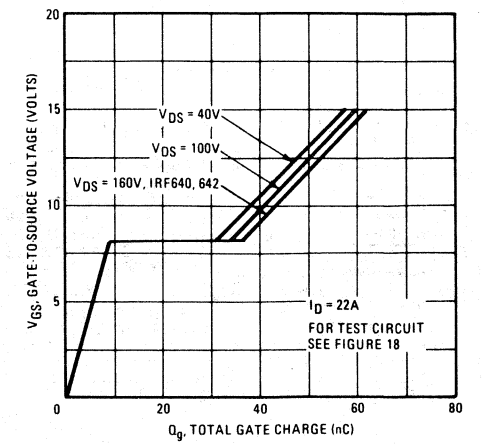


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

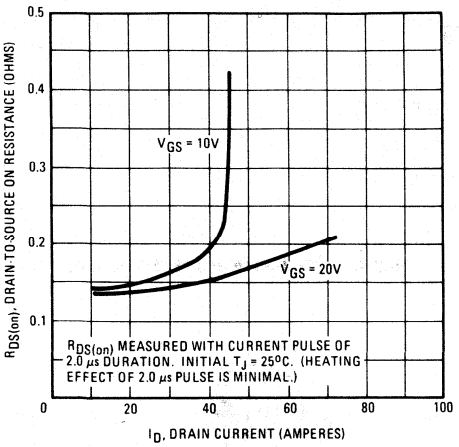


Fig. 12 – Typical On-Resistance Vs. Drain Current

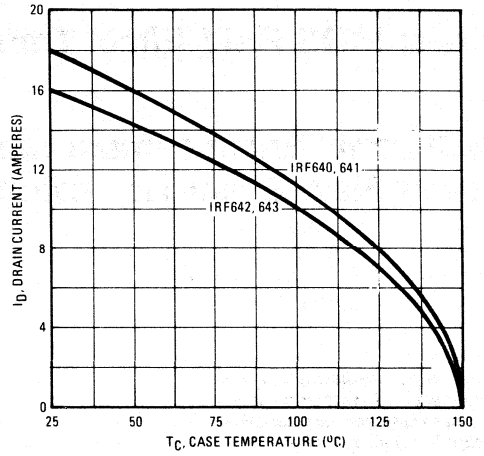


Fig. 13 – Maximum Drain Current Vs. Case Temperature

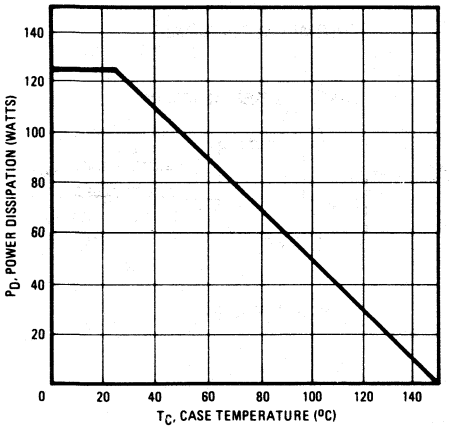


Fig. 14 – Power Vs. Temperature Derating Curve

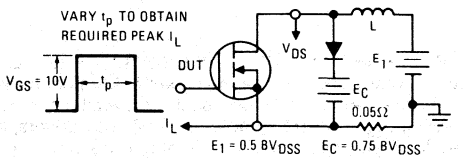


Fig. 15 – Clamped Inductive Test Circuit

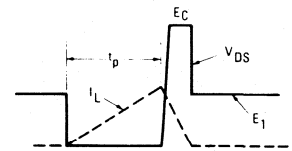


Fig. 16 – Clamped Inductive Waveforms

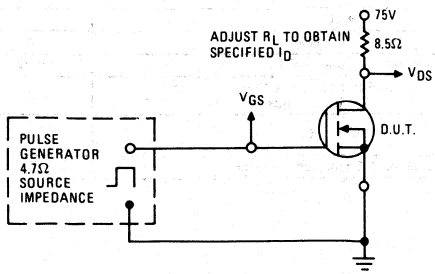


Fig. 17 – Switching Time Test Circuit

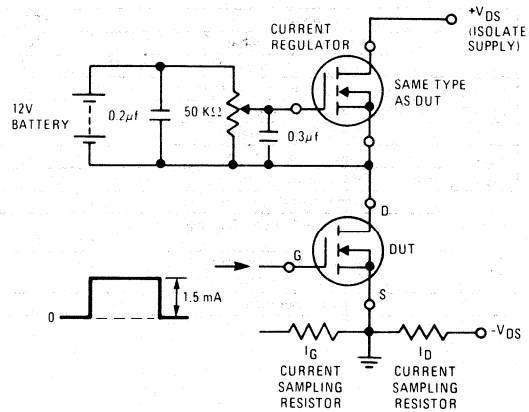


Fig. 18 – Gate Charge Test Circuit

IRF710, IRF711, IRF712, IRF713

File Number **2310**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

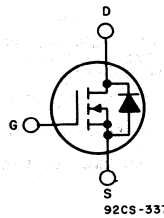
1.3 A and 1.5 A, 350 V - 400 V

$r_{DS(on)}$ = 3.6 Ω and 5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

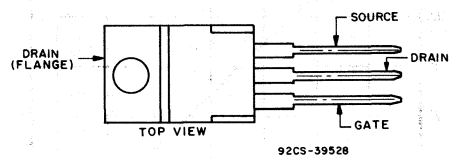


TERMINAL DIAGRAM

The IRF710, IRF711, IRF712, and IRF713 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

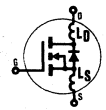
Absolute Maximum Ratings

Parameter		IRF710	IRF711	IRF712	IRF713	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	1.5	1.5	1.3	1.3	A
I_D @ T_C = 100°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current ③	6.0	6.0	5.0	5.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		6.0	6.0	5.0	5.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF710, IRF712	400	–	–	V	V_{GS} = 0V
		IRF711, IRF713	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF710, IRF711	1.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRF712, IRF713	1.3	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF710, IRF711	–	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRF712, IRF713	–	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 0.8A
C_{iss}	Input Capacitance	ALL	–	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	35	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	8.0	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	3.0	10	ns	$V_{DD} \approx 0.5\,BV_{DSS}$, I_D = 0.8A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	5.0	10	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	6.0	7.5	nC	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	3.0	4.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF710, IRF711	–	–	1.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF712, IRF713	–	–	1.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF710, IRF711	–	–	6.0	A	
		IRF712, IRF713	–	–	5.0	A	
V_{SD}	Diode Forward Voltage ②	IRF710, IRF711	–	–	1.6	V	T_C = 25°C, I_S = 1.5A, V_{GS} = 0V
		IRF712, IRF713	–	–	1.5	V	T_C = 25°C, I_S = 1.3A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	380	–	ns	T_J = 150°C, I_F = 1.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.7	–	μC	T_J = 150°C, I_F = 1.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF710, IRF711, IRF712, IRF713

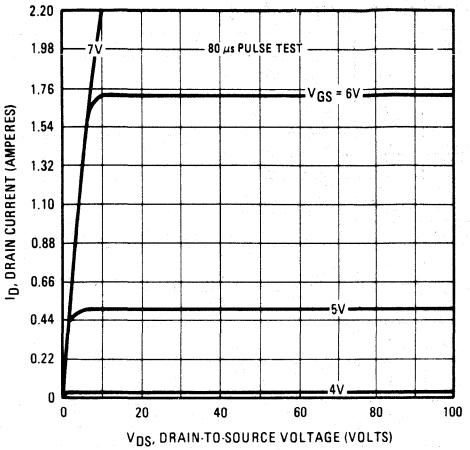


Fig. 1 — Typical Output Characteristics

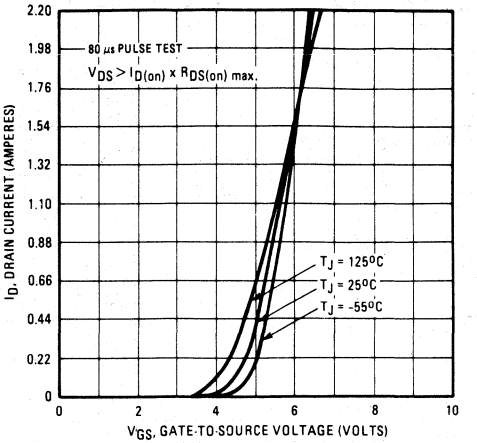


Fig. 2 — Typical Transfer Characteristics

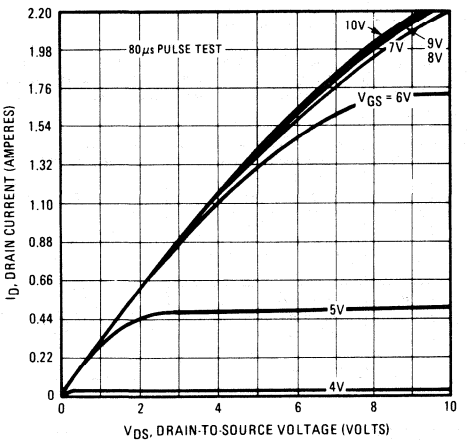


Fig. 3 — Typical Saturation Characteristics

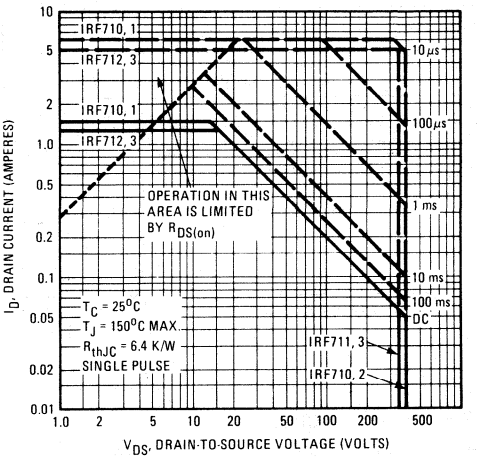


Fig. 4 — Maximum Safe Operating Area

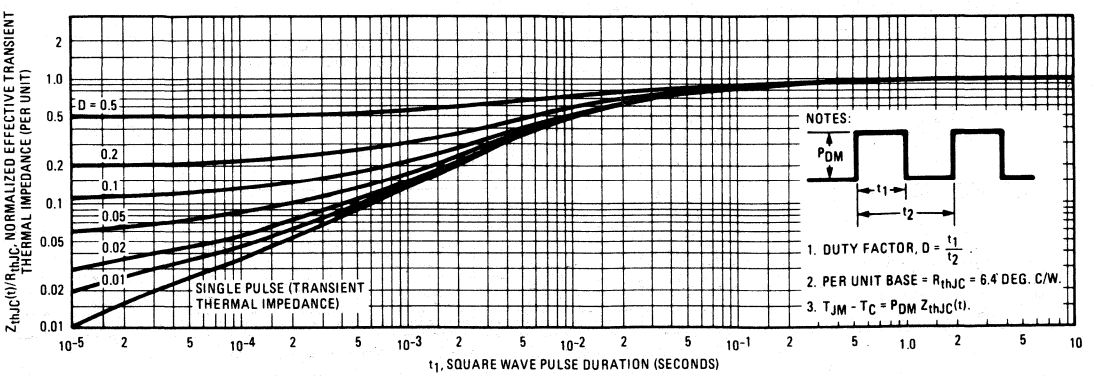


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

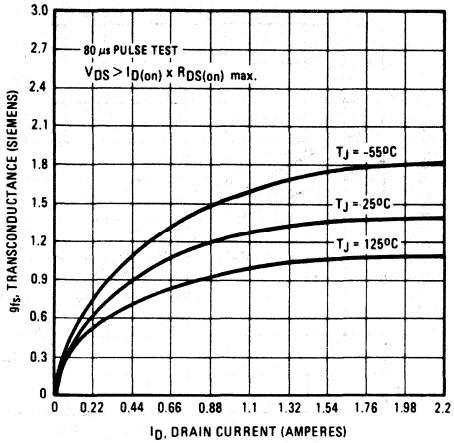


Fig. 6 — Typical Transconductance Vs. Drain Current

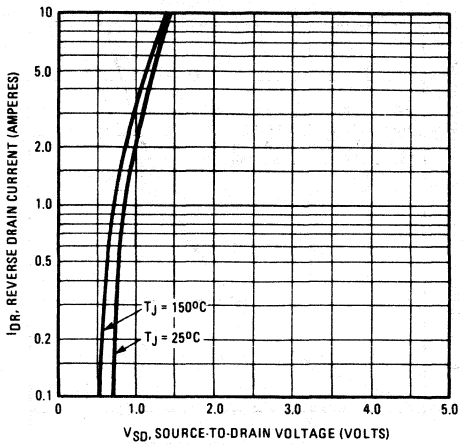


Fig. 7 — Typical Source-Drain Diode Forward Voltage

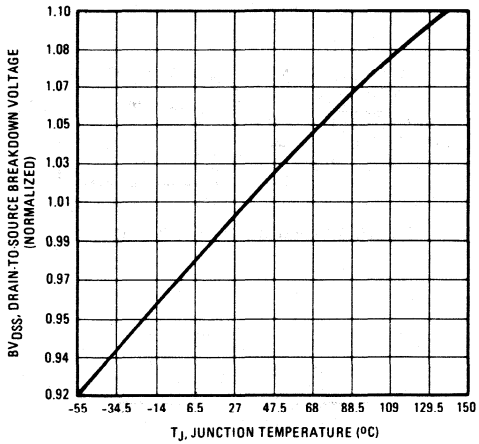


Fig. 8 — Breakdown Voltage Vs. Temperature

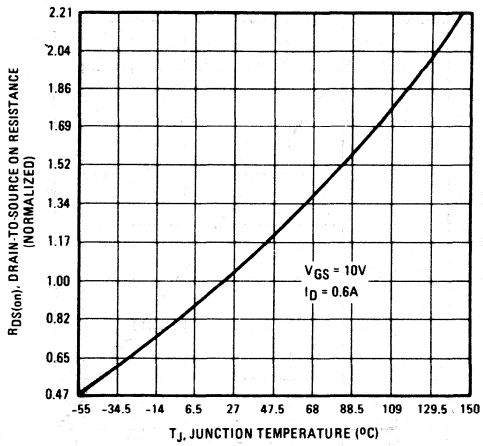


Fig. 9 — Normalized On-Resistance Vs. Temperature

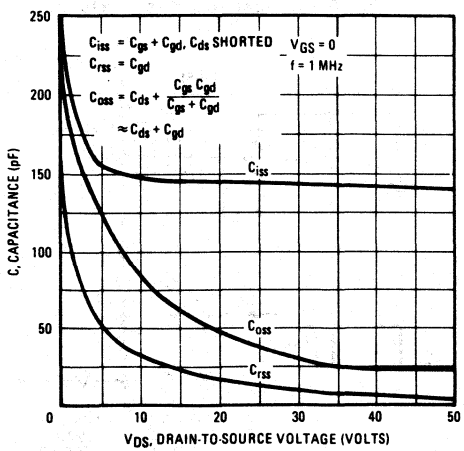


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

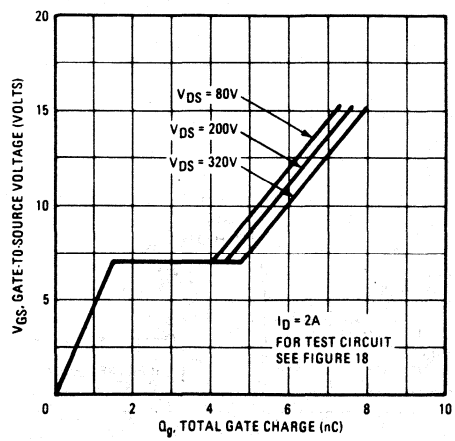


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF710, IRF711, IRF712, IRF713

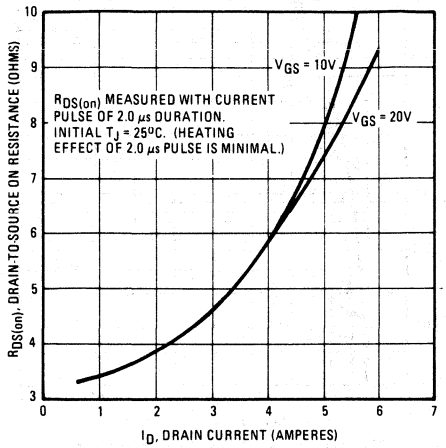


Fig. 12 – Typical On-Resistance Vs. Drain Current

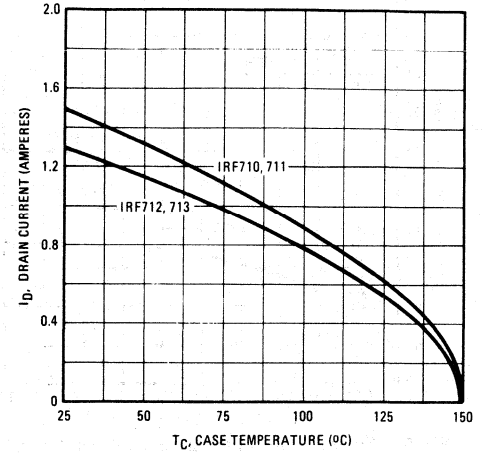


Fig. 13 – Maximum Drain Current Vs. Case Temperature

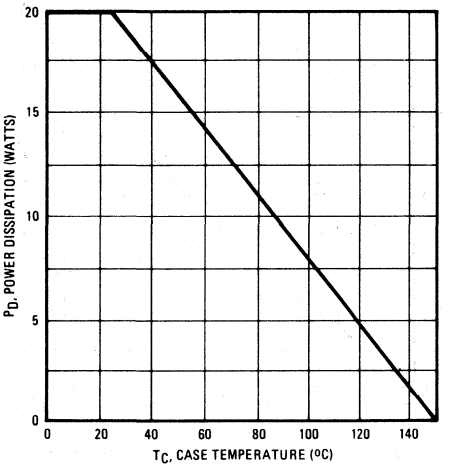


Fig. 14 – Power Vs. Temperature Derating Curve

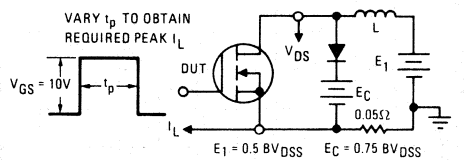


Fig. 15 – Clamped Inductive Test Circuit

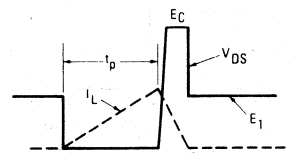


Fig. 16 – Clamped Inductive Waveforms

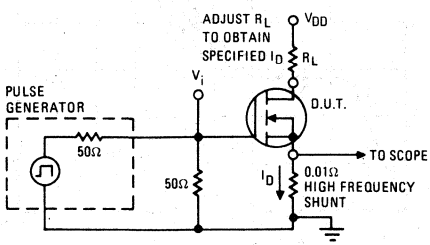


Fig. 17 – Switching Time Test Circuit

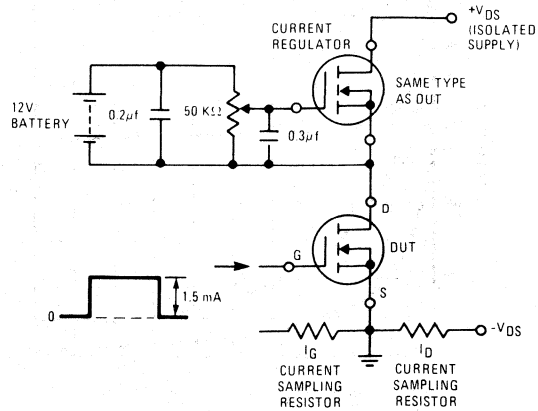


Fig. 18 – Gate Charge Test Circuit

File Number 1579

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.5A and 3.0A, 350V-400V

$r_{DS}(on)$ = 1.8 Ω and 2.5 Ω

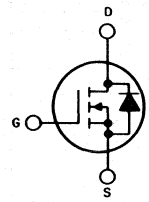
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF720, IRF721, IRF722 and IRF723 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

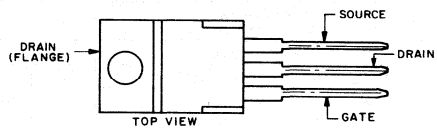
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

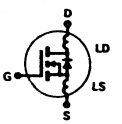
Parameter		IRF720	IRF721	IRF722	IRF723	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		12	12	10	10	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF720, IRF721, IRF722, IRF723

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF720 IRF722	400	–	–	V	V_{GS} = 0V
		IRF721 IRF723	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF720 IRF721	3.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF722 IRF723	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF720 IRF721	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF722 IRF723	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF720 IRF721	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF722 IRF723	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF720 IRF721	–	–	12	A	
		IRF722 IRF723	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	IRF720 IRF721	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		IRF722 IRF723	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

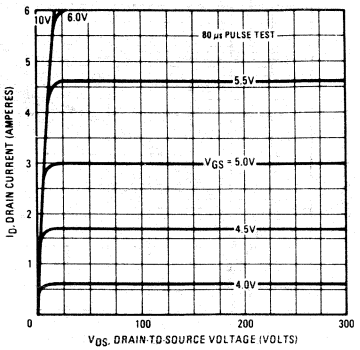


Fig. 1 — Typical Output Characteristics

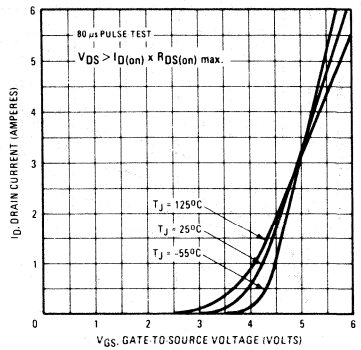


Fig. 2 — Typical Transfer Characteristics

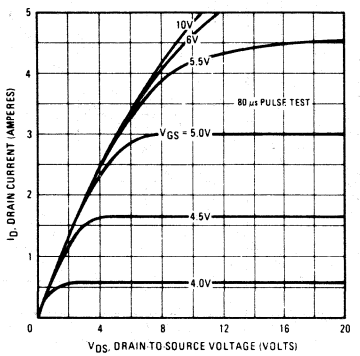


Fig. 3 — Typical Saturation Characteristics

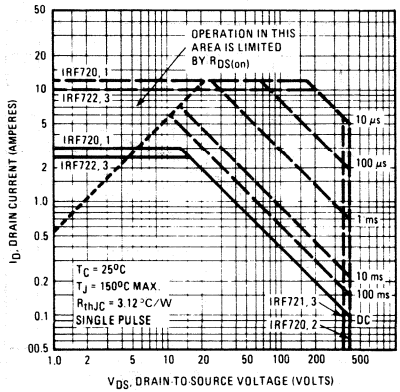


Fig. 4 — Maximum Safe Operating Area

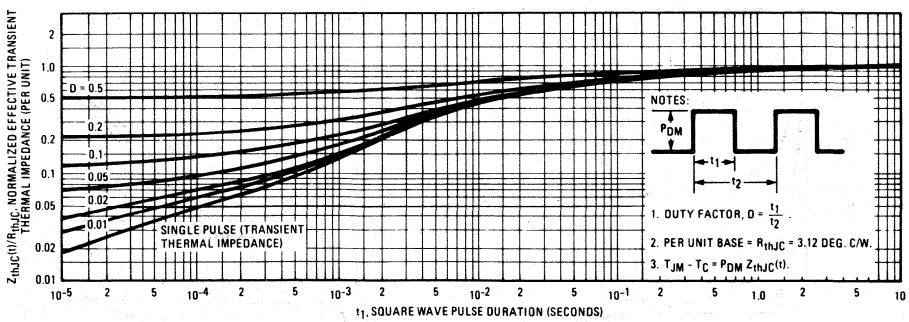


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

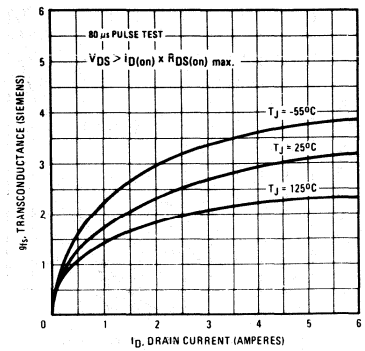


Fig. 6 – Typical Transconductance Vs. Drain Current

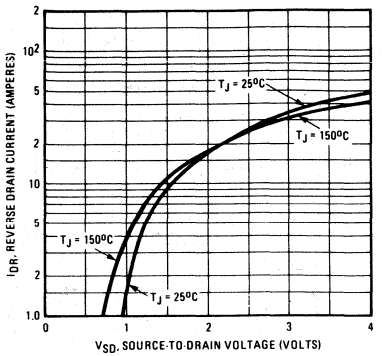


Fig. 7 – Typical Source-Drain Diode Forward Voltage

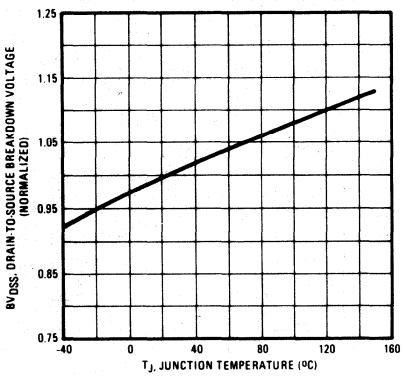


Fig. 8 – Breakdown Voltage Vs. Temperature

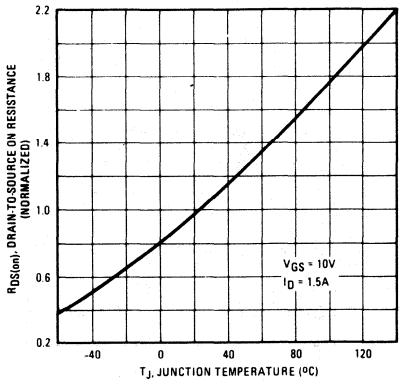


Fig. 9 – Normalized On-Resistance Vs. Temperature

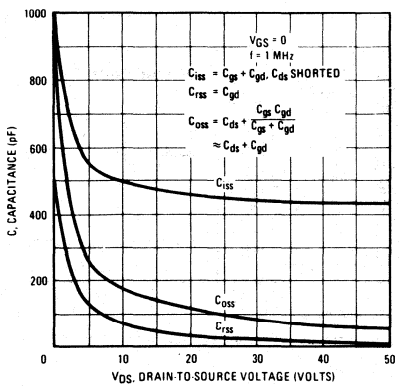


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

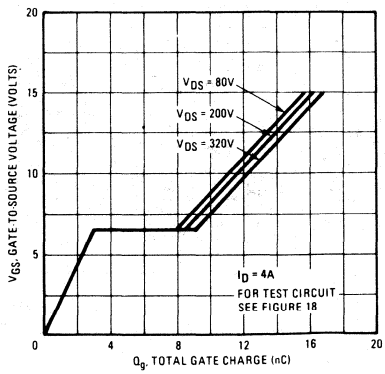


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

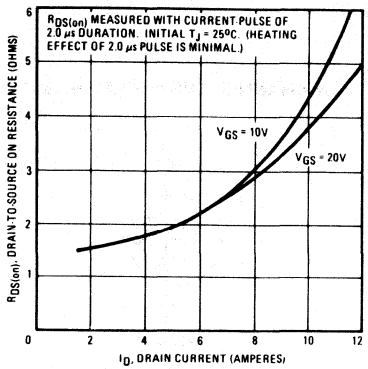


Fig. 12 – Typical On-Resistance Vs. Drain Current

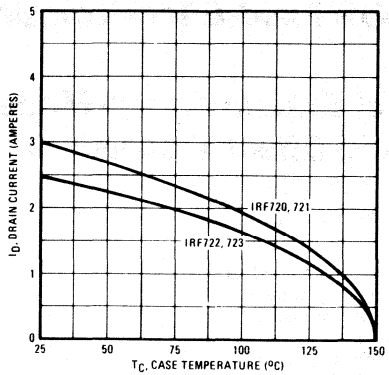


Fig. 13 – Maximum Drain Current Vs. Case Temperature

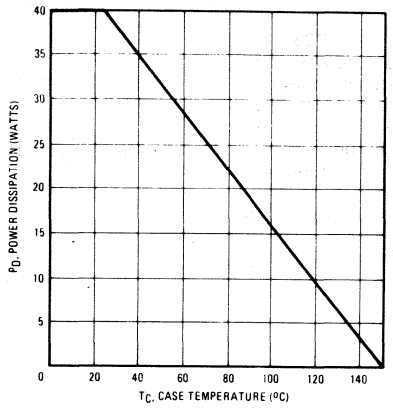


Fig. 14 – Power Vs. Temperature Derating Curve

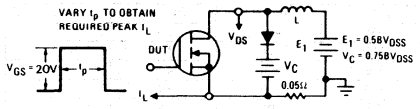


Fig. 15 – Clamped Inductive Test Circuit

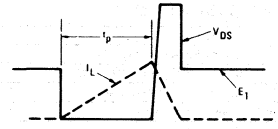


Fig. 16 – Clamped Inductive Waveforms

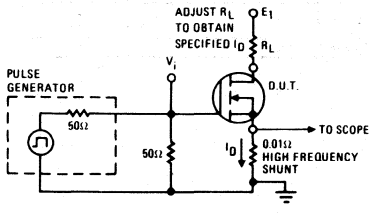


Fig. 17 – Switching Time Test Circuit

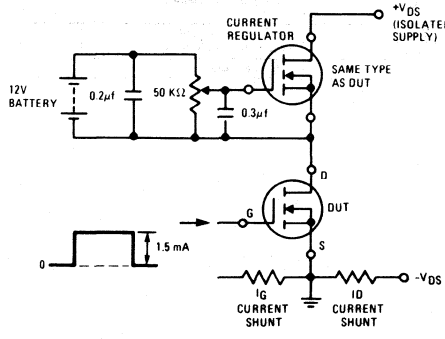


Fig. 18 – Gate Charge Test Circuit

IRF730, IRF731, IRF732, IRF733

File Number **1580**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

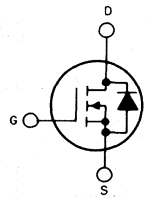
4.5A and 5.5A, 350V-400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



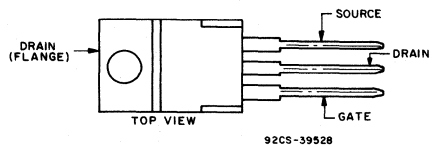
92CS-33741

TERMINAL DIAGRAM

The IRF730, IRF731, IRF732 and IRF733 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

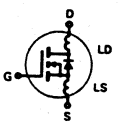
Absolute Maximum Ratings

Parameter		IRF730	IRF731	IRF732	IRF733	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF730 IRF732	400	–	–	V	V_{GS} = 0V
		IRF731 IRF733	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF730 IRF731	5.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF732 IRF733	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF730 IRF731	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF732 IRF733	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	17	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	11	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF730 IRF731	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF732 IRF733	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF730 IRF731	–	–	22	A	
		IRF732 IRF733	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	IRF730 IRF731	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF732 IRF733	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF730, IRF731, IRF732, IRF733

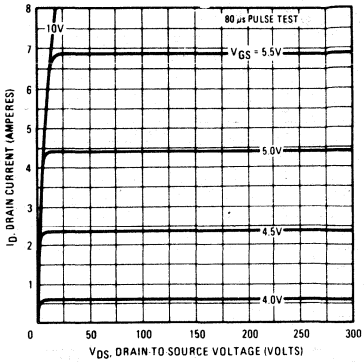


Fig. 1 — Typical Output Characteristics

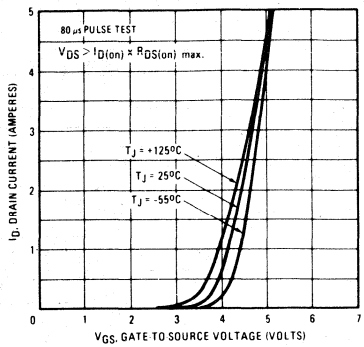


Fig. 2 — Typical Transfer Characteristics

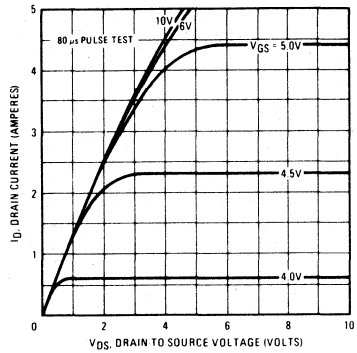


Fig. 3 — Typical Saturation Characteristics

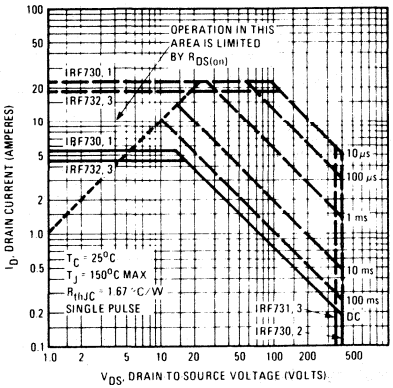


Fig. 4 — Maximum Safe Operating Area

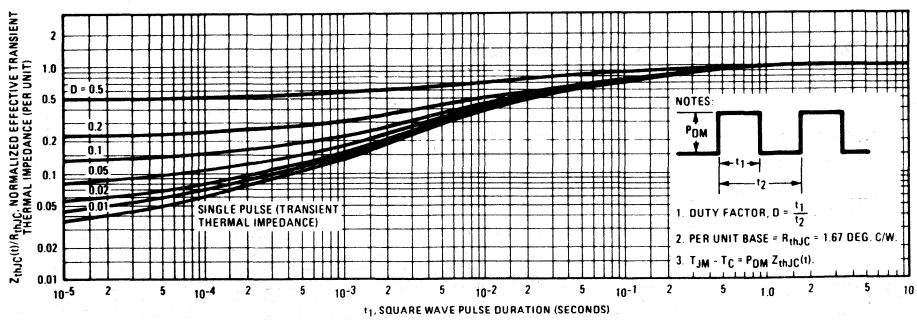


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

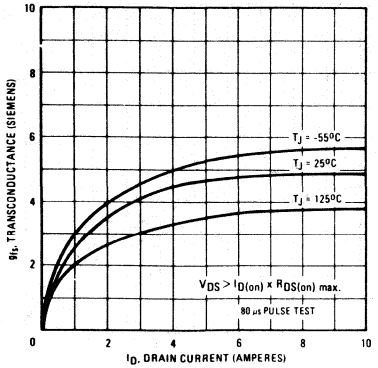


Fig. 6 – Typical Transconductance Vs. Drain Current

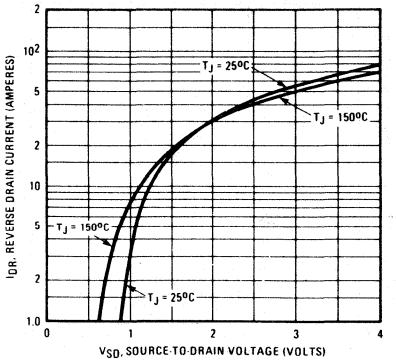


Fig. 7 – Typical Source-Drain Diode Forward Voltage

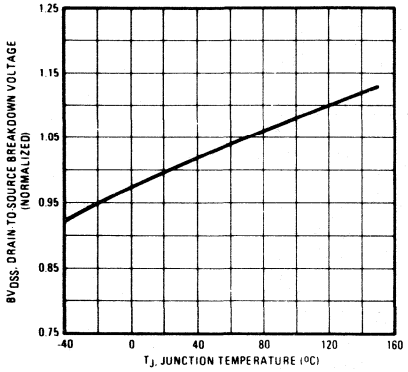


Fig. 8 – Breakdown Voltage Vs. Temperature

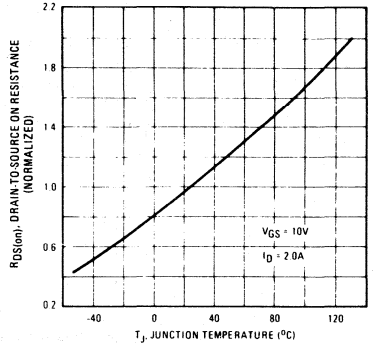


Fig. 9 – Normalized On-Resistance Vs. Temperature

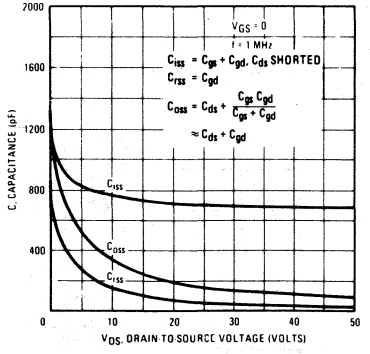


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

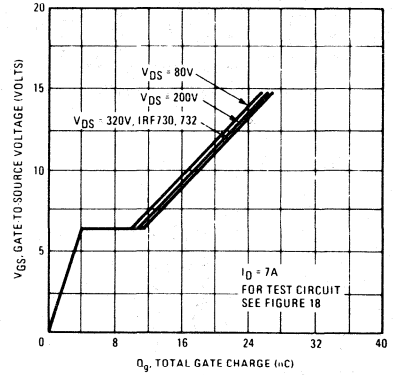


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF730, IRF731, IRF732, IRF733

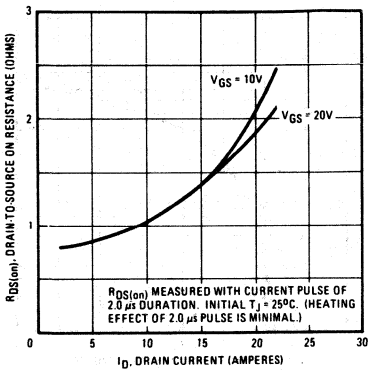


Fig. 12 – Typical On-Resistance Vs. Drain Current

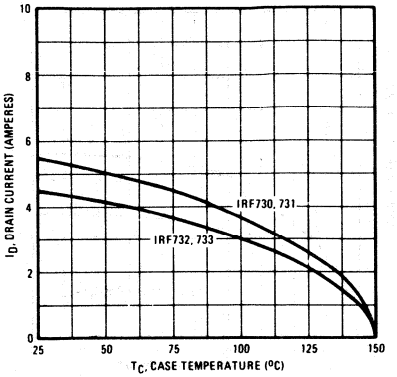


Fig. 13 – Maximum Drain Current Vs. Case Temperature

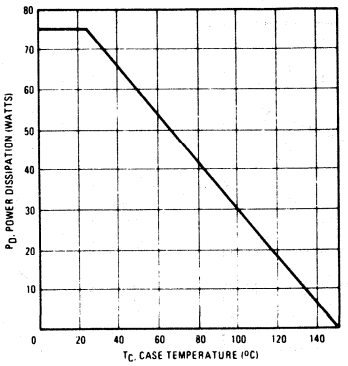


Fig. 14 – Power Vs. Temperature Derating Curve

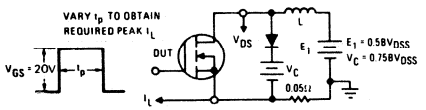


Fig. 15 – Clamped Inductive Test Circuit

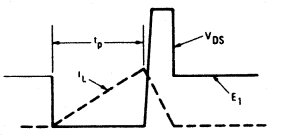


Fig. 16 – Clamped Inductive Waveforms

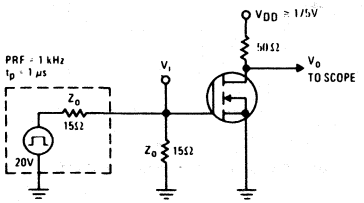


Fig. 17 – Switching Time Test Circuit

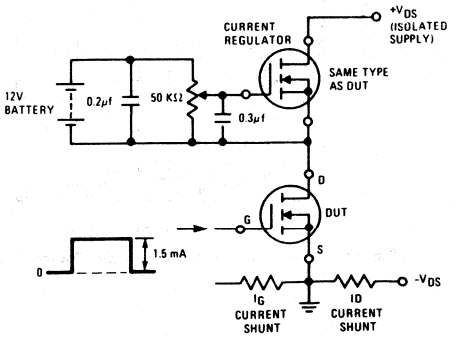


Fig. 18 – Gate Charge Test Circuit

File Number **2311**

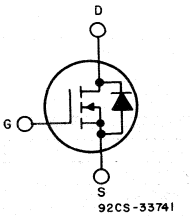
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8 A and 10 A, 350 V - 400 V
$r_{DS(on)}$ = 0.55 Ω and 0.8 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

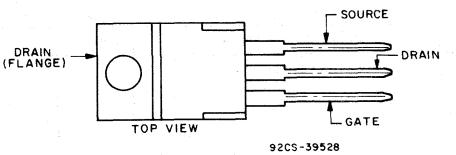


TERMINAL DIAGRAM

The IRF740, IRF741, IRF742, and IRF743 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

Absolute Maximum Ratings

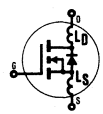
Parameter		IRF740	IRF741	IRF742	IRF743	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		40	40	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF740, IRF741, IRF742, IRF743

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF740 IRF742	400	–	–	V	V_{GS} = 0V
		IRF741 IRF743	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF740 IRF741	10	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF742 IRF743	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF740 IRF741	–	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF742 IRF743	–	.68	.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	1250	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5.0	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	45	90	ns	
t_f	Fall Time	ALL	–	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	18	27	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	23	35	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF740 IRF741	–	–	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF742 IRF743	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF740 IRF741	–	–	40	A	
		IRF742 IRF743	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF740 IRF741	–	–	2.0	V	T_C = 25°C, I_S = 10A, V_{GS} = 0V
		IRF742 IRF743	–	–	1.9	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 10A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	5.7	–	μC	T_J = 150°C, I_F = 10A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

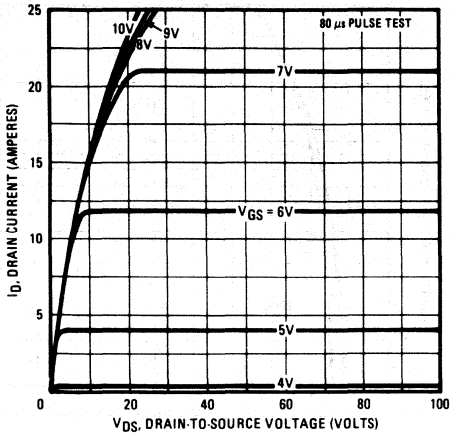


Fig. 1 — Typical Output Characteristics

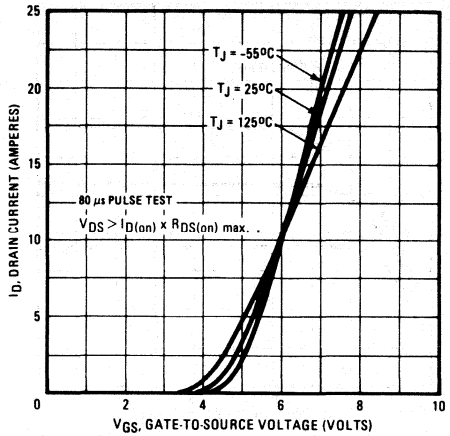


Fig. 2 — Typical Transfer Characteristics

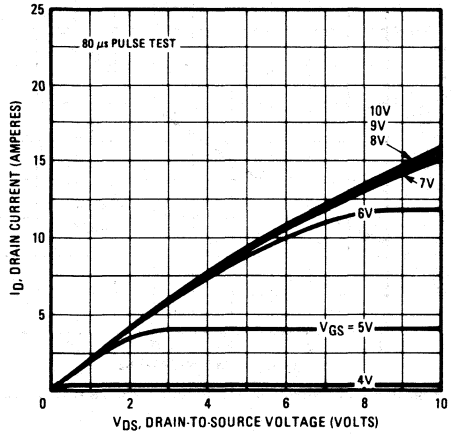


Fig. 3 — Typical Saturation Characteristics

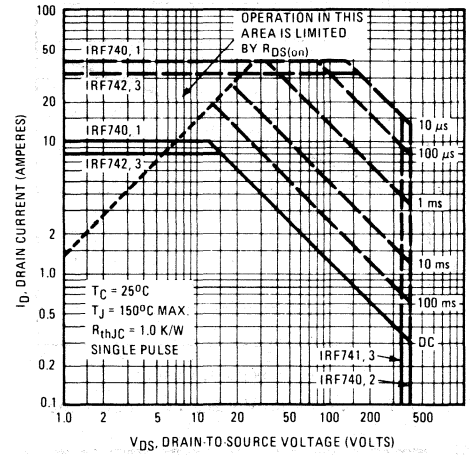


Fig. 4 — Maximum Safe Operating Area

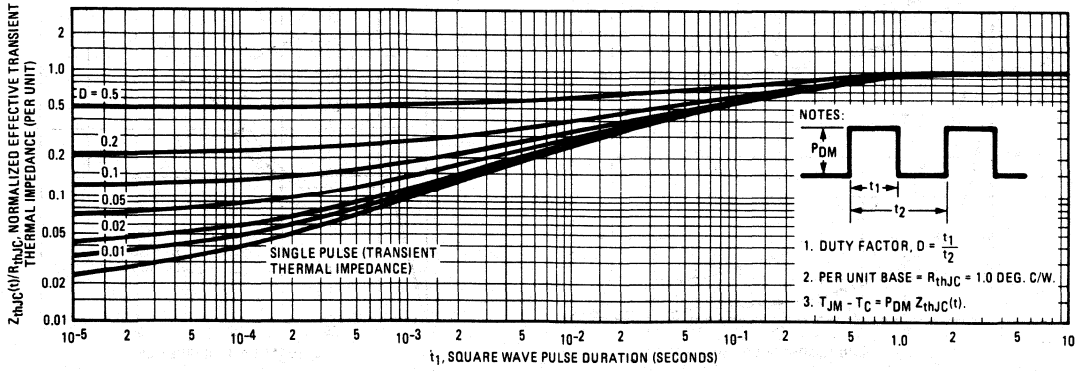


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

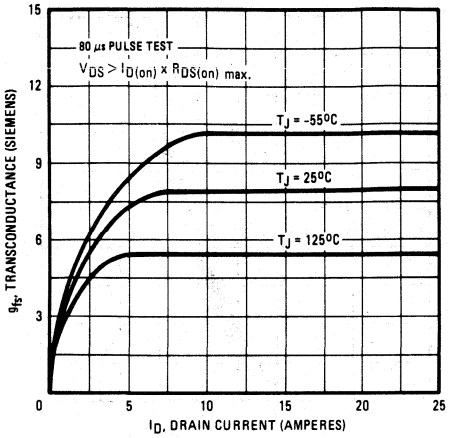


Fig. 6 — Typical Transconductance Vs. Drain Current

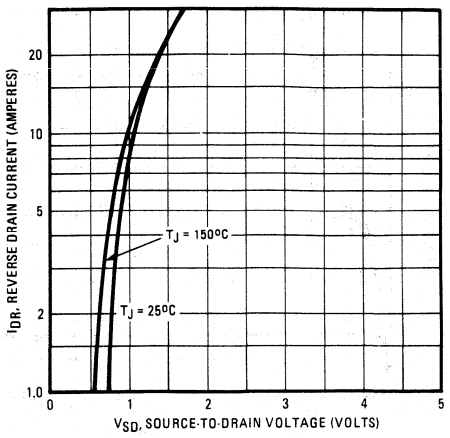


Fig. 7 — Typical Source-Drain Diode Forward Voltage

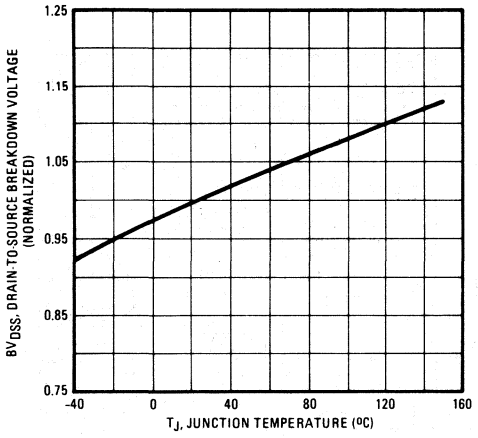


Fig. 8 — Breakdown Voltage Vs. Temperature

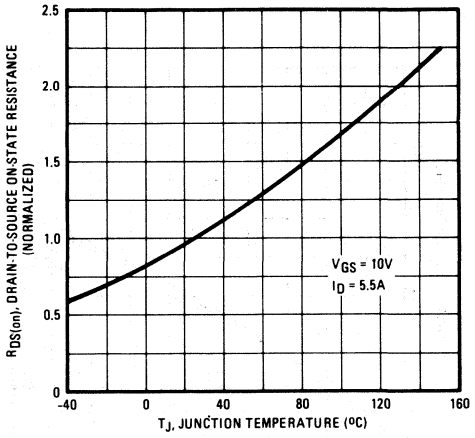
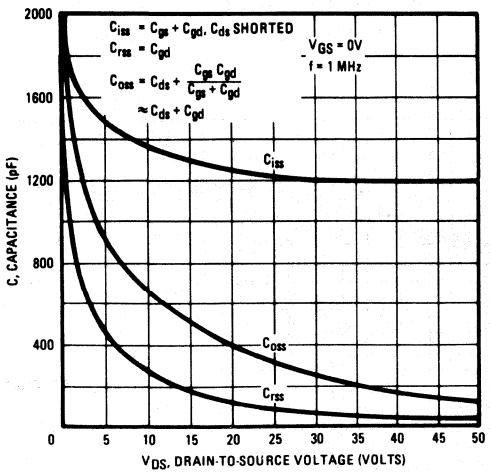


Fig. 9 — Normalized On-Resistance Vs. Temperature



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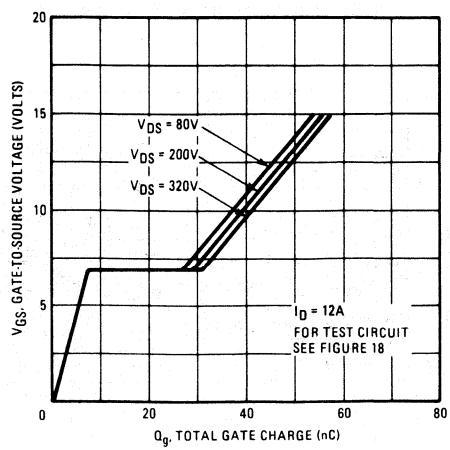


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

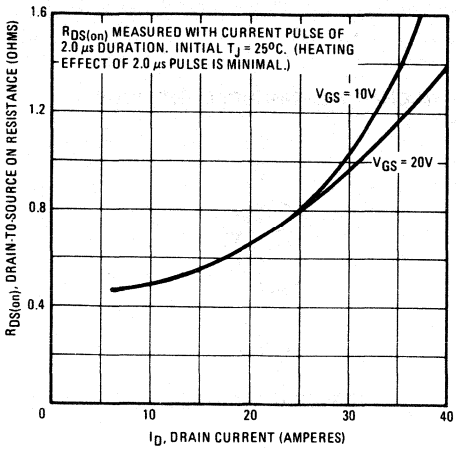


Fig. 12 – Typical On-Resistance Vs. Drain Current

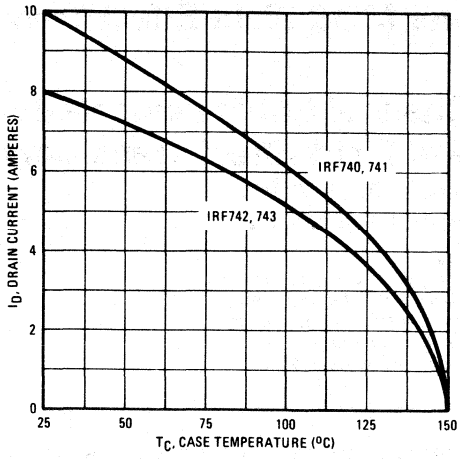


Fig. 13 – Maximum Drain Current Vs. Case Temperature

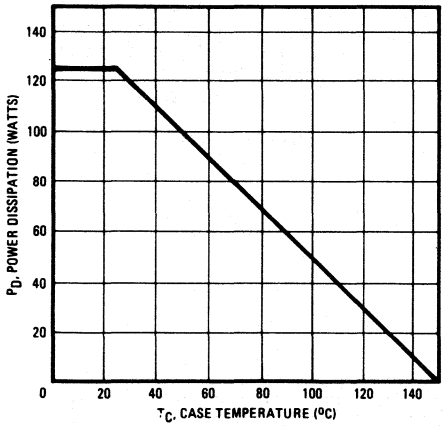


Fig. 14 – Power Vs. Temperature Derating Curve

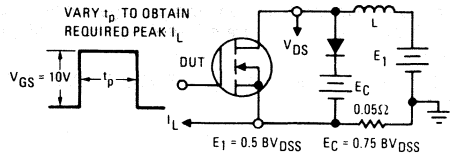


Fig. 15 – Clamped Inductive Test Circuit

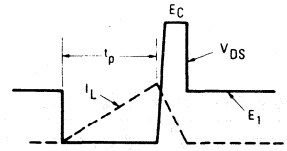


Fig. 16 – Clamped Inductive Waveforms

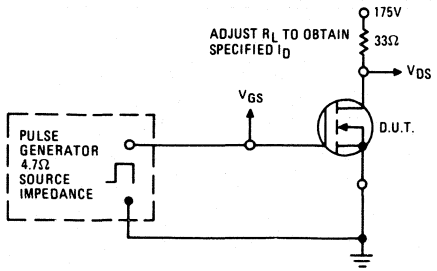


Fig. 17 – Switching Time Test Circuit

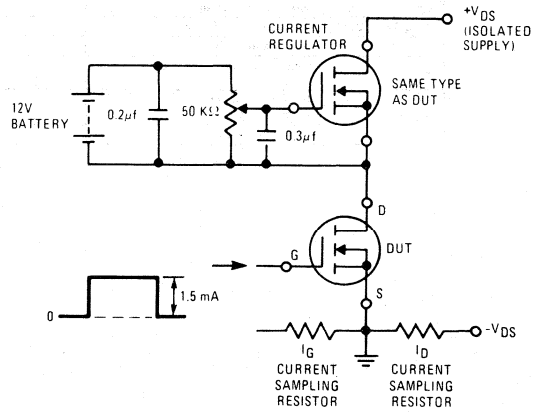


Fig. 18 – Gate Charge Test Circuit

IRF820, IRF821, IRF822, IRF823

File Number **1581**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

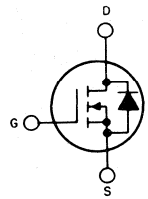
2.0A and 2.5A, 450V-500V

$r_{DS}(on)$ = 3.0 Ω and 4.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

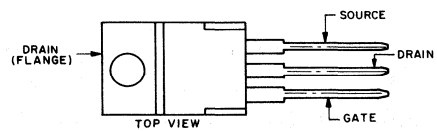
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF820, IRF821, IRF822 and IRF823 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

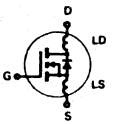
Absolute Maximum Ratings

Parameter		IRF820	IRF821	IRF822	IRF823	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF820 IRF822	500	–	–	V	V_{GS} = 0V
		IRF821 IRF823	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF820 IRF821	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF822 IRF823	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF820 IRF821	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF822 IRF823	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	7.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL		–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL		1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL		–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF820 IRF821	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF822 IRF823	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF820 IRF821	–	–	10	A	
		IRF822 IRF823	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF820 IRF821	–	–	1.6	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF822 IRF823	–	–	1.5	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF820, IRF821, IRF822, IRF823

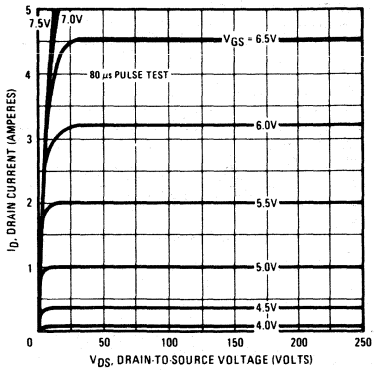


Fig. 1 — Typical Output Characteristics

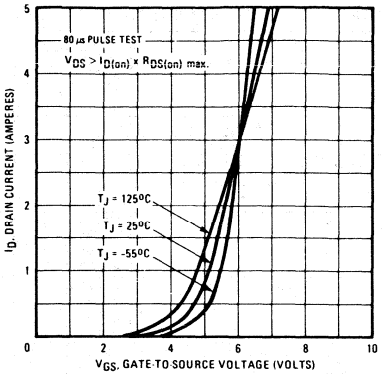


Fig. 2 — Typical Transfer Characteristics

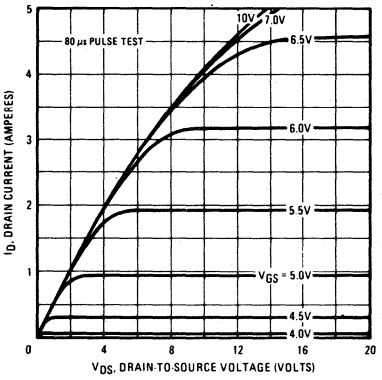


Fig. 3 — Typical Saturation Characteristics

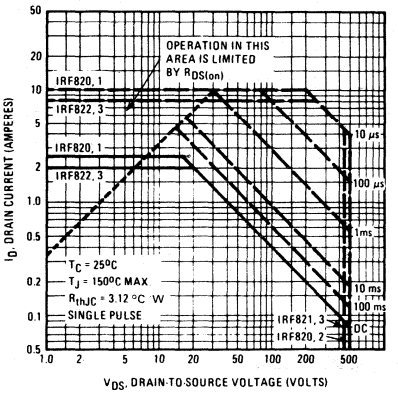


Fig. 4 — Maximum Safe Operating Area

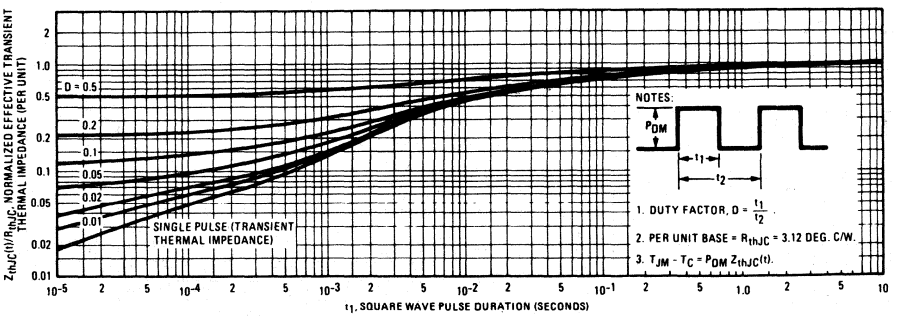


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

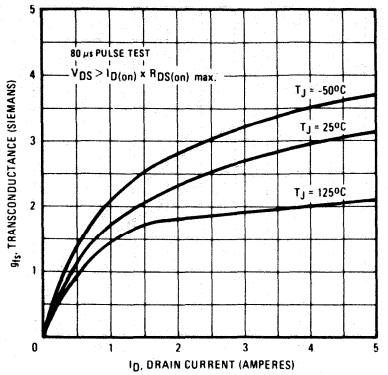


Fig. 6 – Typical Transconductance Vs. Drain Current

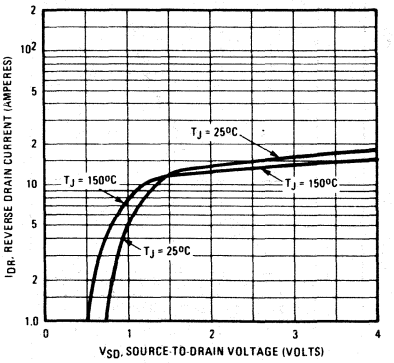


Fig. 7 – Typical Source-Drain Diode Forward Voltage

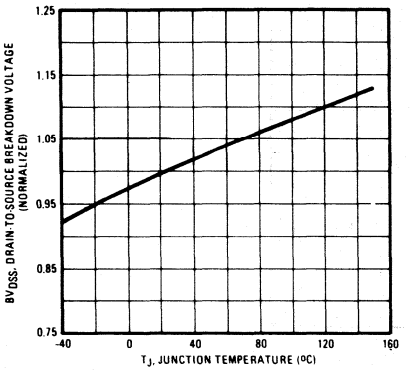


Fig. 8 – Breakdown Voltage Vs. Temperature

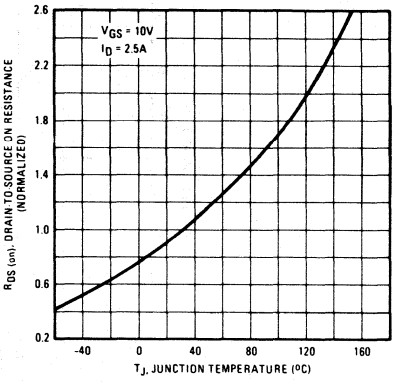


Fig. 9 – Normalized On-Resistance Vs. Temperature

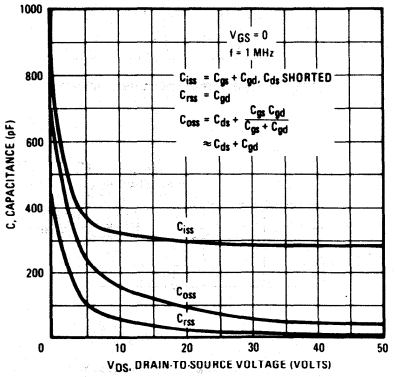


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

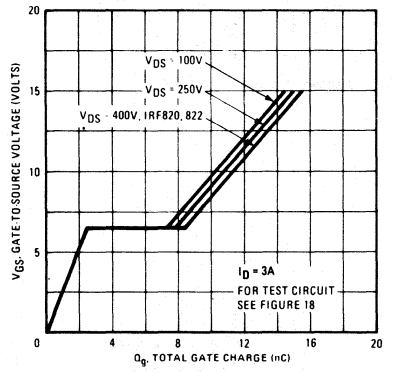


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF820, IRF821, IRF822, IRF823

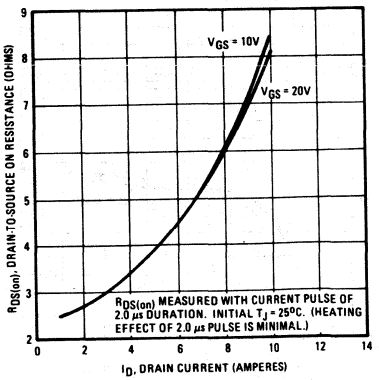


Fig. 12 – Typical On-Resistance Vs. Drain Current

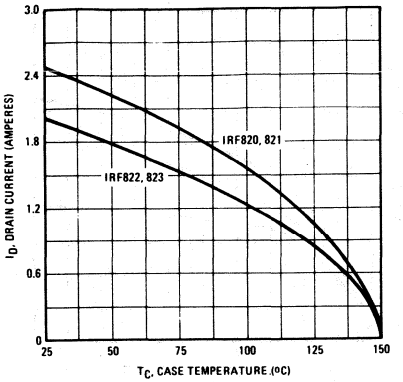


Fig. 13 – Maximum Drain Current Vs. Case Temperature

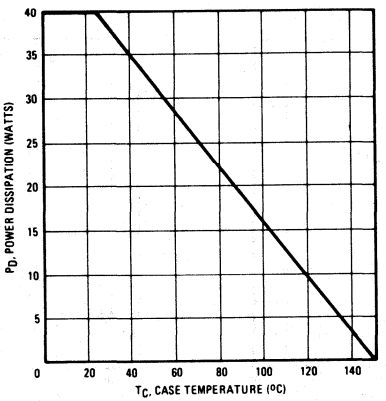


Fig. 14 – Power Vs. Temperature Derating Curve

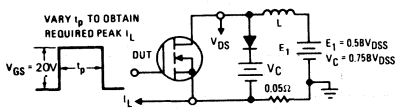


Fig. 15 – Clamped Inductive Test Circuit

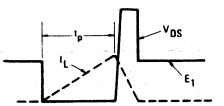


Fig. 16 – Clamped Inductive Waveforms

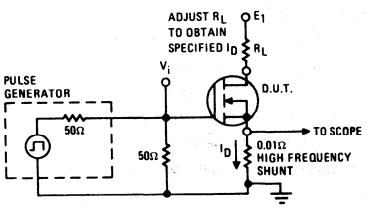


Fig. 17 – Switching Time Test Circuit

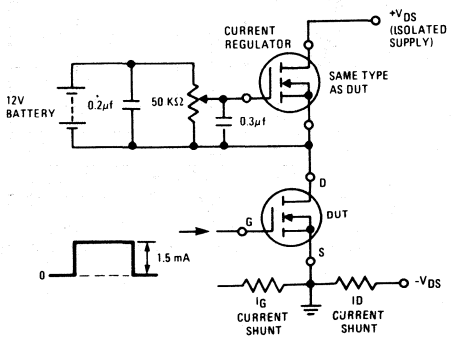


Fig. 18 – Gate Charge Test Circuit

File Number **1582**

IRF830, IRF831, IRF832, IRF833

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

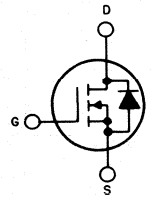
4.0A and 4.5A, 450V-500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

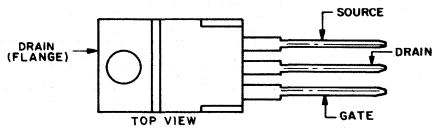
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF830, IRF831, IRF832 and IRF833 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

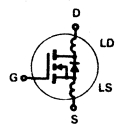
Parameter		IRF830	IRF831	IRF832	IRF833	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		18	18	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF830, IRF831, IRF832, IRF833

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF830 IRF832	500	–	–	V	V_{GS} = 0V
		IRF831 IRF833	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF830 IRF831	4.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF832 IRF833	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF830 IRF831	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF832 IRF833	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.25	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 2.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	17	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	17	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF830 IRF831	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF832 IRF833	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF830 IRF831	–	–	18	A	
		IRF832 IRF833	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF830 IRF831	–	–	1.6	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF832 IRF833	–	–	1.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

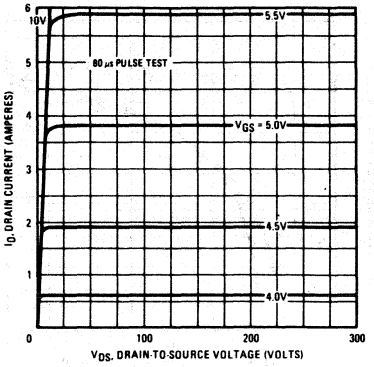


Fig. 1 – Typical Output Characteristics

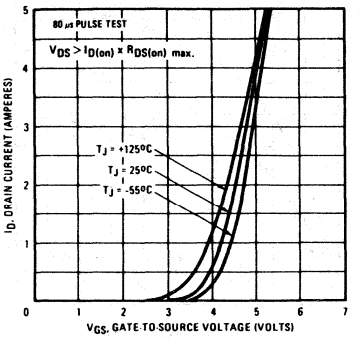


Fig. 2 – Typical Transfer Characteristics

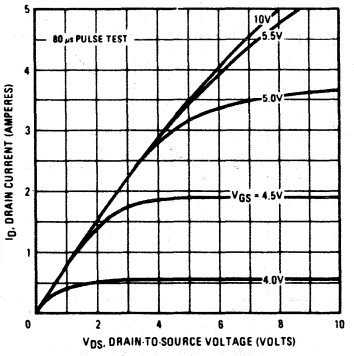


Fig. 3 – Typical Saturation Characteristics

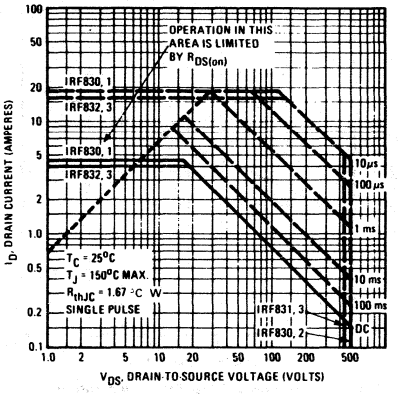


Fig. 4 – Maximum Safe Operating Area

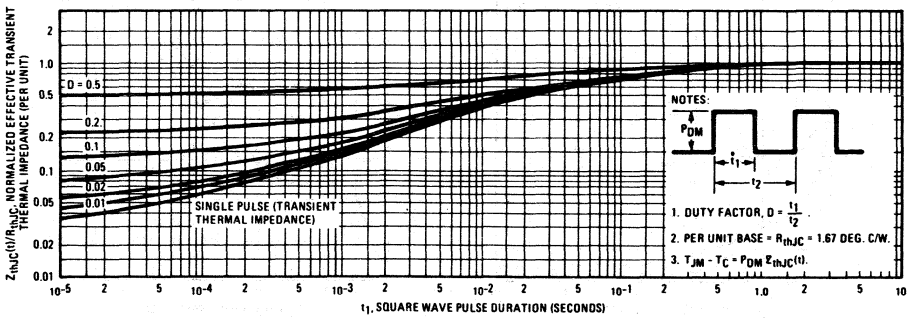


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

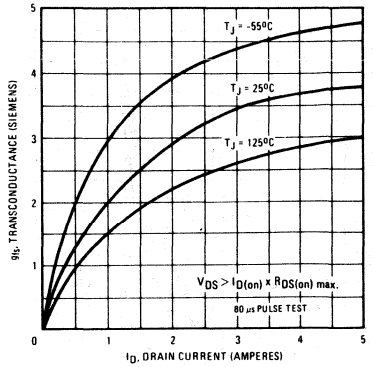


Fig. 6 — Typical Transconductance Vs. Drain Current

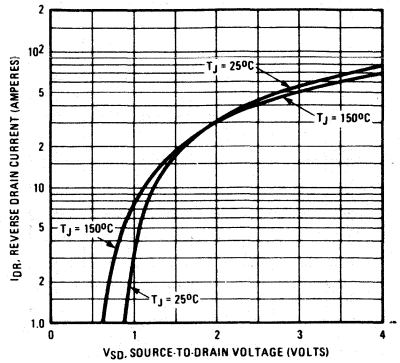


Fig. 7 — Typical Source-Drain Diode Forward Voltage

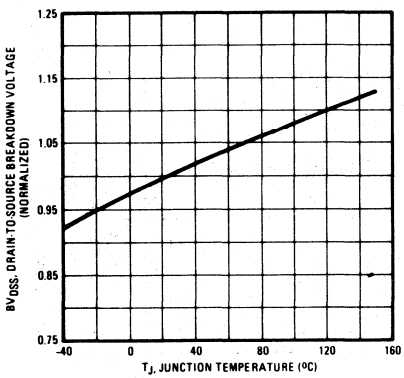


Fig. 8 — Breakdown Voltage Vs. Temperature

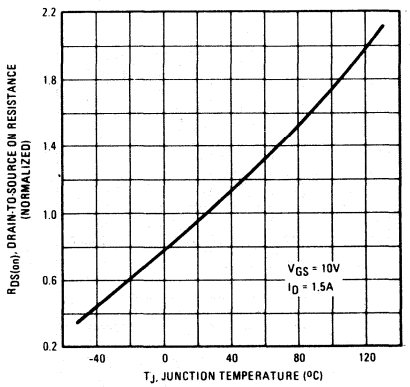


Fig. 9 — Normalized On-Resistance Vs. Temperature

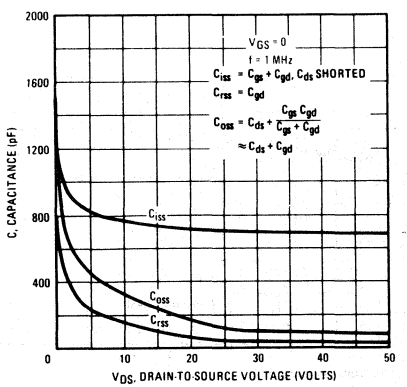


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

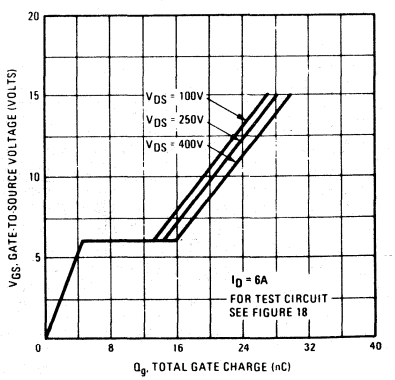


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

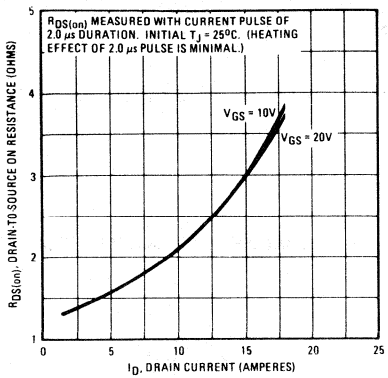


Fig. 12 – Typical On-Resistance Vs. Drain Current

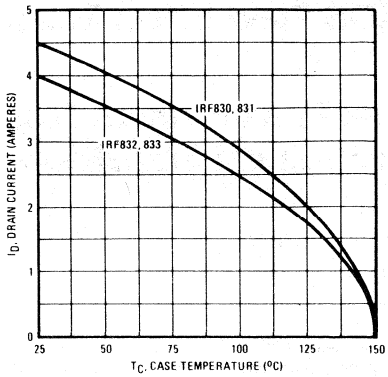


Fig. 13 – Maximum Drain Current Vs. Case Temperature

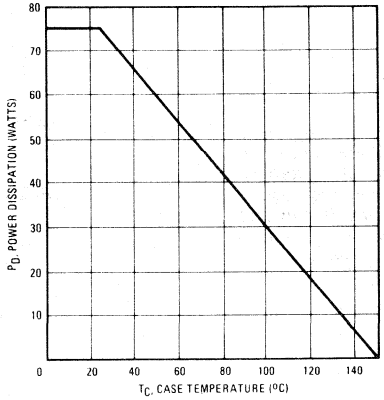


Fig. 14 – Power Vs. Temperature Derating Curve

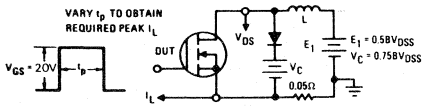


Fig. 15 – Clamped Inductive Test Circuit

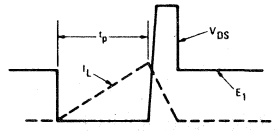


Fig. 16 – Clamped Inductive Waveforms

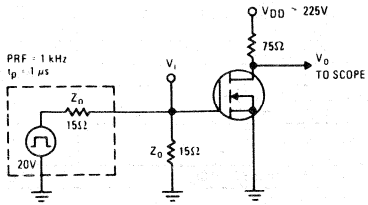


Fig. 17 – Switching Time Test Circuit

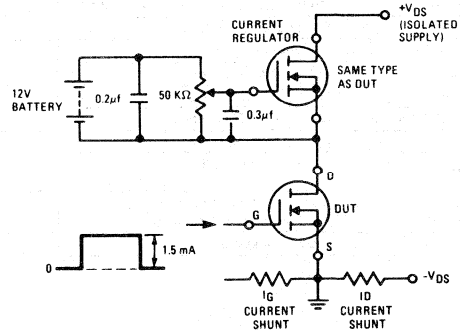


Fig. 18 – Gate Charge Test Circuit

IRF840, IRF841, IRF842, IRF843

File Number **2312**

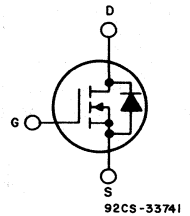
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

7 A and 8 A, 450 V - 500 V
$r_{DS(on)}$ = 0.85 Ω and 1.1 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

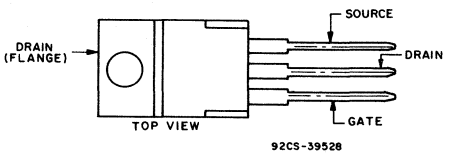


TERMINAL DIAGRAM

The IRF840, IRF841, IRF842, and IRF843 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

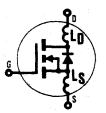
Absolute Maximum Ratings

	Parameter	IRF840	IRF841	IRF842	IRF843	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF840 IRF842	500	–	–	V	V_{GS} = 0V
		IRF841 IRF843	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF840 IRF841	8.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF842 IRF843	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF840 IRF841	–	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF842 IRF843	–	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	1225	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	85	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 200V, I_D = 4.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	42	90	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	20	30	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	22	33	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF840 IRF841	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF842 IRF843	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF840 IRF841	–	–	32	A	
		IRF842 IRF843	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF840 IRF841	–	–	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 100A/μs
		IRF842 IRF843	–	–	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 100A/μs
t_{rr}	Reverse Recovery Time	ALL	–	1100	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.4	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF840, IRF841, IRF842, IRF843

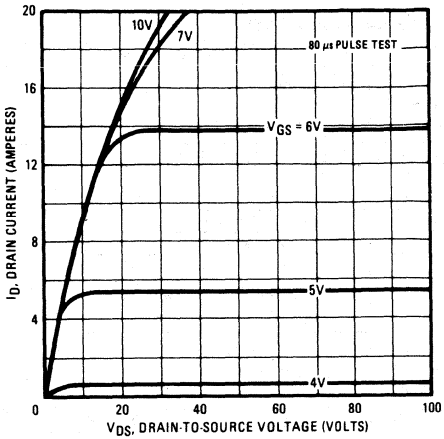


Fig. 1 — Typical Output Characteristics

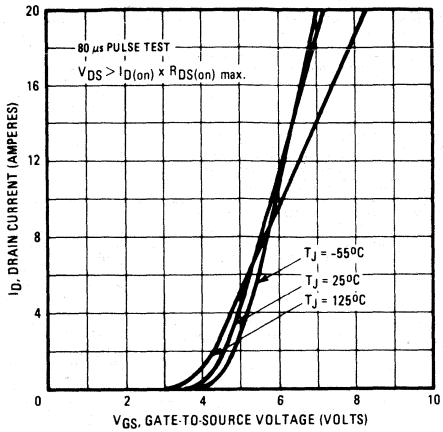


Fig. 2 — Typical Transfer Characteristics

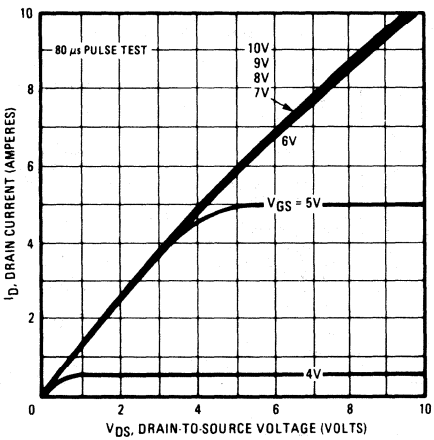


Fig. 3 — Typical Saturation Characteristics

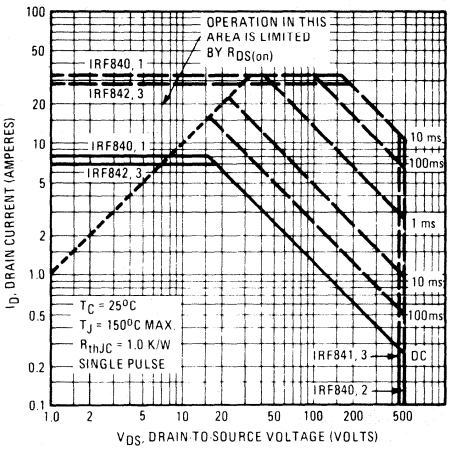


Fig. 4 — Maximum Safe Operating Area

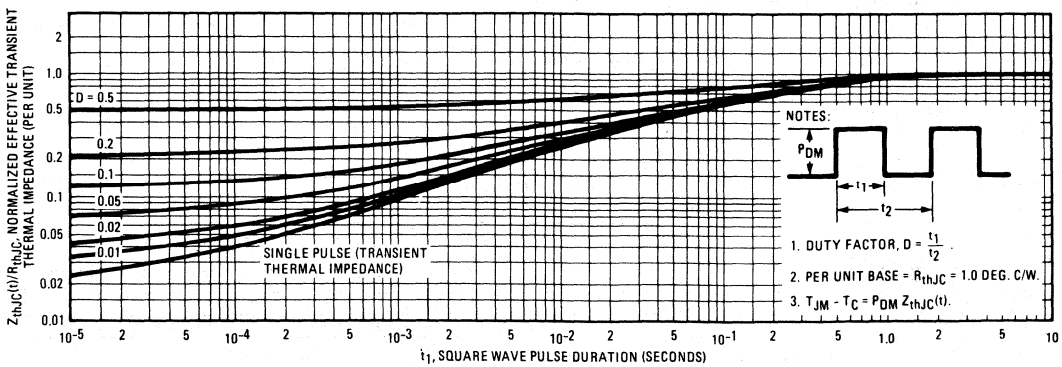


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

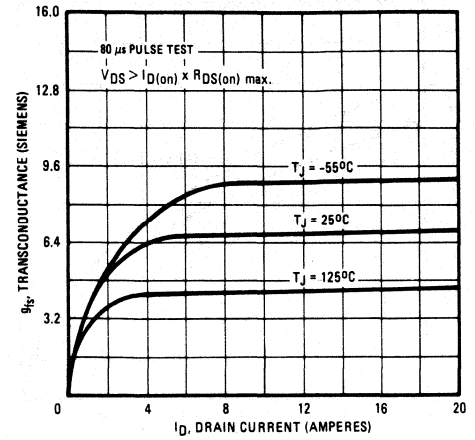


Fig. 6 — Typical Transconductance Vs. Drain Current

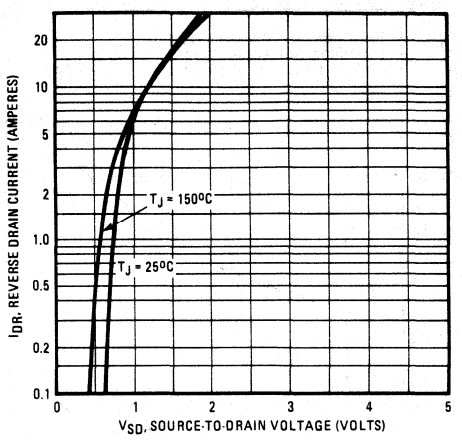


Fig. 7 — Typical Source-Drain Diode Forward Voltage

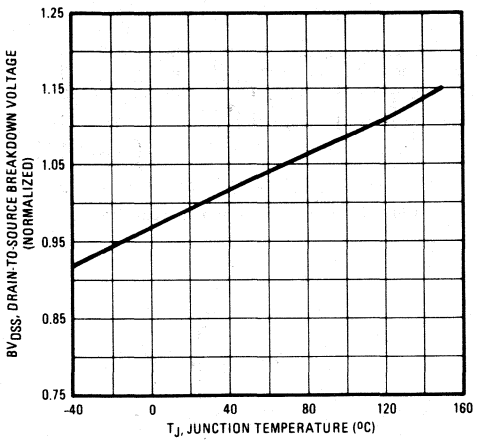


Fig. 8 — Breakdown Voltage Vs. Temperature

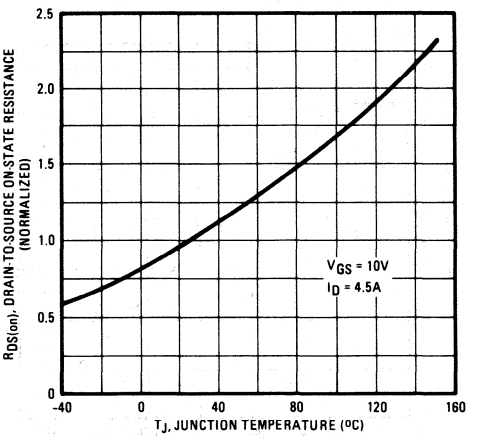


Fig. 9 — Normalized On-Resistance Vs. Temperature

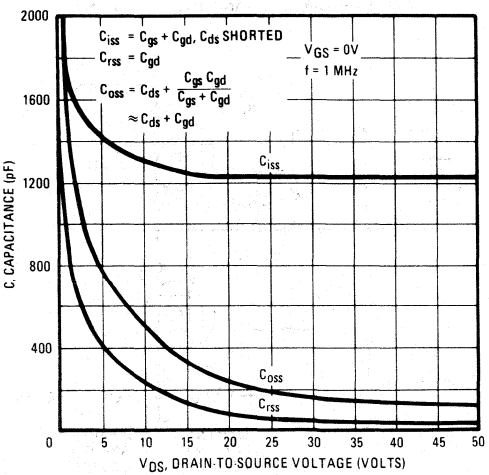


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

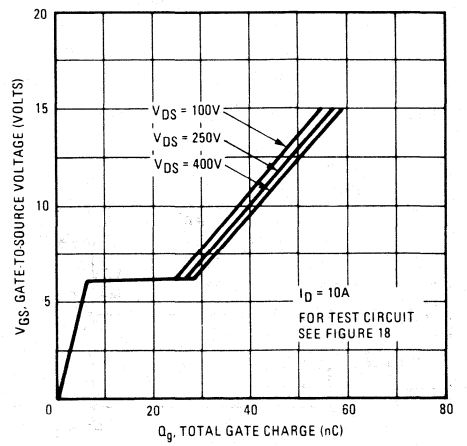


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF840, IRF841, IRF842, IRF843

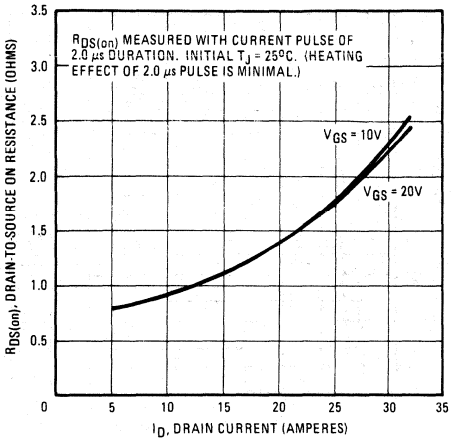


Fig. 12 – Typical On-Resistance Vs. Drain Current

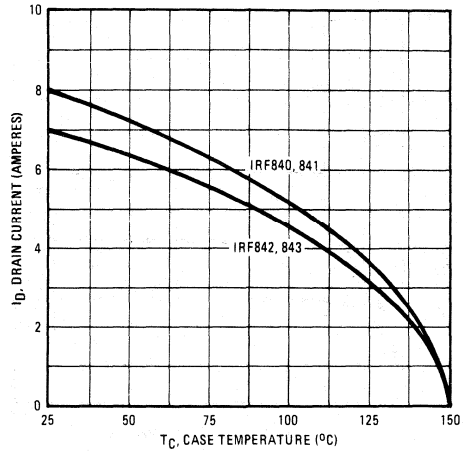


Fig. 13 – Maximum Drain Current Vs. Case Temperature

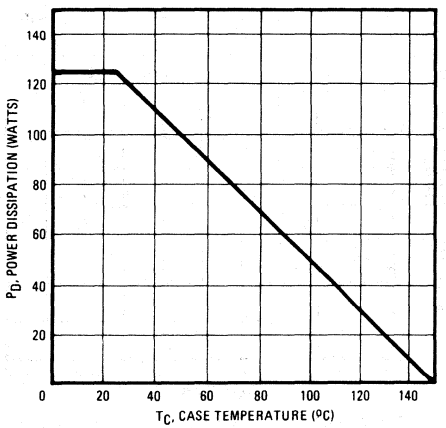


Fig. 14 – Power Vs. Temperature Derating Curve

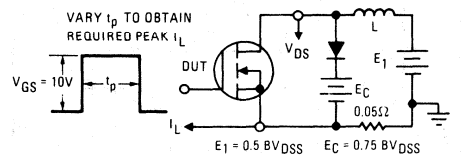


Fig. 15 – Clamped Inductive Test Circuit

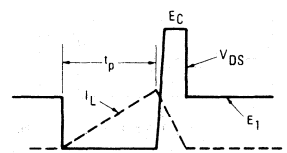


Fig. 16 – Clamped Inductive Waveforms

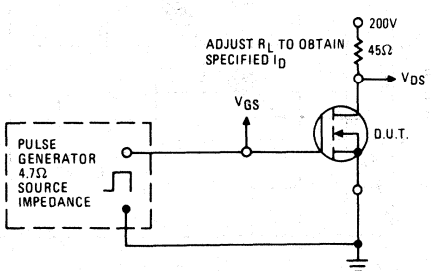


Fig. 17 – Switching Time Test Circuit

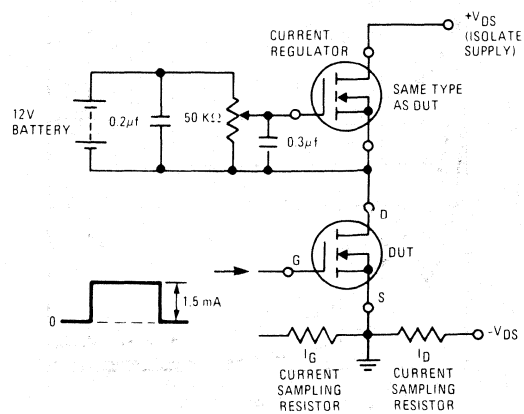


Fig. 18 – Gate Charge Test Circuit

File Number **2314**

IRFD110, IRFD111, IRFD112, IRFD113

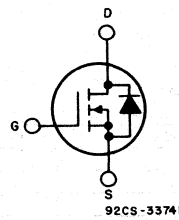
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.8 A and 1 A, 60 V - 100 V
$r_{DS(on)}$ = 0.6 Ω and 0.8 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

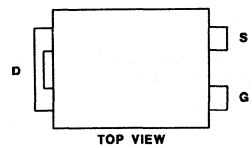


TERMINAL DIAGRAM

The IRFD110, IRFD111, IRFD112, and IRFD113 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-pin DIP package.

TERMINAL DESIGNATION



4-PIN DIP

ABSOLUTE MAXIMUM RATINGS

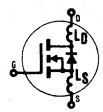
	Parameter	IRFD110	IRFD111	IRFD112	IRFD113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_A = 25°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current	8.0	8.0	6.4	6.4	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100 μH				A
		8.0	8.0	6.4	6.4	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD110, IRFD111, IRFD112, IRFD113

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD110, 2	100	–	–	V	V_{GS} = 0V
		IRFD111, 3	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD110, 2	1.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD111, 3	0.8	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD110, 2	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRFD111, 3	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	–	135	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	80	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.8A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.0	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	3.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	11	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD110, 2	–	–	1.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD111, 3	–	–	0.8	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD110, 2	–	–	8.0	A	
		IRFD111, 3	–	–	6.4	A	
V_{SD}	Diode Forward Voltage ②	IRFD110, 2	–	–	2.5	V	T_A = 25°C, I_S = 1.0A, V_{GS} = 0V
		IRFD111, 3	–	–	2.0	V	T_A = 25°C, I_S = 0.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	μC	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

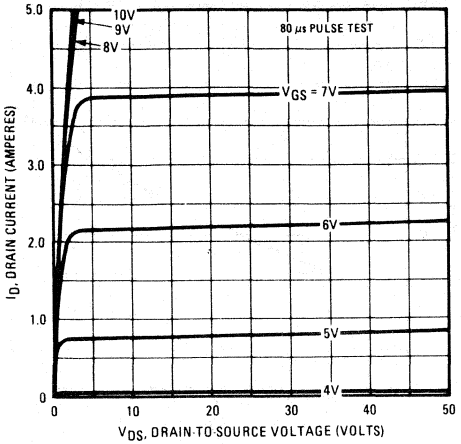


Fig. 1 — Typical Output Characteristics

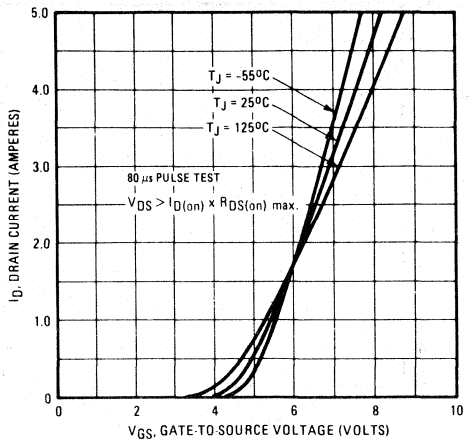


Fig. 2 — Typical Transfer Characteristics

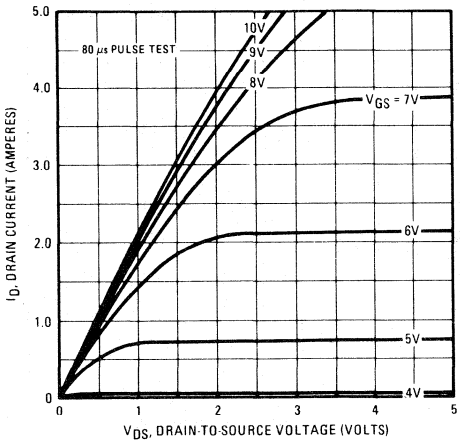


Fig. 3 — Typical Saturation Characteristics

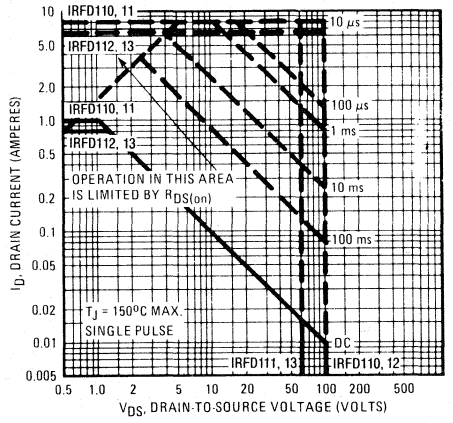


Fig. 4 — Maximum Safe Operating Area

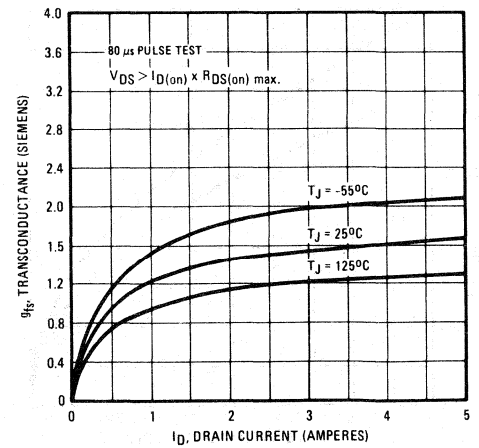


Fig. 5 — Typical Transconductance Vs. Drain Current

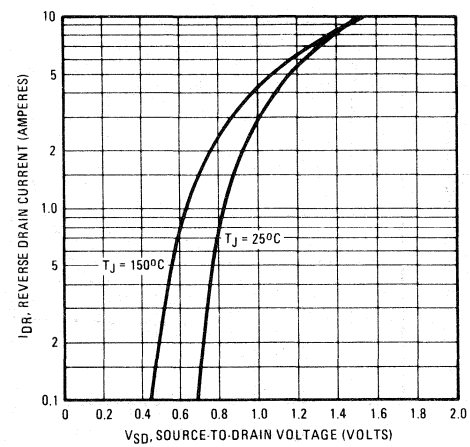


Fig. 6 — Typical Source-Drain Diode Forward Voltage

IRFD110, IRFD111, IRFD112, IRFD113

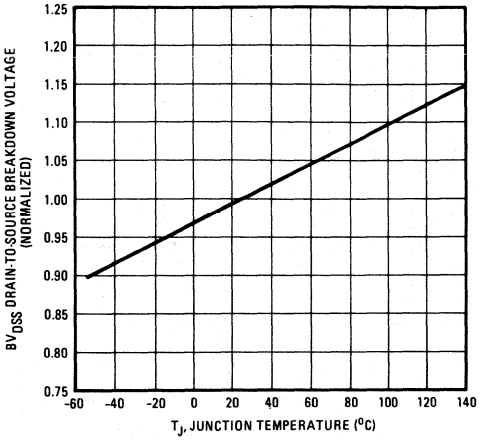


Fig. 7 — Breakdown Voltage Vs. Temperature

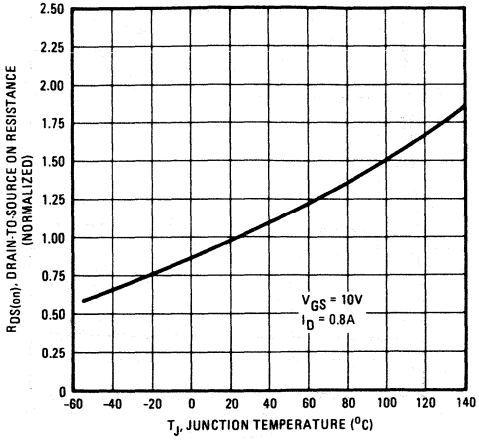


Fig. 8 — Normalized On-Resistance Vs. Temperature

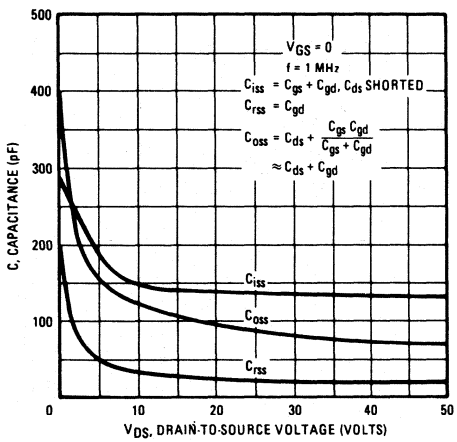


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

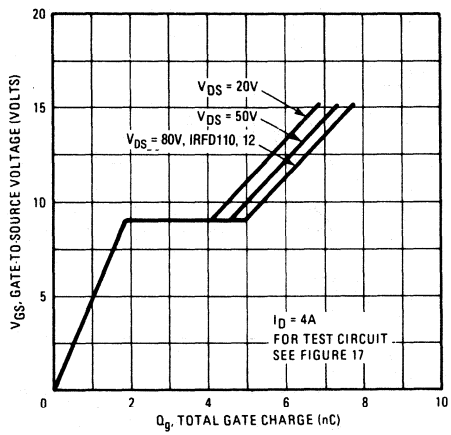


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

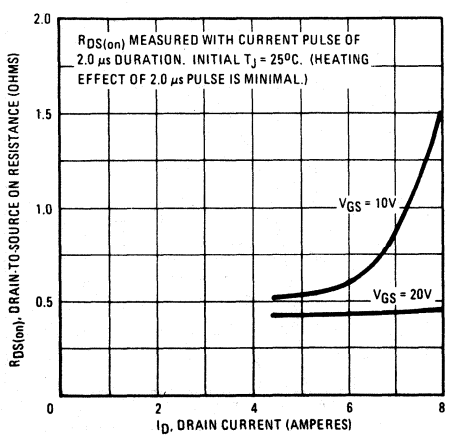


Fig. 11 — Typical On-Resistance Vs. Drain Current

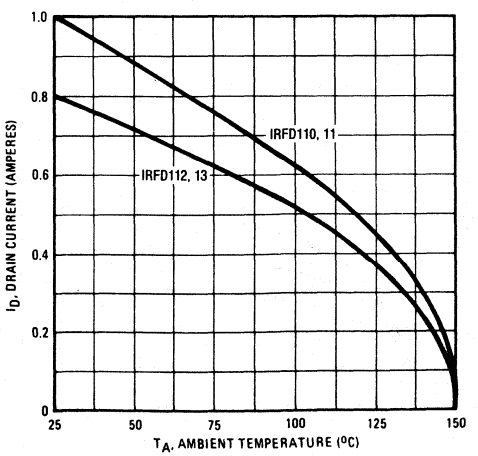


Fig. 12 — Maximum Drain Current Vs. Case Temperature

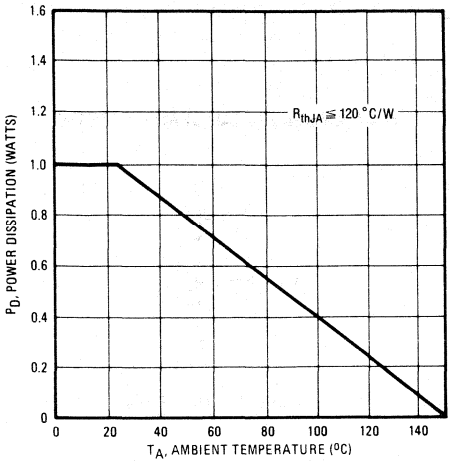


Fig. 13 – Power Vs. Temperature Derating Curve

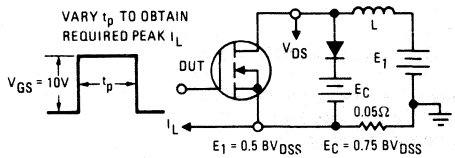


Fig. 14 – Clamped Inductive Test Circuit

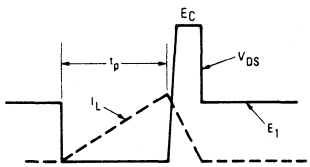


Fig. 15 – Clamped Inductive Waveforms

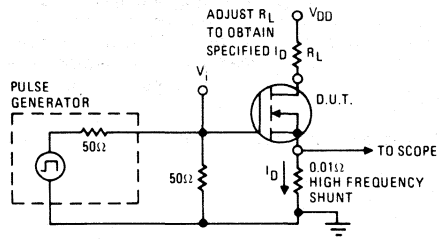


Fig. 16 – Switching Time Test Circuit

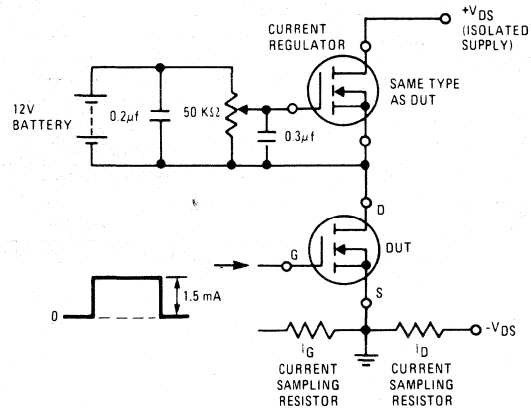


Fig. 17 – Gate Charge Test Circuit

IRFD120, IRFD121, IRFD122, IRFD123

File Number **2315**

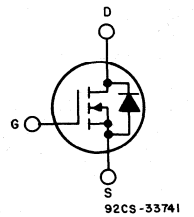
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

1.1 A and 1.3 A, 60 V - 100 V
$r_{DS(on)}$ = 0.3 Ω and 0.4 Ω

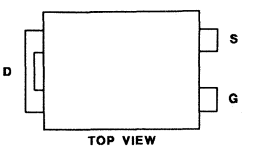
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



4-PIN DIP

The IRFD120, IRFD121, IRFD122, and IRFD123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-pin DIP package.

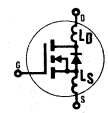
ABSOLUTE MAXIMUM RATINGS

Parameter		IRFD120	IRFD121	IRFD122	IRFD123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_A = 25°C	Continuous Drain Current	1.3	1.3	1.1	1.1	A
I_{DM}	Pulsed Drain Current	5.2	5.2	4.4	4.4	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100 μH				A
		5.2	5.2	4.4	4.4	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFD120, 2	100	–	–	V	V_{GS} = 0V
		IRFD121, 3	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD120, 1	1.3	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD122, 3	1.1	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFD120, 1	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 0.6A
		IRFD122, 3	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.9	1.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.6A
C_{iss}	Input Capacitance	ALL	–	450	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	200	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.6A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 5.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	5.0	7.5	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD120, 1	–	–	1.3	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD122, 3	–	–	1.1	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD120, 1	–	–	5.2	A	
		IRFD122, 3	–	–	4.4	A	
V_{SD}	Diode Forward Voltage ②	IRFD120, 1	–	–	2.5	V	T_C = 25°C, I_S = 1.3A, V_{GS} = 0V
		IRFD122, 3	–	–	2.3	V	T_C = 25°C, I_S = 1.1A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 1.3A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 1.3A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

IRFD120, IRFD121, IRFD122, IRFD123

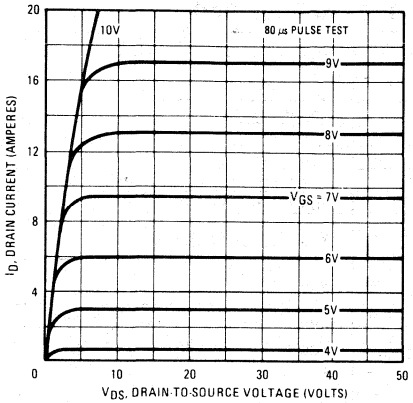


Fig. 1 — Typical Output Characteristics

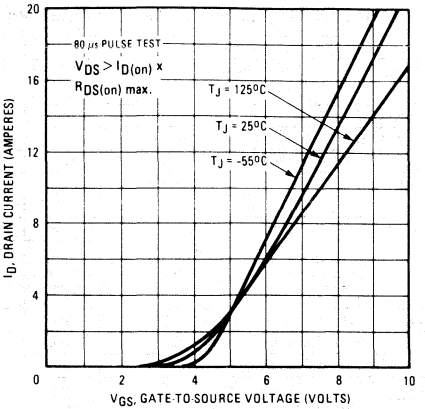


Fig. 2 — Typical Transfer Characteristics

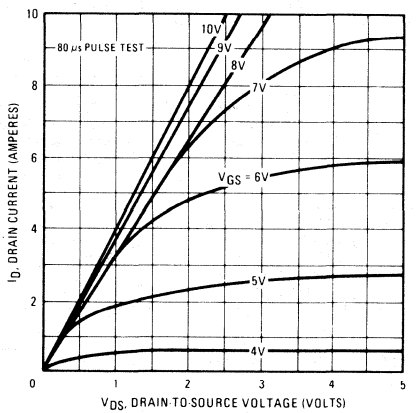


Fig. 3 — Typical Saturation Characteristics

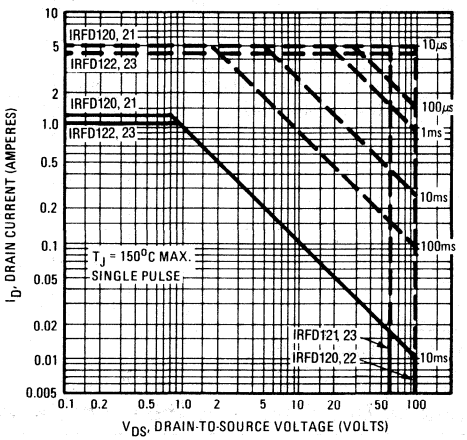


Fig. 4 — Maximum Safe Operating Area

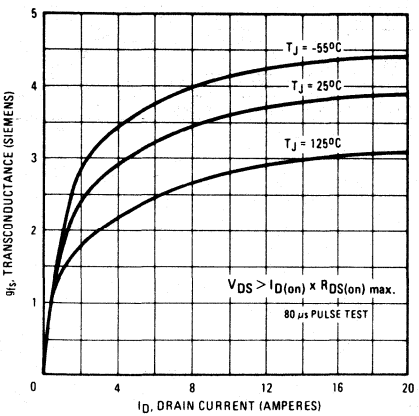


Fig. 5 — Typical Transconductance Vs. Drain Current

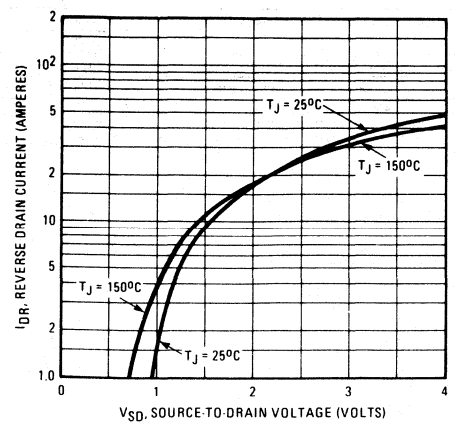


Fig. 6 — Typical Source-Drain Diode Forward Voltage

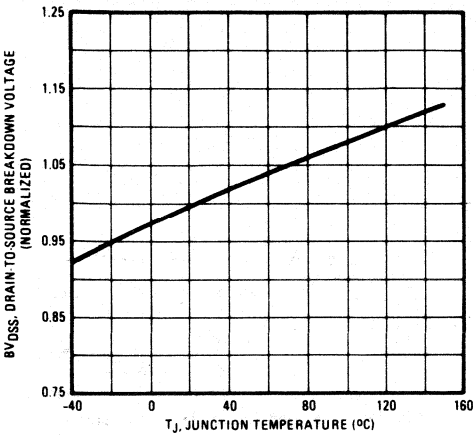


Fig. 7 — Breakdown Voltage Vs. Temperature

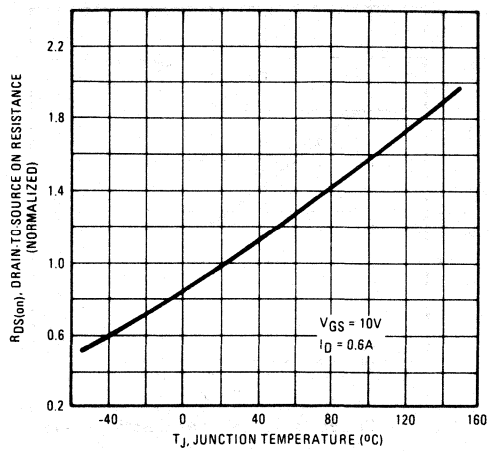


Fig. 8 — Normalized On-Resistance Vs. Temperature

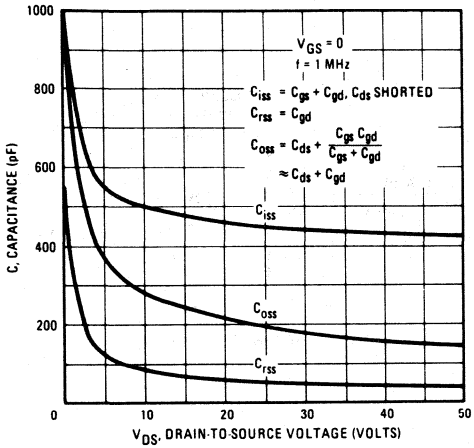


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

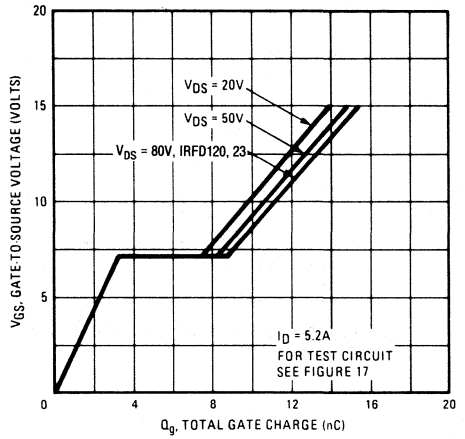


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

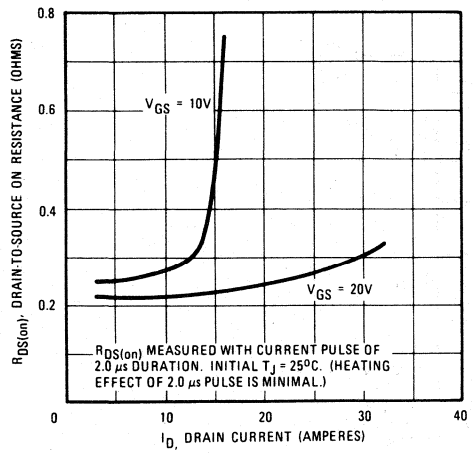


Fig. 11 — Typical On-Resistance Vs. Drain Current

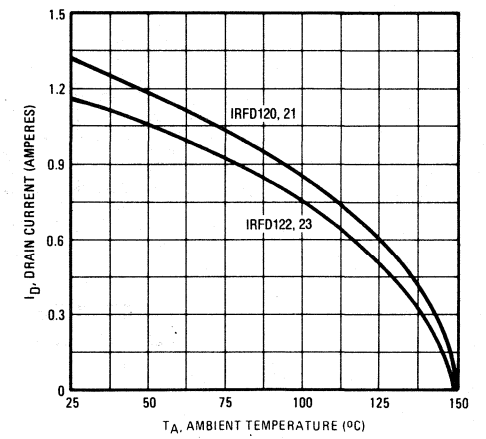


Fig. 12 — Maximum Drain Current Vs. Case Temperature

IRFD120, IRFD121, IRFD122, IRFD123

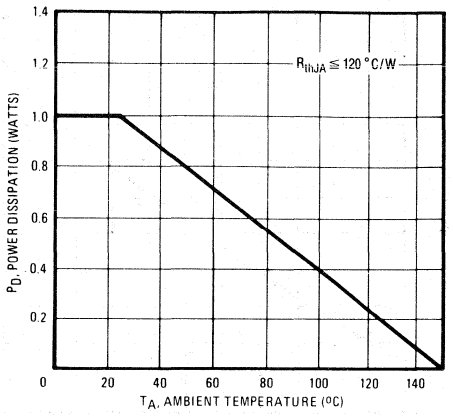


Fig. 13 – Power Vs. Temperature Derating Curve

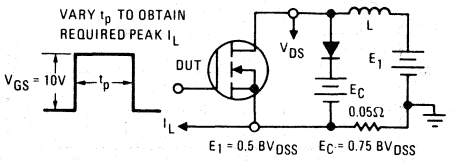


Fig. 14 – Clamped Inductive Test Circuit

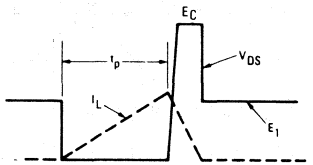


Fig. 15 – Clamped Inductive Waveforms

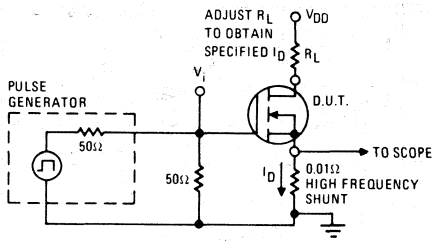


Fig. 16 – Switching Time Test Circuit

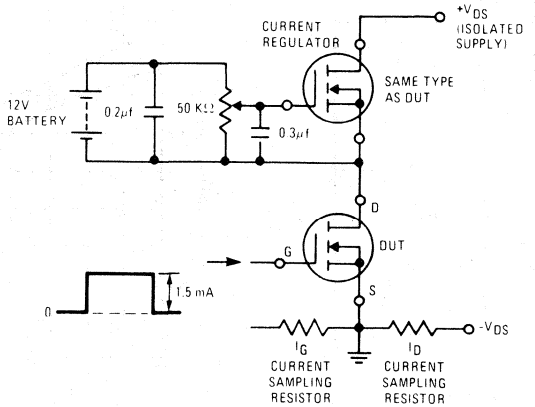


Fig. 17 – Gate Charge Test Circuit

File Number **2313**

IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

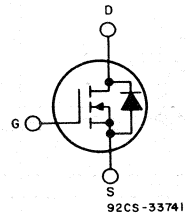
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.4 A and 0.5 A, 60 V - 100 V
$r_{DS(on)}$ = 2.4 Ω and 3.2 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

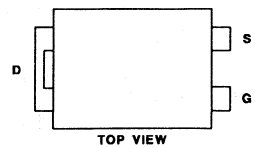


TERMINAL DIAGRAM

The IRFD1Z0, IRFD1Z1, IRFD1Z2, and IRFD1Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-pin DIP package.

TERMINAL DESIGNATION



4-PIN DIP

ABSOLUTE MAXIMUM RATINGS

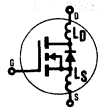
	Parameter	IRFD1Z0	IRFD1Z1	IRFD1Z2	IRFD1Z3	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_A = 25°C	Continuous Drain Current	0.5	0.5	0.4	0.4	A
I_{DM}	Pulsed Drain Current	4.0	4.0	3.2	3.2	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100 μH				A
		4.0	4.0	3.2	3.2	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD1Z0, 2	100	–	–	V	V_{GS} = 0V
		IRFD1Z1, 3	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD1Z0, 1	0.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD1Z2, 3	0.4	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD1Z0, 1	–	2.2	2.4	Ω	V_{GS} = 10V, I_D = 0.25A
		IRFD1Z2, 3	–	2.8	3.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.25	0.35	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.25A
C_{iss}	Input Capacitance	ALL	–	50	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	20	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	5.0	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.25A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	2.0	3.0	nC	V_{GS} = 10V, I_D = 1.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	1.0	1.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	1.0	1.5	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD1Z0, 1	–	–	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD1Z2, 3	–	–	0.4	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD1Z0, 1	–	–	4.0	A	
		IRFD1Z2, 3	–	–	3.2	A	
V_{SD}	Diode Forward Voltage ②	IRFD1Z0, 1	–	–	1.4	V	T_A = 25°C, I_S = 0.5A, V_{GS} = 0V
		IRFD1Z2, 3	–	–	1.3	V	T_A = 25°C, I_S = 0.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	μC	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

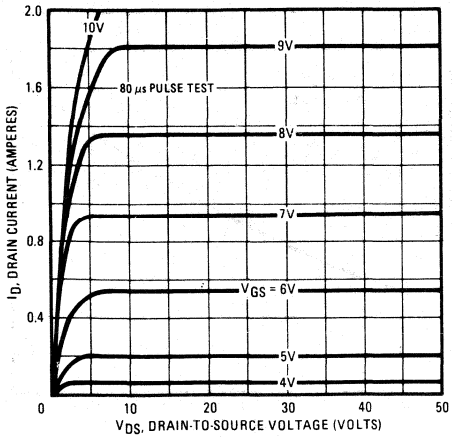


Fig. 1 — Typical Output Characteristics

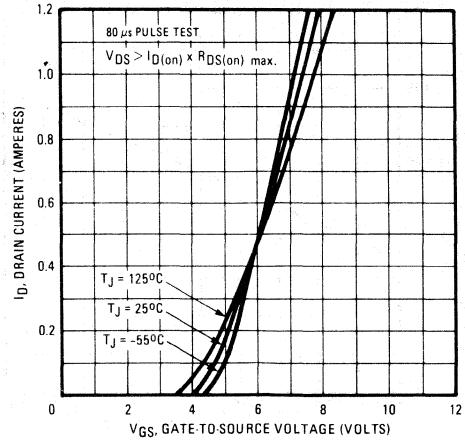


Fig. 2 — Typical Transfer Characteristics

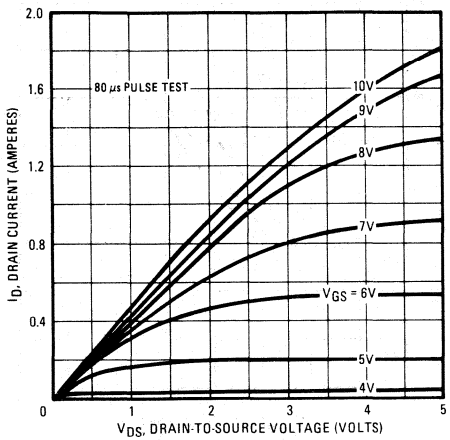


Fig. 3 — Typical Saturation Characteristics

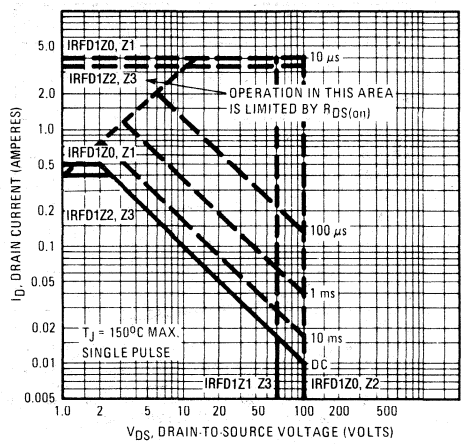


Fig. 4 — Maximum Safe Operating Area

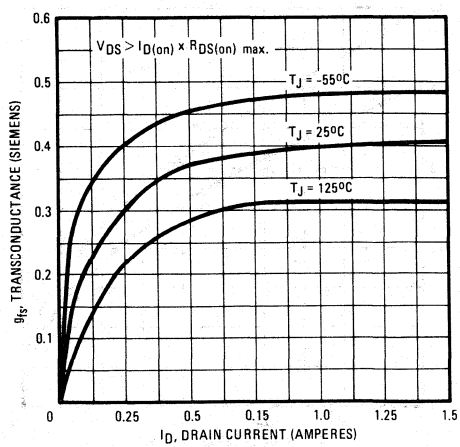


Fig. 5 — Typical Transconductance Vs. Drain Current

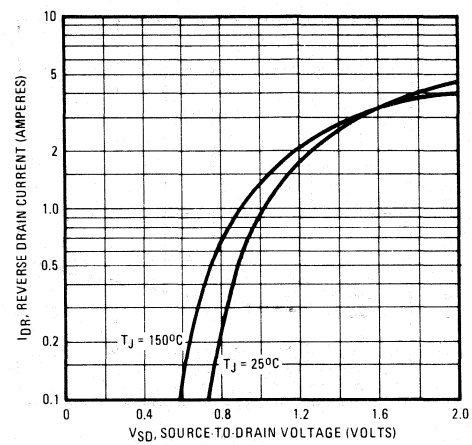


Fig. 6 — Typical Source-Drain Diode Forward Voltage

IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

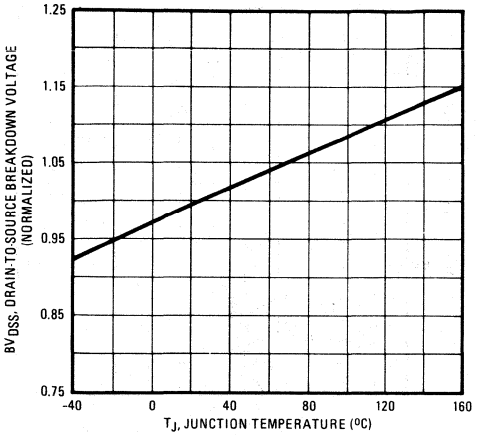


Fig. 7 — Breakdown Voltage Vs. Temperature

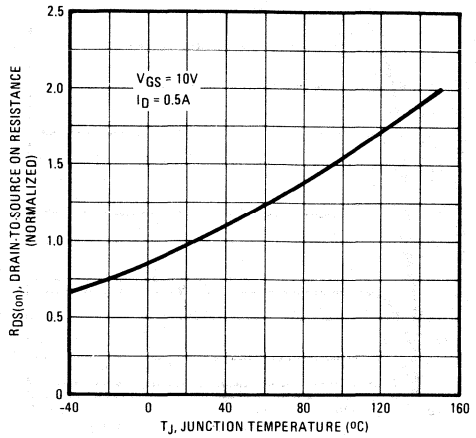


Fig. 8 — Normalized On-Resistance Vs. Temperature

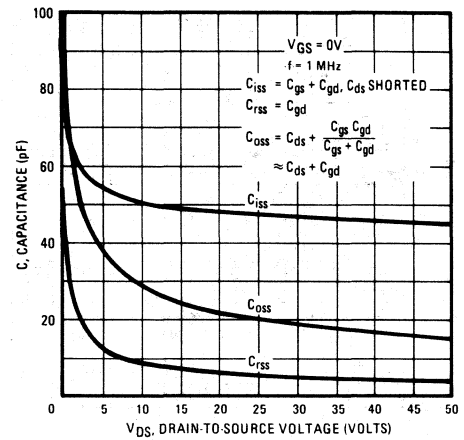


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

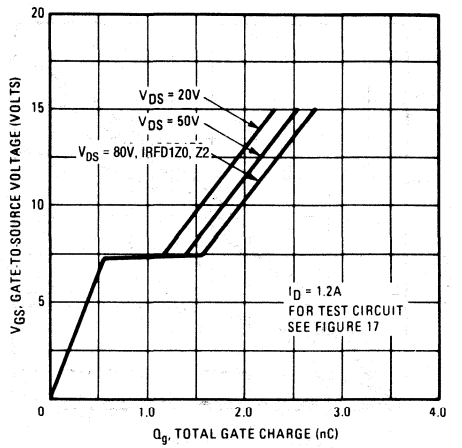


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

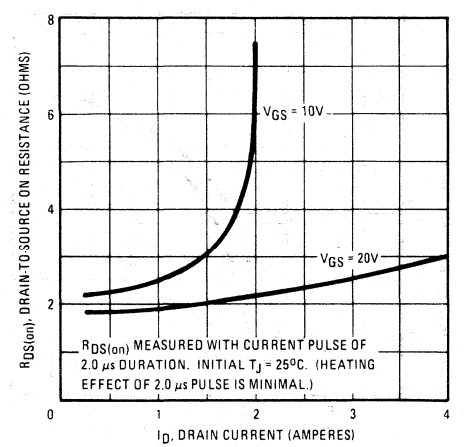


Fig. 11 — Typical On-Resistance Vs. Drain Current

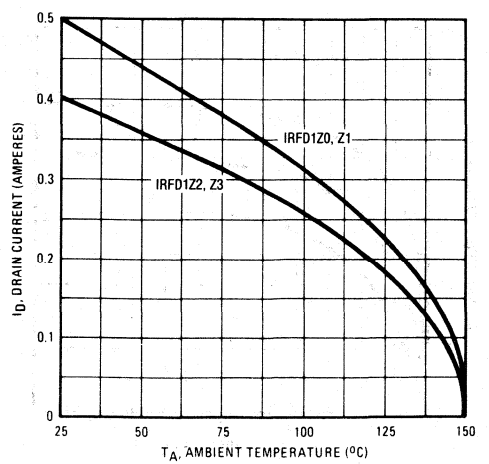


Fig. 12 — Maximum Drain Current Vs. Case Temperature

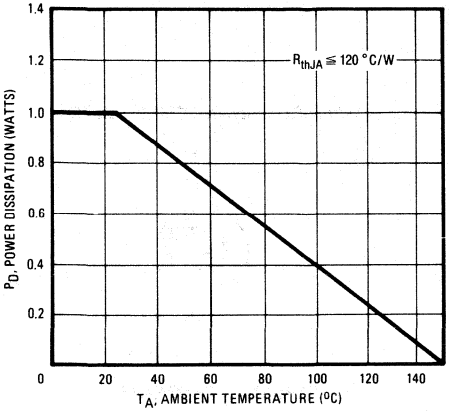


Fig. 13 – Power Vs. Temperature Derating Curve

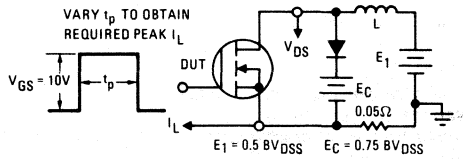


Fig. 14 – Clamped Inductive Test Circuit

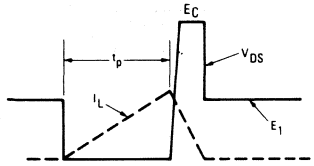


Fig. 15 – Clamped Inductive Waveforms

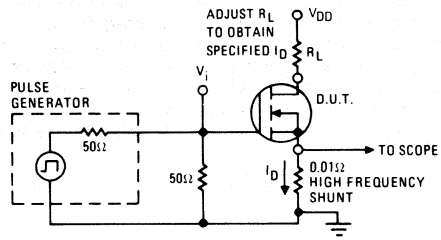


Fig. 16 – Switching Time Test Circuit

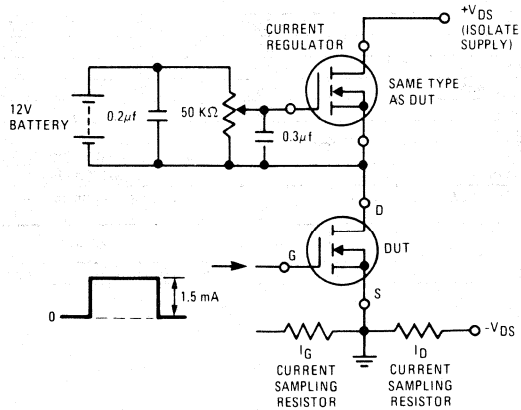


Fig. 17 – Gate Charge Test Circuit

IRFD210, IRFD211, IRFD212, IRFD213

File Number **2316**

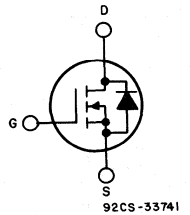
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.45 A and 0.6 A, 150 V - 200 V
$r_{DS(on)}$ = 1.5 Ω and 2.4 Ω

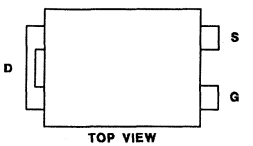
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



4-PIN DIP

The IRFD210, IRFD211, IRFD212, and IRFD213 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-pin DIP package.

Absolute Maximum Ratings

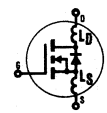
Parameter		IRFD210	IRFD211	IRFD212	IRFD213	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	200	150	200	150	V
I_D @ T_A = 25°C	Continuous Drain Current	0.6	0.6	0.45	0.45	A
I_{DM}	Pulsed Drain Current	2.5	2.5	1.8	1.8	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100 μH				A
		2.5	2.5	1.8	1.8	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD210, IRFD211, IRFD212, IRFD213

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFD210, 2	200	–	–	V	V_{GS} = 0V
		IRFD211, 3	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD210, 1	0.6	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD212, 3	0.45	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFD210, 1	–	1.0	1.5	Ω	V_{GS} = 10V, I_D = 0.3A
		IRFD212, 3	–	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	0.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.3A
C_{iss}	Input Capacitance	ALL	–	135	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	60	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	16	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	8.0	15	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.3A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	10	15	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	3.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD210, 1	–	–	0.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD212, 3	–	–	0.45	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD210, 1	–	–	2.5	A	
		IRFD212, 3	–	–	1.8	A	
V_{SD}	Diode Forward Voltage ②	IRFD210, 1	–	–	2.0	V	T_A = 25°C, I_S = 0.6A, V_{GS} = 0V
		IRFD212, 3	–	–	1.8	V	T_A = 25°C, I_S = 0.45A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	290	–	ns	T_J = 150°C, I_F = 0.6A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.0	–	μC	T_J = 150°C, I_F = 0.6A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

IRFD210, IRFD211, IRFD212, IRFD213

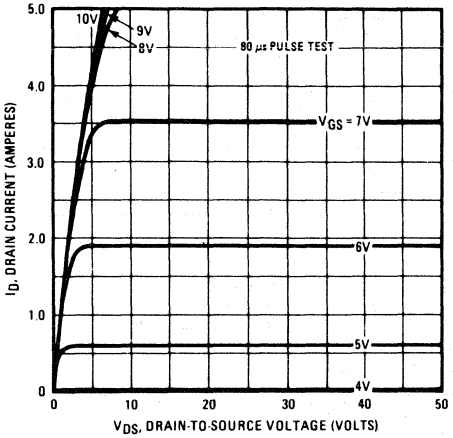


Fig. 1 — Typical Output Characteristics

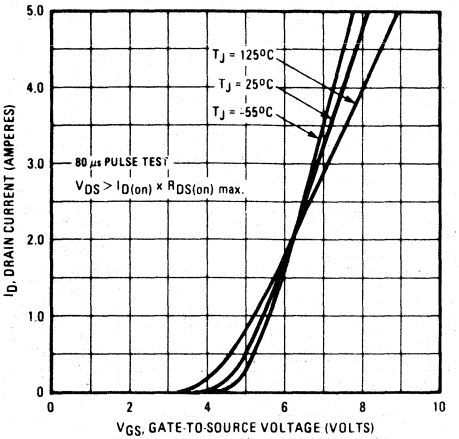


Fig. 2 — Typical Transfer Characteristics

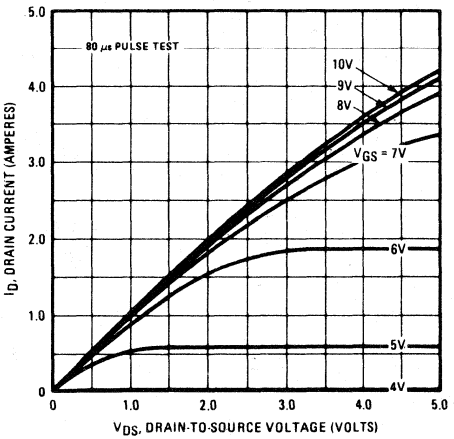


Fig. 3 — Typical Saturation Characteristics

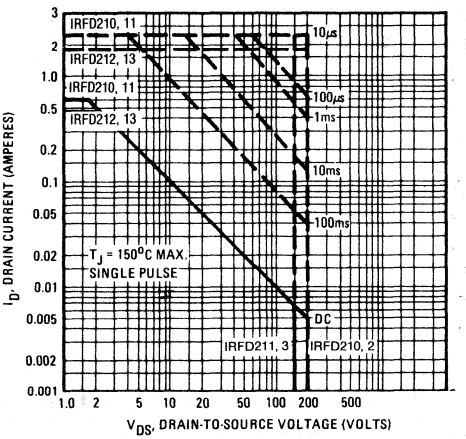


Fig. 4 — Maximum Safe Operating Area

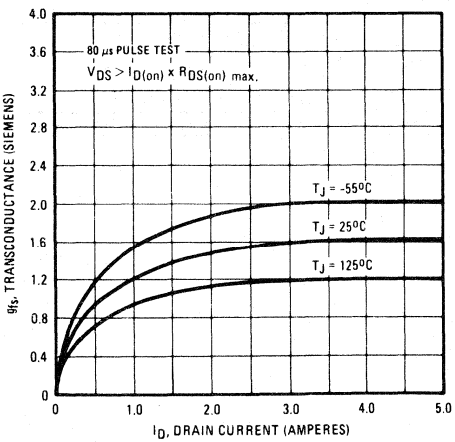


Fig. 5 — Typical Transconductance Vs. Drain Current

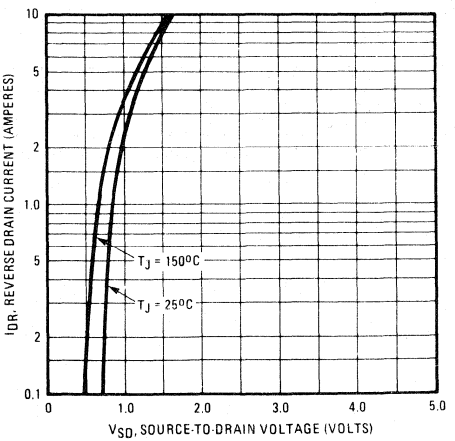


Fig. 6 — Typical Source-Drain Diode Forward Voltage

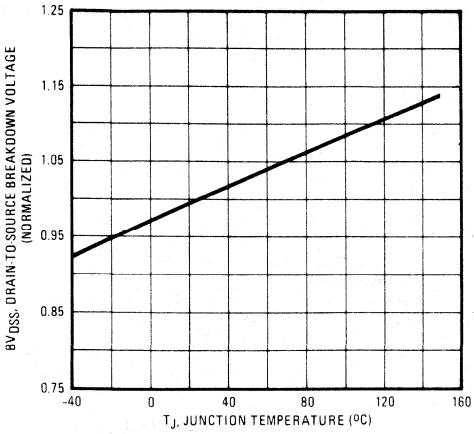


Fig. 7 — Breakdown Voltage Vs. Temperature

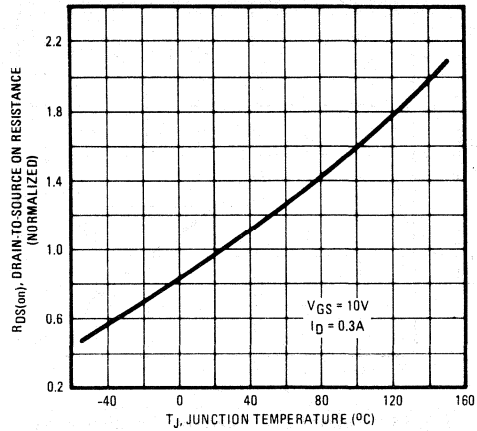


Fig. 8 — Normalized On-Resistance Vs. Temperature

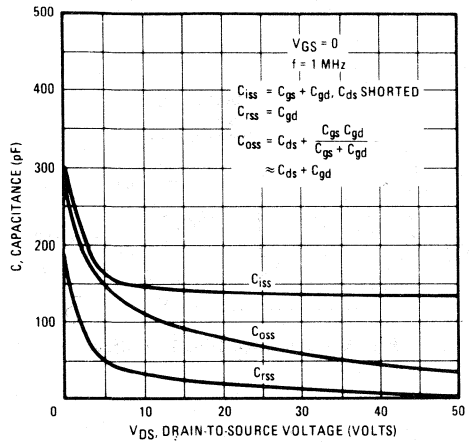


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

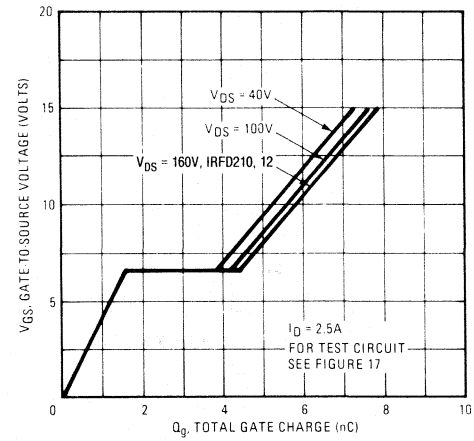


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

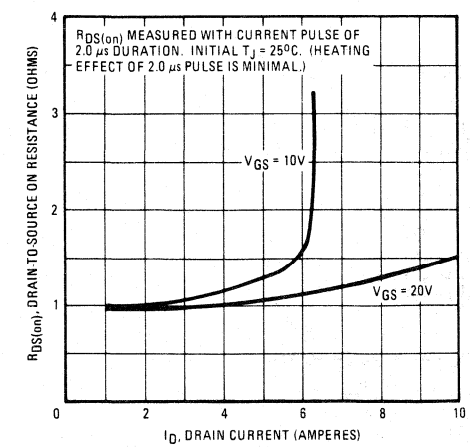


Fig. 11 — Typical On-Resistance Vs. Drain Current

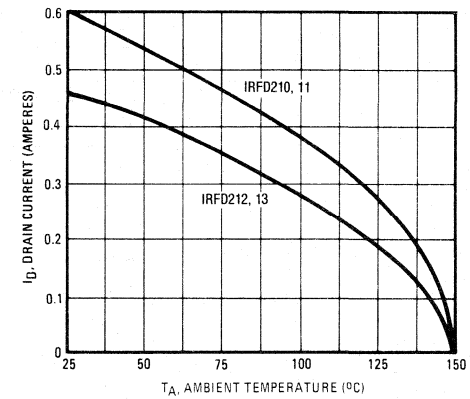


Fig. 12 — Maximum Drain Current Vs. Case Temperature

IRFD210, IRFD211, IRFD212, IRFD213

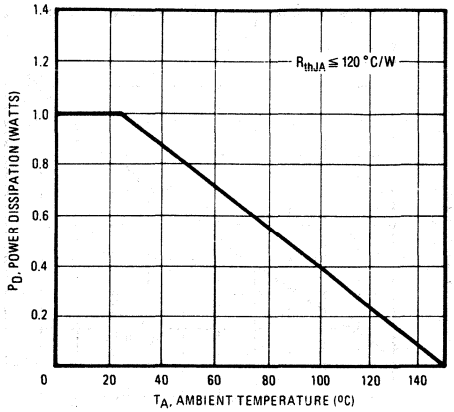


Fig. 13 – Power Vs. Temperature Derating Curve

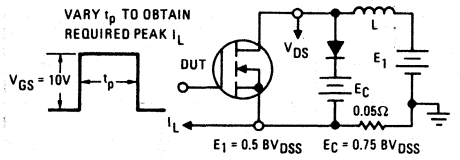


Fig. 14 – Clamped Inductive Test Circuit

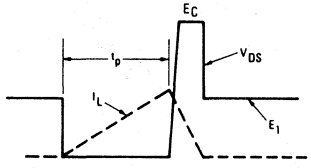


Fig. 15 – Clamped Inductive Waveforms

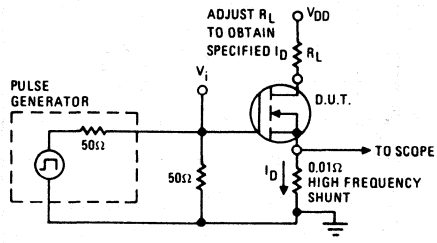


Fig. 16 – Switching Time Test Circuit

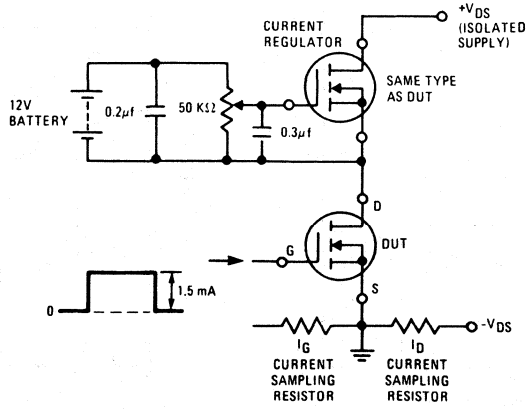


Fig. 17 – Gate Charge Test Circuit

File Number **2317**

IRFD220, IRFD221, IRFD222, IRFD223

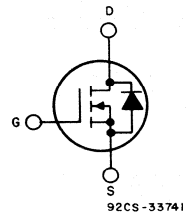
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.7 A and 0.8 A, 150 V - 200 V
$r_{DS(on)}$ = 0.8 Ω and 1.2 Ω

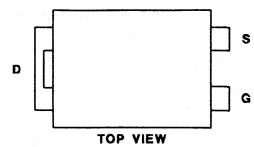
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



TOP VIEW

4-PIN DIP

The IRFD220, IRFD221, IRFD222, and IRFD223 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-pin DIP package.

Absolute Maximum Ratings

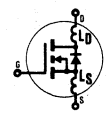
	Parameter	IRFD220	IRFD221	IRFD222	IRFD223	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	200	150	200	150	V
I_D @ T_A = 25°C	Continuous Drain Current	0.8	0.8	0.7	0.7	A
I_{DM}	Pulsed Drain Current	6.4	6.4	5.6	5.6	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100 μH				A
		6.4	6.4	5.6	5.6	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD220, IRFD221, IRFD222, IRFD223

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD220, 2	200	–	–	V	V_{GS} = 0V
		IRFD221, 3	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD220, 1	0.8	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD222, 3	0.7	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD220, 1	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 0.4A
		IRFD222, 3	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.1	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.4A
C_{iss}	Input Capacitance	ALL	–	450	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	150	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5BV_{DSS}, I_D = 0.4A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	5.0	7.5	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD220, 1	–	–	0.8	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD222, 3	–	–	0.7	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD220, 1	–	–	6.4	A	
		IRFD222, 3	–	–	5.6	A	
V_{SD}	Diode Forward Voltage ②	IRFD220, 1	–	–	2.0	V	T_A = 25°C, I_S = 0.8A, V_{GS} = 0V
		IRFD222, 3	–	–	1.8	V	T_A = 25°C, I_S = 0.7A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	150	–	ns	T_J = 150°C, I_F = 0.8A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.6	–	μC	T_J = 150°C, I_F = 0.8A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

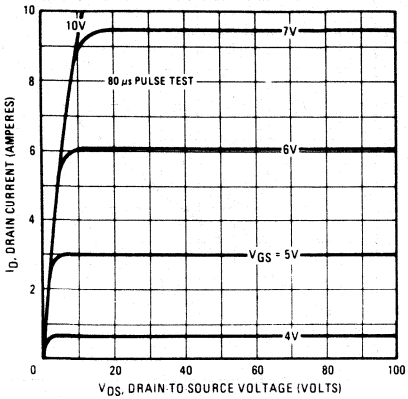


Fig. 1 – Typical Output Characteristics

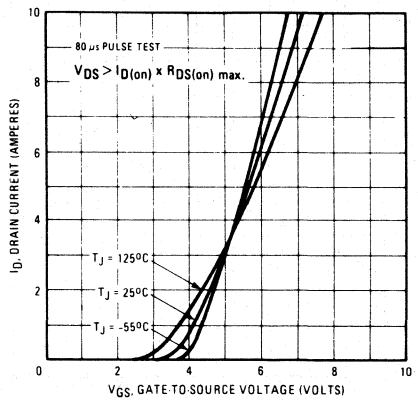


Fig. 2 – Typical Transfer Characteristics

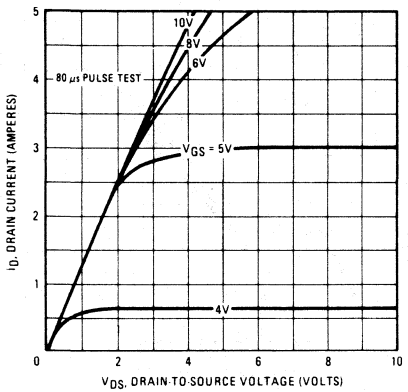


Fig. 3 – Typical Saturation Characteristics

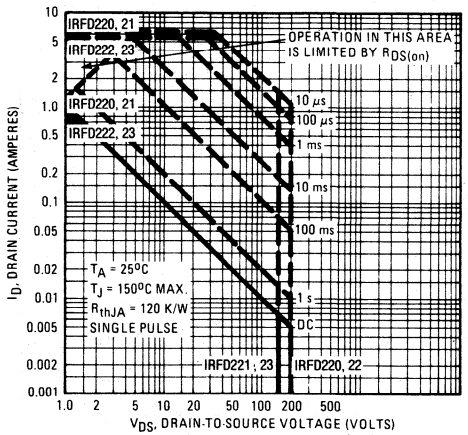


Fig. 4 – Maximum Safe Operating Area

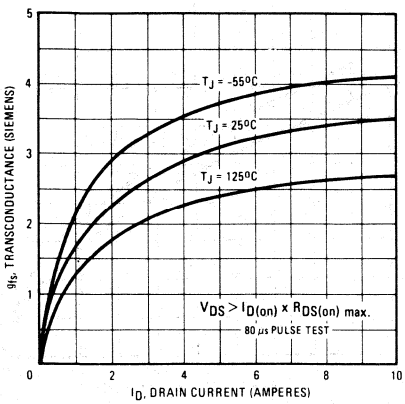


Fig. 5 – Typical Transconductance Vs. Drain Current

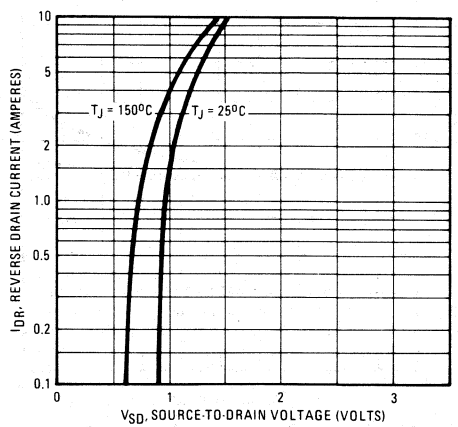


Fig. 6 – Typical Source-Drain Diode Forward Voltage

IRFD220, IRFD221, IRFD222, IRFD223

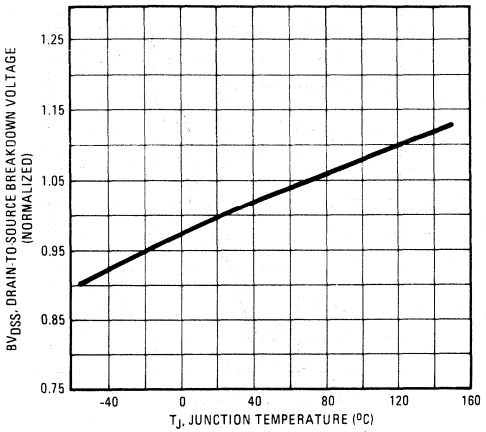


Fig. 7 — Breakdown Voltage Vs. Temperature

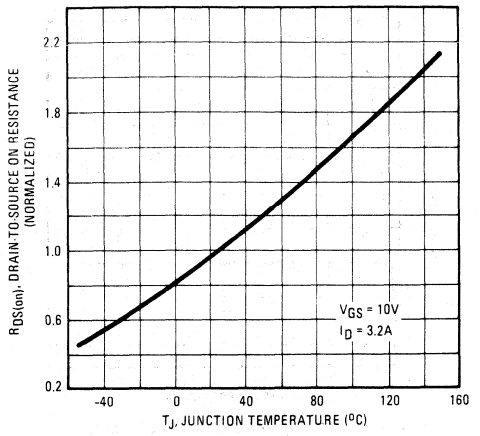


Fig. 8 — Normalized On-Resistance Vs. Temperature

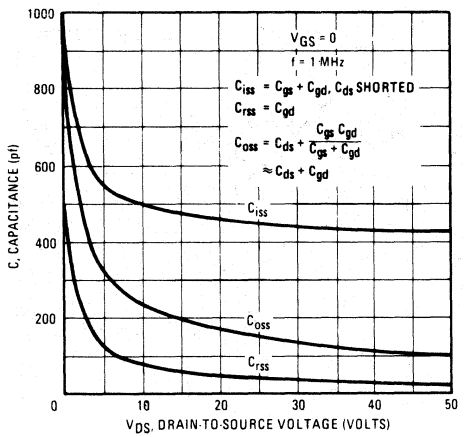


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

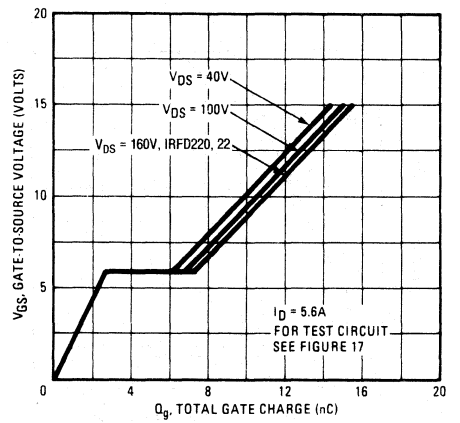


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

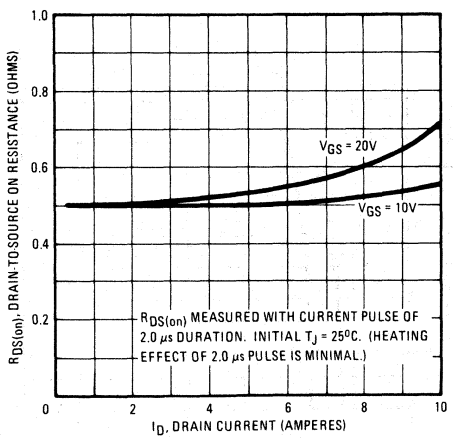


Fig. 11 — Typical On-Resistance Vs. Drain Current

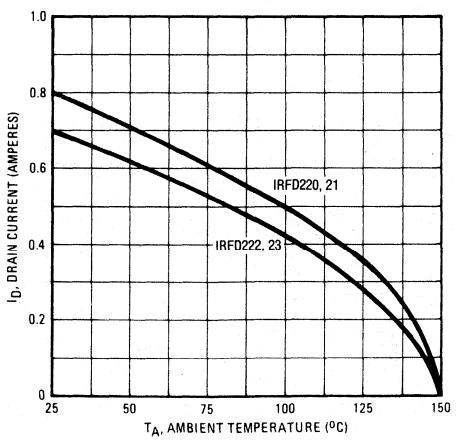


Fig. 12 — Maximum Drain Current Vs. Case Temperature

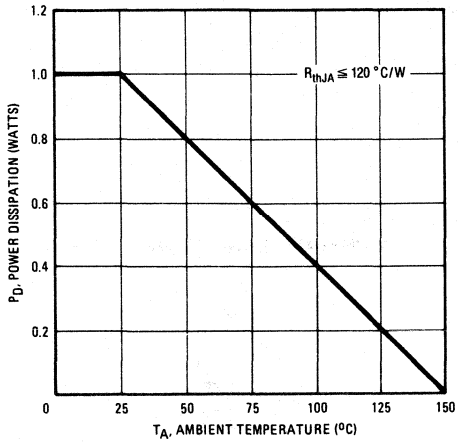


Fig. 13 – Power Vs. Temperature Derating Curve

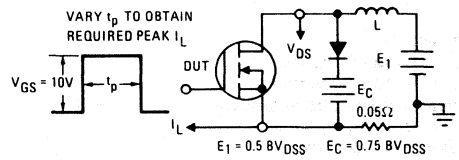


Fig. 14 – Clamped Inductive Test Circuit

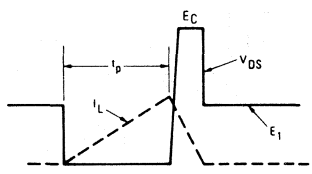


Fig. 15 – Clamped Inductive Waveforms

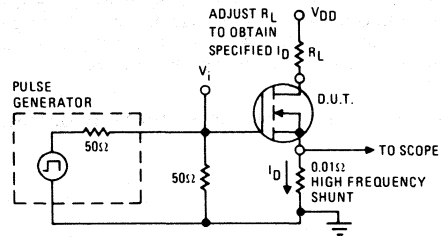


Fig. 16 – Switching Time Test Circuit

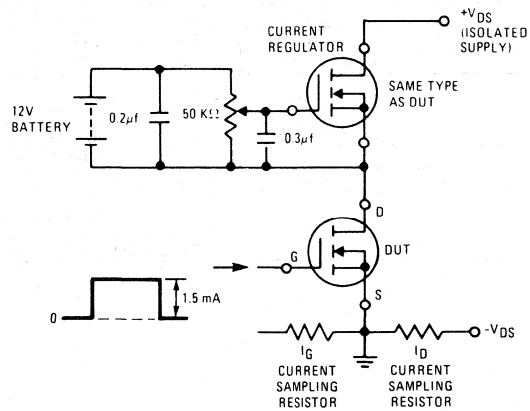


Fig. 17 – Gate Charge Test Circuit

IRFD2Z0, IRFD2Z1, IRFD2Z2, IRFD2Z3

File Number **2329**

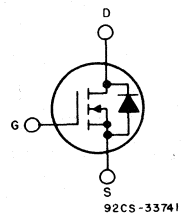
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.30 A and 0.32 A, 150 V - 200 V
$r_{DS(on)}$ = 5.0 Ω and 6.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

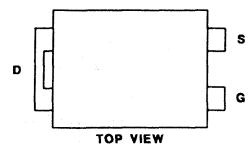


TERMINAL DIAGRAM

The IRFD2Z0, IRFD2Z1, IRFD2Z2, and IRFD2Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-pin DIP package.

TERMINAL DESIGNATION



4-PIN DIP

ABSOLUTE-MAXIMUM RATINGS

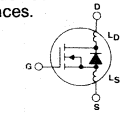
CHARACTERISTIC		IRFD2Z0	IRFD2Z1	IRFD2Z2	IRFD2Z3	UNITS
Drain-Source Voltage ①	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	200	150	200	150	V
Continuous Drain Current	I_D @ T_C = 25°C	0.32	0.32	0.30	0.30	A
Pulsed Drain Current	I_{DM}	1.5	1.5	1.4	1.4	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	1.0 (See Fig. 13)				W
Linear Derating Factor		0.008 (See Fig. 13)				W/°C
Inductive Current, Clamped ③	I_{LM}	1.5	1.5	1.4	1.4	A
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

IRFD2Z0, IRFD2Z1, IRFD2Z2, IRFD2Z3

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFD2Z0 IRFD2Z2	200	—	—	V	V_{GS} = 0 V
		IRFD2Z1 IRFD2Z3	150	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125° C
On-State Drain Current ②	$I_{D(on)}$	IRFD2Z0 IRFD2Z1	0.32	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFD2Z2 IRFD2Z3	0.30	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFD2Z0 IRFD2Z1	—	4.6	5.0	Ω	V_{GS} = 10 V, I_D = 0.15 A
		IRFD2Z2 IRFD2Z3	—	5.7	6.5	Ω	
Forward Transconductance ②	g_{fs}	ALL	0.6	0.11	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = 0.15 A
Input Capacitance	C_{iss}	ALL	—	37	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 9
Output Capacitance	C_{oss}	ALL	—	15	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	4.0	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	15	—	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 0.15 A, Z_O = 50 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	10	—	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	22	—	ns	
Fall Time	t_f	ALL	—	28	—	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	2.5	4.0	nC	V_{GS} = 10 V, I_D = 1.5 A, V_{DS} = 0.8 V Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	1.5	2.8	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	1.5	2.8	nC	
Internal Drain Inductance	L_D	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

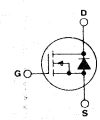


THERMAL RESISTANCE

Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	120	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFD2Z0 IRFD2Z1	—	—	0.32	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD2Z2 IRFD2Z3	—	—	0.30	A	
Pulse Source Current (Body Diode)	I_{SM}	IRFD2Z0 IRFD2Z1	—	—	1.5	A	
		IRFD2Z2 IRFD2Z3	—	—	1.4	A	
Diode Forward Voltage ②	V_{SD}	IRFD2Z0 IRFD2Z1	—	—	1.3	V	T_C = 25° C, I_S = 0.32 A, V_{GS} = 0 V
		IRFD2Z2 IRFD2Z3	—	—	1.3	V	T_C = 25° C, I_S = 0.30 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	125	—	ns	T_J = 150° C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.2	—	μC	T_J = 150° C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25° C to 150° C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ (See Fig. 14 and 15) L = 100 μH

IRFD2Z0, IRFD2Z1, IRFD2Z2, IRFD2Z3

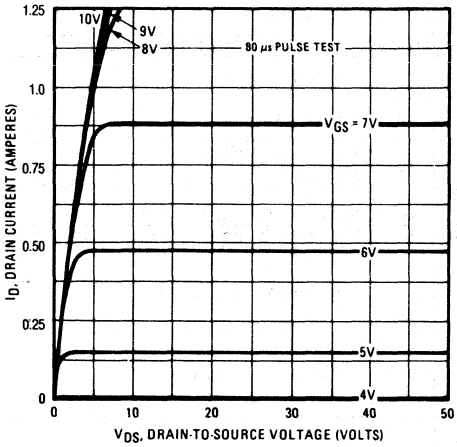


Fig. 1 — Typical Output Characteristics

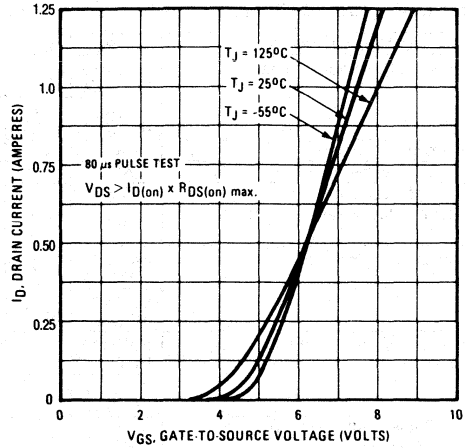


Fig. 2 — Typical Transfer Characteristics

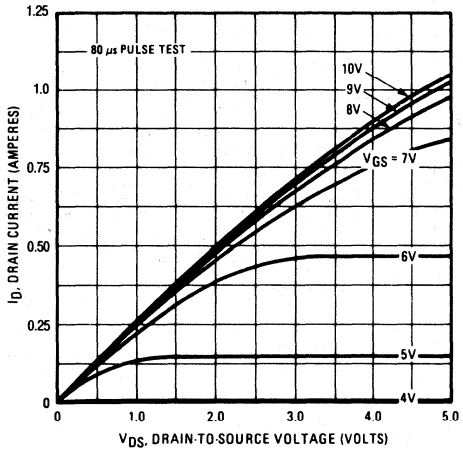


Fig. 3 — Typical Saturation Characteristics

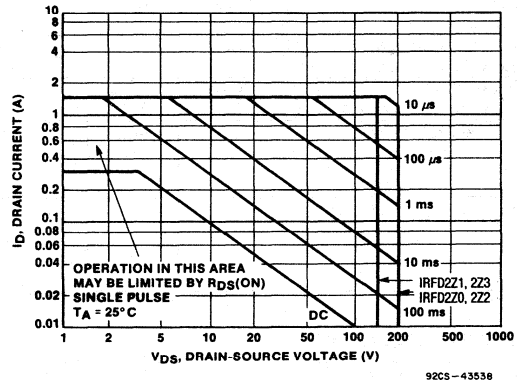


Fig. 4 — Maximum Safe Operating Area

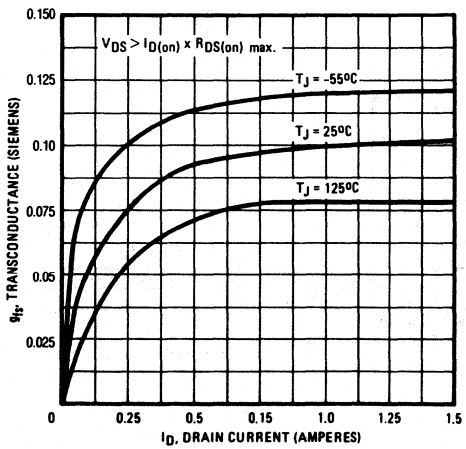


Fig. 5 — Typical Transconductance Vs. Drain Current

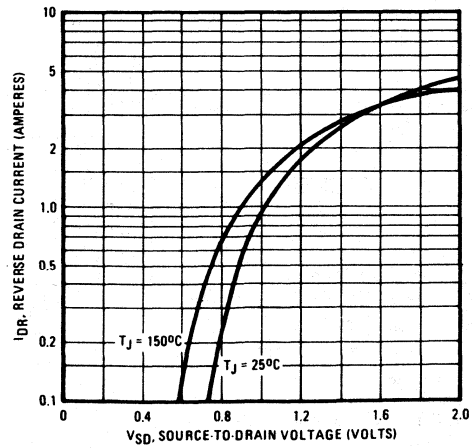


Fig. 6 — Typical Source-Drain Diode Forward Voltage

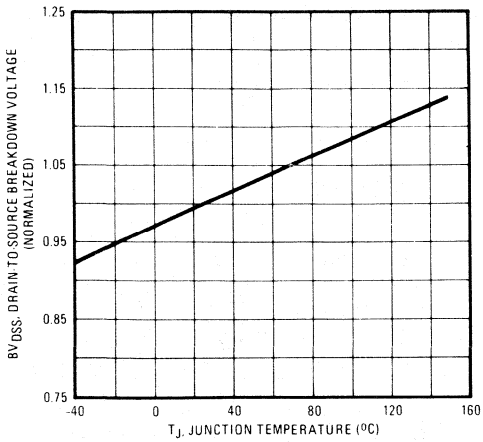


Fig. 7 — Breakdown Voltage Vs. Temperature

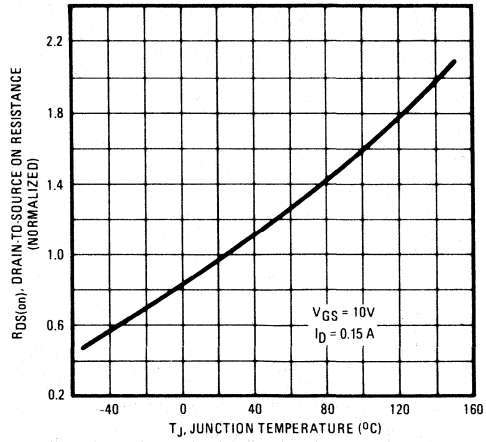


Fig. 8 — Normalized On-Resistance Vs. Temperature

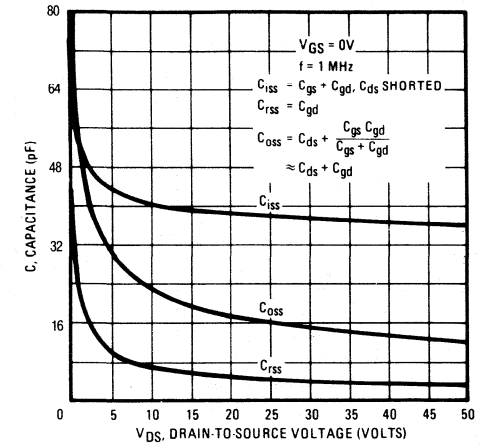


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

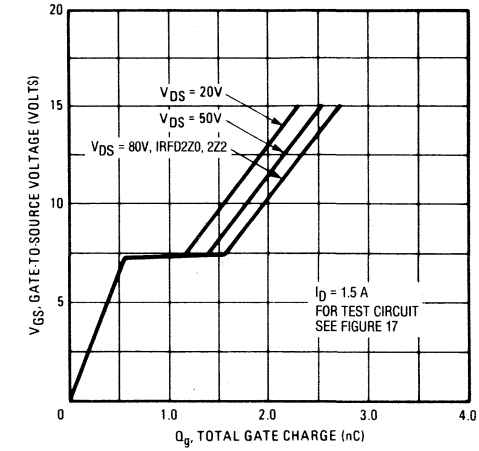


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

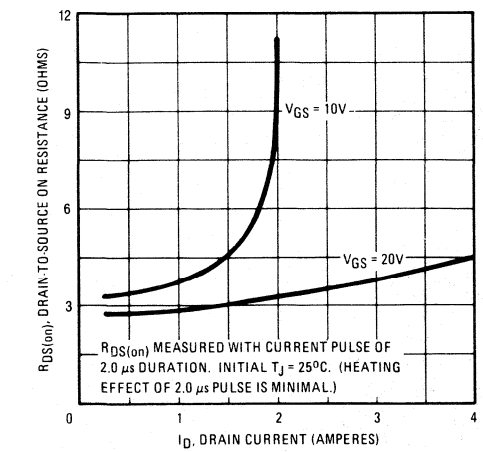


Fig. 11 — Typical On-Resistance Vs. Drain Current

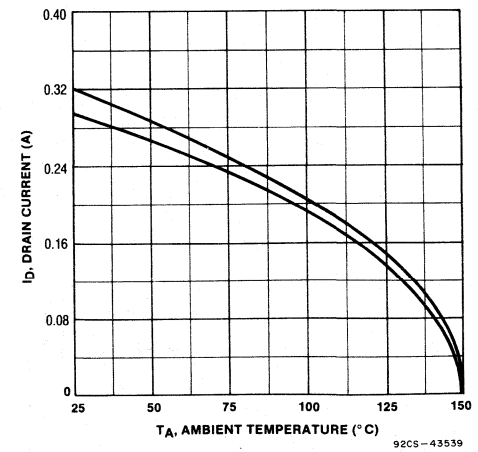


Fig. 12 — Maximum Drain Current Vs. Case Temperature

IRFD2Z0, IRFD2Z1, IRFD2Z2, IRFD2Z3

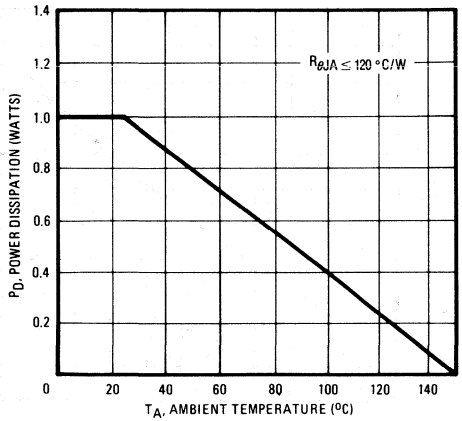


Fig. 13 – Power Vs. Temperature Derating Curve

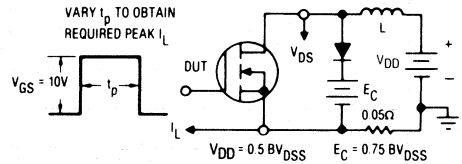


Fig. 14 — Clamped Inductive Test Circuit

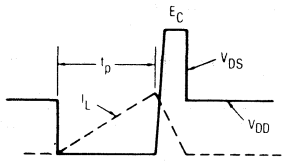


Fig. 15 — Clamped Inductive Waveforms

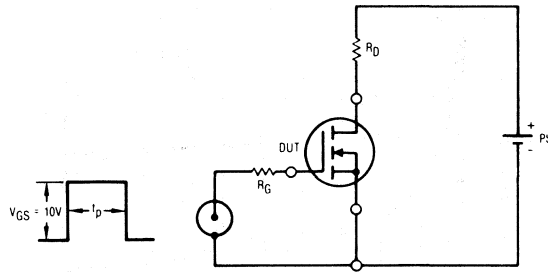


Fig. 16 – Switching Time Test Circuit

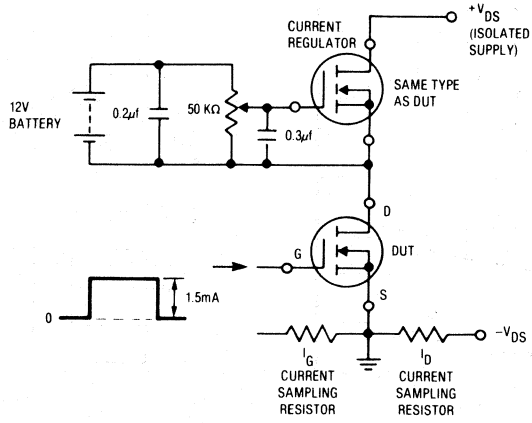


Fig. 17 — Gate Charge Test Circuit

File Number **2325**

IRFD310, IRFD311, IRFD312, IRFD313

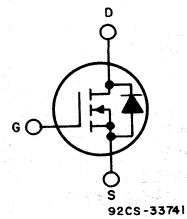
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.3 A and 0.4 A, 350 V - 400 V
$r_{DS(on)}$ = 3.6 Ω and 5.0 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

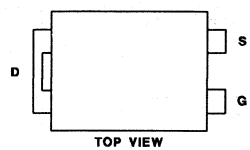


TERMINAL DIAGRAM

The IRFD310, IRFD311, IRFD312, and IRFD313 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

TERMINAL DESIGNATION



4-PIN DIP

Absolute Maximum Ratings

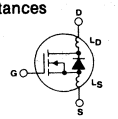
Parameter		IRFD310	IRFD311	IRFD312	IRFD313	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	0.4	0.4	0.3	0.3	A
I_{DM}	Pulsed Drain Current ③	1.6	1.6	1.2	1.2	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1 (See Fig. 14)				W
	Linear Derating Factor	0.008 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped ④	1.6	1.6	1.2	1.2	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD310, IRFD311, IRFD312, IRFD313

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD310 IRFD312	400	—	—	V	$V_{GS} = 0V$
		IRFD311 IRFD313	350	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRFD310 IRFD311	0.4	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRFD312 IRFD313	0.3	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD310 IRFD311	—	3.3	3.6	Ω	$V_{GS} = 10V$, $I_D = 0.2A$
		IRFD312 IRFD313	—	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 0.2A$
C_{iss}	Input Capacitance	ALL	—	135	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	35	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	8.0	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	3.0	10	ns	$V_{DD} \simeq 0.5BV_{DSS}$, $I_D = 0.2A$, $Z_0 = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	5.0	10	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	$V_{GS} = 10V$, $I_D = 0.4A$, $V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	3.0	4.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

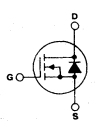


Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD310 IRFD311	—	—	0.4	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD312 IRFD313	—	—	0.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFD310 IRFD311	—	—	1.6	A	
		IRFD312 IRFD313	—	—	1.2	A	
V_{SD}	Diode Forward Voltage ②	IRFD310 IRFD311	—	—	1.6	V	$T_C = 25°C$, $I_S = 1.6A$, $V_{GS} = 0V$
		IRFD312 IRFD313	—	—	1.5	V	$T_C = 25°C$, $I_S = 1.2A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	$T_J = 150°C$, $I_F = 1.6A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.7	—	μC	$T_J = 150°C$, $I_F = 1.6A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ See figs. 14, 15. L = 100 μH.

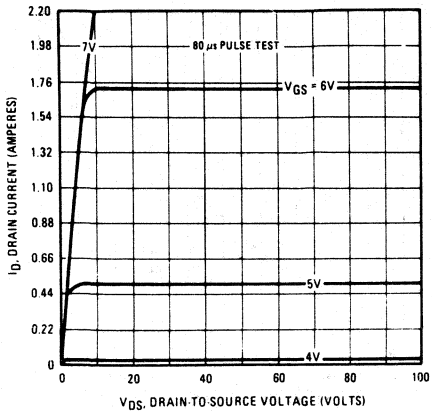


Fig. 1 — Typical Output Characteristics

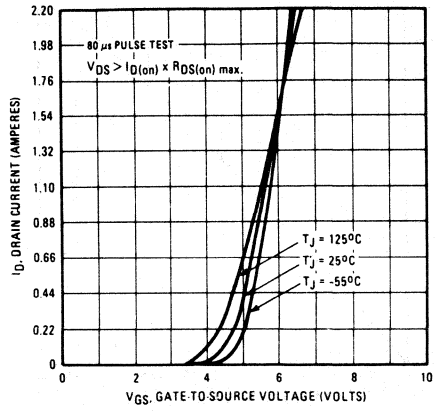


Fig. 2 — Typical Transfer Characteristics

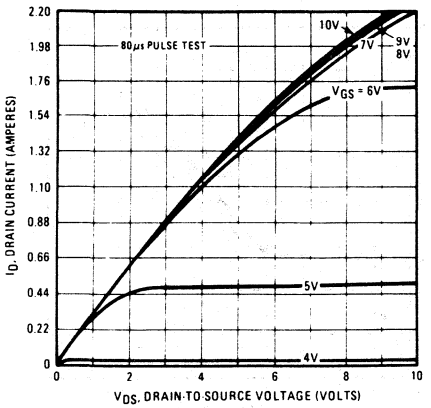


Fig. 3 — Typical Saturation Characteristics

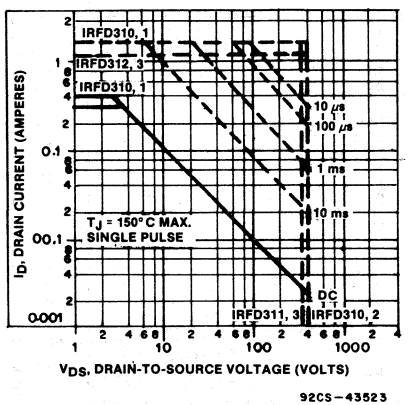


Fig. 4 — Maximum Safe Operating Area

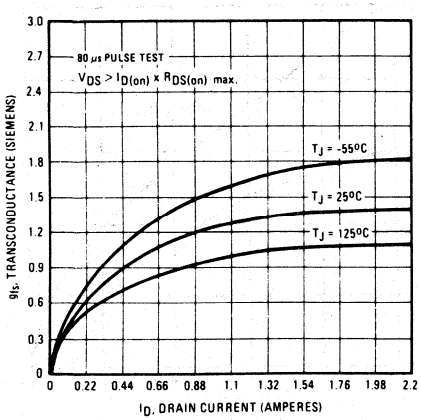


Fig. 5 — Typical Transconductance Vs. Drain Current

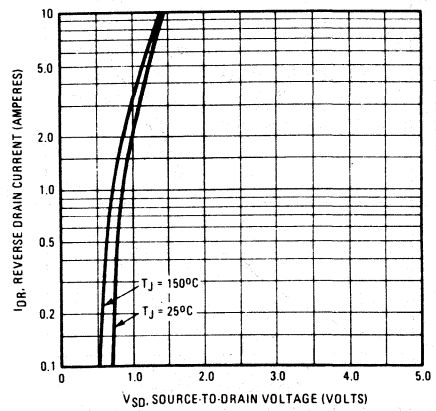


Fig. 6 — Typical Source-Drain Diode Forward Voltage

IRFD310, IRFD311, IRFD312, IRFD313

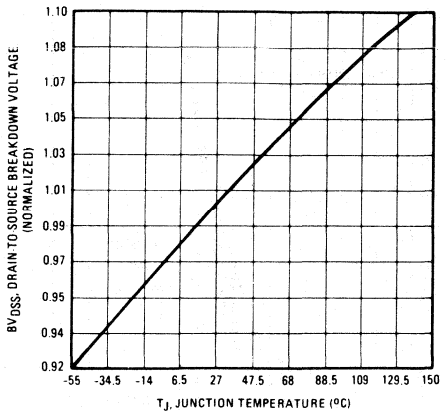


Fig. 7 — Breakdown Voltage Vs. Temperature

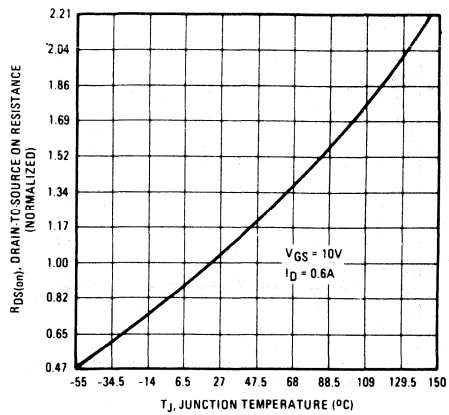


Fig. 8 — Normalized On-Resistance Vs. Temperature

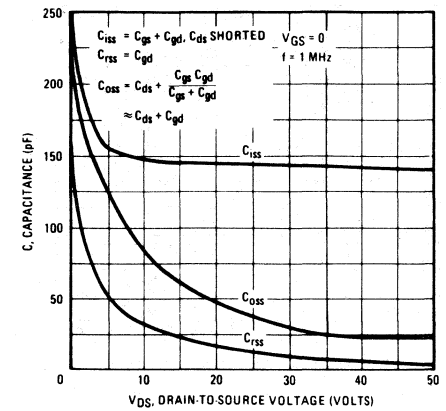


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

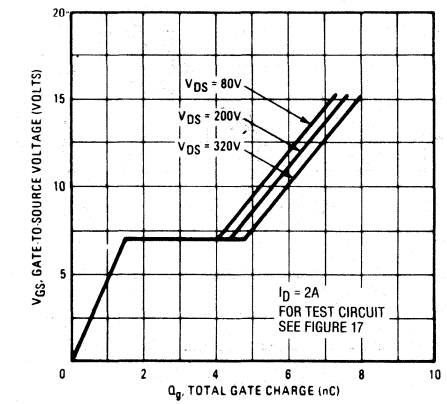


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

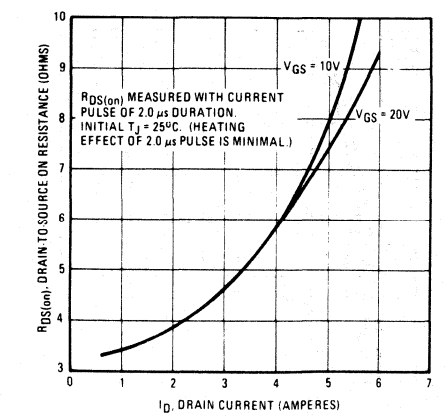


Fig. 11 — Typical On-Resistance Vs. Drain Current

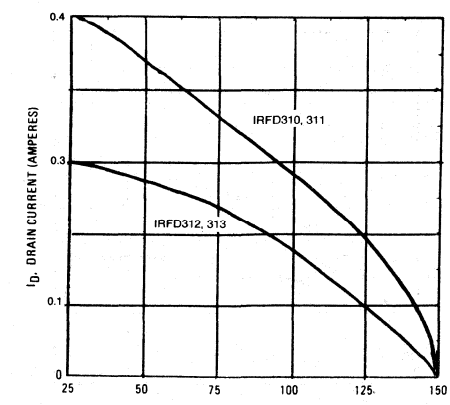
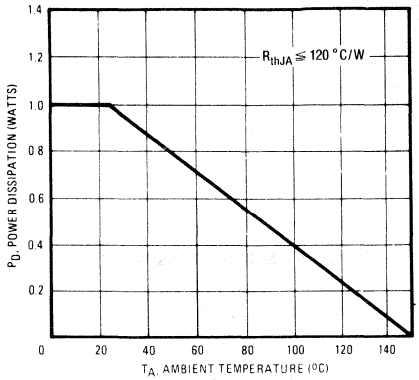


Fig. 12 — Maximum Drain Current Vs. Case Temperature



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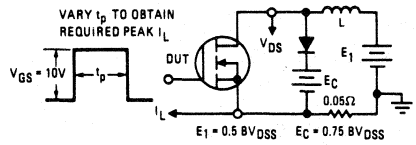


Fig. 14 — Clamped inductive test circuit.

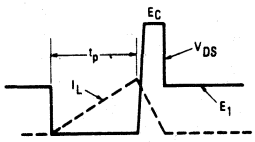


Fig. 15 — Clamped inductive waveforms.

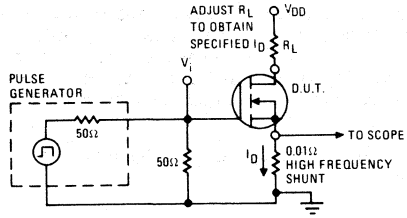


Fig. 16 — Switching Time Test Circuit

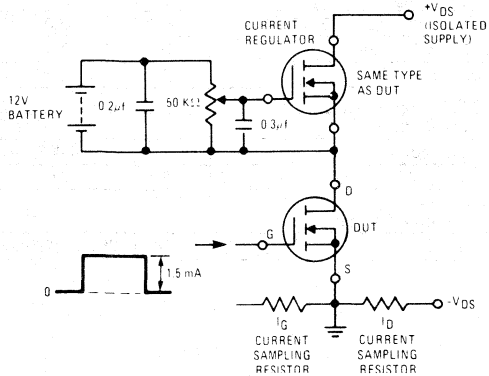


Fig. 17 — Gate Charge Test Circuit

IRFD320, IRFD321, IRFD322, IRFD323

File Number **2325**

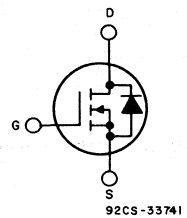
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.5 A and 0.4 A, 350 V – 400 V
$r_{DS(on)}$ = 1.8 Ω and 2.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

· **N-CHANNEL ENHANCEMENT MODE**

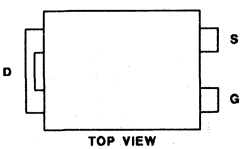


TERMINAL DIAGRAM

The IRFD320, IRFD321, IRFD322, and IRFD323 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

TERMINAL DESIGNATION



4-PIN DIP

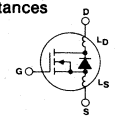
Absolute Maximum Ratings

Parameter		IRFD320	IRFD321	IRFD322	IRFD323	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	0.5	0.5	0.4	0.4	A
I_{DM}	Pulsed Drain Current ③	2.0	2.0	1.6	1.6	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
I_{LM}	Inductive Current, Clamped ④	2.0	2.0	1.6	1.6	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD320 IRFD322	400	—	—	V	V_{GS} = 0V
		IRFD321 IRFD323	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD320 IRFD321	0.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFD322 IRFD323	0.4	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD320 IRFD321	—	1.5	1.8	Ω	V_{GS} = 10V, I_D = 0.25A
		IRFD322 IRFD323	—	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.25A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \approx 0.5BV_{DSS}$, I_D = 0.25A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V_{GS} = 10V, I_D = 0.5A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

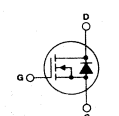


Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD320 IRFD321	—	—	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD322 IRFD323	—	—	0.4	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFD320 IRFD321	—	—	2.0	A	
		IRFD322 IRFD323	—	—	1.6	A	
V_{SD}	Diode Forward Voltage ②	IRFD320 IRFD321	—	—	1.6	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
		IRFD322 IRFD323	—	—	1.5	V	T_C = 25°C, I_S = 1.6A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ See figs. 14, 15. L = 100 μH.

IRFD320, IRFD321, IRFD322, IRFD323

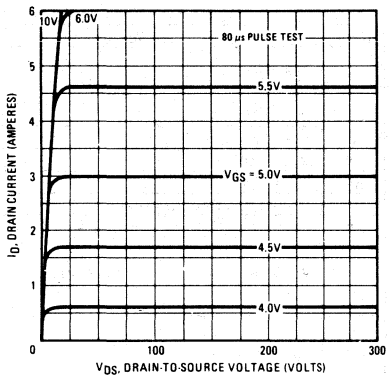


Fig. 1 — Typical Output Characteristics

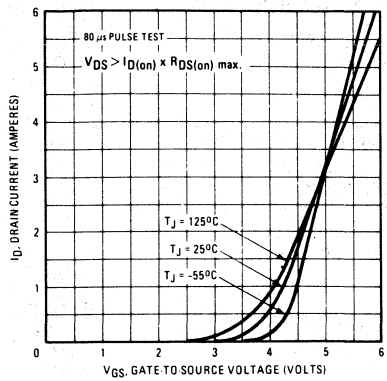


Fig. 2 — Typical Transfer Characteristics

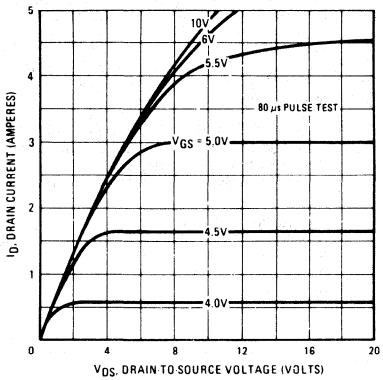


Fig. 3 — Typical Saturation Characteristics

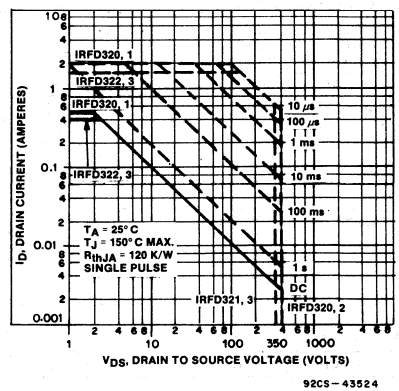


Fig. 4 — Maximum Safe Operating Area

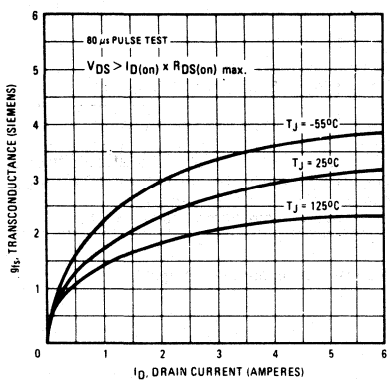


Fig. 5 — Typical Transconductance Vs. Drain Current

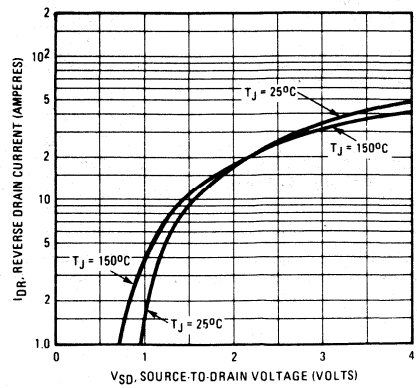


Fig. 6 — Typical Source-Drain Diode Forward Voltage

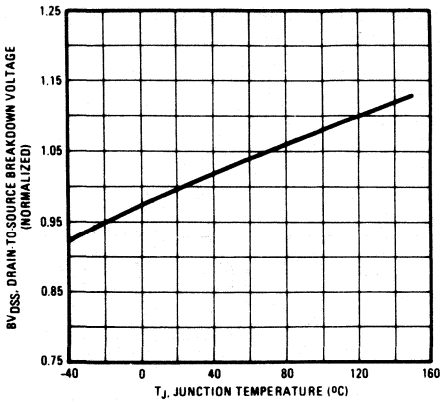


Fig. 7 — Breakdown Voltage Vs. Temperature

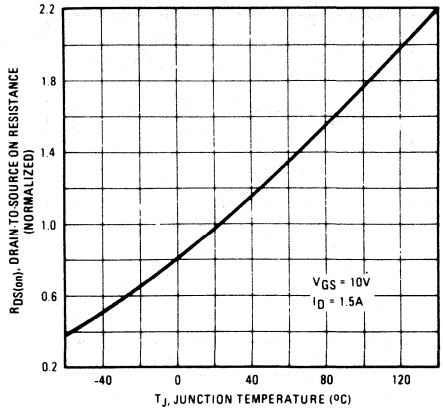


Fig. 8 — Normalized On-Resistance Vs. Temperature

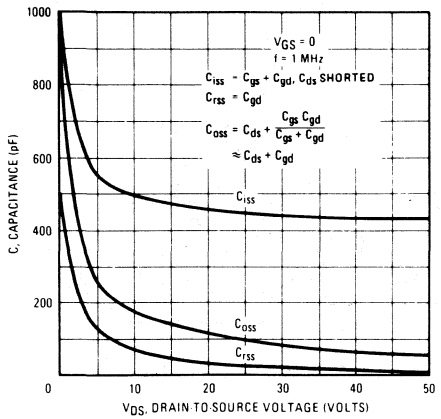


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

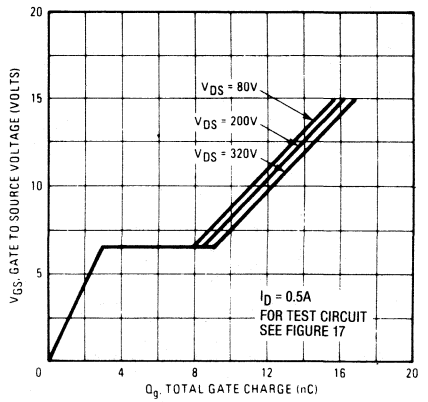


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

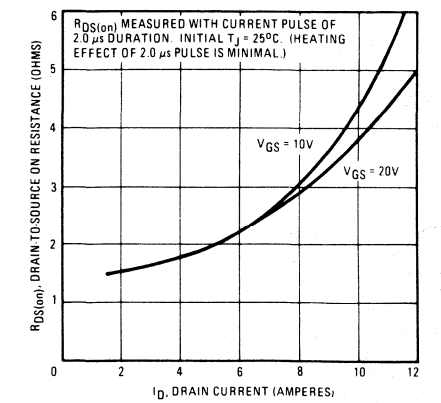


Fig. 11 — Typical On-Resistance Vs. Drain Current

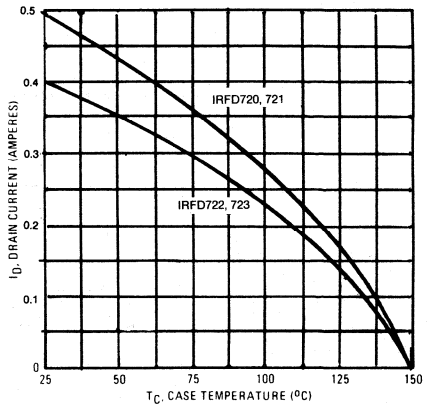


Fig. 12 — Maximum Drain Current Vs. Case Temperature

IRFD320, IRFD321, IRFD322, IRFD323

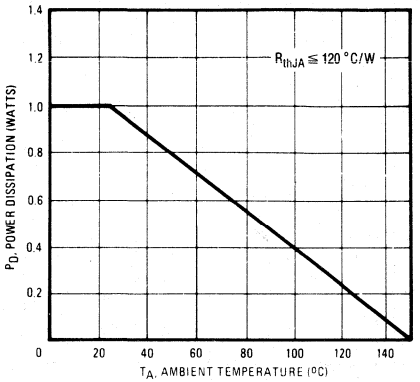


Fig. 13 — Power Vs. Temperature Derating Curve

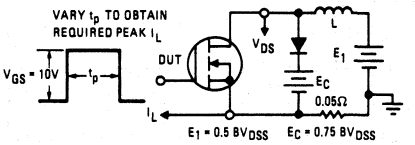


Fig. 14 — Clamped inductive test circuit.

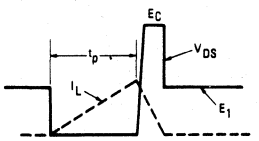


Fig. 15 — Clamped inductive waveforms.

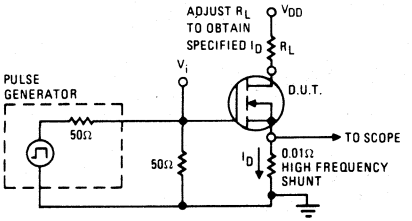


Fig. 16 — Switching Time Test Circuit

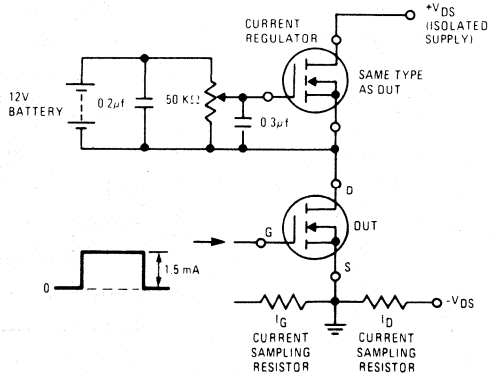


Fig. 17 — Gate Charge Test Circuit

File Number **1562**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3.0A and 3.5A, 60V-100V

$r_{DS}(on)$ = 0.6 Ω and 0.8 Ω

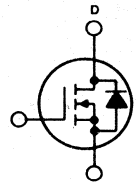
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRFF110, IRFF111, IRFF112 and IRFF113 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

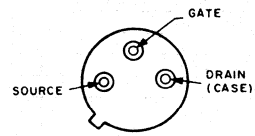
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

Absolute Maximum Ratings

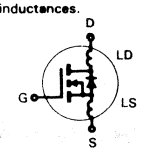
	Parameter	IRFF110	IRFF111	IRFF112	IRFF113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		14	14	12	12	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF110, IRFF111, IRFF112, IRFF113

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF110 IRFF112	100	–	–	V	V_{GS} = 0V
		IRFF111 IRFF113	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF110 IRFF111	3.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRFF112 IRFF113	3.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF110 IRFF111	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF112 IRFF113	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	135	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	$V_{DD} \approx 0.5\,BV_{DSS}$, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	3.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF110 IRFF111	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF112 IRFF113	–	–	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF110 IRFF111	–	–	14	A	
		IRFF112 IRFF113	–	–	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF110 IRFF111	–	–	2.5	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF112 IRFF113	–	–	2.0	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	200	–	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.0	–	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

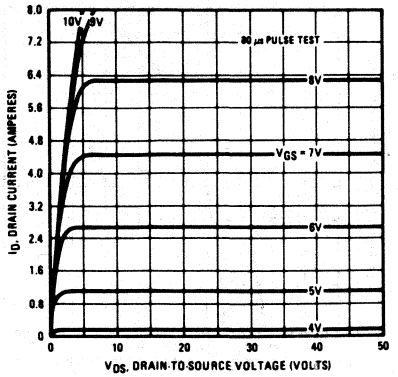


Fig. 1 – Typical Output Characteristics

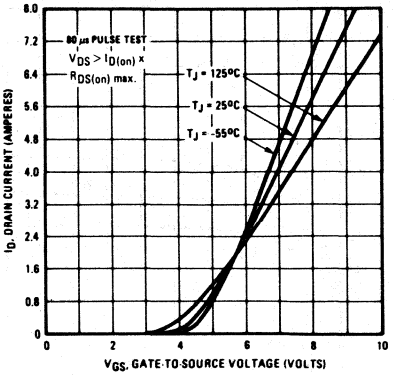


Fig. 2 – Typical Transfer Characteristics

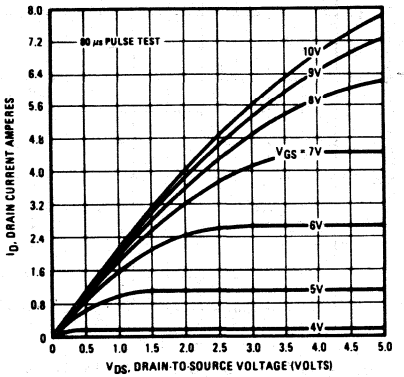


Fig. 3 – Typical Saturation Characteristics

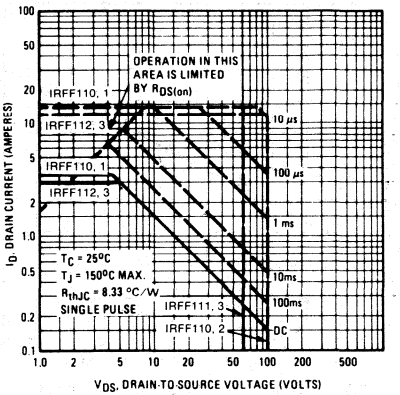


Fig. 4 – Maximum Safe Operating Area

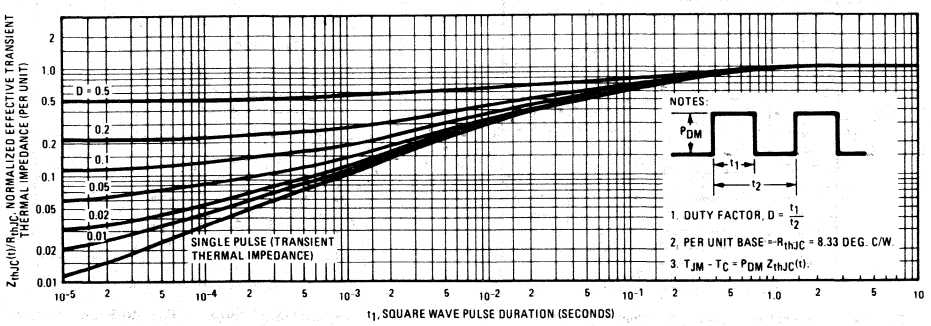


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

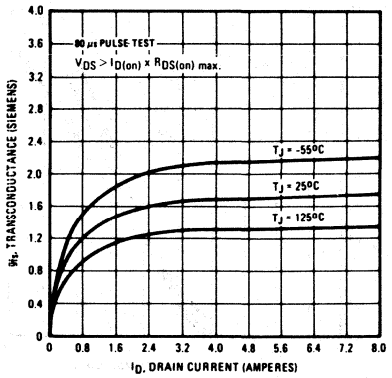


Fig. 6 – Typical Transconductance Vs. Drain Current

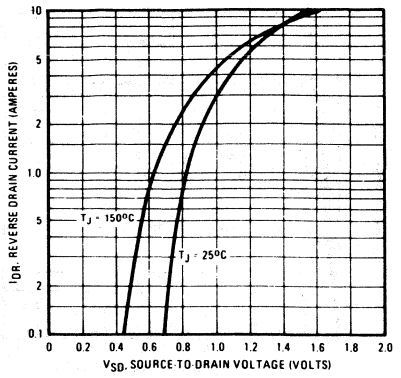


Fig. 7 – Typical Source-Drain Diode Forward Voltage

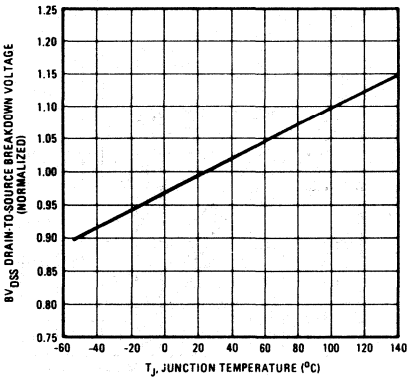


Fig. 8 – Breakdown Voltage Vs. Temperature

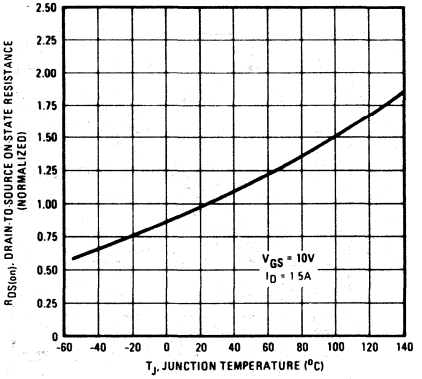


Fig. 9 – Normalized On-Resistance Vs. Temperature

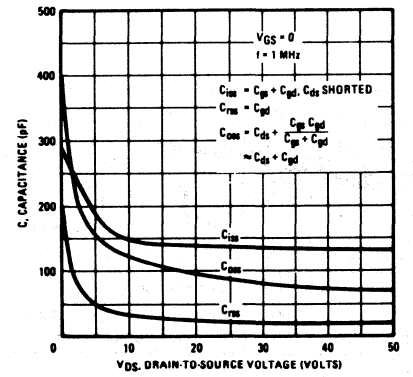


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

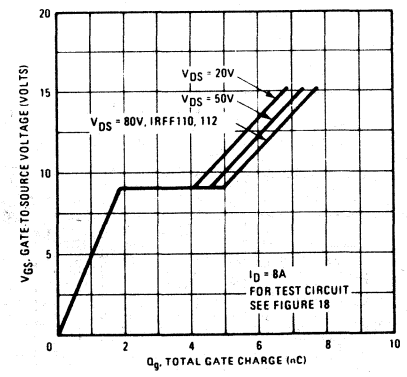


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

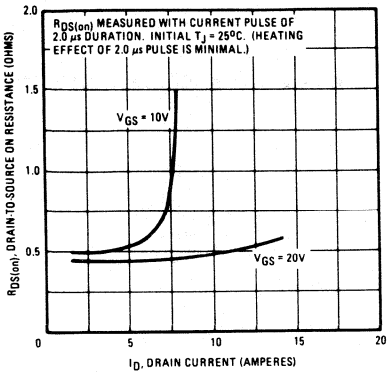


Fig. 12 – Typical On-Resistance Vs. Drain Current

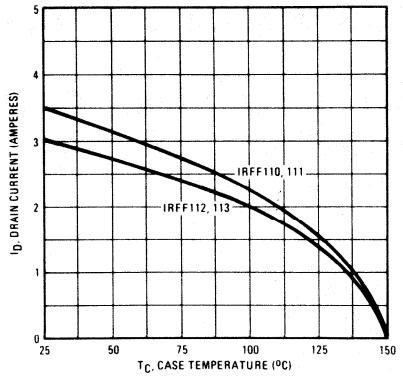


Fig. 13 – Maximum Drain Current Vs. Case Temperature

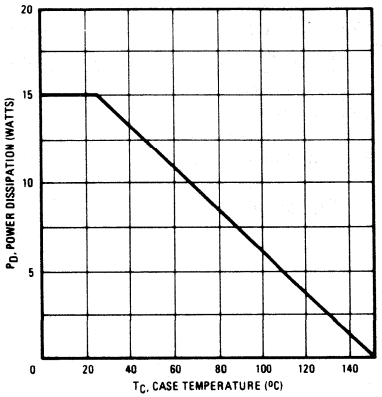


Fig. 14 – Power Vs. Temperature Derating Curve

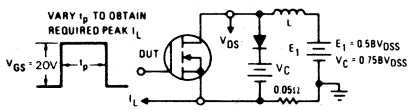


Fig. 15 – Clamped Inductive Test Circuit

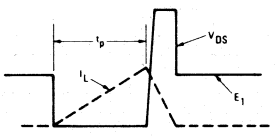


Fig. 16 – Clamped Inductive Waveforms

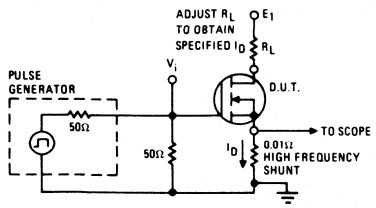


Fig. 17 – Switching Time Test Circuit

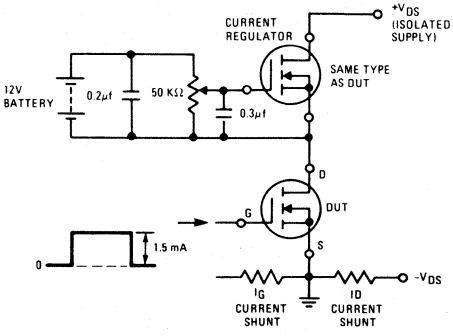


Fig. 18 – Gate Charge Test Circuit

IRFF120, IRFF121, IRFF122, IRFF123

File Number **1563**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

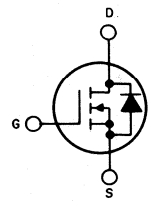
5.0A and 6.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

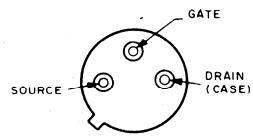
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

The IRFF120, IRFF121, IRFF122 and IRFF123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

Absolute Maximum Ratings

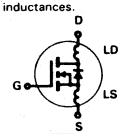
Parameter		IRFF120	IRFF121	IRFF122	IRFF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	24	24	20	20	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		24	24	20	20	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF120, IRFF121, IRFF122, IRFF123

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF120 IRFF122	100	–	–	V	V_{GS} = 0V
		IRFF121 IRFF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF120 IRFF121	6.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF122 IRFF123	5.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF120 IRFF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3.0A
		IRFF122 IRFF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	37	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	6.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF120 IRFF121	–	–	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF122 IRFF123	–	–	5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF120 IRFF121	–	–	24	A	
		IRFF122 IRFF123	–	–	20	A	
V_{SD}	Diode Forward Voltage ②	IRFF120 IRFF121	–	–	2.5	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
		IRFF122 IRFF123	–	–	2.3	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.2	–	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRFF120, IRFF121, IRFF122, IRFF123

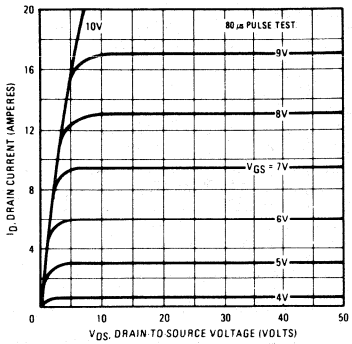


Fig. 1 — Typical Output Characteristics

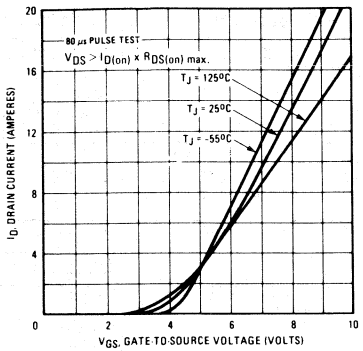


Fig. 2 — Typical Transfer Characteristics

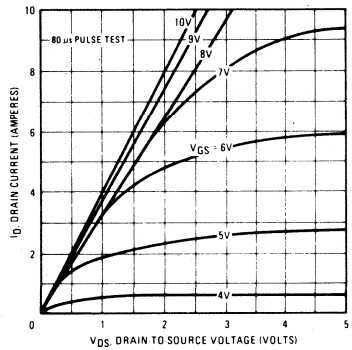


Fig. 3 — Typical Saturation Characteristics

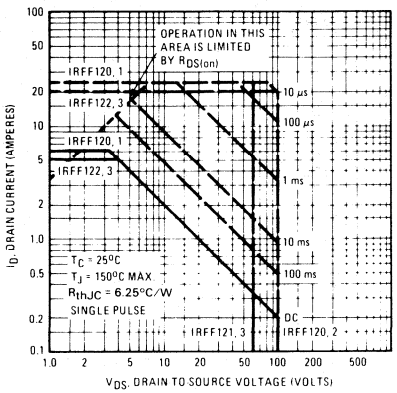


Fig. 4 — Maximum Safe Operating Area

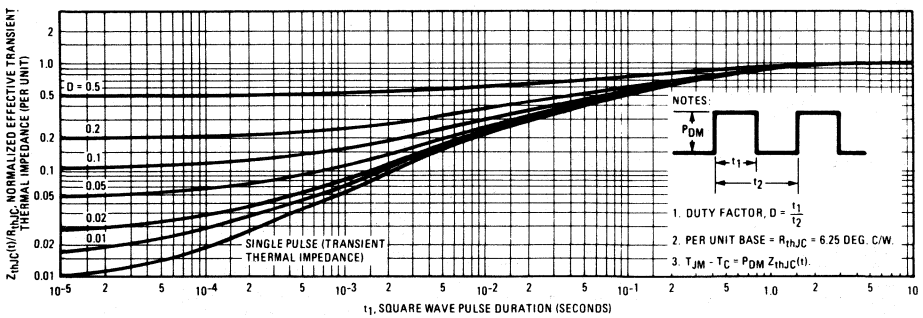


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

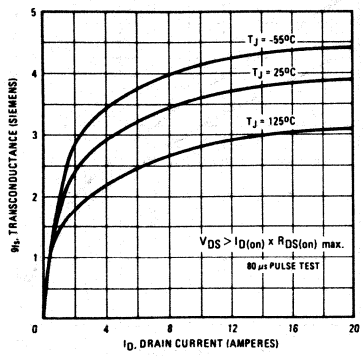


Fig. 6 — Typical Transconductance Vs. Drain Current

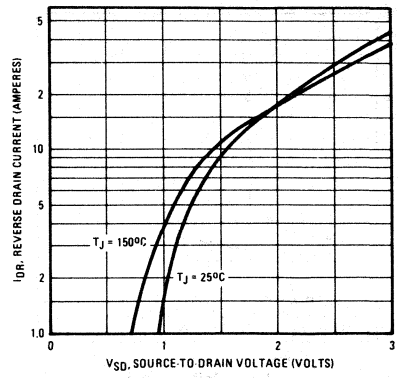


Fig. 7 — Typical Source-Drain Diode Forward Voltage

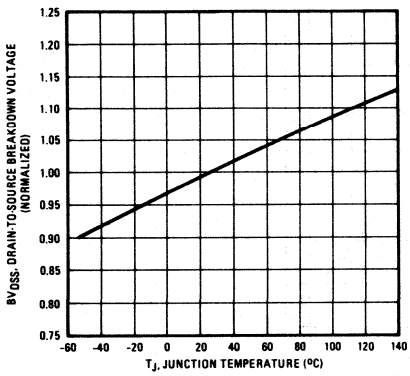


Fig. 8 — Breakdown Voltage Vs. Temperature

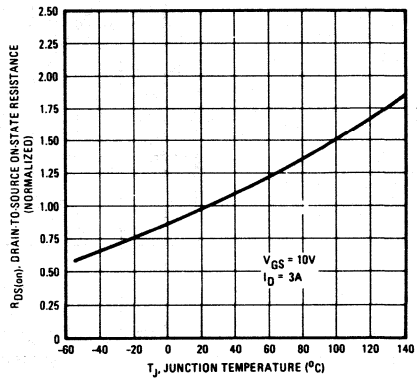


Fig. 9 — Normalized On-Resistance Vs. Temperature

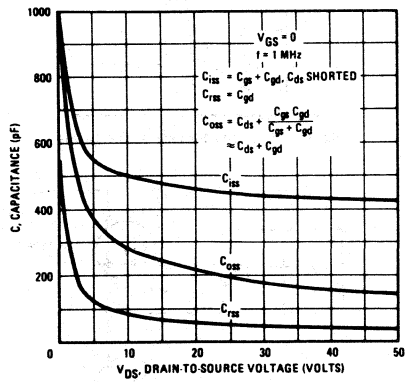


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

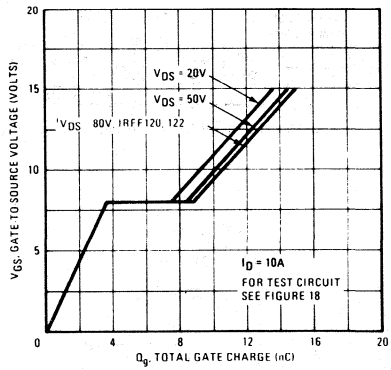


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRFF120, IRFF121, IRFF122, IRFF123

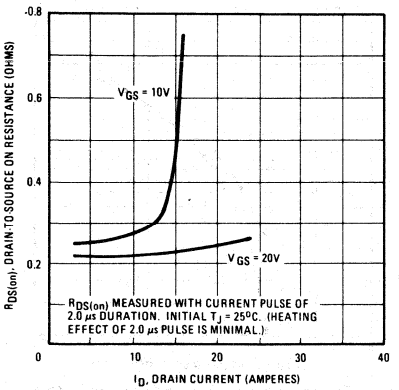


Fig. 12 – Typical On-Resistance Vs. Drain Current

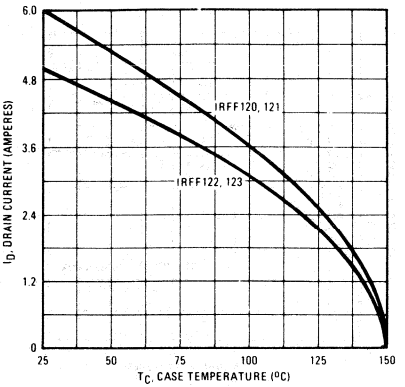


Fig. 13 – Maximum Drain Current Vs. Case Temperature

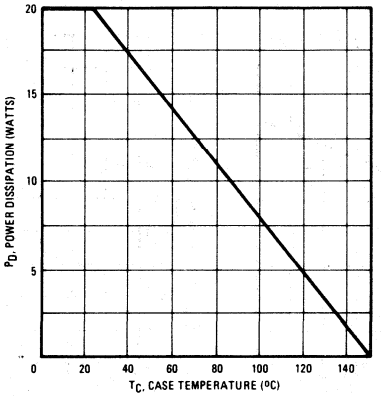


Fig. 14 – Power Vs. Temperature Derating Curve

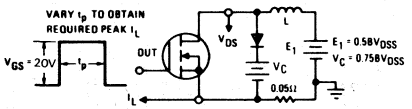


Fig. 15 – Clamped Inductive Test Circuit

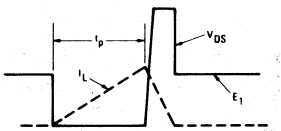


Fig. 16 – Clamped Inductive Waveforms

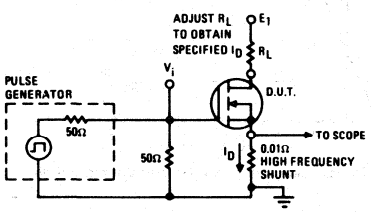


Fig. 17 – Switching Time Test Circuit

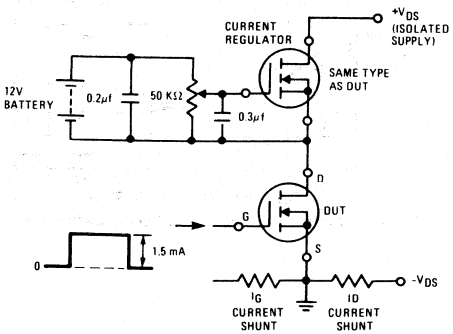


Fig. 18 – Gate Charge Test Circuit

File Number **1564**

IRFF130, IRFF131, IRFF132, IRFF133

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

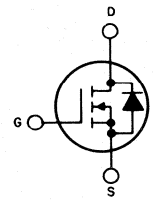
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRFF130, IRFF131, IRFF132 and IRFF133 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

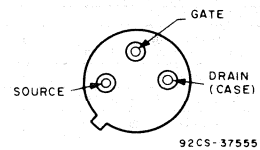
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

Absolute Maximum Ratings

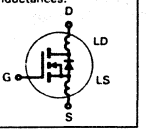
	Parameter	IRFF130	IRFF131	IRFF132	IRFF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF130, IRFF131, IRFF132, IRFF133

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF130 IRFF132	100	–	–	V	V_{GS} = 0V
		IRFF131 IRFF133	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF130 IRFF131	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF132 IRFF133	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF130 IRFF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 4.0A
		IRFF132 IRFF133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	50	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	80	150	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	80	150	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	14	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	14	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF130 IRFF131	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF132 IRFF133	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF130 IRFF131	–	–	32	A	
		IRFF132 IRFF133	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRFF130 IRFF131	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRFF132 IRFF133	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.5	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

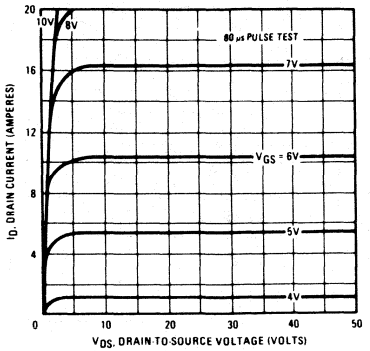


Fig. 1 – Typical Output Characteristics

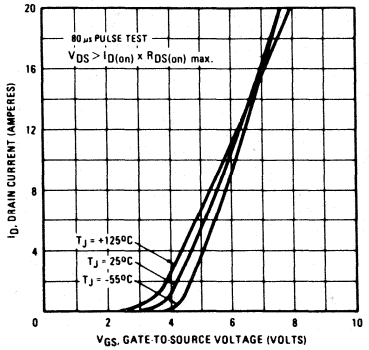


Fig. 2 – Typical Transfer Characteristics

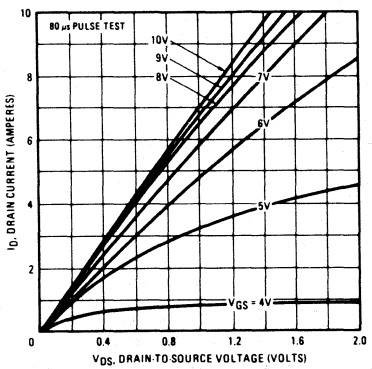


Fig. 3 – Typical Saturation Characteristics

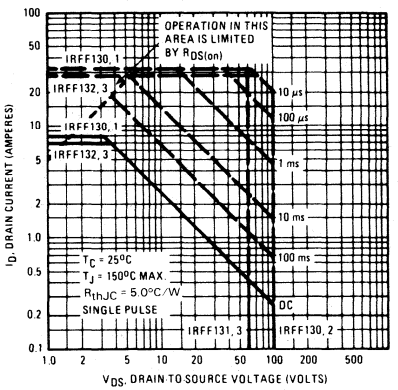


Fig. 4 – Maximum Safe Operating Area

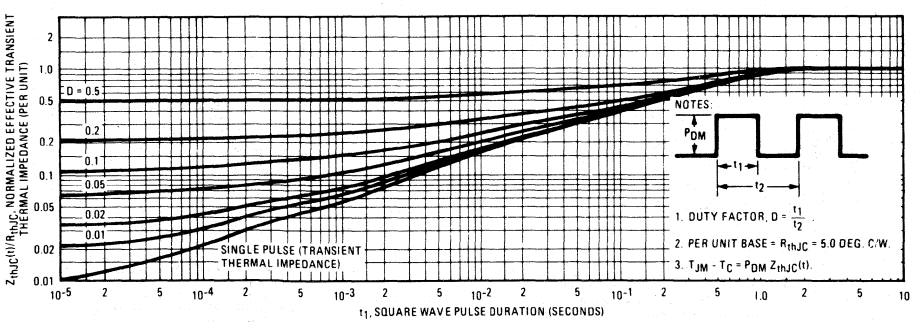


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFF130, IRFF131, IRFF132, IRFF133

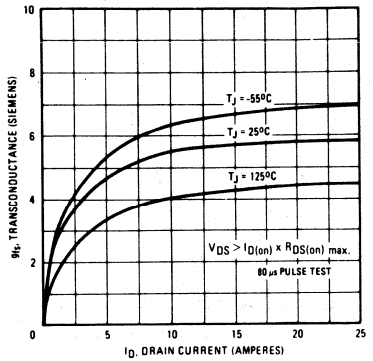


Fig. 6 – Typical Transconductance Vs. Drain Current

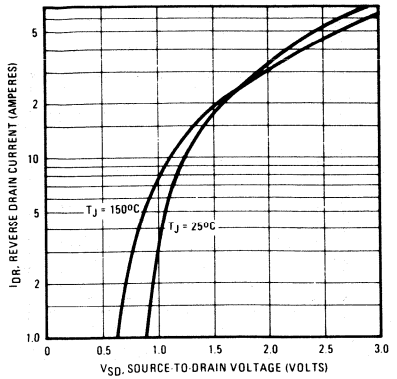


Fig. 7 – Typical Source-Drain Diode Forward Voltage

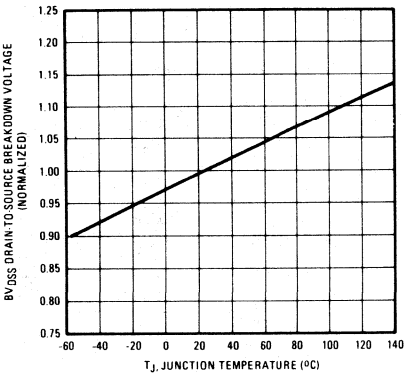


Fig. 8 – Breakdown Voltage Vs. Temperature

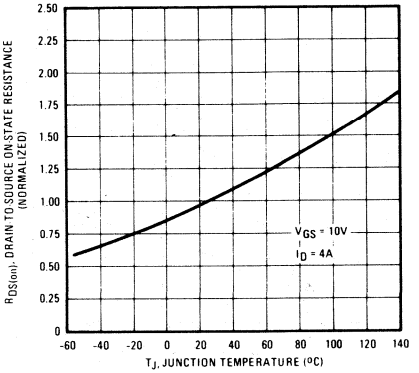


Fig. 9 – Normalized On-Resistance Vs. Temperature

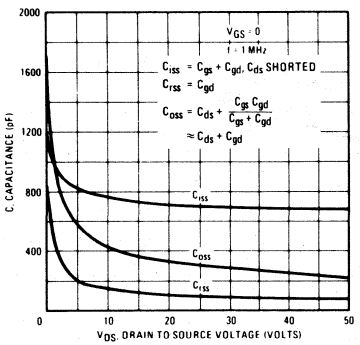


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

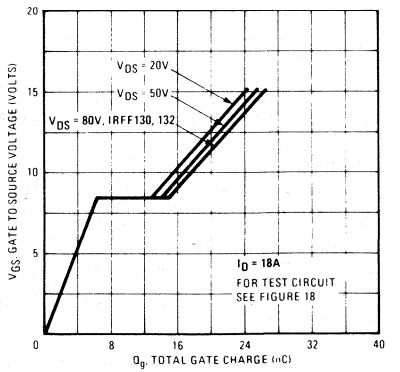


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

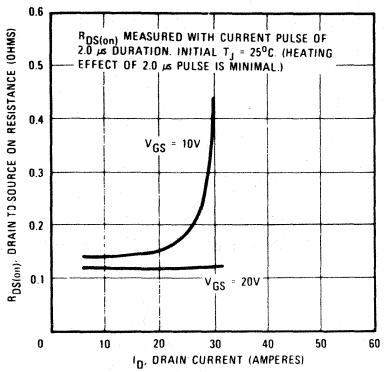


Fig. 12 – Typical On-Resistance Vs. Drain Current

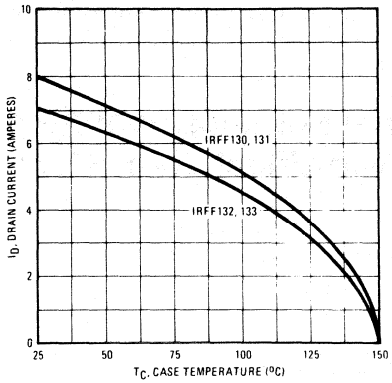


Fig. 13 – Maximum Drain Current Vs. Case Temperature

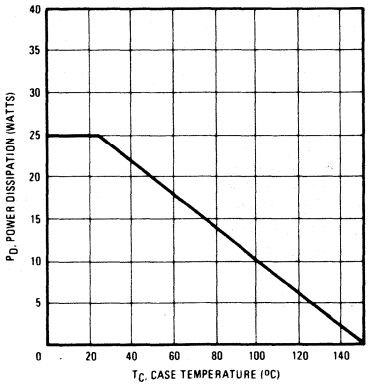


Fig. 14 – Power Vs. Temperature Derating Curve

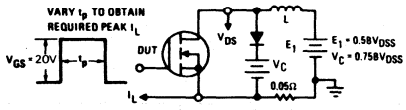


Fig. 15 – Clamped Inductive Test Circuit

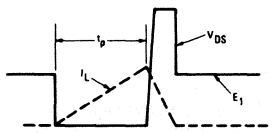


Fig. 16 – Clamped Inductive Waveforms

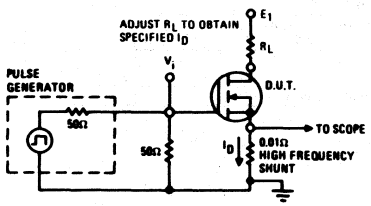


Fig. 17 – Switching Time Test Circuit

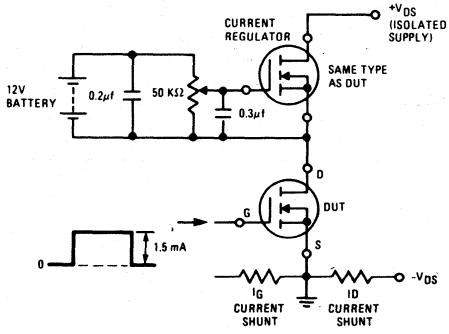


Fig. 18 – Gate Charge Test Circuit

IRFF210, IRFF211, IRFF212, IRFF213

File Number **1887**

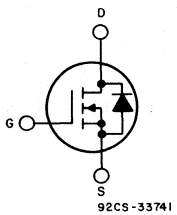
N-Channel Enhancement-Mode Power Field-Effect Transistors

1.8A and 2.2A, 150V - 200V
$r_{DS(on)}$ = 1.5Ω and 2.4Ω

Features:

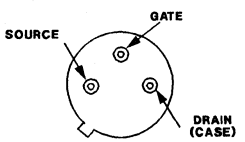
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF210, IRFF211, IRFF212 and IRFF213 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

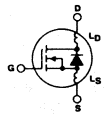
Absolute Maximum Ratings

	Parameter	IRFF210	IRFF211	IRFF212	IRFF213	Units
V_{DS}	Drain – Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.2	2.2	1.8	1.8	A
I_{DM}	Pulsed Drain Current ③	9.0	9.0	7.5	7.5	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		9.0	9.0	7.5	7.5	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFF210 IRFF212	200	–	–	V	V_{GS} = 0V
		IRFF211 IRFF213	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	–100	nA	V_{GS} = –20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF210 IRFF211	2.2	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF212 IRFF213	1.8	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFF210 IRFF211	–	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		IRFF212 IRFF213	–	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	–	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	60	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	16	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	8.0	15	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	10	15	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 4.5A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	3.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

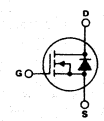


Thermal Resistance

R_{thJC}	Junction to Case	ALL	—	—	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF210 IRFF211	–	–	2.2	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF212 IRFF213	–	–	1.8	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF210 IRFF211	–	–	9.0	A	
		IRFF212 IRFF213	–	–	7.5	A	
V_{SD}	Diode Forward Voltage ②	IRFF210 IRFF211	–	–	2.0	V	T_C = 25°C, I_S = 2.2A, V_{GS} = 0V
		IRFF212 IRFF213	–	–	1.8	V	T_C = 25°C, I_S = 1.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	290	–	ns	T_J = 150°C, I_F = 2.2A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.0	–	μC	T_J = 150°C, I_F = 2.2A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRFF210, IRFF211, IRFF212, IRFF213

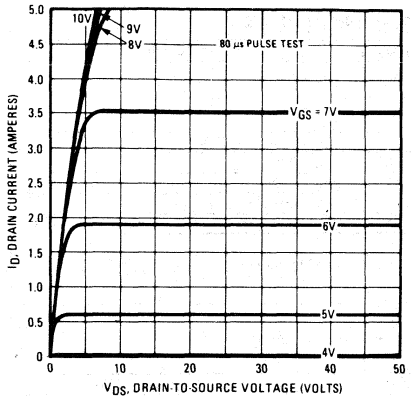


Fig. 1 - Typical output characteristics.

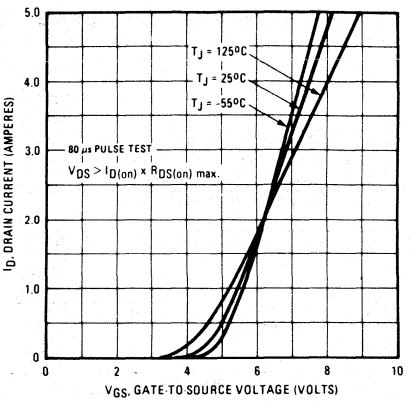


Fig. 2 - Typical transfer characteristics.

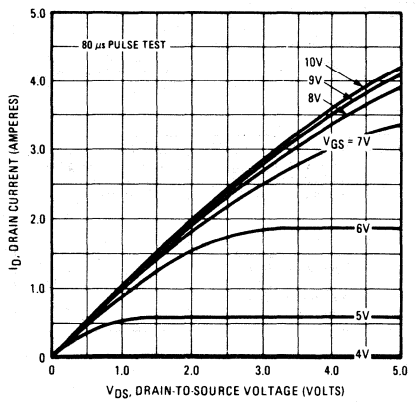


Fig. 3 - Typical saturation characteristics.

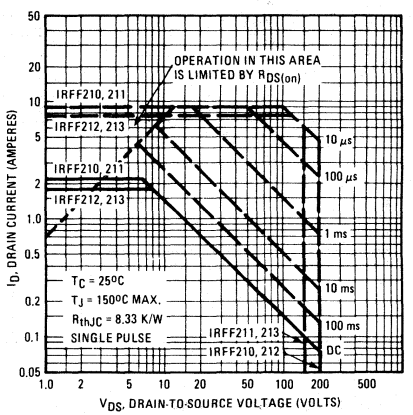


Fig. 4 - Maximum safe operating area.

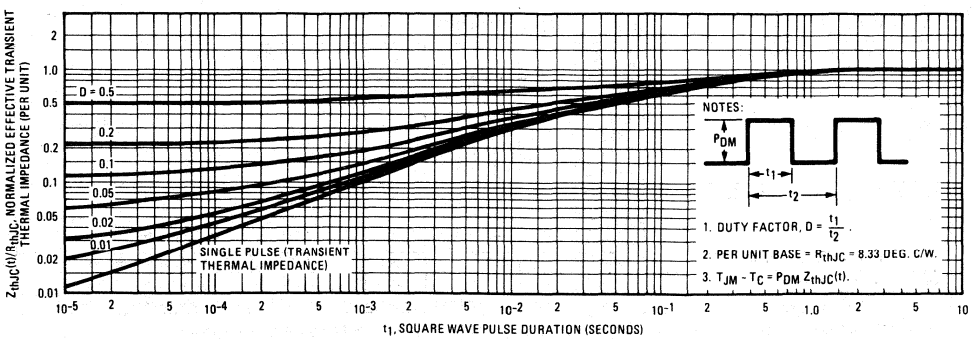


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

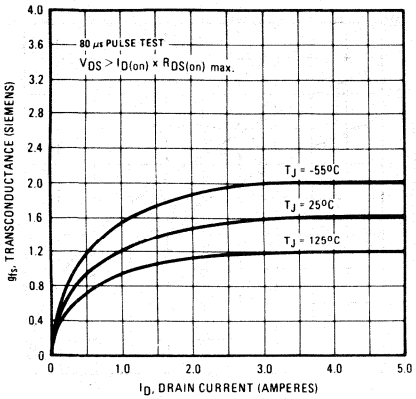


Fig. 6 - Typical transconductance vs. drain current.

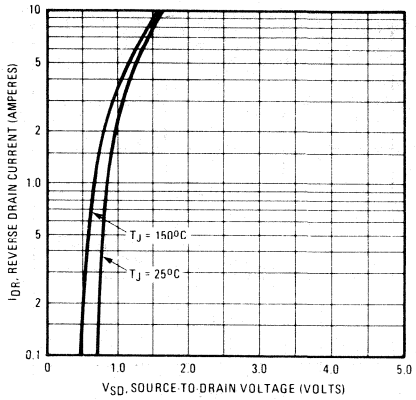


Fig. 7 - Typical source-drain diode forward voltage.

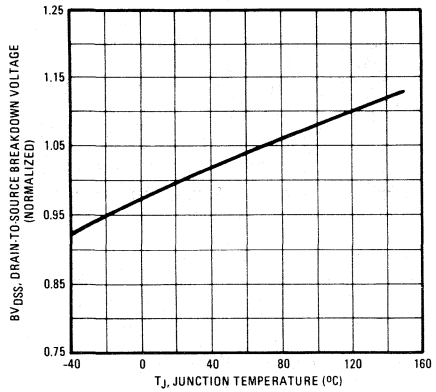


Fig. 8 - Breakdown voltage vs. temperature.

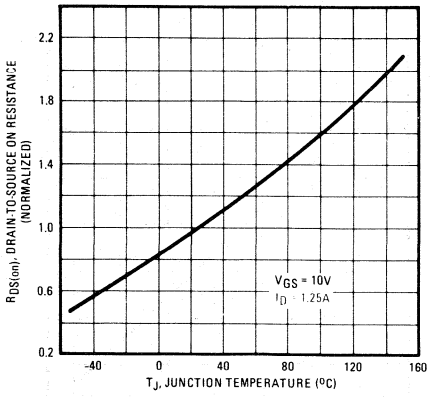


Fig. 9 - Normalized on-resistance vs. temperature.

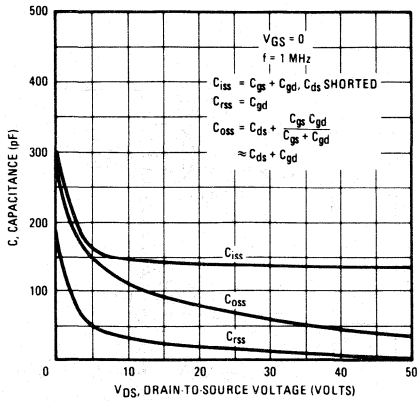


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

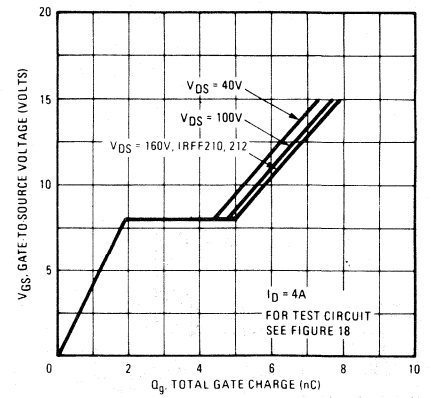


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF210, IRFF211, IRFF212, IRFF213

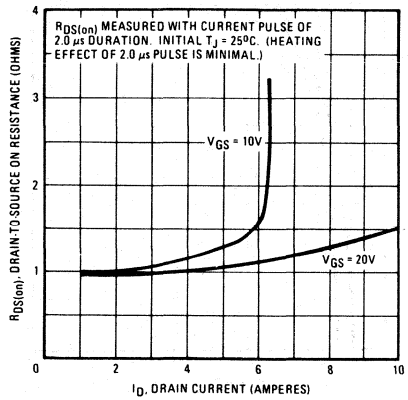


Fig. 12 - Typical on-resistance vs. drain current.

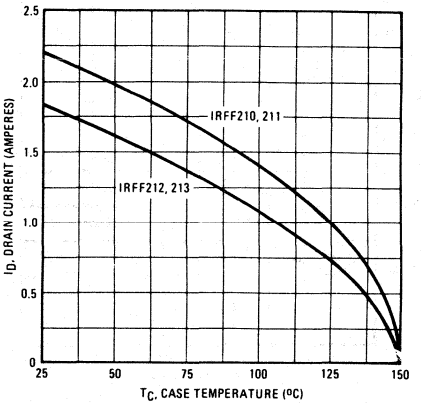


Fig. 13 - Maximum drain current vs. case temperature.

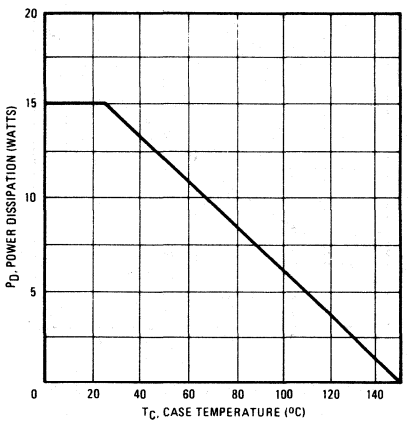


Fig. 14 - Power vs. temperature derating curve.

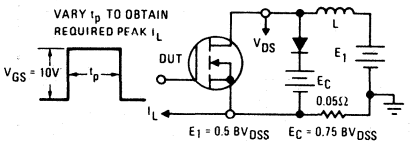


Fig. 15 - Clamped inductive test circuit.

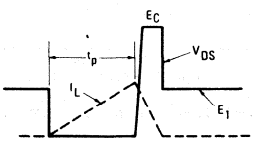


Fig. 16 - Clamped inductive waveforms.

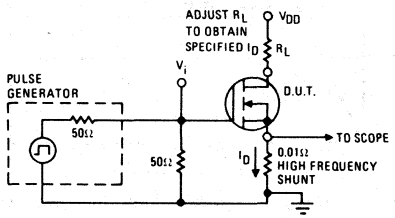


Fig. 17 - Switching time test circuit.

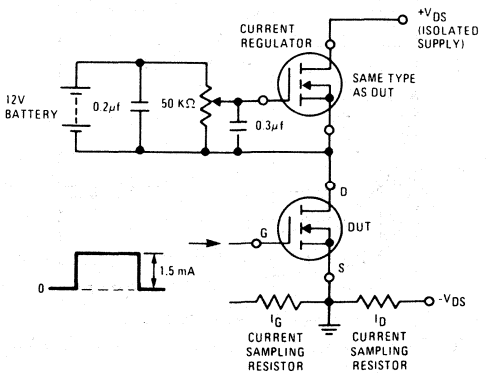


Fig. 18 - Gate charge test circuit.

File Number **1889**

IRFF220, IRFF221, IRFF222, IRFF223

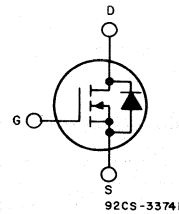
N-Channel Enhancement-Mode Power Field-Effect Transistors

3.0A and 3.5A, 150V - 200V
$r_{DS(on)}$ = 0.8Ω and 1.2Ω

Features:

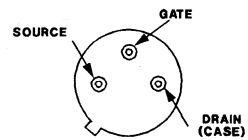
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF220, IRFF221, IRFF222 and IRFF223 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

Absolute Maximum Ratings

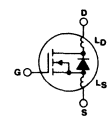
	Parameter	IRFF220	IRFF221	IRFF222	IRFF223	Units
V_{DS}	Drain – Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		14	14	12	12	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF220, IRFF221, IRFF222, IRFF223

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF220 IRFF222	200	–	–	V	V_{GS} = 0V
		IRFF221 IRFF223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	–	–	–100	nA	V_{GS} = –20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF220 IRFF221	3.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF222 IRFF223	3.0	–	–	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF220 IRFF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.0A
		IRFF222 IRFF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.25	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.0A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 2.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	7.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

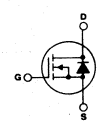


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF220 IRFF221	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF222 IRFF223	–	–	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF220 IRFF221	–	–	14	A	
		IRFF222 IRFF223	–	–	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF220 IRFF221	–	–	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF222 IRFF223	–	–	1.8	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

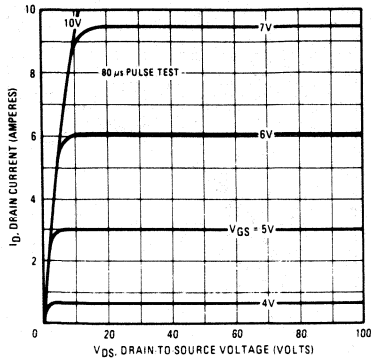


Fig. 1 - Typical output characteristics.

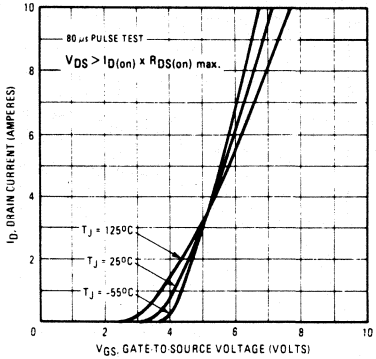


Fig. 2 - Typical transfer characteristics.

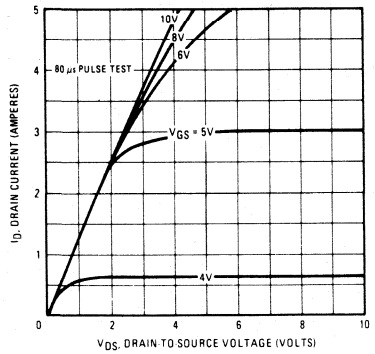


Fig. 3 - Typical saturation characteristics.

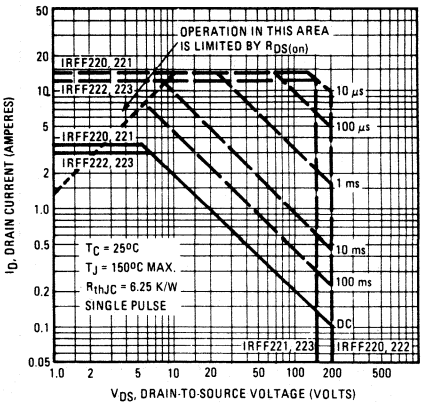


Fig. 4 - Maximum safe operating area.

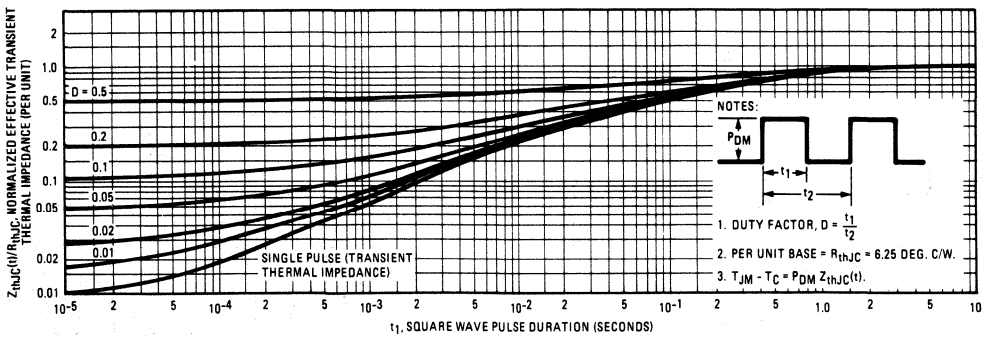


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFF220, IRFF221, IRFF222, IRFF223

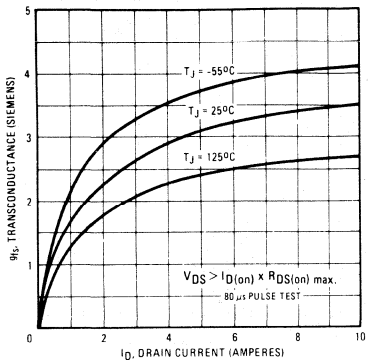


Fig. 6 - Typical transconductance vs. drain current.

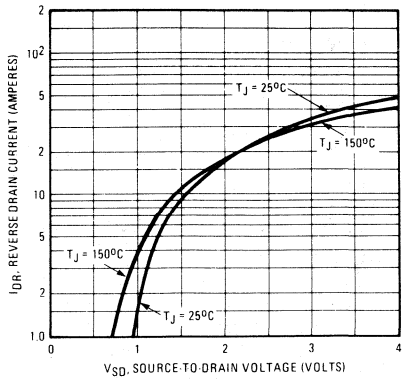


Fig. 7 - Typical source-drain diode forward voltage.

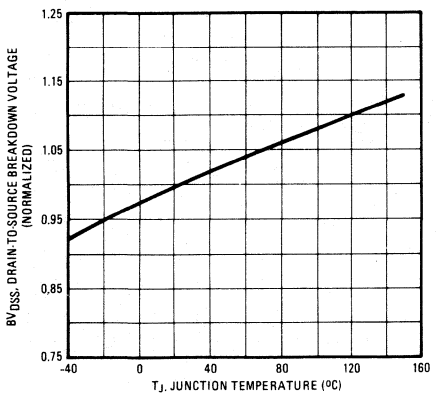


Fig. 8 - Breakdown voltage vs. temperature.

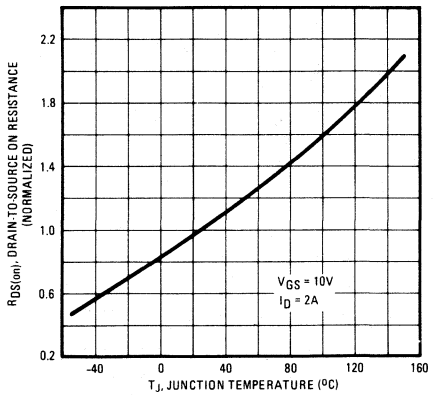


Fig. 9 - Normalized on-resistance vs. temperature.

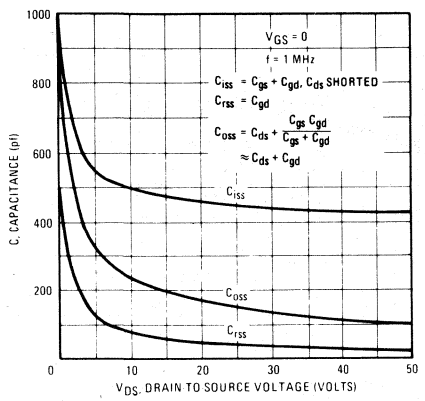


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

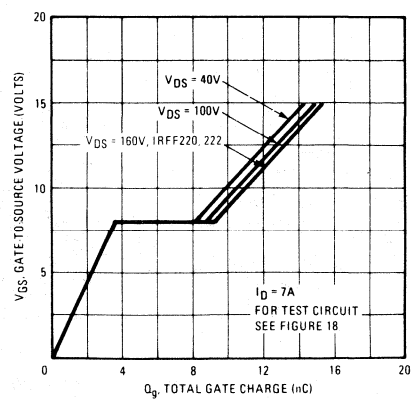


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

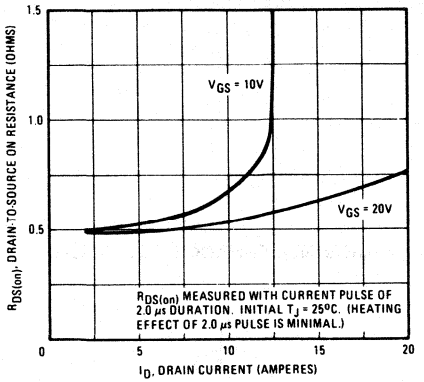


Fig. 12 - Typical on-resistance vs. drain current.

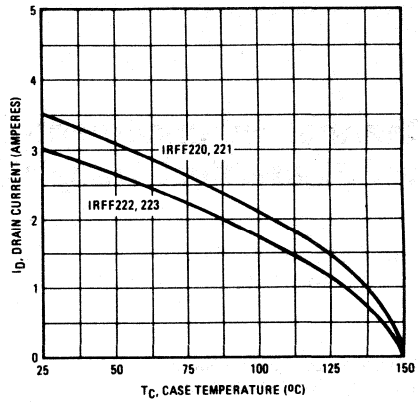


Fig. 13 - Maximum drain current vs. case temperature.

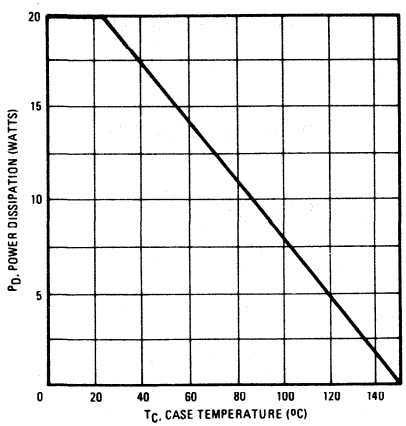


Fig. 14 - Power vs. temperature derating curve.

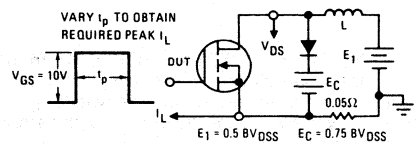


Fig. 15 - Clamped inductive test circuit.

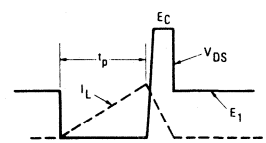


Fig. 16 - Clamped inductive waveforms.

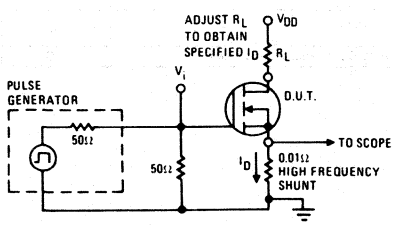


Fig. 17 - Switching time test circuit.

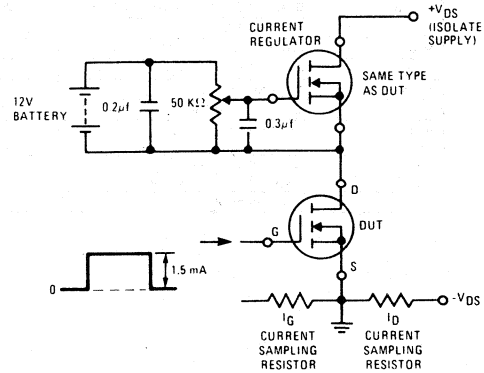


Fig. 18 - Gate charge test circuit.

IRFF230, IRFF231 IRFF232, IRFF233

File Number **1892**

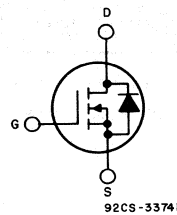
N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5A and 5.5A, 150V - 200V
$r_{DS(on)}$ = 0.4Ω and 0.6Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

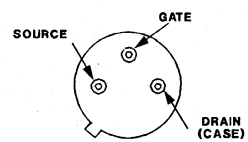


TERMINAL DIAGRAM

The IRFF230, IRFF231, IRFF232 and IRFF233 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

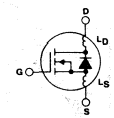
Absolute Maximum Ratings

Parameter		IRFF230	IRFF231	IRFF232	IRFF233	Units
V_{DS}	Drain – Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF230, IRFF232	200	–	–	V	V_{GS} = 0V
		IRFF231, IRFF233	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF230, IRFF231	5.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF232, IRFF233	4.5	–	–	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF230, IRFF231	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 3.0A
		IRFF232, IRFF233	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	4.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 11A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	15	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	15	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

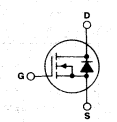


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF230, IRFF231	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF232, IRFF233	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF230, IRFF231	–	–	22	A	
		IRFF232, IRFF233	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	IRFF230, IRFF231	–	–	2.0	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRFF232, IRFF233	–	–	1.8	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRFF230, IRFF231, IRFF232, IRFF233

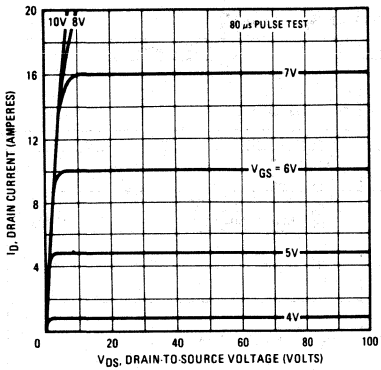


Fig. 1 - Typical output characteristics.

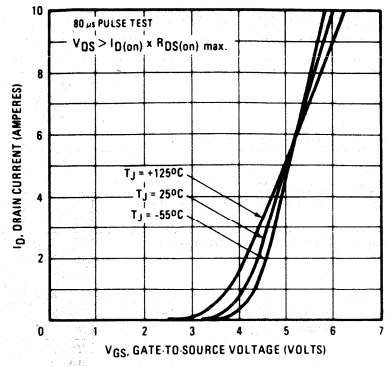


Fig. 2 - Typical transfer characteristics.

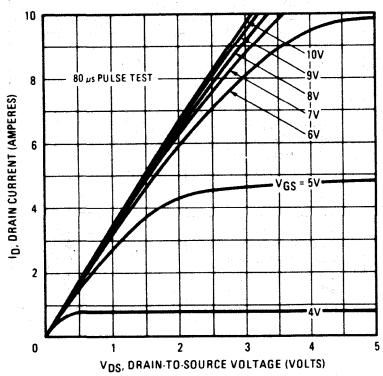


Fig. 3 - Typical saturation characteristics.

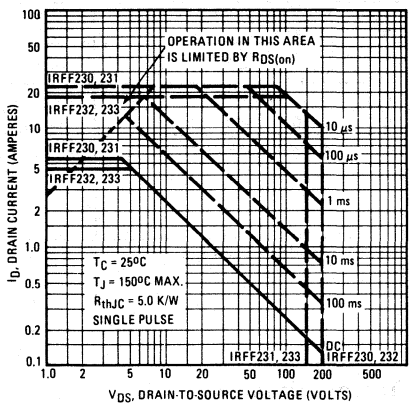


Fig. 4 - Maximum safe operating area.

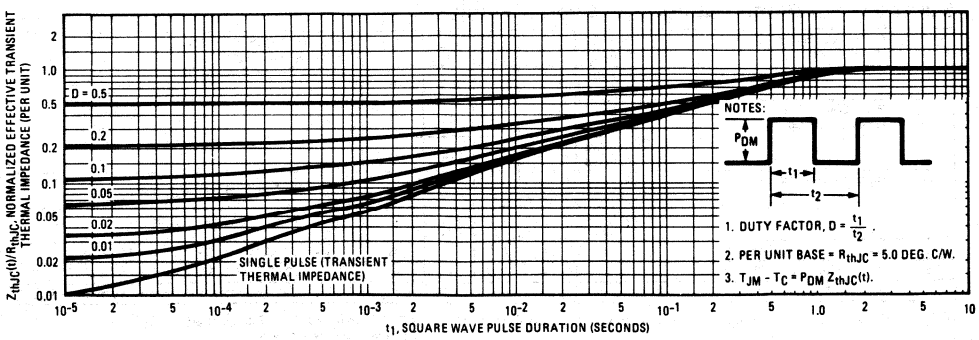


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

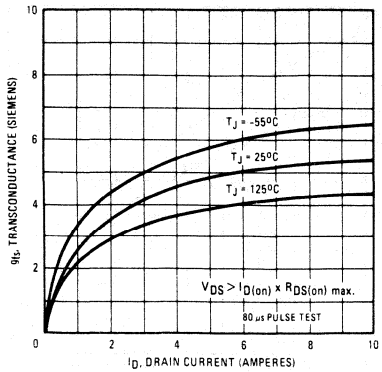


Fig. 6 - Typical transconductance vs. drain current.

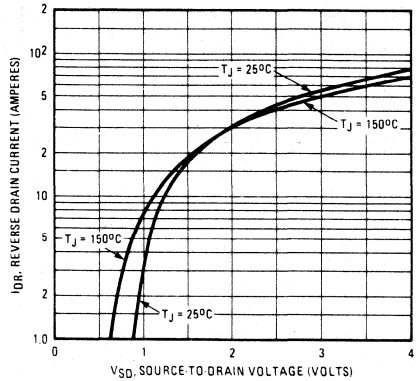


Fig. 7 - Typical source-drain diode forward voltage.

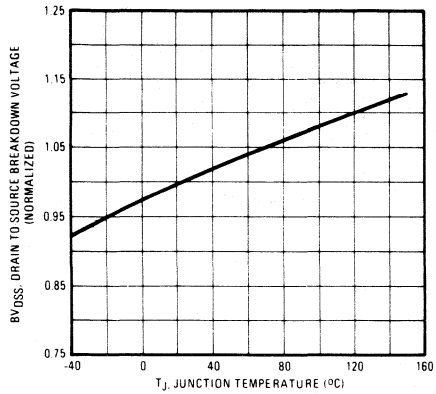


Fig. 8 - Breakdown voltage vs. temperature.

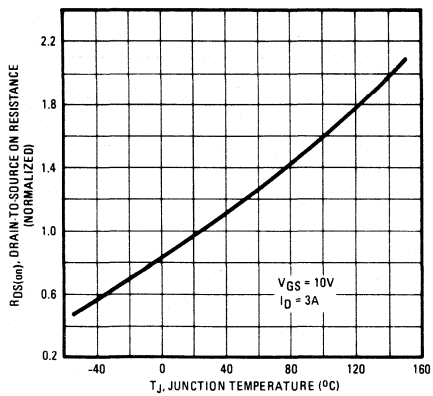


Fig. 9 - Normalized on-resistance vs. temperature.

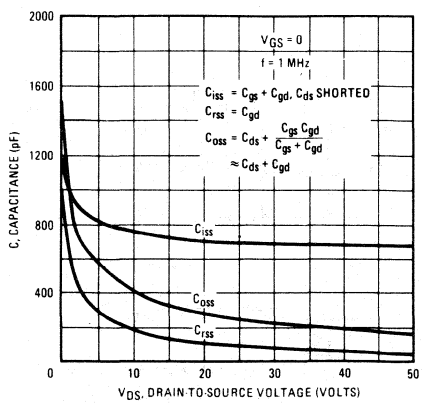


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

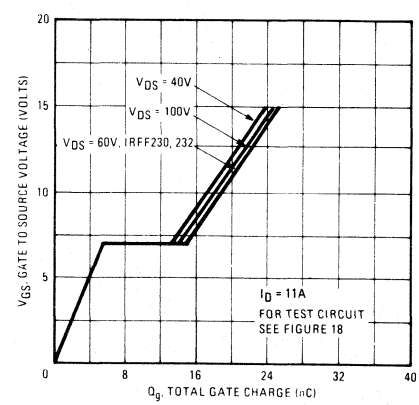


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF230, IRFF231, IRFF232, IRFF233

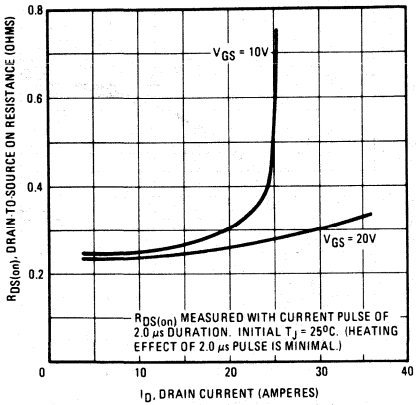


Fig. 12 - Typical on-resistance vs. drain current.

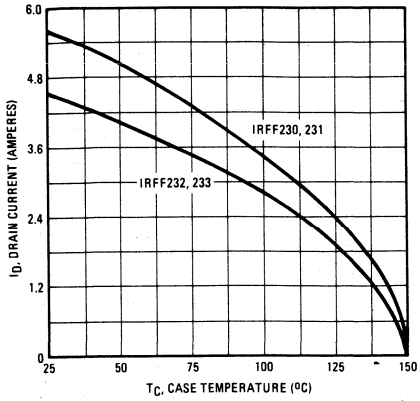


Fig. 13 - Maximum drain current vs. case temperature.

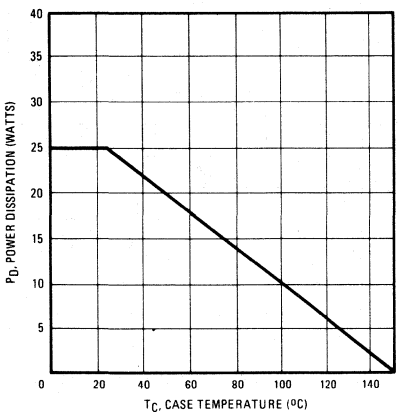


Fig. 14 - Power vs. temperature derating curve.

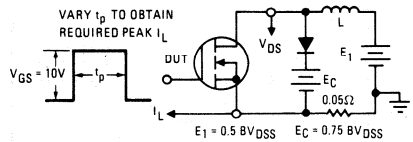


Fig. 15 - Clamped inductive test circuit.

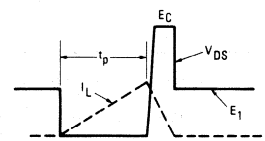


Fig. 16 - Clamped inductive waveforms.

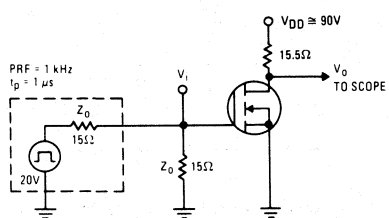


Fig. 17 - Switching time test circuit.

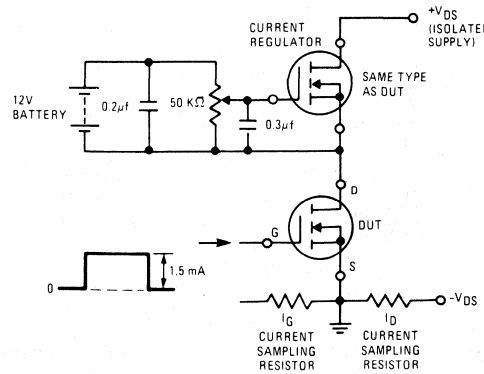


Fig. 18 - Gate charge test circuit.

File Number **1888**

IRFF310, IRFF311, IRFF312, IRFF313

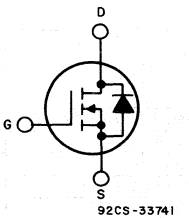
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

1.15A and 1.35 A, 350 V - 400 V
$r_{DS(on)}$ = 3.6 Ω and 5 Ω

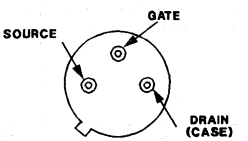
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF310, IRFF311, IRFF312, and IRFF313 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

Absolute Maximum Ratings

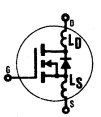
	Parameter	IRFF310	IRFF311	IRFF312	IRFF313	Units
V_{DS}	Drain – Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	1.35	1.35	1.15	1.15	A
I_{DM}	Pulsed Drain Current ③	5.5	5.5	4.5	4.5	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		5.5	5.5	4.5	4.5	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF310, IRFF311, IRFF312, IRFF313

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFF310 IRFF312	400	–	–	V	V_{GS} = 0V
		IRFF311 IRFF313	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF310 IRFF311	1.35	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF312 IRFF313	1.15	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFF310 IRFF311	–	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRFF312 IRFF313	–	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	–	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	35	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	8.0	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	3.0	10	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.8A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	5.0	10	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	6.0	7.5	nC	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	3.0	4.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	4.5	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF310 IRFF311	–	–	1.35	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF312 IRFF313	–	–	1.15	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF310 IRFF311	–	–	5.5	A	
		IRFF312 IRFF313	–	–	4.5	A	
V_{SD}	Diode Forward Voltage ②	IRFF310 IRFF311	–	–	1.6	V	T_C = 25°C, I_S = 1.35A, V_{GS} = 0V
		IRFF312 IRFF313	–	–	1.5	V	T_C = 25°C, I_S = 1.15A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	380	–	ns	T_J = 150°C, I_F = 1.35A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.7	–	μC	T_J = 150°C, I_F = 1.35A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

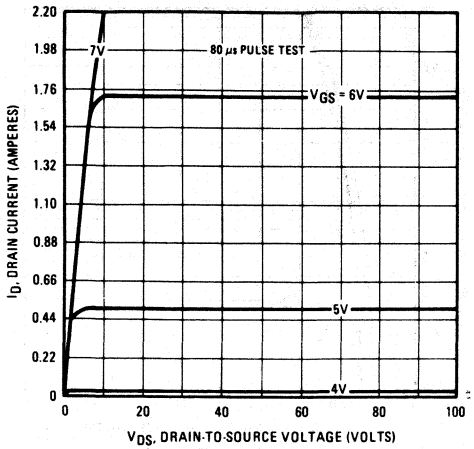


Fig. 1 – Typical Output Characteristics

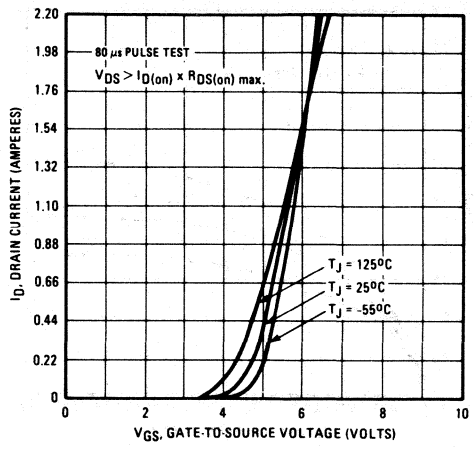


Fig. 2 – Typical Transfer Characteristics

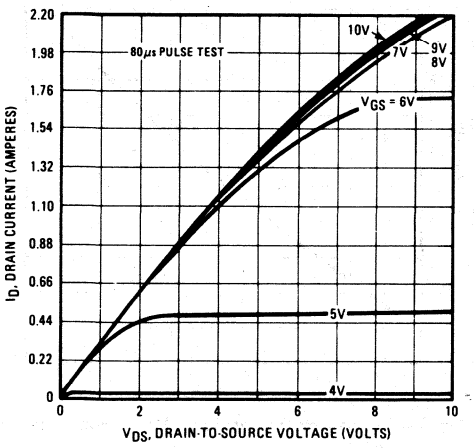


Fig. 3 – Typical Saturation Characteristics

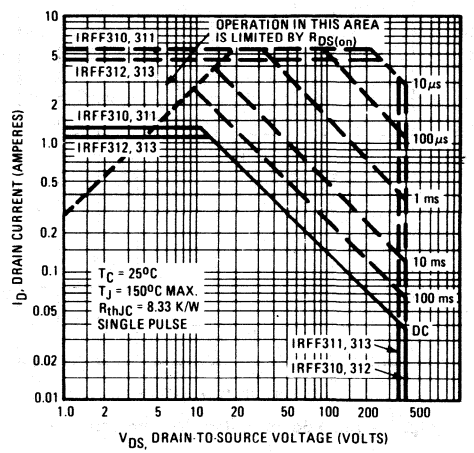


Fig. 4 – Maximum Safe Operating Area

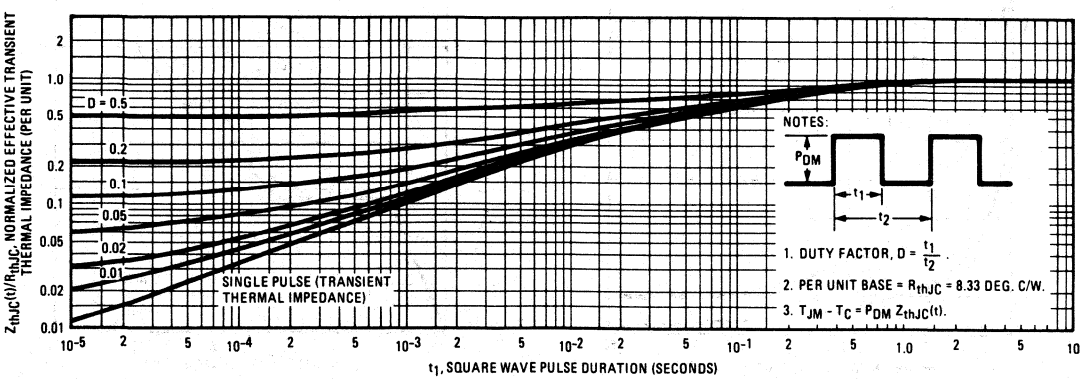


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFF310, IRFF311, IRFF312, IRFF313

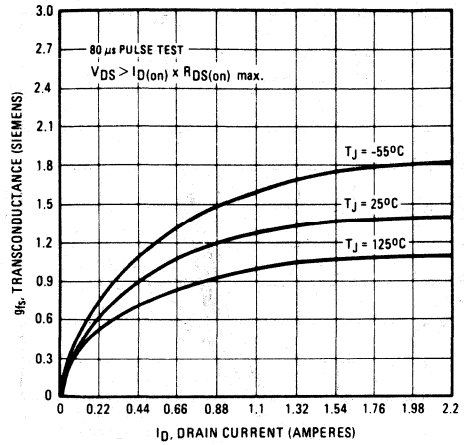


Fig. 6 — Typical Transconductance Vs. Drain Current

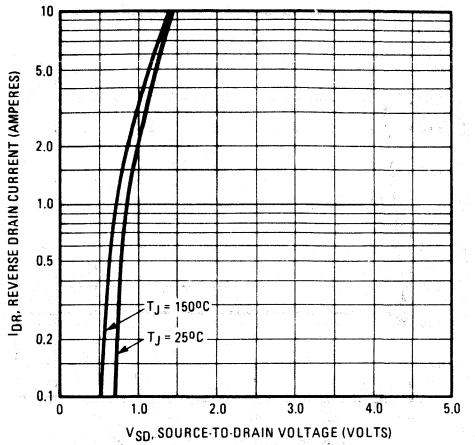


Fig. 7 — Typical Source-Drain Diode Forward Voltage

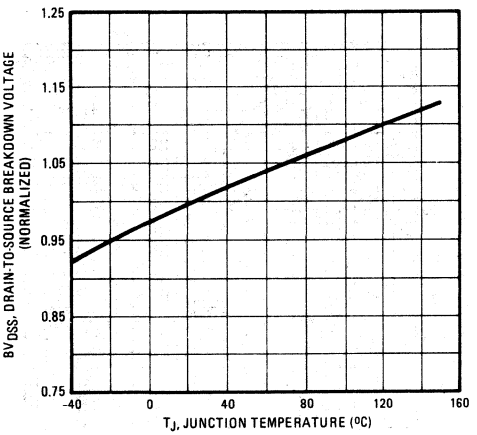


Fig. 8 — Breakdown Voltage Vs. Temperature

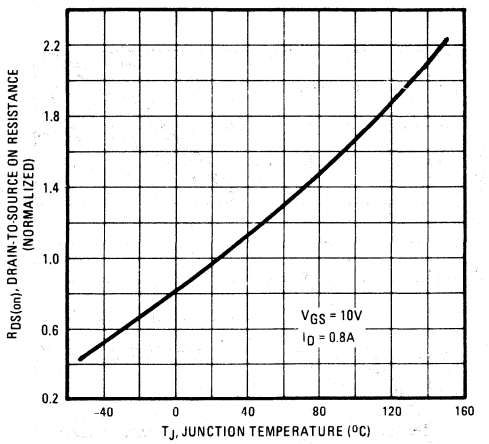


Fig. 9 — Normalized On-Resistance Vs. Temperature

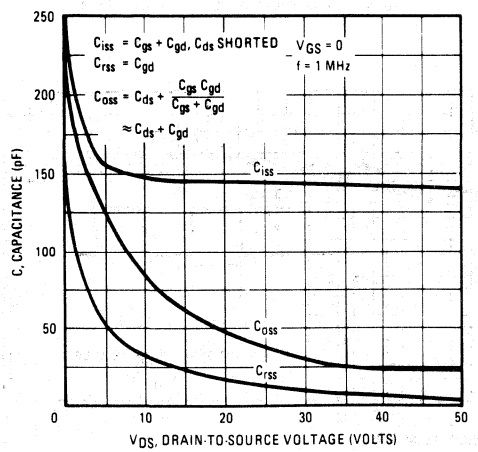


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

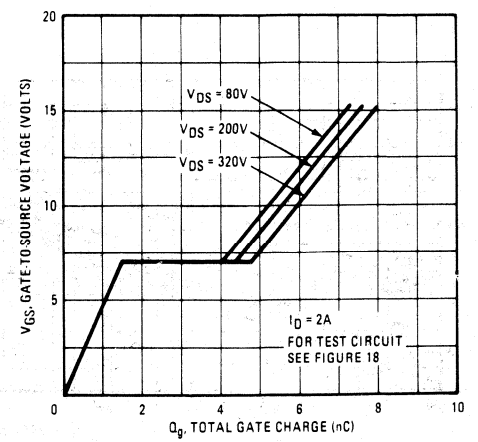


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

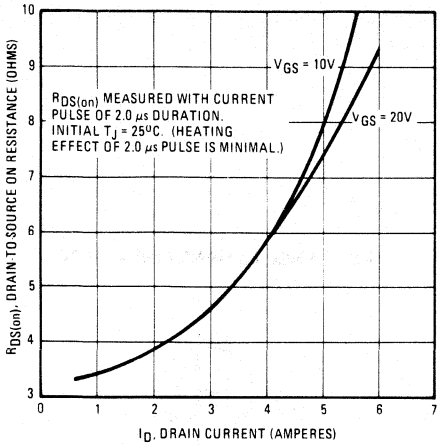


Fig. 12 – Typical On-Resistance Vs. Drain Current

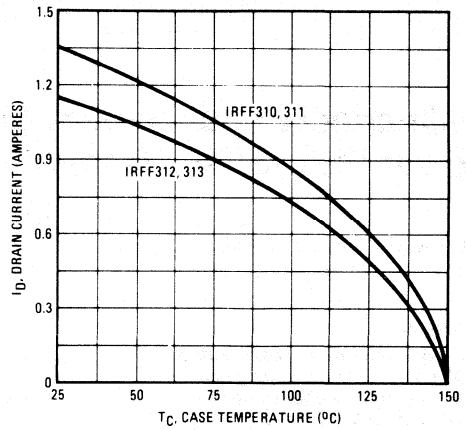


Fig. 13 – Maximum Drain Current Vs. Case Temperature

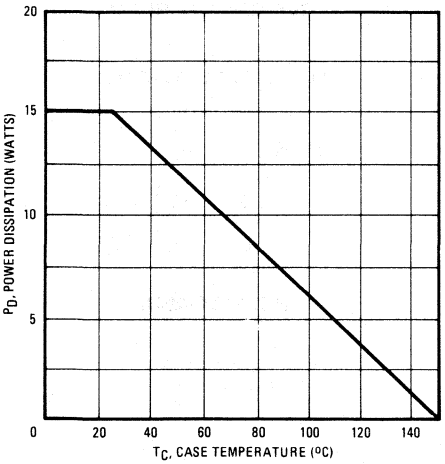


Fig. 14 – Power Vs. Temperature Derating Curve

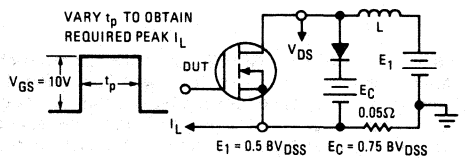


Fig. 15 – Clamped Inductive Test Circuit

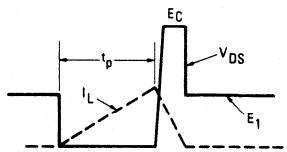


Fig. 16 – Clamped Inductive Waveforms

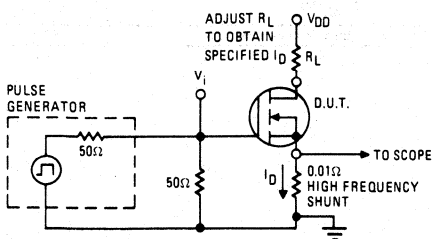


Fig. 17 – Switching Time Test Circuit

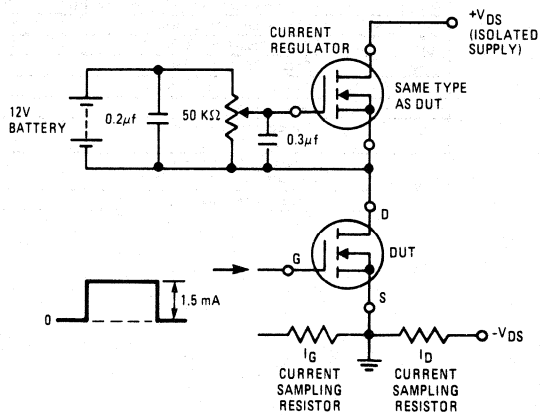


Fig. 18 – Gate Charge Test Circuit

IRFF320, IRFF321, IRFF322, IRFF323

File Number **1890**

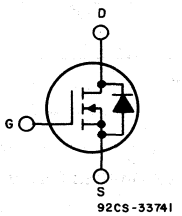
N-Channel Enhancement-Mode Power Field-Effect Transistors

2.0A and 2.5A, 350V - 400V
$r_{DS(on)}$ = 1.8Ω and 2.5Ω

Features:

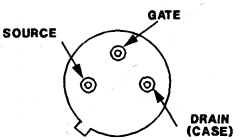
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF320, IRFF321, IRFF322 and IRFF323 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

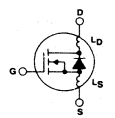
Absolute Maximum Ratings

Parameter		IRFF320	IRFF321	IRFF322	IRFF323	Units
V_{DS}	Drain – Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF320 IRFF322	400	–	–	V	V_{GS} = 0V
		IRFF321 IRFF323	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF320 IRFF321	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF322 IRFF323	2.0	–	–	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF320 IRFF321	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.25A
		IRFF322 IRFF323	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 5.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

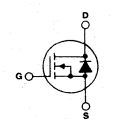


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF320 IRFF321	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF322 IRFF323	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF320 IRFF321	–	–	10	A	
		IRFF322 IRFF323	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRFF320 IRFF321	–	–	1.6	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRFF322 IRFF323	–	–	1.5	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRFF320, IRFF321, IRFF322, IRFF323

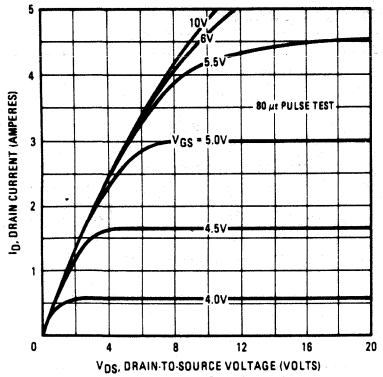


Fig. 1 - Typical output characteristics.

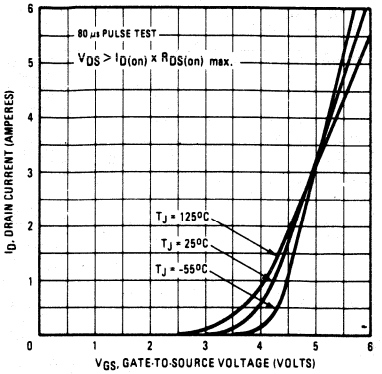


Fig. 2 - Typical transfer characteristics.

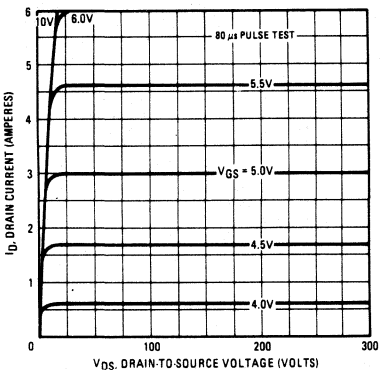


Fig. 3 - Typical saturation characteristics.

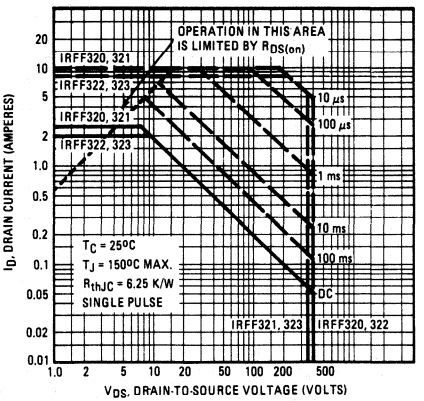


Fig. 4 - Maximum safe operating area.

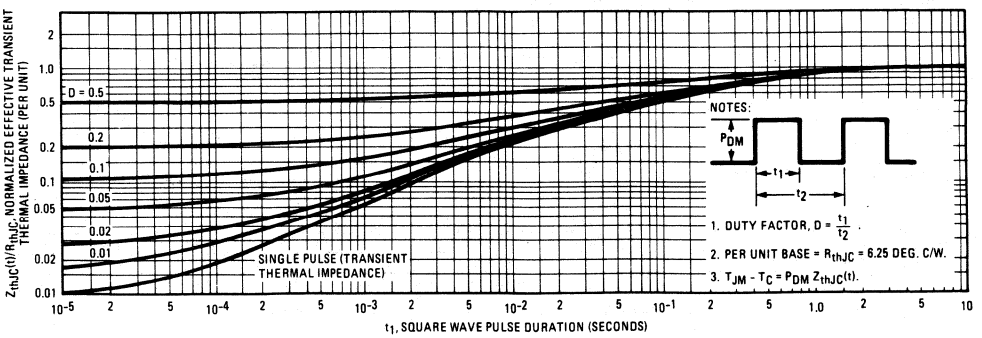


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

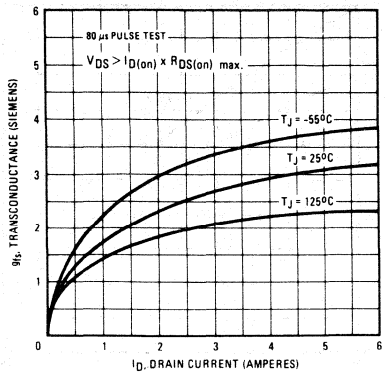


Fig. 6 - Typical transconductance vs. drain current.

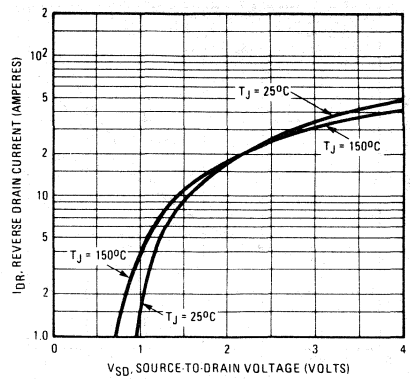


Fig. 7 - Typical source-drain diode forward voltage.

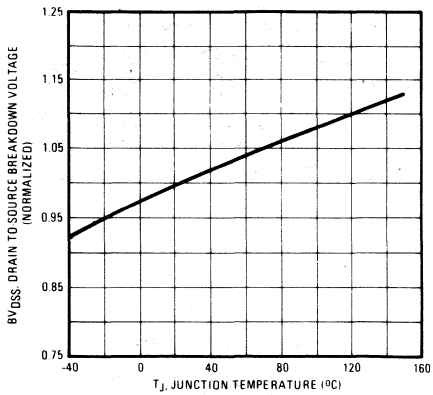


Fig. 8 - Breakdown voltage vs. temperature.

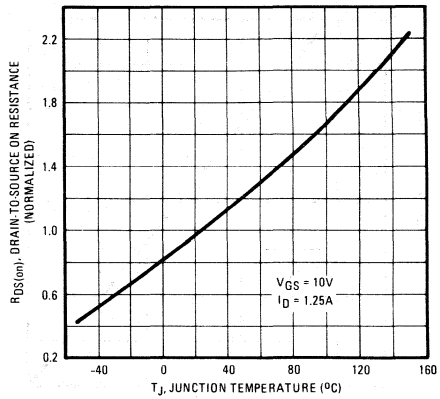


Fig. 9 - Normalized on-resistance vs. temperature.

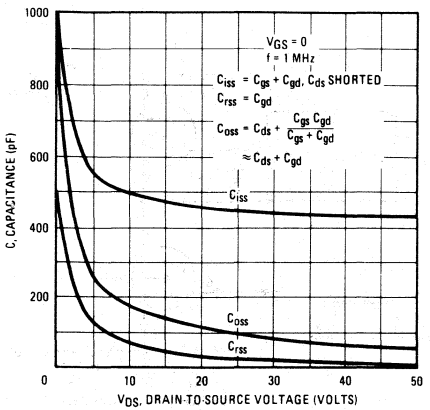


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

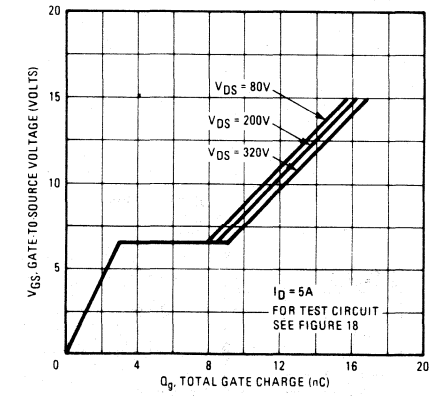


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF320, IRFF321, IRFF322, IRFF323

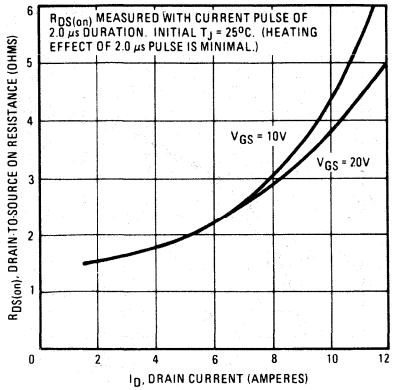


Fig. 12 - Typical on-resistance vs. drain current.

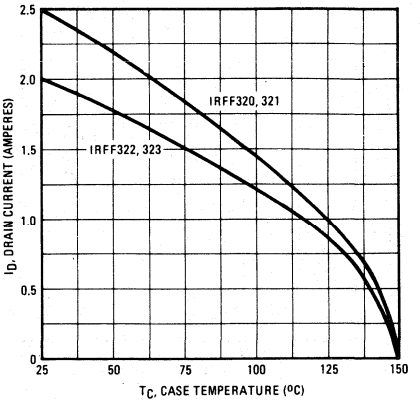


Fig. 13 - Maximum drain current vs. case temperature.

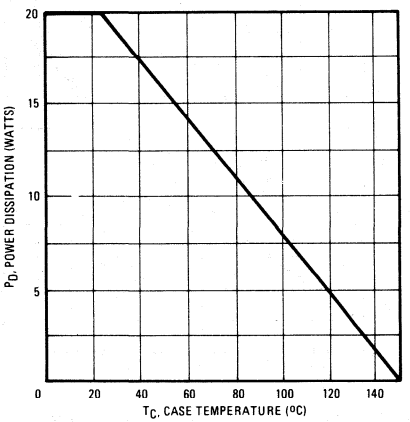


Fig. 14 - Power vs. temperature derating curve.

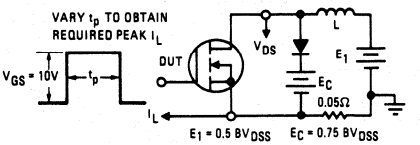


Fig. 15 - Clamped inductive test circuit.

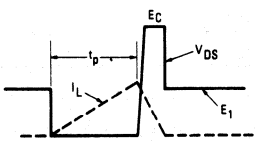


Fig. 16 - Clamped inductive waveforms.

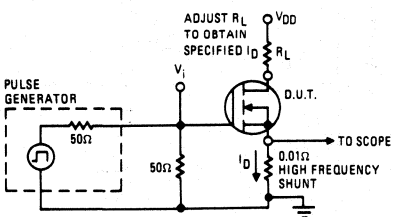


Fig. 17 - Switching time test circuit.

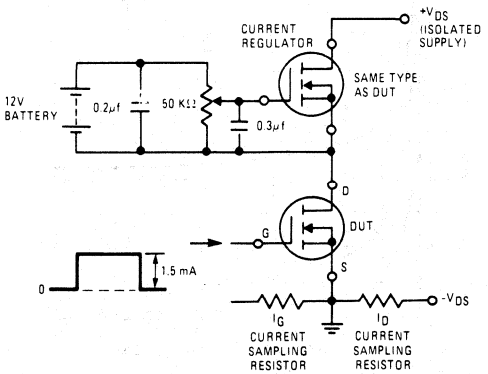


Fig. 18 - Gate charge test circuit.

File Number **1893**

IRFF330, IRFF331, IRFF332, IRFF333

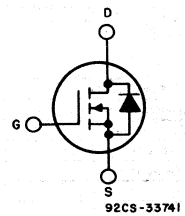
N-Channel Enhancement-Mode Power Field-Effect Transistors

3.0A and 3.5A, 350V - 400V
$r_{DS(on)}$ = 1.0Ω and 1.5Ω

Features:

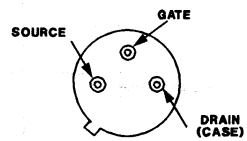
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF330, IRFF331, IRFF332 and IRFF333 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

Absolute Maximum Ratings

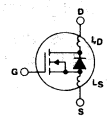
Parameter		IRFF330	IRFF331	IRFF332	IRFF333	Units
V_{DS}	Drain – Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		14	14	12	12	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF330, IRFF331, IRFF332, IRFF333

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFF330 IRFF332	400	–	–	V	V_{GS} = 0V
		IRFF331 IRFF333	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF330 IRFF331	3.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF332 IRFF333	3.0	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFF330 IRFF331	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 2.0A
		IRFF332 IRFF333	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.0	3.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.0A
C_{iss}	Input Capacitance	ALL	–	700	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 2.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	17	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	11	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

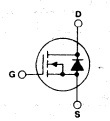


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF330 IRFF331	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF332 IRFF333	–	–	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF330 IRFF331	–	–	14	A	
		IRFF332 IRFF333	–	–	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF330 IRFF331	–	–	1.6	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF332 IRFF333	–	–	1.5	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

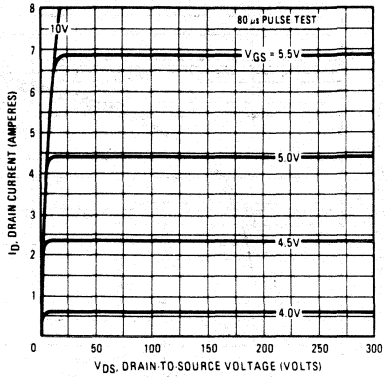


Fig. 1 - Typical output characteristics.

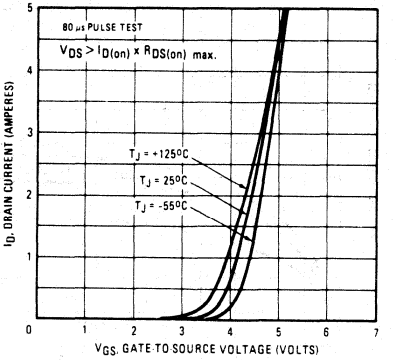


Fig. 2 - Typical transfer characteristics.

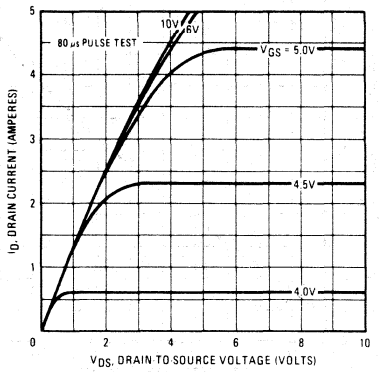


Fig. 3 - Typical saturation characteristics.

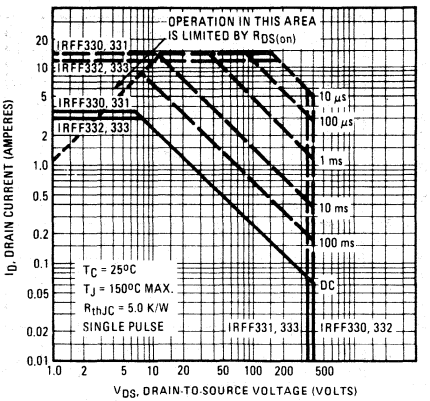


Fig. 4 - Maximum safe operating area.

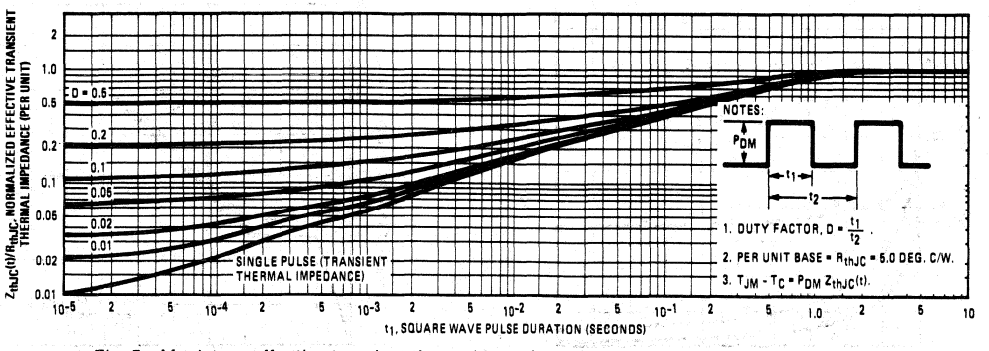


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFF330, IRFF331, IRFF332, IRFF333

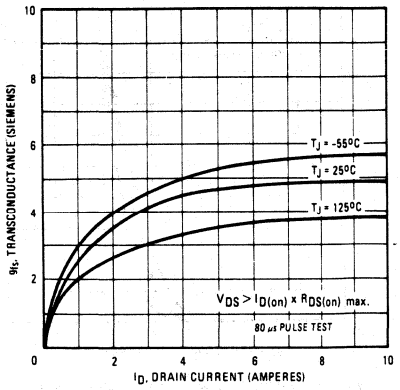


Fig. 6 - Typical transconductance vs. drain current.

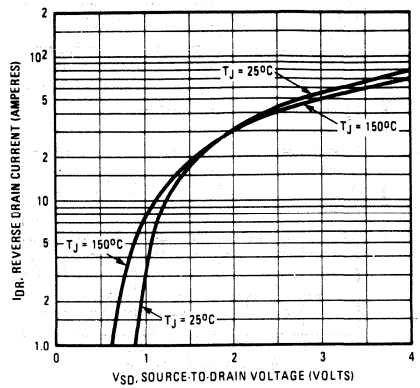


Fig. 7 - Typical source-drain diode forward voltage.

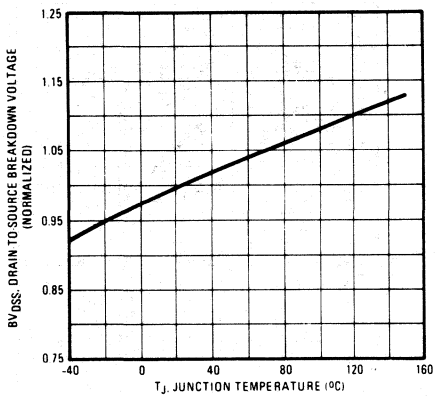


Fig. 8 - Breakdown voltage vs. temperature.

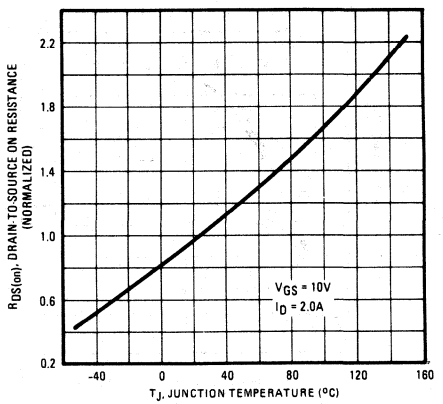


Fig. 9 - Normalized on-resistance vs. temperature.

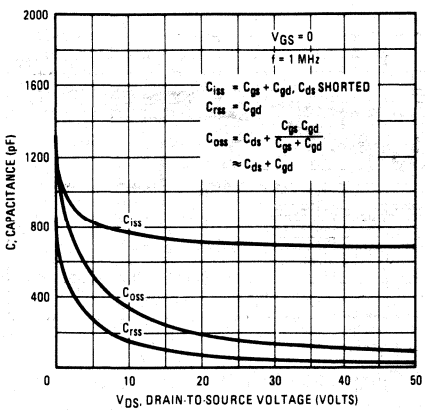


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

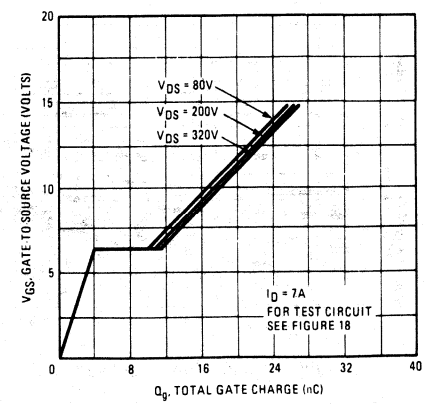


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

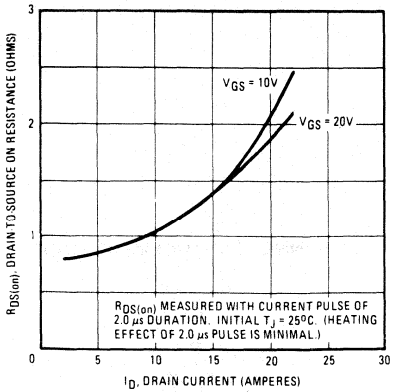


Fig. 12 - Typical on-resistance vs. drain current.

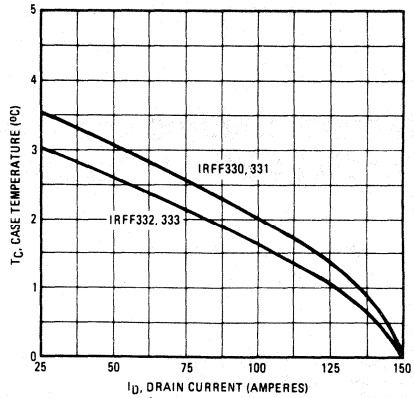


Fig. 13 - Maximum drain current vs. case temperature.

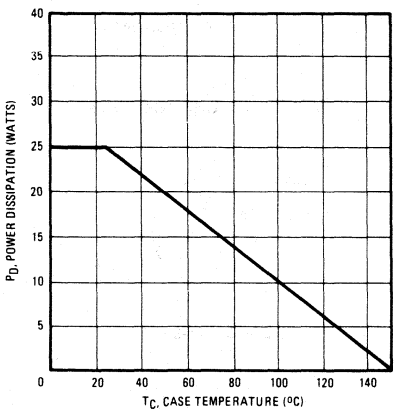


Fig. 14 - Power vs. temperature derating curve.

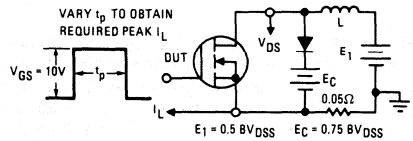


Fig. 15 - Clamped inductive test circuit.

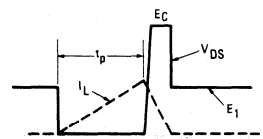


Fig. 16 - Clamped inductive waveforms.

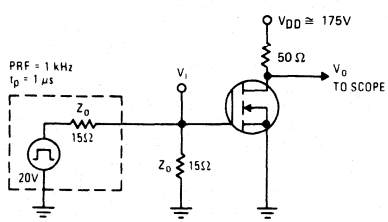


Fig. 17 - Switching time test circuit.

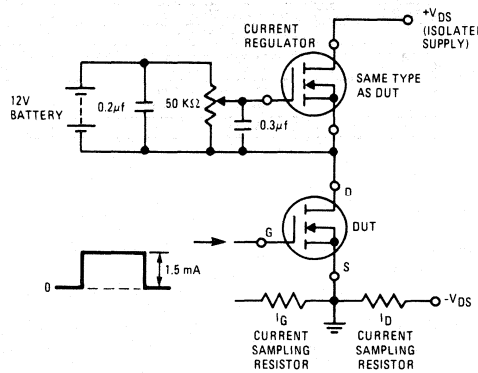


Fig. 18 - Gate charge test circuit.

IRFF420, IRFF421, IRFF422, IRFF423

File Number **1891**

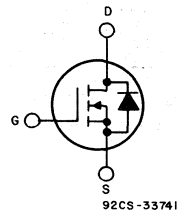
N-Channel Enhancement-Mode Power Field-Effect Transistors

1.4A and 1.6A, 450V - 500V
$r_{DS(on)}$ = 3.0Ω and 4.0Ω

Features:

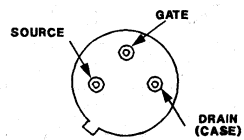
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF420, IRFF421, IRFF422 and IRFF423 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

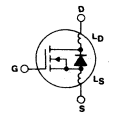
Absolute Maximum Ratings

Parameter		IRFF420	IRFF421	IRFF422	IRFF423	Units
V_{DS}	Drain — Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 20 kΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	1.6	1.6	1.4	1.4	A
I_{DM}	Pulsed Drain Current ③	6.5	6.5	5.5	5.5	A
V_{GS}	Gate — Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		6.5	6.5	5.5	5.5	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF420, IRFF422	500	–	–	V	V_{GS} = 0V
		IRFF421, IRFF423	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF420, IRFF421	1.6	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF422, IRFF423	1.4	–	–	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF420, IRFF421	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRFF422, IRFF423	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	7.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	9.0	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

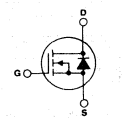


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF420, IRFF421	–	–	1.8	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF422, IRFF423	–	–	1.4	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF420, IRFF421	–	–	6.5	A	
		IRFF422, IRFF423	–	–	5.5	A	
V_{SD}	Diode Forward Voltage ②	IRFF420, IRFF421	–	–	1.4	V	T_C = 25°C, I_S = 1.8A, V_{GS} = 0V
		IRFF422, IRFF423	–	–	1.3	V	T_C = 25°C, I_S = 1.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 1.8A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 1.8A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRFF420, IRFF421, IRFF422, IRFF423

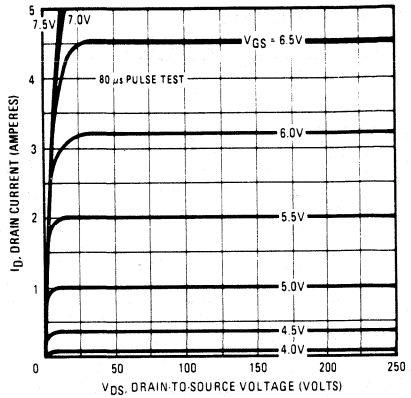


Fig. 1 - Typical output characteristics.

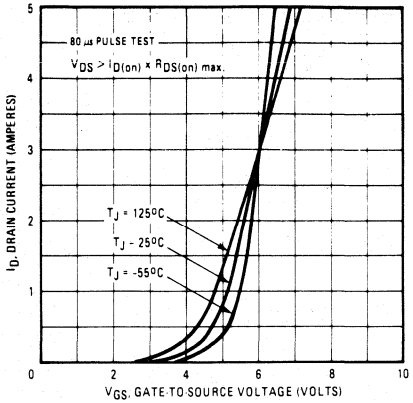


Fig. 2 - Typical transfer characteristics.

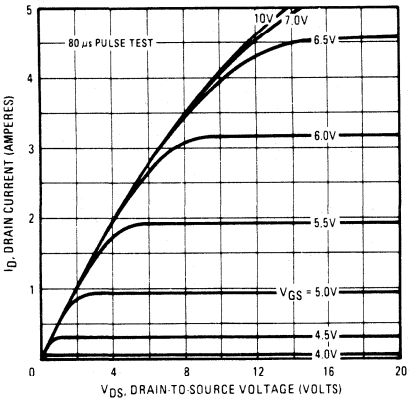


Fig. 3 - Typical saturation characteristics.

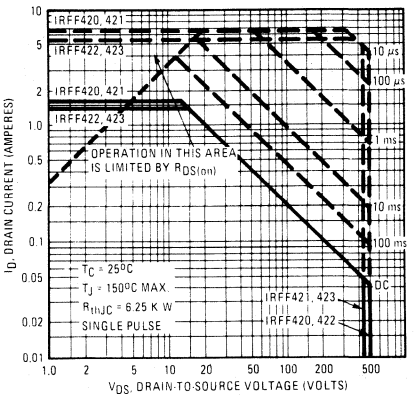


Fig. 4 - Maximum safe operating area.

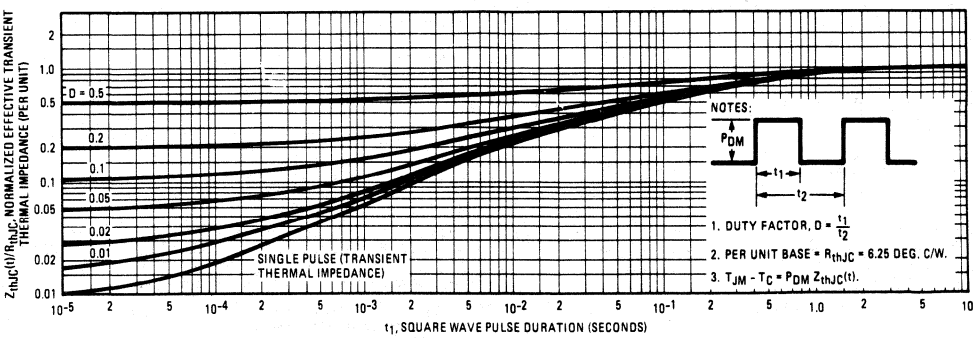


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

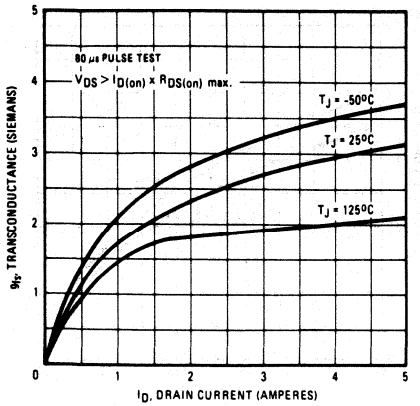


Fig. 6 - Typical transconductance vs. drain current.

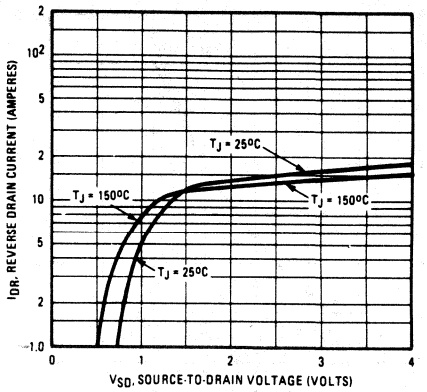


Fig. 7 - Typical source-drain diode forward voltage.

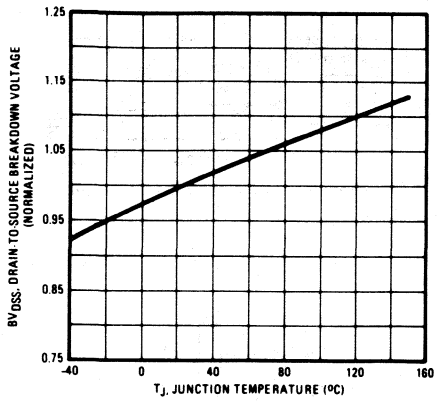


Fig. 8 - Breakdown voltage vs. temperature.

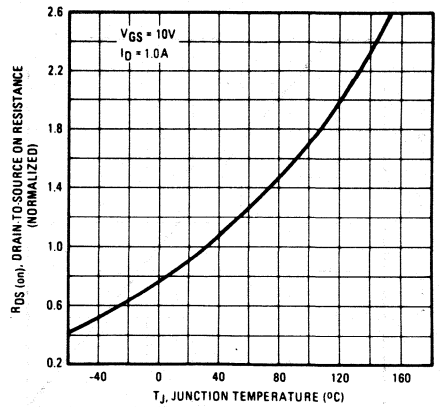


Fig. 9 - Normalized on-resistance vs. temperature.

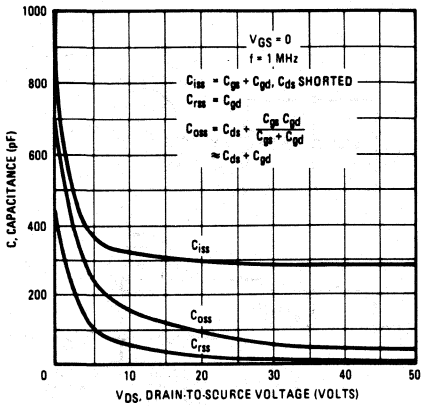


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

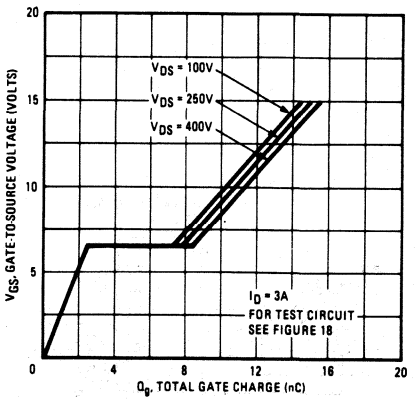


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF420, IRFF421, IRFF422, IRFF423

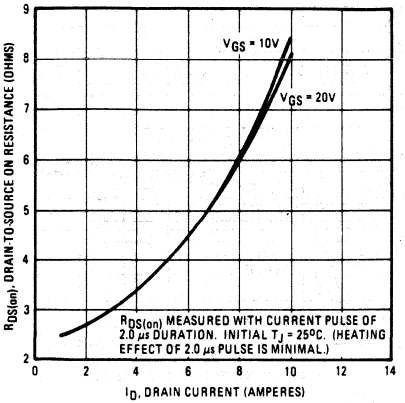


Fig. 12 - Typical on-resistance vs. drain current.

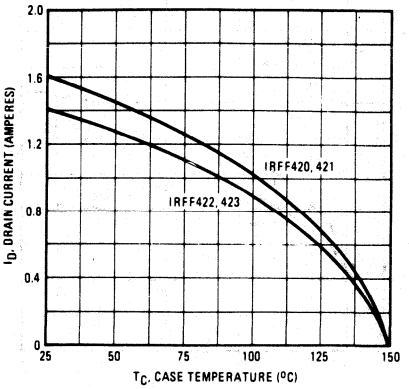
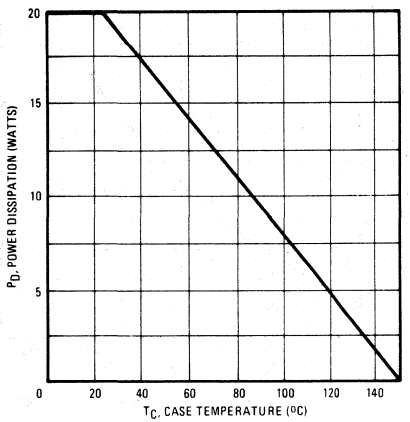


Fig. 13 - Maximum drain current vs. case temperature.



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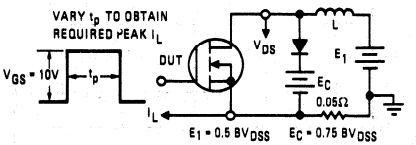


Fig. 15 - Clamped inductive test circuit.

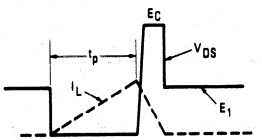


Fig. 16 - Clamped inductive waveforms.

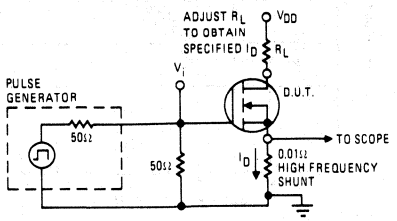


Fig. 17 - Switching time test circuit.

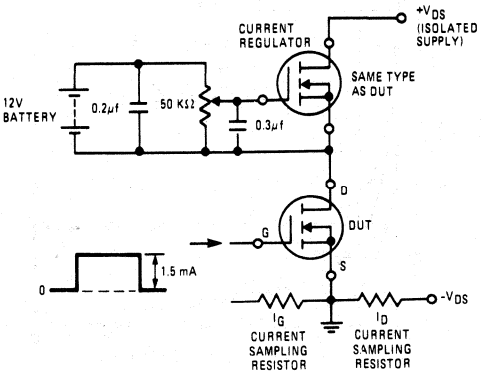


Fig. 18 - Gate charge test circuit.

File Number **1894**

IRFF430, IRFF431, IRFF432, IRFF433

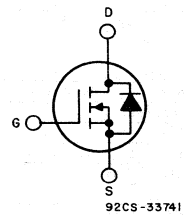
N-Channel Enhancement-Mode Power Field-Effect Transistors

2.25A and 2.75A, 450V - 500V
$r_{DS(on)}$ = 1.5Ω and 2.0Ω

Features:

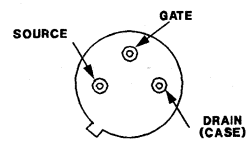
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF430, IRFF431, IRFF432 and IRFF433 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

Absolute Maximum Ratings

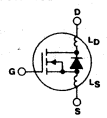
Parameter		IRFF430	IRFF431	IRFF432	IRFF433	Units
V_{DS}	Drain – Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.75	2.75	2.25	2.25	A
I_{DM}	Pulsed Drain Current ③	11	11	9.0	9.0	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		11	11	9.0	9.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF430, IRFF431, IRFF432, IRFF433

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFF430 /IRFF432	500	–	–	V	V_{GS} = 0V
		IRFF431 IRFF433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF430 IRFF431	2.75	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF432 IRFF433	2.25	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFF430 IRFF431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF432 IRFF433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 1.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	17	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	17	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

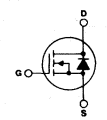


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF430 IRFF431	–	–	2.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF432 IRFF433	–	–	2.25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF430 IRFF431	–	–	11	A	
		IRFF432 IRFF433	–	–	9.0	A	
V_{SD}	Diode Forward Voltage ②	IRFF430 IRFF431	–	–	1.4	V	T_C = 25°C, I_S = 2.75A, V_{GS} = 0V
		IRFF432 IRFF433	–	–	1.3	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

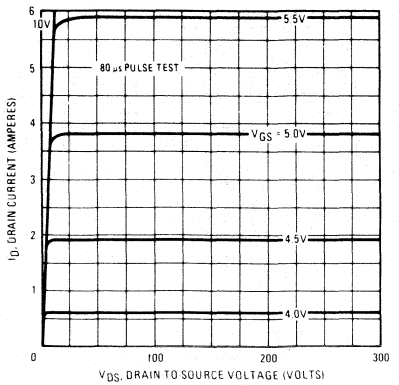


Fig. 1 - Typical output characteristics.

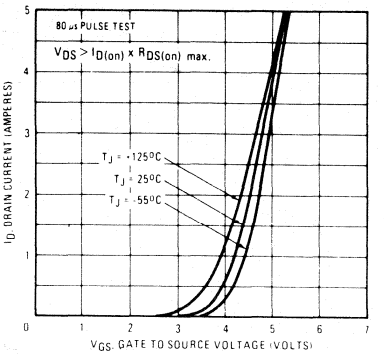


Fig. 2 - Typical transfer characteristics.

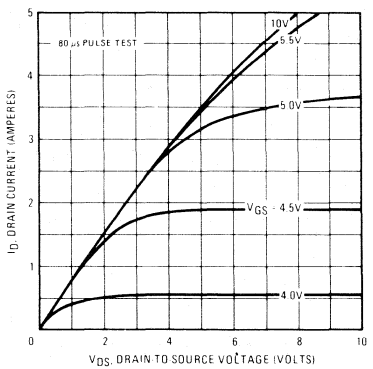


Fig. 3 - Typical saturation characteristics.

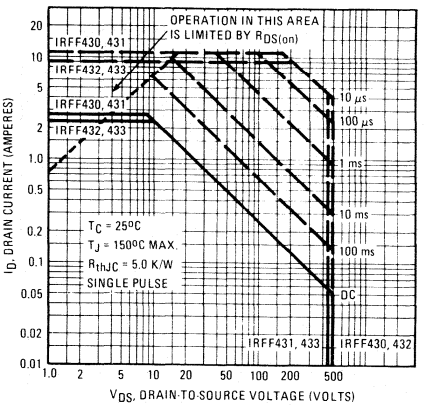


Fig. 4 - Maximum safe operating area.

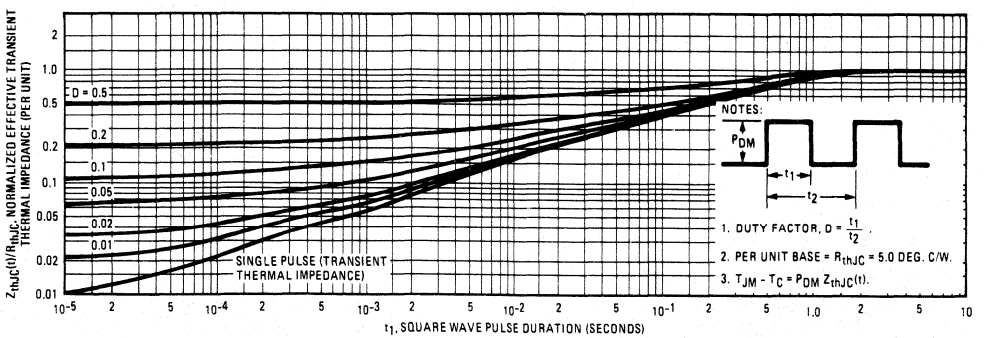


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

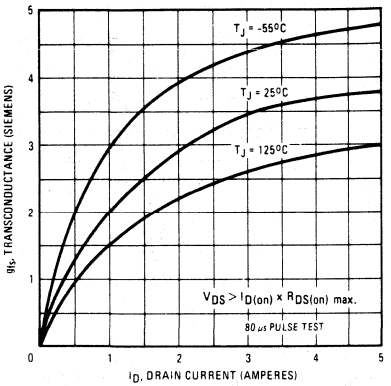


Fig. 6 - Typical transconductance vs. drain current.

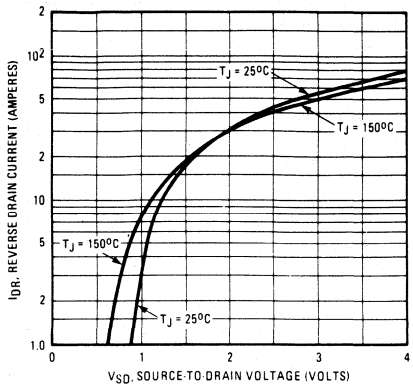


Fig. 7 - Typical source-drain diode forward voltage.

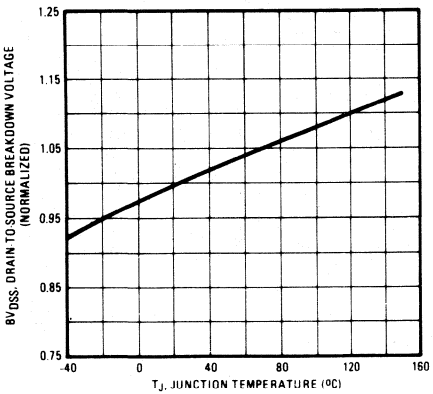


Fig. 8 - Breakdown voltage vs. temperature.

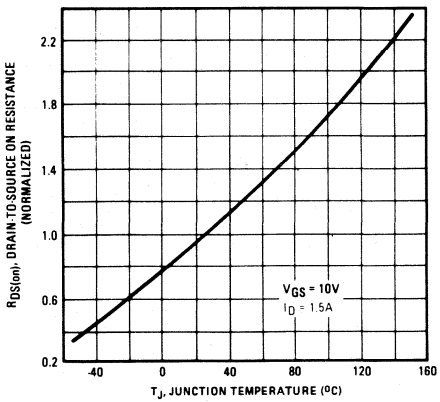


Fig. 9 - Normalized on-resistance vs. temperature.

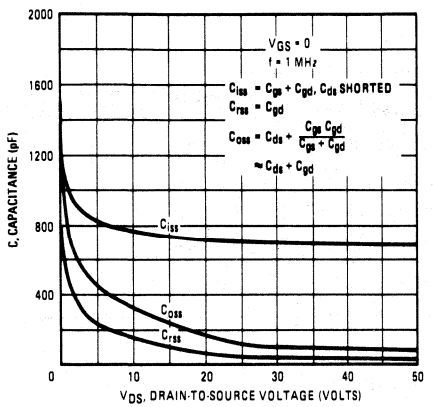


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

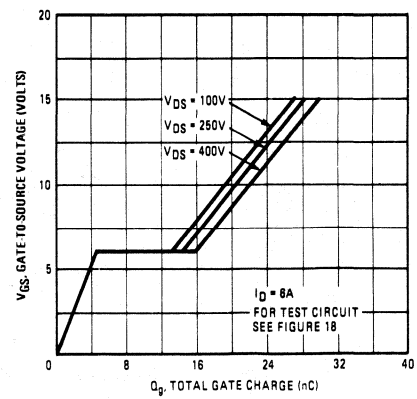


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

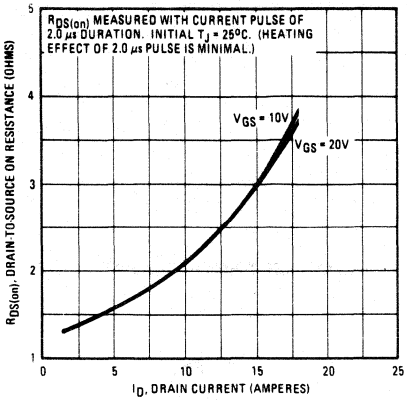


Fig. 12 - Typical on-resistance vs. drain current.

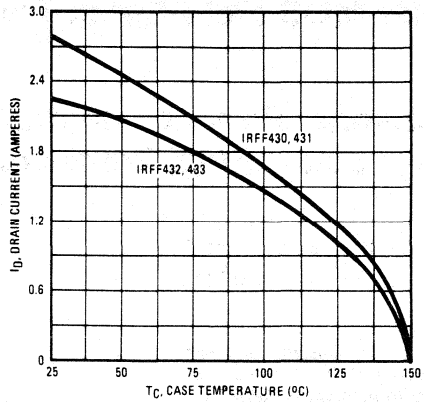


Fig. 13 - Maximum drain current vs. case temperature.

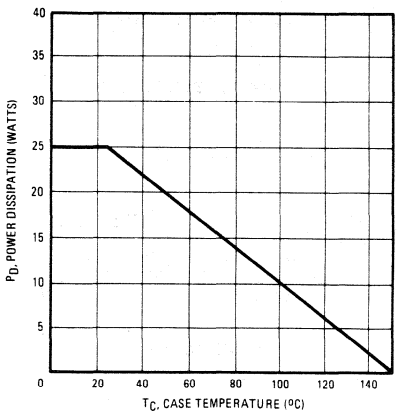


Fig. 14 - Power vs. temperature derating curve.

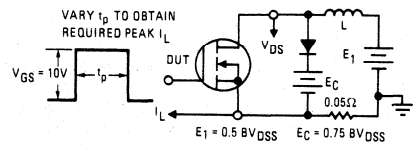


Fig. 15 - Clamped inductive test circuit.

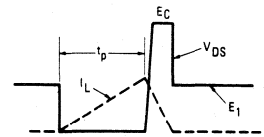


Fig. 16 - Clamped inductive waveforms.

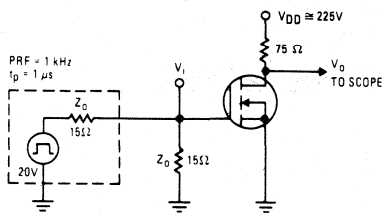


Fig. 17 - Switching time test circuit.

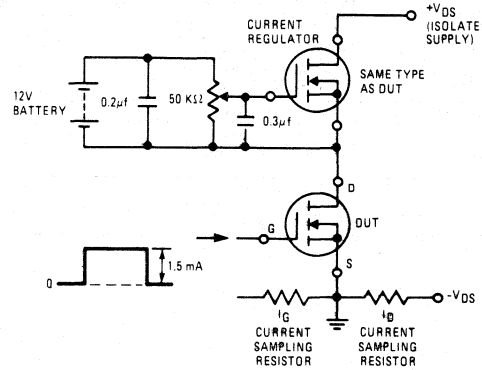


Fig. 18 - Gate charge test circuit.

IRFP150, IRFP151, IRFP152, IRFP153

File Number **2318**

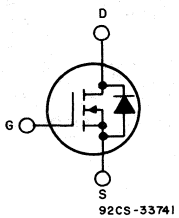
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

34 A and 40 A, 60 V - 100 V
$r_{DS(on)}$ = 0.055 Ω and 0.08 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

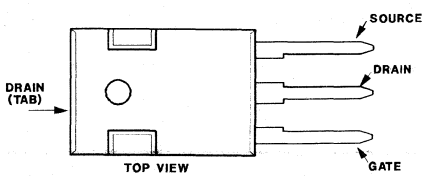


TERMINAL DIAGRAM

The IRFP150, IRFP151, IRFP152, and IRFP153 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

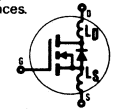
Absolute Maximum Ratings

	Parameter	IRFP150	IRFP151	IRFP152	IRFP153	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current ⑤	40		34		A
I_D @ T_C = 100°C	Continuous Drain Current	26		22		A
I_{DM}	Pulsed Drain Current ②	160		140		A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	180				W
	Linear Derating Factor	1.4				W/°C
I_{LM}	Inductive Current, Clamped	160	(See Fig. 14) L = 100μH	140		A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP150 IRFP152	100	–	–	V	V_{GS} = 0V
		IRFP151 IRFP153	60	–	–	V	I_D = 250 μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating × 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ④ ⑤	IRFP150 IRFP151	40	–	–	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)max.}$, V_{GS} = 10V
		IRFP152 IRFP153	34	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ④	IRFP150 IRFP151	–	0.045	0.055	Ω	V_{GS} = 10V, I_D = 22A
		IRFP152 IRFP153	–	0.060	0.080	Ω	
g_{fs}	Forward Transconductance ④	ALL	13	20	–	S (℧)	V_{DS} = 2 × V_{GS}, I_{DS} = 20.5
C_{iss}	Input Capacitance	ALL	–	2400	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	–	1000	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	–	200	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	24	ns	V_{DD} = 50V, I_D ≈ 38A, R_G = 6.8Ω, R_D = 1.3Ω
t_r	Rise Time	ALL	–	140	210	ns	See Fig. 16
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	59	89	ns	(MOSFET switching times are essentially independent of
t_f	Fall Time	ALL	–	92	140	ns	operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	73	110	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially
Q_{gs}	Gate-Source Charge	ALL	–	18	27	nC	independent of operating temperature.)
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	41	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP150 IRFP151	–	–	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP152 IRFP153	–	–	34	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP150 IRFP151	–	–	170	A	
		IRFP152 IRFP153	–	–	140	A	
V_{SD}	Diode Forward Voltage ②	ALL	–	–	2.5	V	T_C = 25°C, I_S = 41A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	98	220	530	ns	T_J = 25°C, I_F = 38A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	0.41	0.97	2.5	μC	T_J = 25°C, I_F = 38A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.70	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.10	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	40	°C/W	Typical socket mount
	Mounting Torque	ALL	–	–	10	in. • lbs.	Standard 6-32 screw

① T_J = 25°C to 150°C.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ @ V_{dd} = 25V, T_j = 25°C, L = 100 μH, RG = 25Ω

④ Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

⑤ I_D current limited by pin diameter

IRFP150, IRFP151, IRFP152, IRFP153

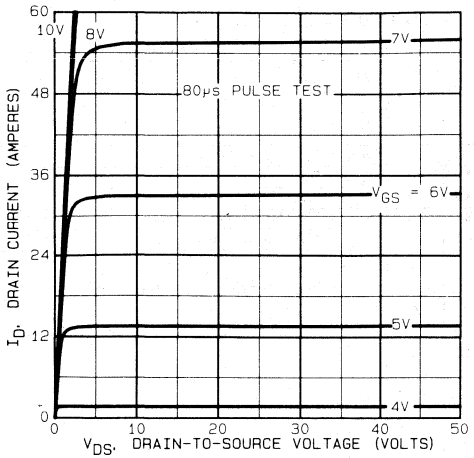


Fig. 1 — Typical Output Characteristics

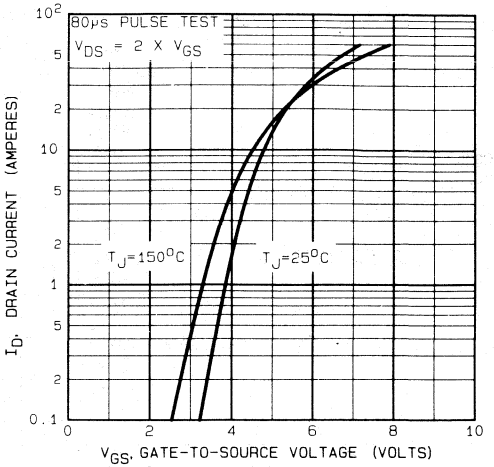


Fig. 2 — Typical Transfer Characteristics

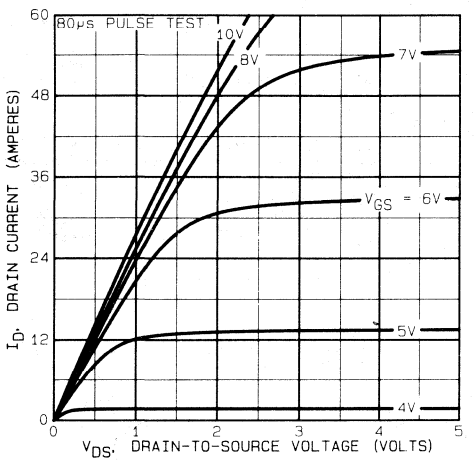


Fig. 3 — Typical Saturation Characteristics

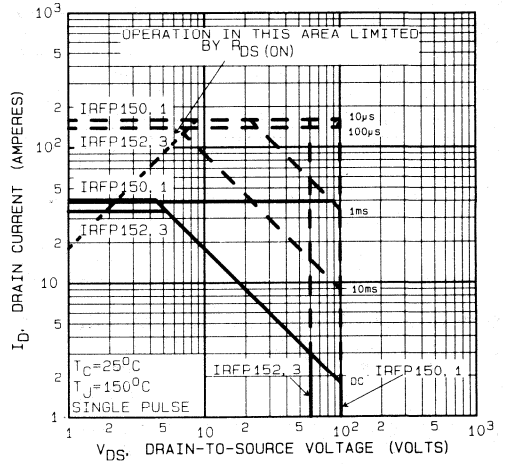


Fig. 4 — Maximum Safe Operating Area

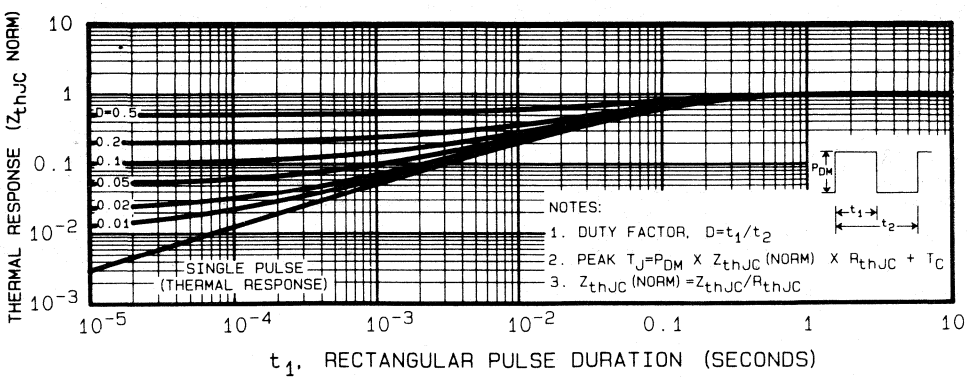


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to Case Vs. Pulse Duration

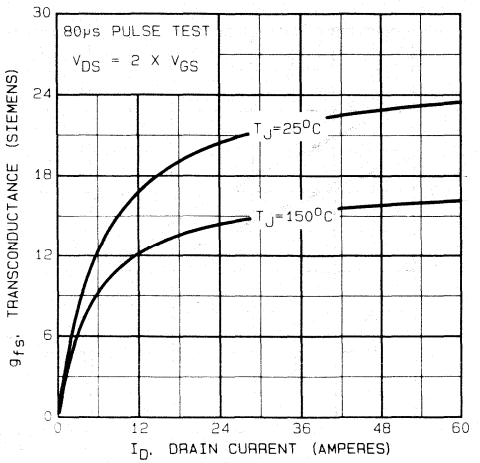


Fig. 6 — Typical Transconductance Vs. Drain Current

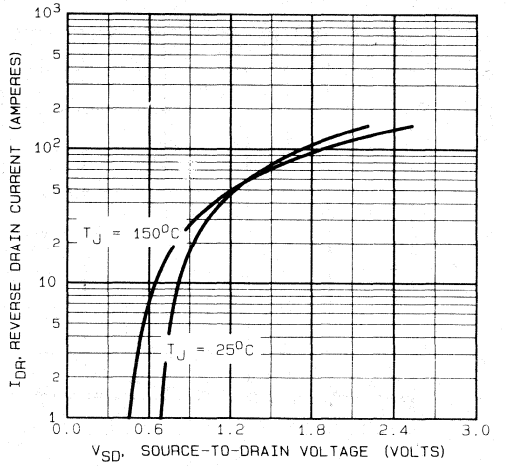


Fig. 7 — Typical Source-Drain Diode Forward Voltage

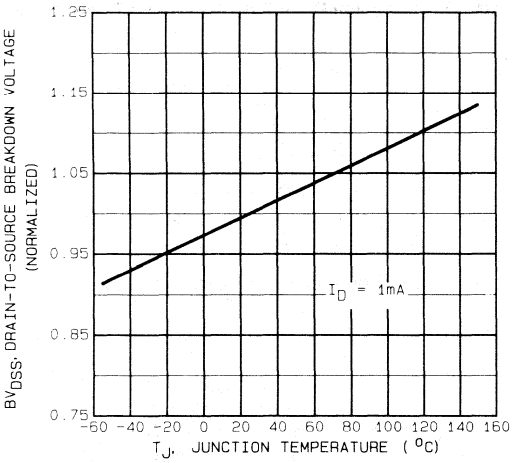


Fig. 8 — Breakdown Voltage Vs. Temperature

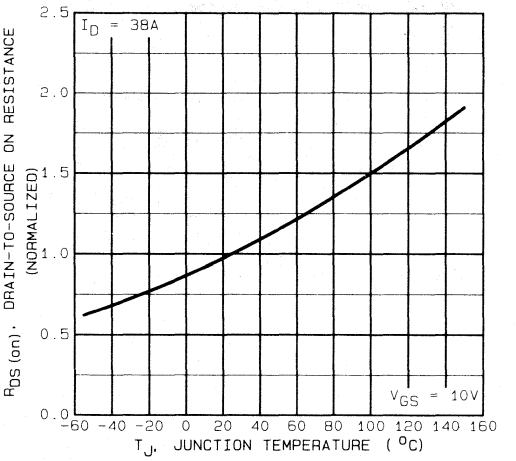


Fig. 9 — Normalized On-Resistance Vs. Temperature

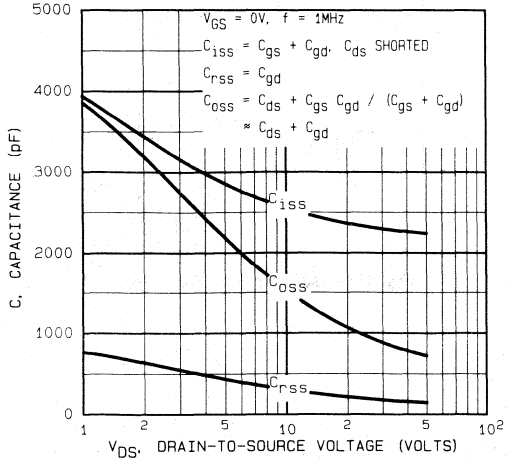


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

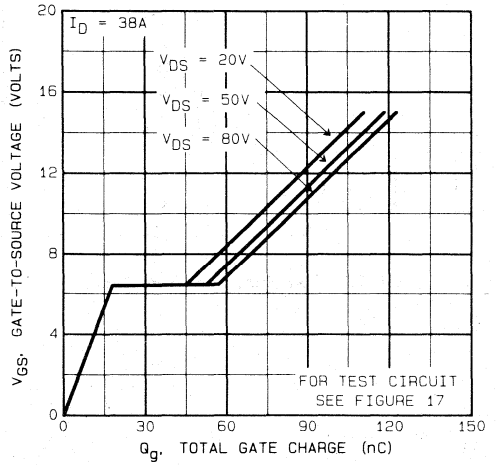


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRFP150, IRFP151, IRFP152, IRFP153

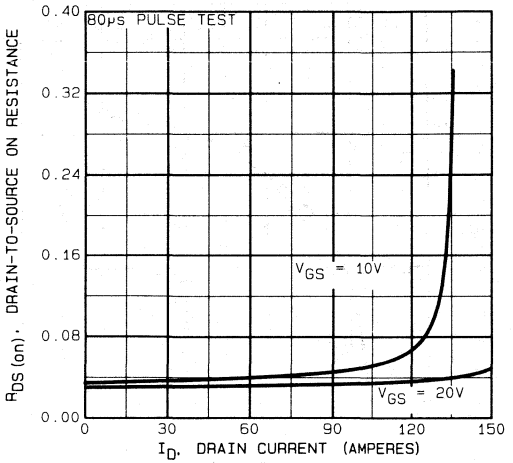


Fig. 12 — Typical On-Resistance Vs. Drain Current

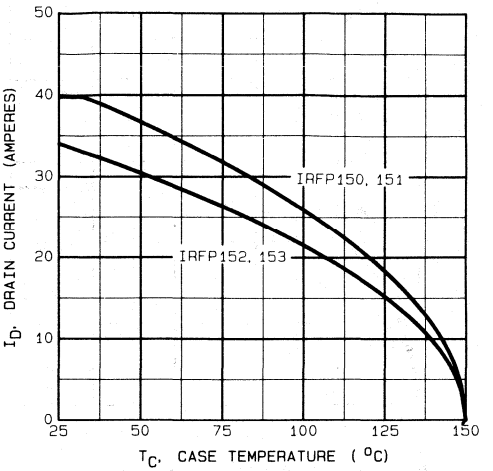


Fig. 13 — Maximum Drain Current Vs. Case Temperature

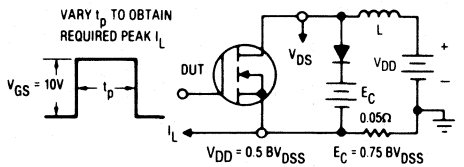


Fig. 14 — Clamped Inductive Test Circuit

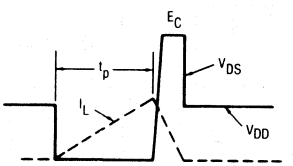


Fig. 15 — Clamped Inductive Waveforms

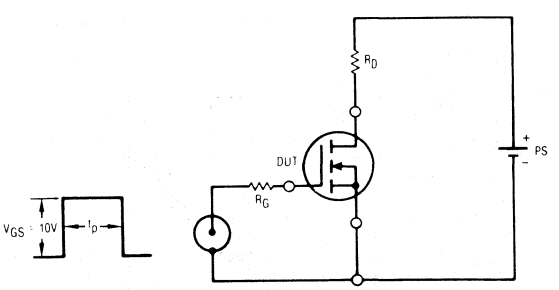


Fig. 16 — Switching Time Test Circuit

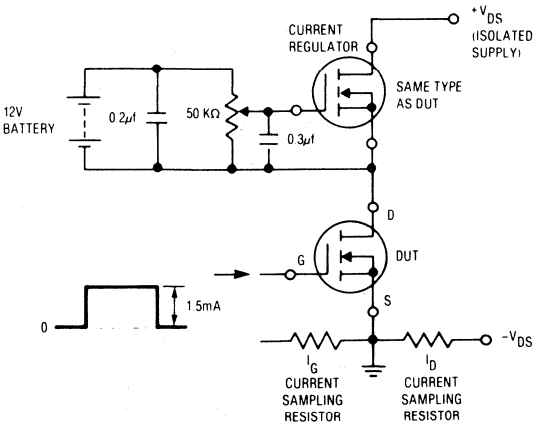


Fig. 17 — Gate Charge Test Circuit

File Number **2330**

IRFP250, IRFP251, IRFP252, IRFP253

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

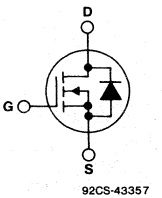
25 A and 30 A, 150 V - 200 V
$r_{DS(on)}$ = 0.085 Ω and 0.120 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRFP250, IRFP251, IRFP252, and IRFP253 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

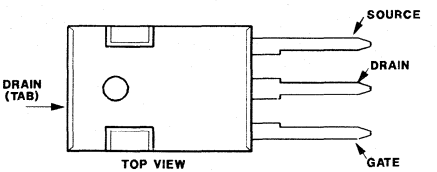
N-CHANNEL ENHANCEMENT MODE



92CS-43357

TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-247

Absolute Maximum Ratings

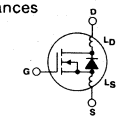
Parameter		IRFP250	IRFP251	IRFP252	IRFP253	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	30	30	25	25	A
I_D @ T_C = 100°C	Continuous Drain Current	19	19	16	16	A
I_{DM}	Pulsed Drain Current ③	120	120	100	100	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped ④	120	120	100	100	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP250, IRFP251, IRFP252, IRFP253

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP250 IRFP252	200	—	—	V	V_{GS} = 0V
		IRFP251 IRFP253	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP250 IRFP251	30	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRFP252 IRFP253	25	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP250 IRFP251	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 16A
		IRFP252 IRFP253	—	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 16A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	800	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	300	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 95V, I_D = 16A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	125	ns	
t_f	Fall Time	ALL	—	—	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	37	56	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	42	63	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

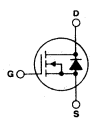


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP250 IRFP251	—	—	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP252 IRFP253	—	—	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP250 IRFP251	—	—	120	A	
		IRFP252 IRFP253	—	—	100	A	
V_{SD}	Diode Forward Voltage ②	IRFP250 IRFP251	—	—	2.0	V	T_C = 25°C, I_S = 30A, V_{GS} = 0V
		IRFP252 IRFP253	—	—	1.8	V	T_C = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	750	—	ns	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.7	—	μC	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ L = 100 μH (See Fig. 15)

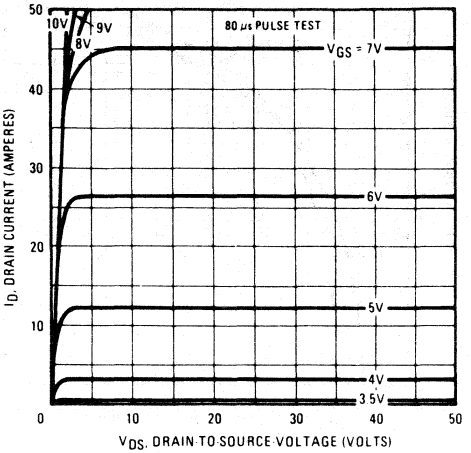


Fig. 1 — Typical Output Characteristics

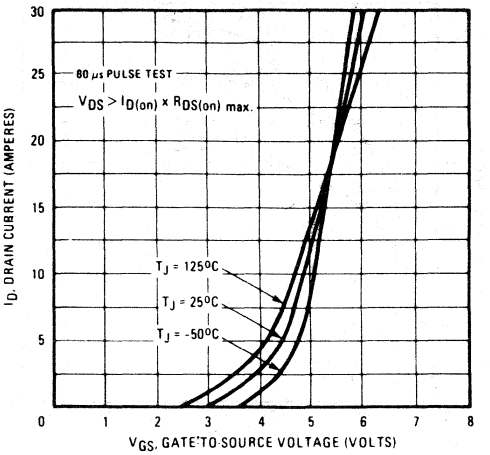


Fig. 2 — Typical Transfer Characteristics

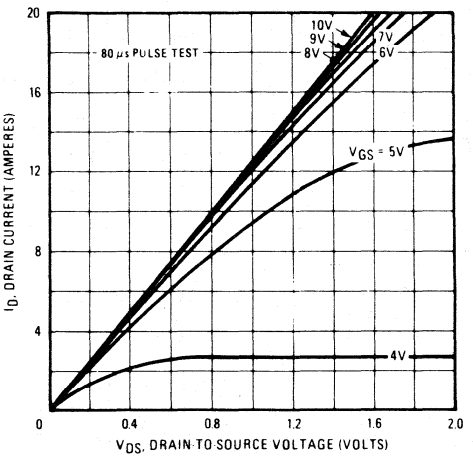


Fig. 3 — Typical Saturation Characteristics

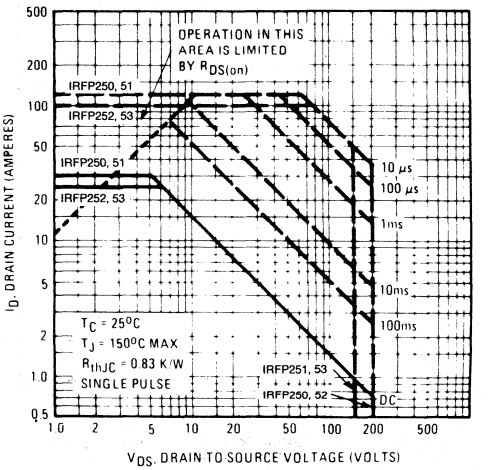


Fig. 4 — Maximum Safe Operating Area

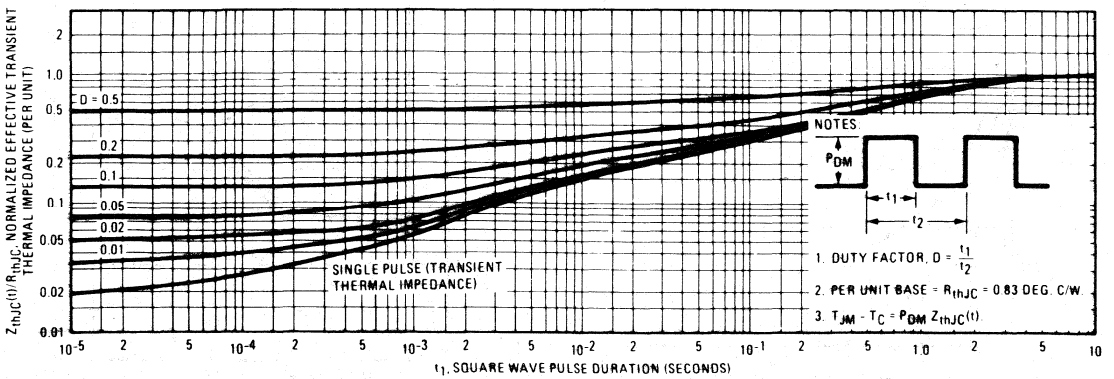


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFP250, IRFP251, IRFP252, IRFP253

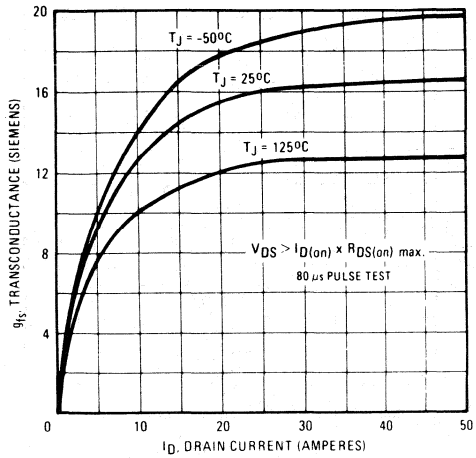


Fig. 6 — Typical Transconductance Vs. Drain Current

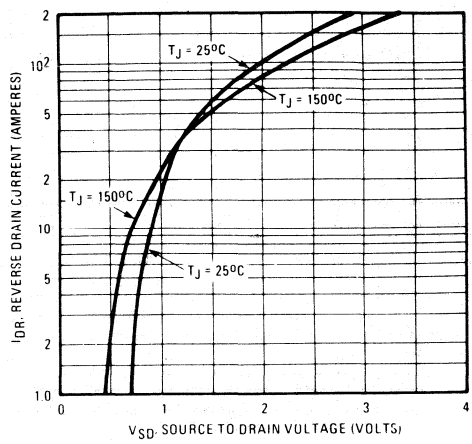


Fig. 7 — Typical Source-Drain Diode Forward Voltage

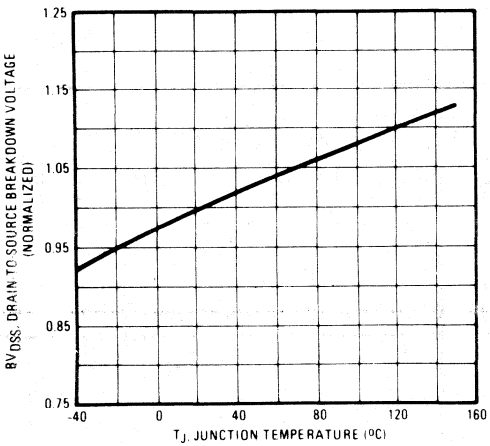


Fig. 8 — Breakdown Voltage Vs. Temperature

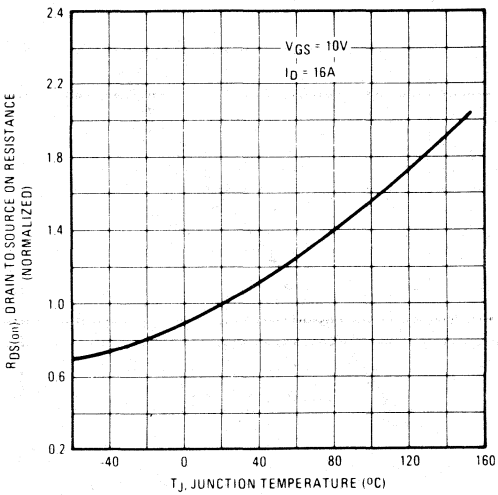


Fig. 9 — Normalized On-Resistance Vs. Temperature

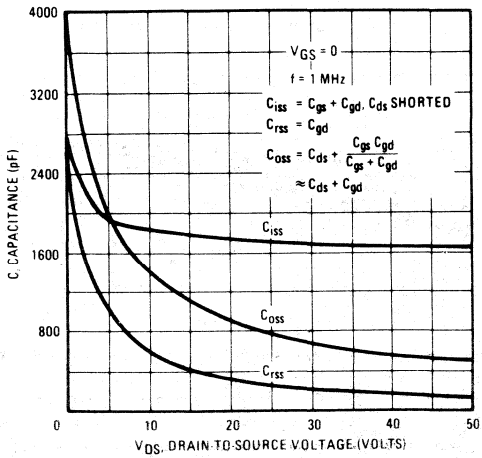


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

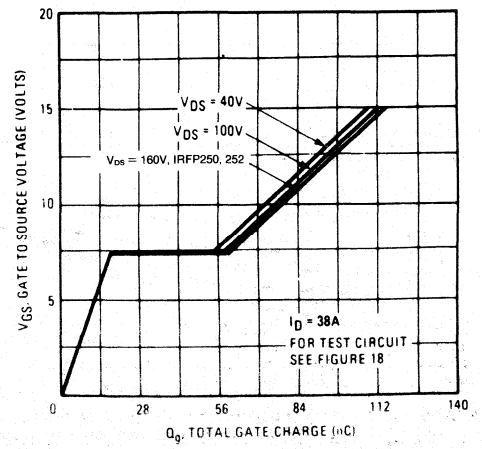


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

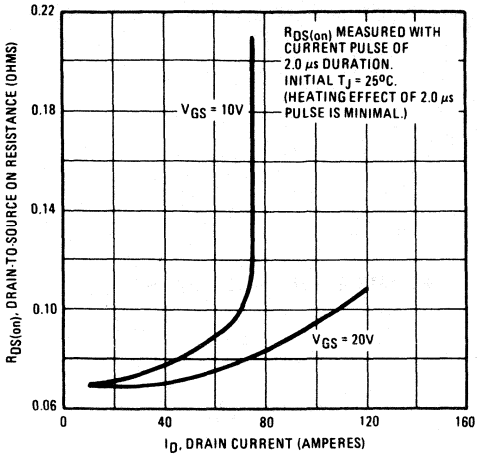


Fig. 12 – Typical On-Resistance Vs. Drain Current

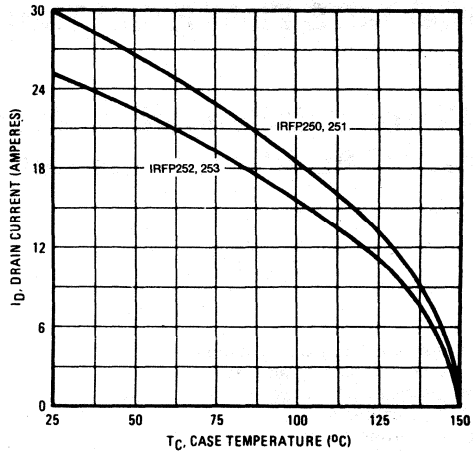


Fig. 13 – Maximum Drain Current Vs. Case Temperature

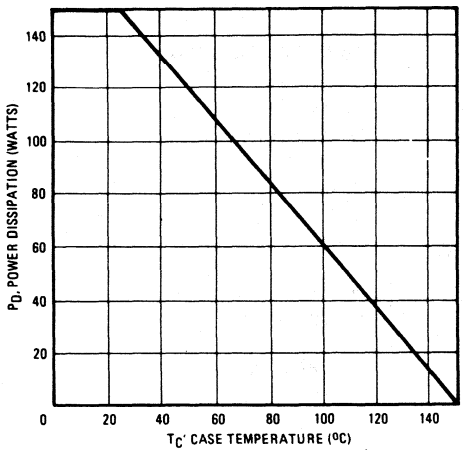


Fig. 14 – Power Vs. Temperature Derating Curve

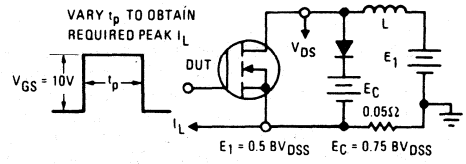


Fig. 15 – Clamped Inductive Test Circuit

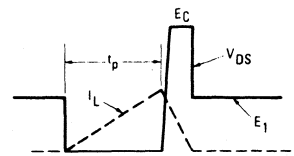


Fig. 16 – Clamped Inductive Waveforms

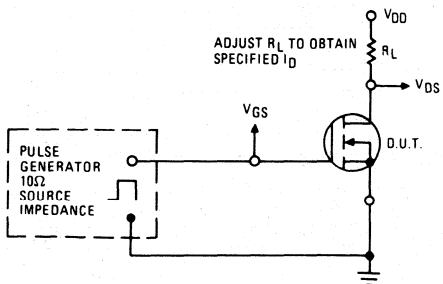


Fig. 17 – Switching Time Test Circuit

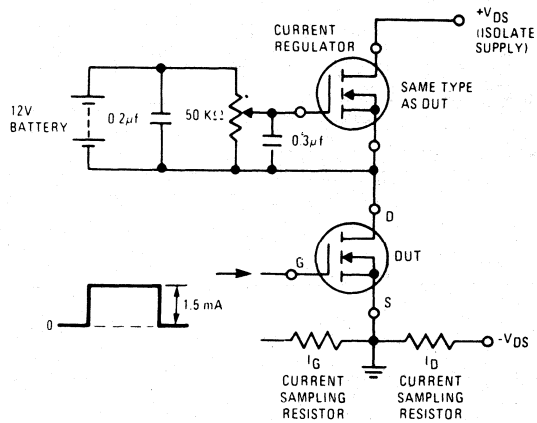


Fig. 18 – Gate Charge Test Circuit

IRFP350, IRFP351, IRFP352, IRFP353

File Number **2319**

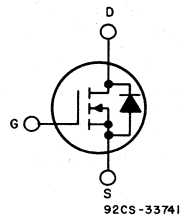
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

14 A and 16 A, 350 V - 400 V
$r_{DS(on)}$ = 0.3 Ω and 0.4 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

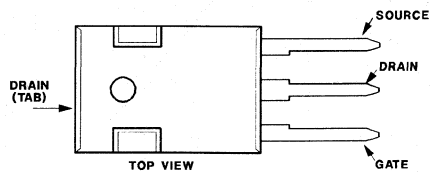


TERMINAL DIAGRAM

The IRFP350, IRFP351, IRFP352, and IRFP353 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

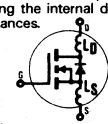
Absolute Maximum Ratings

Parameter		IRFP350	IRFP351	IRFP352	IRFP353	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	16		14		A
I_D @ T_C = 100°C	Continuous Drain Current	10		8.9		A
I_{DM}	Pulsed Drain Current ②	64		56		A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	180				W
	Linear Derating Factor	1.4				W/°C ⑤
I_{LM}	Inductive Current, Clamped	(See Fig. 14) L = 100μH				A
		64		56		
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP350	400	–	–	V	V_{GS} = 0V
		IRFP352					
		IRFP351	350	–	–	V	I_D = 250 μA
		IRFP353					
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating × 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ④	IRFP350	16	–	–	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)max.}$, V_{GS} = 10V
		IRFP351					
		IRFP352	14	–	–	A	
		IRFP353					
$R_{DS(on)}$	Static Drain-Source On-State Resistance ④	IRFP350	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 8.9A
		IRFP351					
		IRFP352	–	0.30	0.40	Ω	
		IRFP353					
g_{fs}	Forward Transconductance ④	ALL	8.0	12	–	S(℧)	V_{DS} = 2 × V_{GS}, I_{DS} = 8.0
C_{iss}	Input Capacitance	ALL	–	2400	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	–	460	–	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	–	99	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	12	18	ns	V_{DD} = 200V, I_D ≈ 15A, R_G = 6.2Ω, R_D = 13Ω
t_r	Rise Time	ALL	–	51	77	ns	See Fig. 16
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	75	110	ns	(MOSFET switching times are essentially independent of
t_f	Fall Time	ALL	–	47	71	ns	operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	87	130	nC	V_{GS} = 10V, I_D = 15A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	15	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	33	50	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.70	°C/W⑤	
R_{thCS}	Case-to-Sink	ALL	–	0.10	–	°C/W⑤	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W⑤	Typical socket mount
	Mounting Torque	ALL	–	–	10	in. • lbs.	Standard 6-32 screw

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP350	–	–	16	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP351					
		IRFP352	–	–	14	A	
		IRFP353					
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP350	–	–	64	A	
		IRFP351					
		IRFP352	–	–	56	A	
		IRFP353					
V_{SD}	Diode Forward Voltage ②	ALL	–	–	1.6	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	270	600	1300	ns	T_J = 25°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	1.7	3.8	8.1	μC	T_J = 25°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ @ V_{dd} = 50V, T_j = 25°C, L = 100 μH, R_G = 25Ω

④ Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

⑤ K/W = °C/W
W/K = W/°C

IRFP350, IRFP351, IRFP352, IRFP353

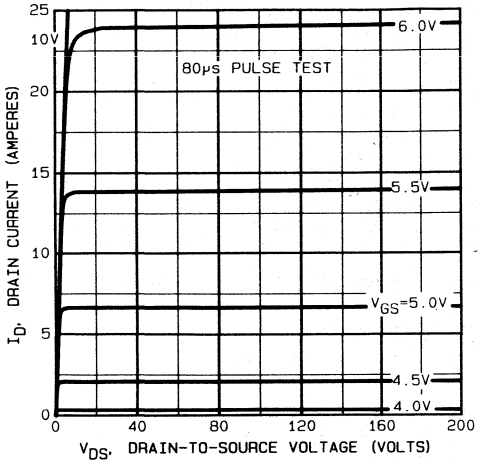


Fig. 1 — Typical Output Characteristics

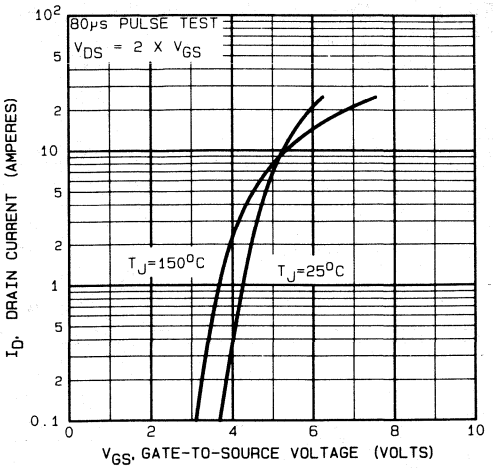


Fig. 2 — Typical Transfer Characteristics

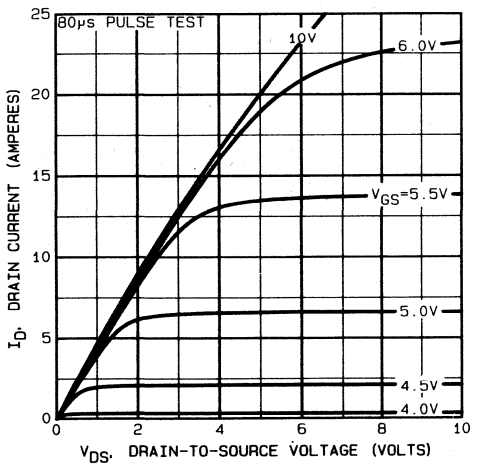


Fig. 3 — Typical Saturation Characteristics

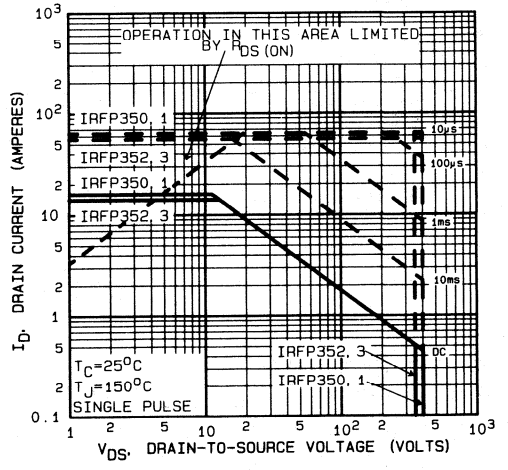


Fig. 4 — Maximum Safe Operating Area

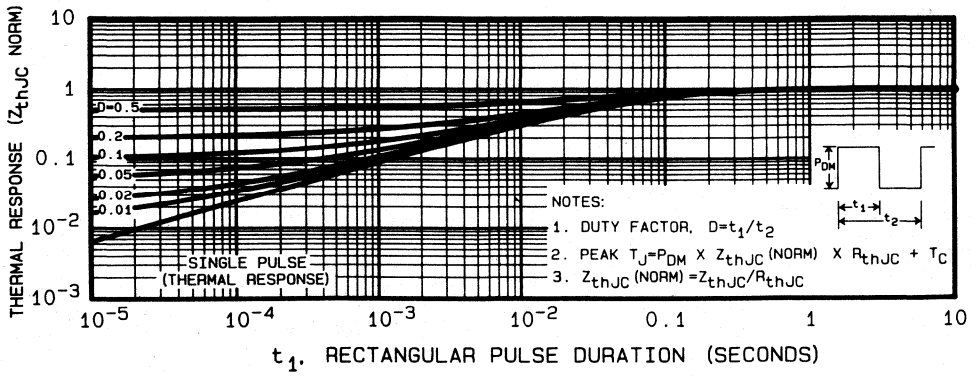


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

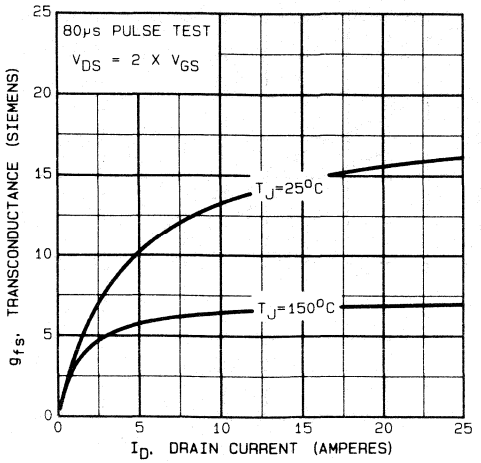


Fig. 6 — Typical Transconductance Vs. Drain Current

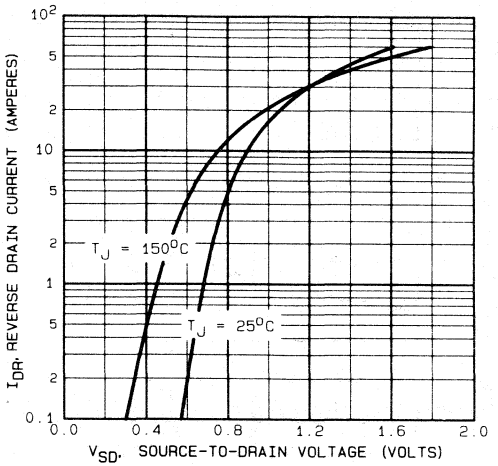


Fig. 7 — Typical Source-Drain Diode Forward Voltage

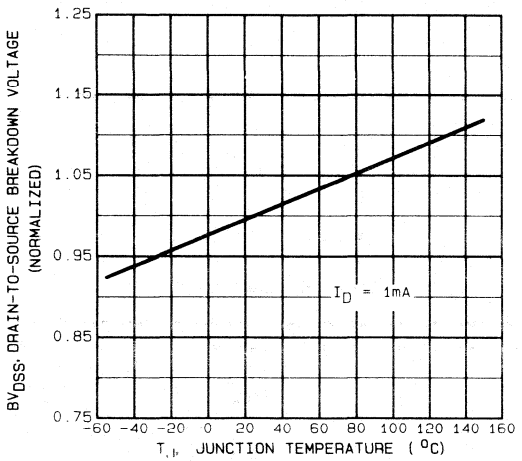


Fig. 8 — Breakdown Voltage Vs. Temperature

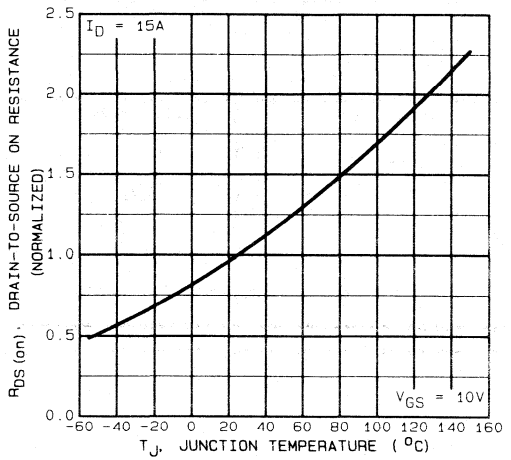


Fig. 9 — Normalized On-Resistance Vs. Temperature

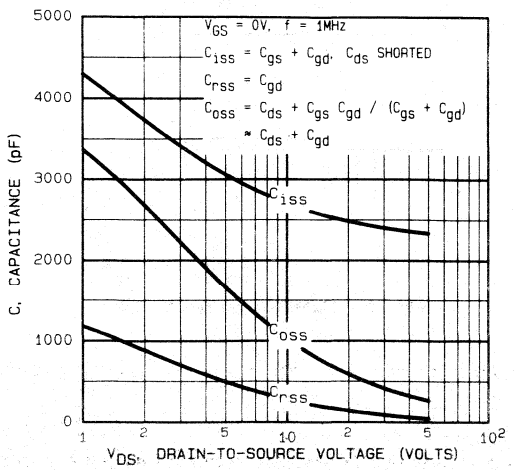


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

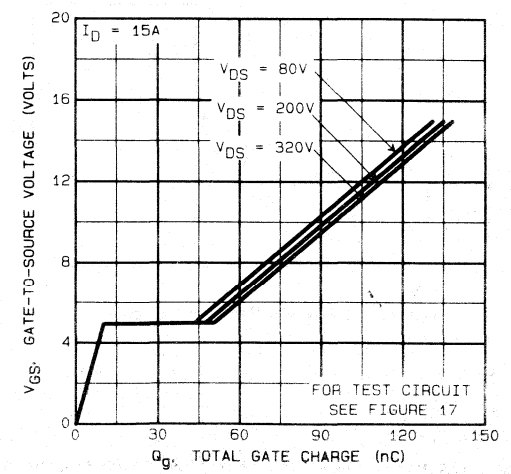


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRFP350, IRFP351, IRFP352, IRFP353

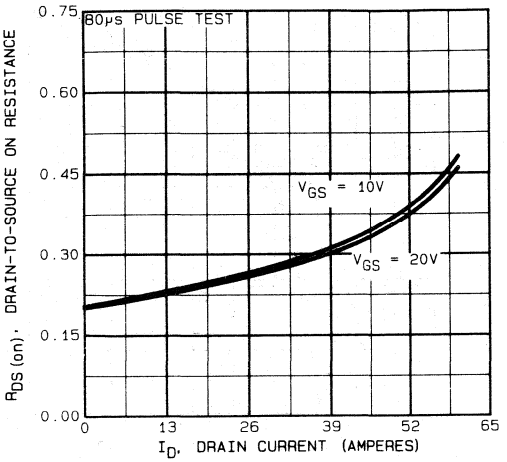


Fig. 12 — Typical On-Resistance Vs. Drain Current

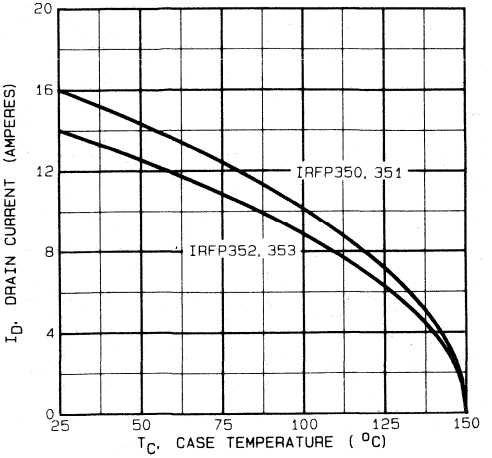


Fig. 13 — Maximum Drain Current Vs. Case Temperature

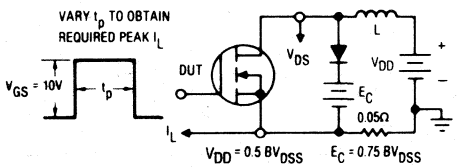


Fig. 14 — Clamped Inductive Test Circuit

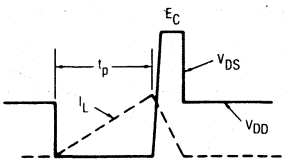


Fig. 15 — Clamped Inductive Waveforms

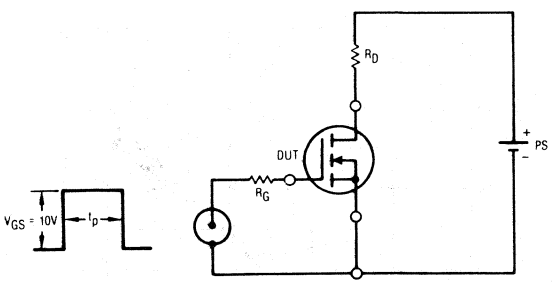


Fig. 16 — Switching Time Test Circuit

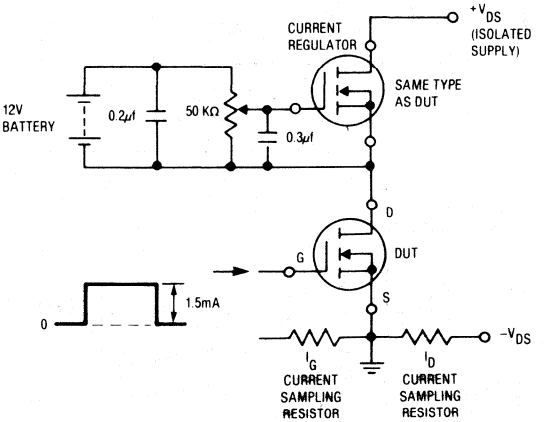


Fig. 17 — Gate Charge Test Circuit

File Number **2331**

IRFP450, IRFP451, IRFP452, IRFP453

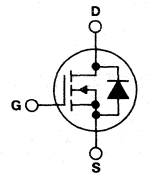
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A and 13 A, 450 V - 500 V
$r_{DS(on)}$ = 0.4 Ω and 0.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



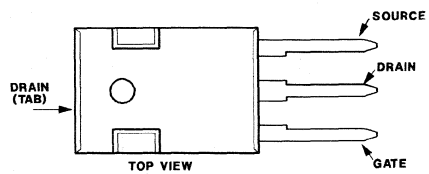
92CS-43357

TERMINAL DIAGRAM

The IRFP450, IRFP451, IRFP452, and IRFP453 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

Absolute Maximum Ratings

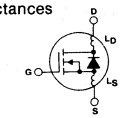
Parameter		IRFP450	IRFP451	IRFP452	IRFP453	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	13	13	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped ④	52	52	48	48	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP450, IRFP451, IRFP452, IRFP453

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP450 IRFP452	500	—	—	V	V_{GS} = 0V
		IRFP451 IRFP453	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP450 IRFP451	13	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFP452 IRFP453	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP450 IRFP451	—	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		IRFP452 IRFP453	—	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 7.0A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 210V, I_D = 7.0A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	150	ns	
t_f	Fall Time	ALL	—	—	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	82	140	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	40	60	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	42	63	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

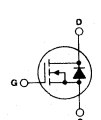


Thermal Resistance

$R_{th}JC$	Junction-to-Case	ALL	—	—	0.83	°C/W	
$R_{th}CS$	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{th}JA$	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP450 IRFP451	—	—	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP452 IRFP453	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP450 IRFP451	—	—	52	A	
		IRFP452 IRFP453	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	IRFP450 IRFP451	—	—	1.4	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
		IRFP452 IRFP453	—	—	1.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1300	—	ns	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	7.4	—	μC	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ L = 100 μH (See Fig. 15)

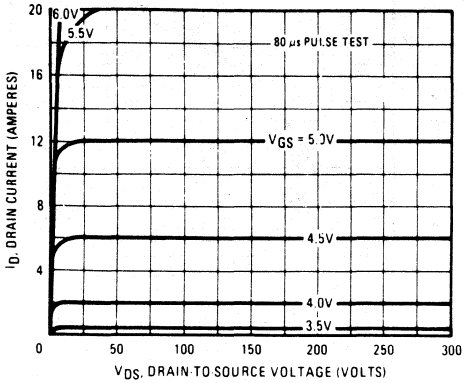


Fig. 1 — Typical Output Characteristics

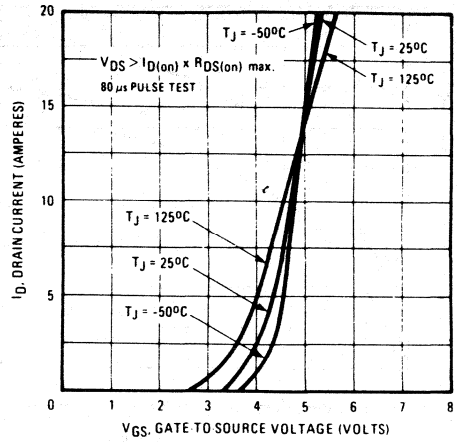


Fig. 2 — Typical Transfer Characteristics

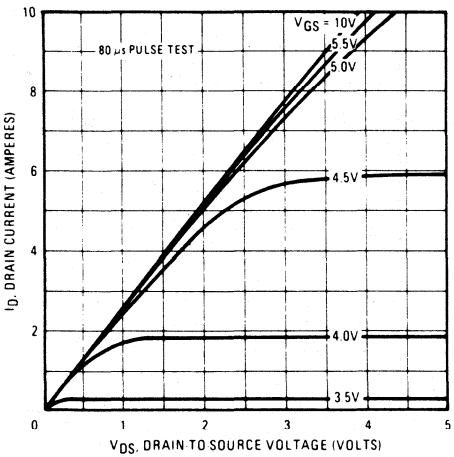


Fig. 3 — Typical Saturation Characteristics

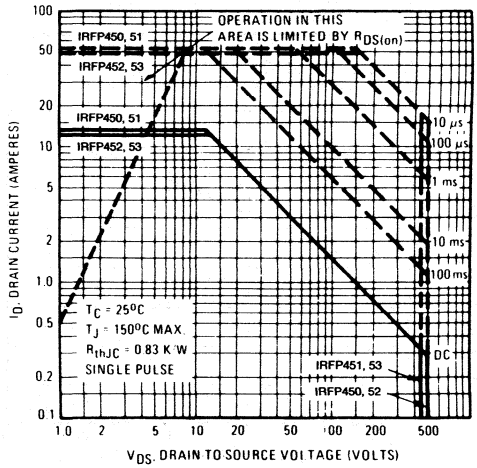


Fig. 4 — Maximum Safe Operating Area

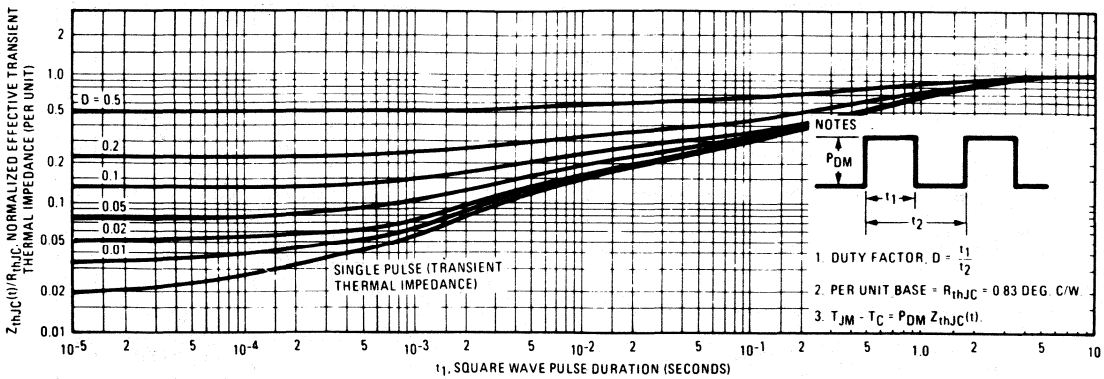


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFP450, IRFP451, IRFP452, IRFP453

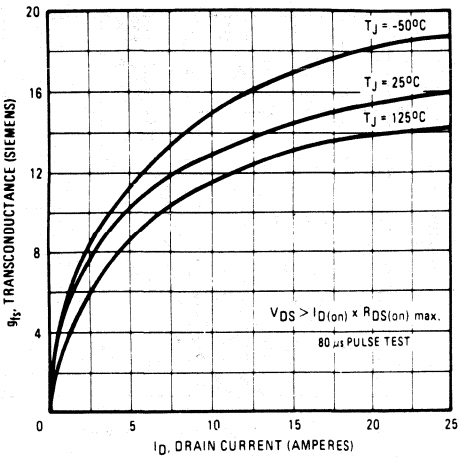


Fig. 6 – Typical Transconductance Vs. Drain Current

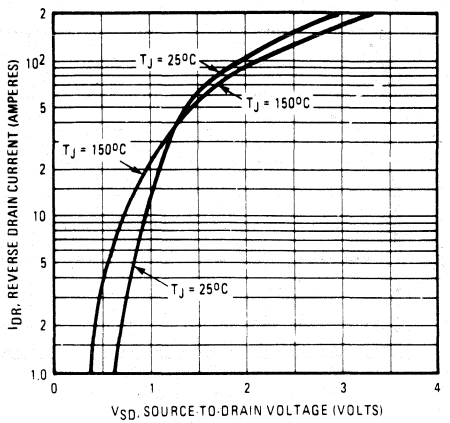


Fig. 7 – Typical Source-Drain Diode Forward Voltage

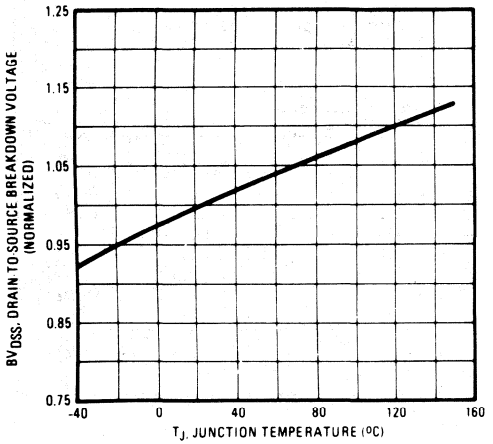


Fig. 8 – Breakdown Voltage Vs. Temperature

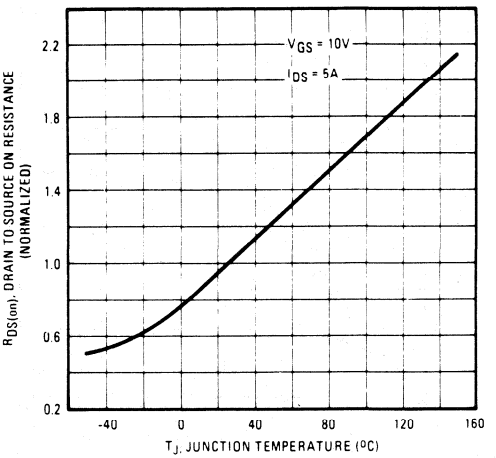


Fig. 9 – Normalized On-Resistance Vs. Temperature

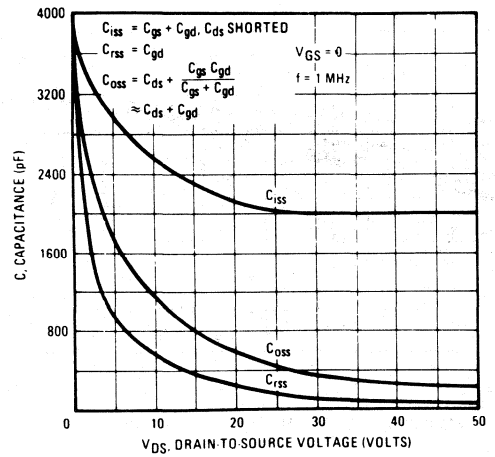


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

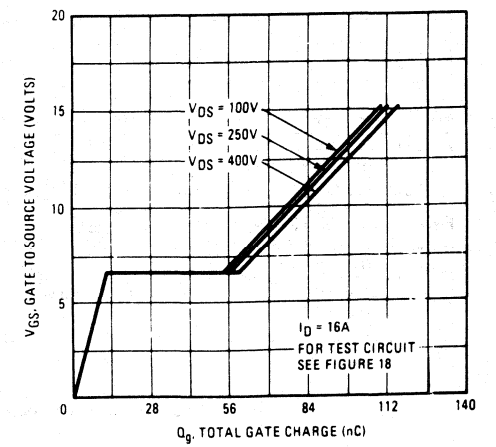


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

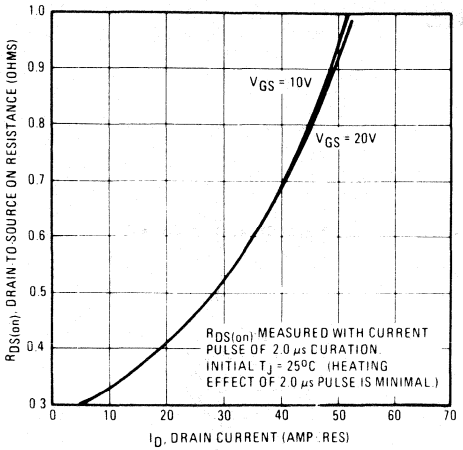


Fig. 12 – Typical On-Resistance Vs. Drain Current

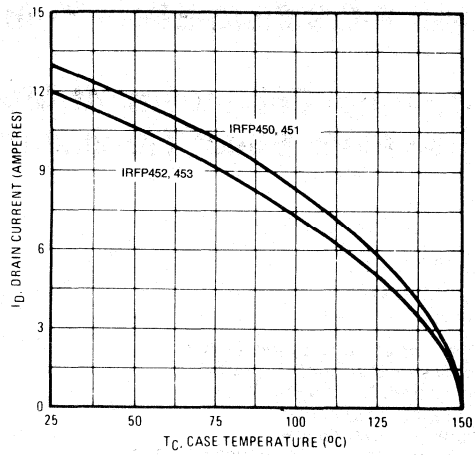


Fig. 13 – Maximum Drain Current Vs. Case Temperature

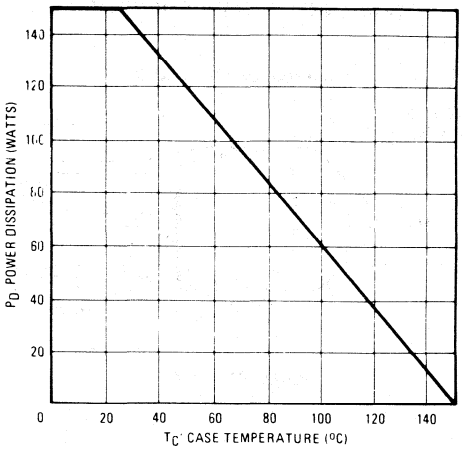


Fig. 14 – Power Vs. Temperature Derating Curve

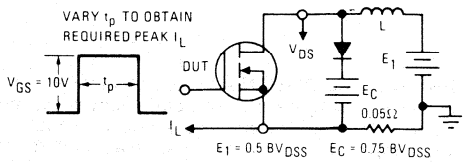


Fig. 15 – Clamped Inductive Test Circuit

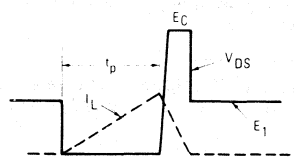


Fig. 16 – Clamped Inductive Waveforms

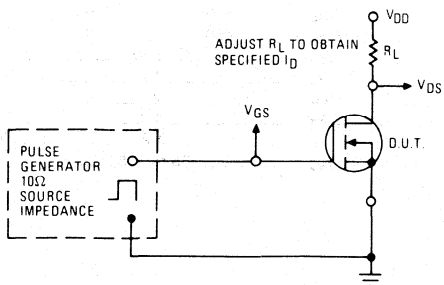


Fig. 17 – Switching Time Test Circuit

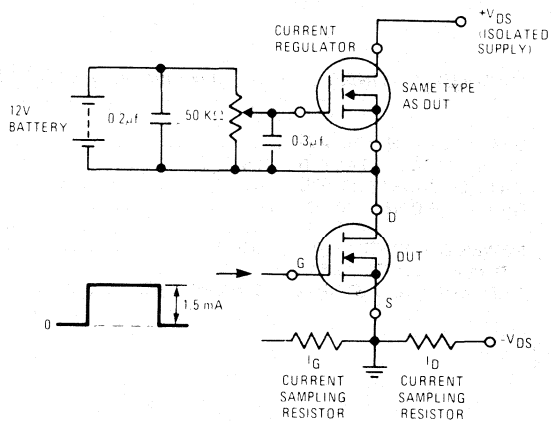


Fig. 18 – Gate Charge Test Circuit

RFH10N45, RFH10N50

File Number **1629**

Power MOS Field-Effect Transistors

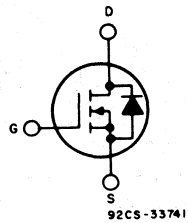
N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 450 V - 500 V
$r_{DS(on)}$ = 0.6 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

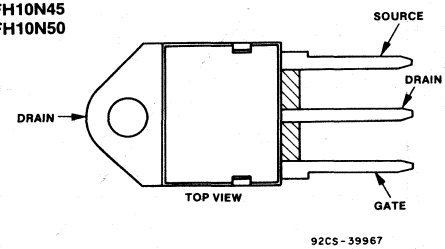
The RFH10N45 and RFH10N50* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH10N45 and RFH10N50 types were formerly RCA developmental numbers TA9579A and TA9579B respectively.

TERMINAL DESIGNATIONS

RFH10N45
RFH10N50



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH10N45	RFH10N50	
DRAIN-SOURCE VOLTAGE	V_{DSS}	450	500	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	450	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	10		A
Pulsed	I_{DM}	20		A
POWER DISSIPATION @ T_C = 25°C	P_T	150		W
Derate above T_C = 25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V	—	1	—	—	μA
		V_{DS} = 400 V	—	—	—	1	
		T_C = 125° C V_{DS} = 360 V	—	50	—	—	
		V_{DS} = 400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 250 V	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	525(typ)	900	525(typ)	900	
Fall Time	t_f	V_{GS} = 10 V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH10N45, RFH10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH10N45, RFH10N50

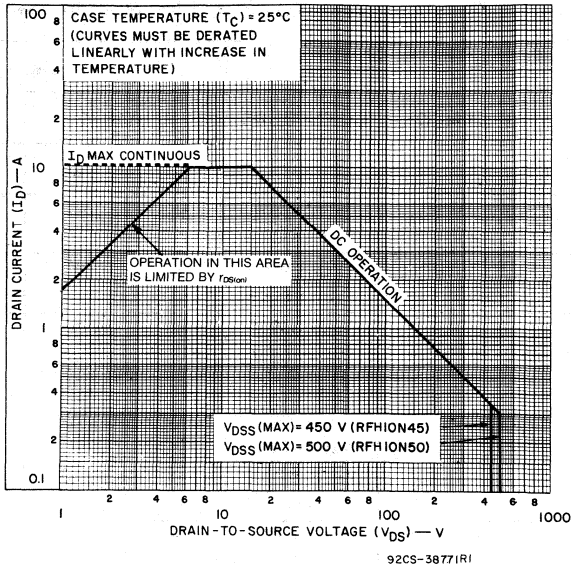


Fig. 1 - Maximum safe operating areas for all types.

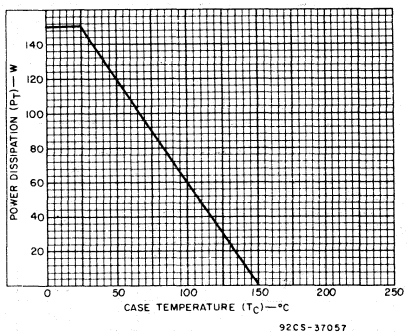


Fig. 2 - Power vs. temperature derating curve for all types.

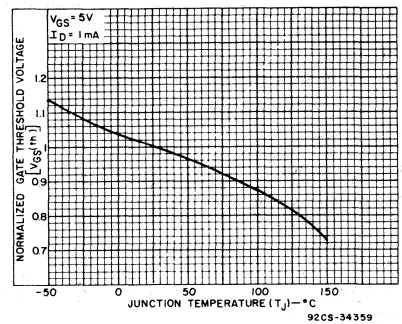


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

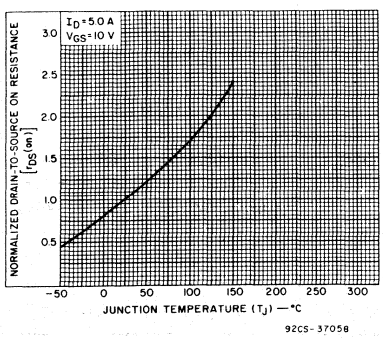


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

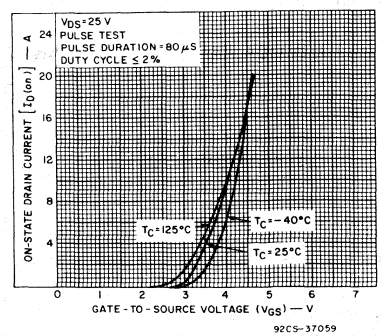


Fig. 5 - Typical transfer characteristics for all types.

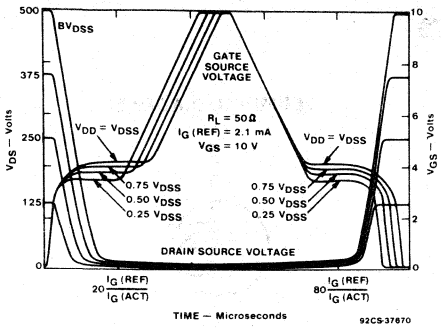


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

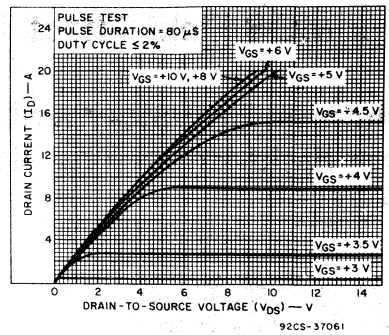


Fig. 7 - Typical saturation characteristics for all types.

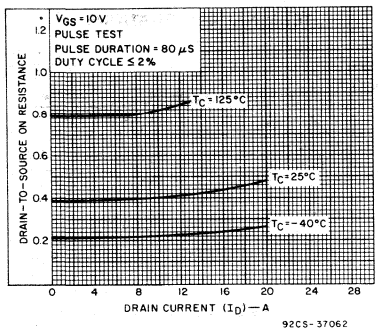


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

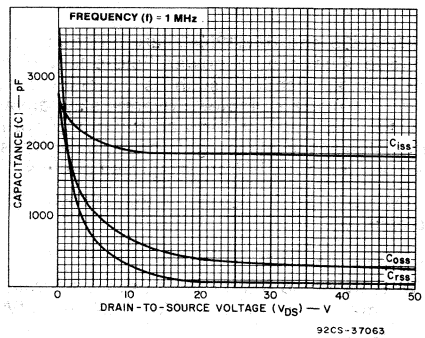


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

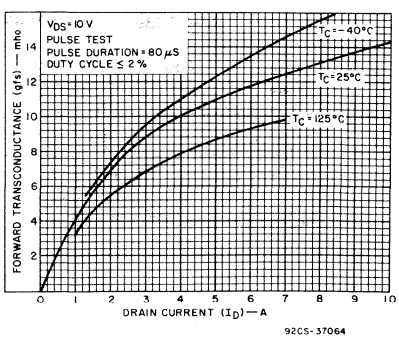


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

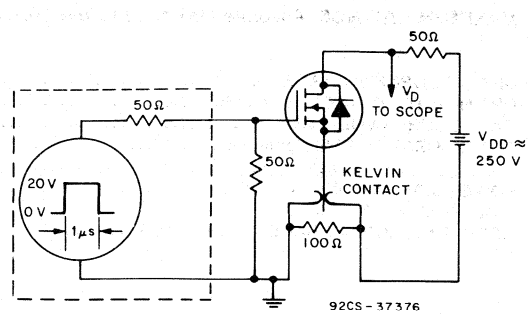


Fig. 11 - Switching Time Test Circuit.

RFH12N35, RFH12N40

File Number **1630**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

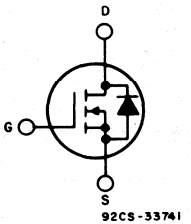
12 A, 350 V - 400 V

$r_{DS(on)}$ = 0.38 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

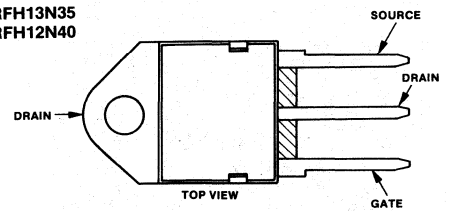
The RFH12N35 and RFH12N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH12N35 and RFH12N40 types were formerly RCA developmental numbers TA9482A and TA9482B respectively.

TERMINAL DESIGNATIONS

RFH13N35
RFH12N40



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH12N35	RFH12N40	
DRAIN-SOURCE VOLTAGE	V_{DSS}	350	400	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	350	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	12		A
Pulsed	I_{DM}	24		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V	—	1	—	—	μA
		V_{DS} = 320 V	—	—	—	1	
		T_C = 125°C					
		V_{DS} = 280 V	—	50	—	—	
		V_{DS} = 320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	2.28	—	2.28	V
		I_D = 12 A V_{GS} = 10 V	—	6.75	—	6.75	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	0.38	—	0.38	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	900	—	900	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 200 V	30(typ)	50	30(typ)	50	ns
Rise Time	t_r	I_D = 6 A	105(typ)	150	105(typ)	150	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	480(typ)	750	480(typ)	750	
Fall Time	t_f	V_{GS} = 10 V	140(typ)	200	140(typ)	200	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH12N35, RFH12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 6A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH12N35, RFH12N40

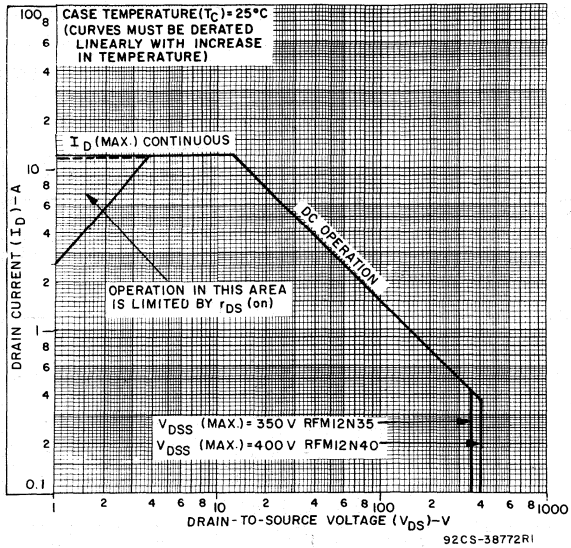


Fig. 1 - Maximum safe operating areas for all types.

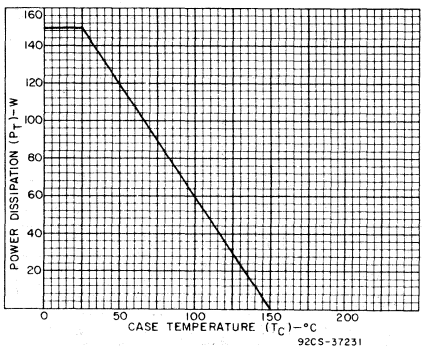


Fig. 2 - Power vs. temperature derating curve for all types.

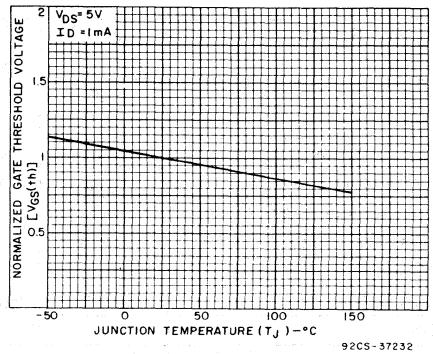


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

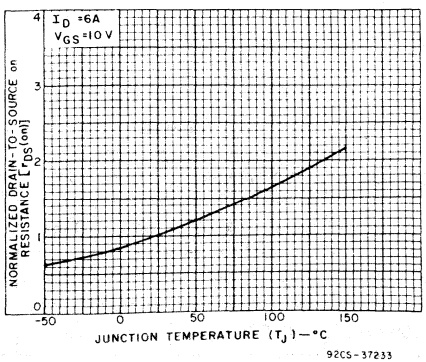


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

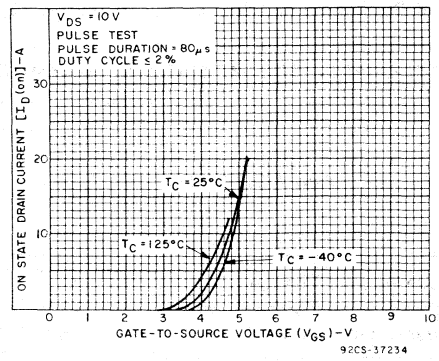


Fig. 5 - Typical transfer characteristics for all types.

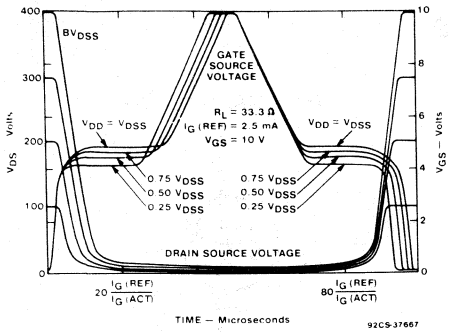


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

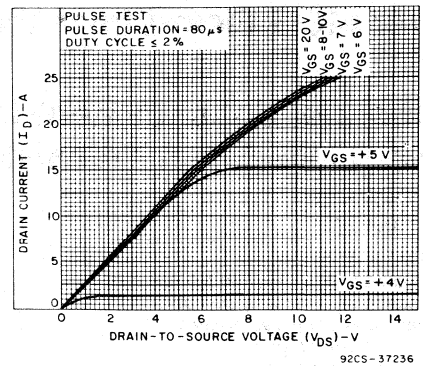


Fig. 7 - Typical saturation characteristics for all types.

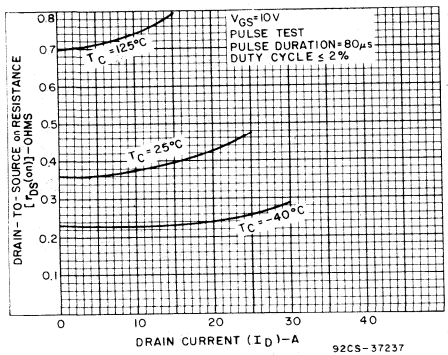


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

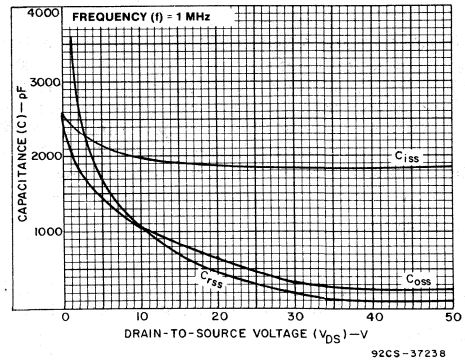


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

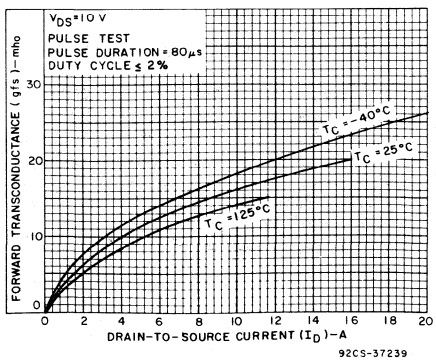


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

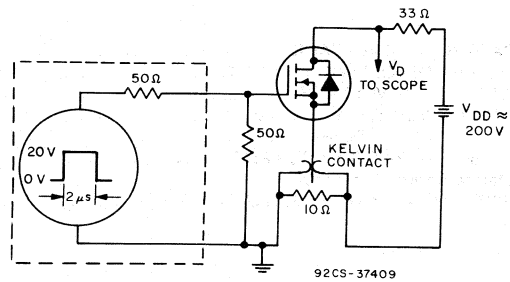


Fig. 11 - Switching Time Test Circuit.

RFH25N18, RFH25N20

File Number **1631**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

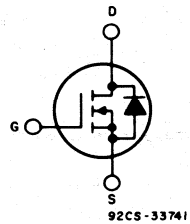
25 A, 180 V - 200 V

$r_{DS(on)}$ = 0.15 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



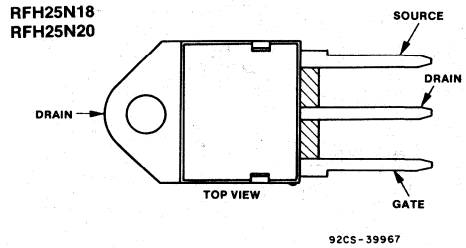
N-CHANNEL ENHANCEMENT MODE

The RFH25N18 and RFH25N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH25N18 and RFH25N20 types were formerly RCA developmental numbers TA9483A and TA9483B respectively.

TERMINAL DESIGNATION



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		RFH25N18	RFH25N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	25		A
Pulsed	I_{DM}	60		A
POWER DISSIPATION @ T_C = 25°C	P_T	150		W
Derate above T_C = 25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFH25N18, RFH25N20

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145 V V_{DS} = 160 V	— —	1 —	— —	— 1	μA
		T_C = 125°C V_{DS} = 145 V V_{DS} = 160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	1.875	—	1.875	V
		I_D = 25 A V_{GS} = 10 V	—	5	—	5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	3500	—	3500	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 100 V I_D = 12.5 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		150(typ)	225	150(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$		300(typ)	400	300(typ)	400	ns
Fall Time	t_f		120(typ)	200	120(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH25N18, RFH25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 12.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	300 (typ.)		300 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH25N18, RFH25N20

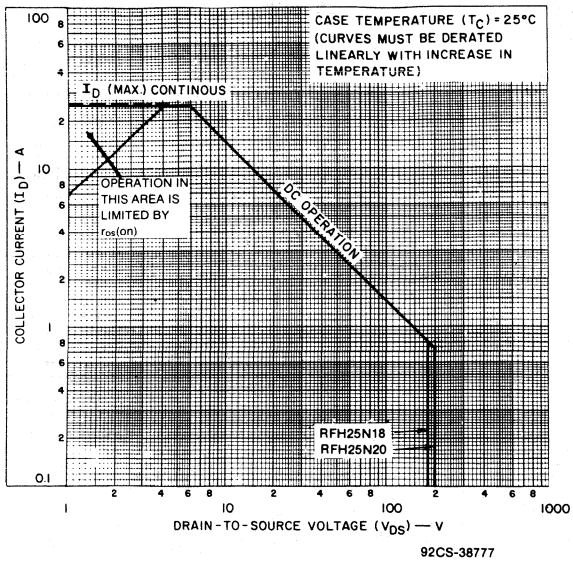


Fig. 1 - Maximum safe operating areas for all types.

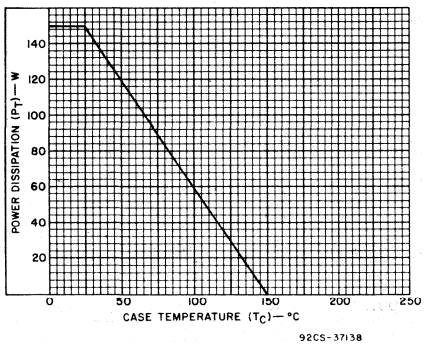


Fig. 2 - Power vs. temperature derating curve for all types.

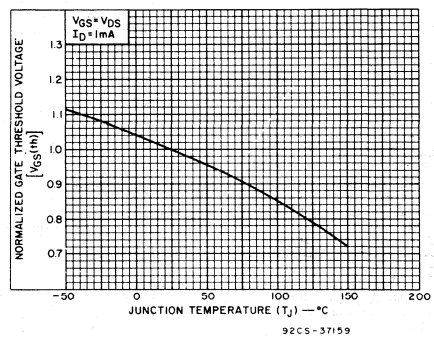


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

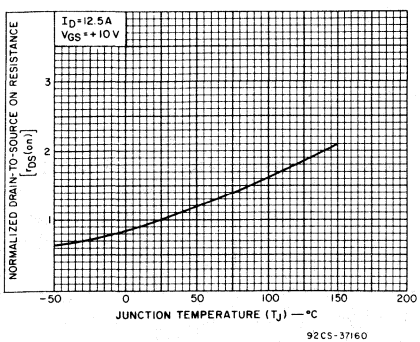


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

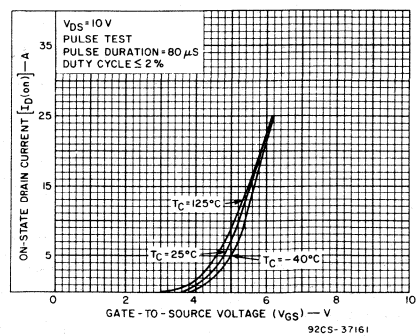


Fig. 5 - Typical transfer characteristics for all types.

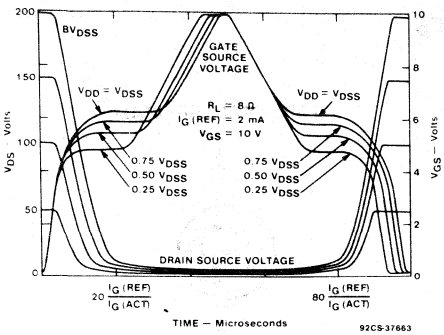


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

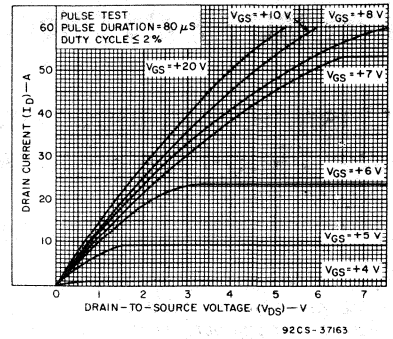


Fig. 7 - Typical saturation characteristics for all types.

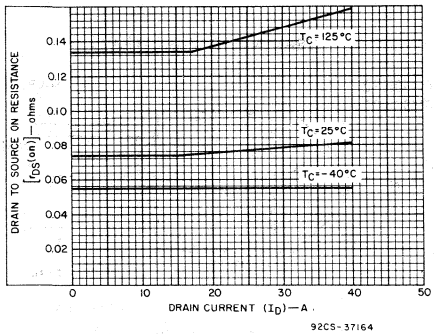


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

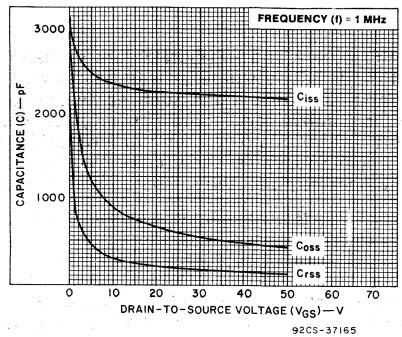


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

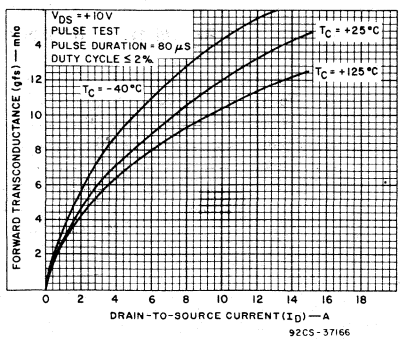


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

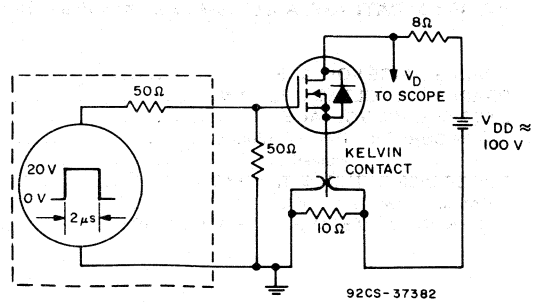


Fig. 11 - Switching Time Test Circuit.

RFH30N12, RFH30N15

File Number **1633**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

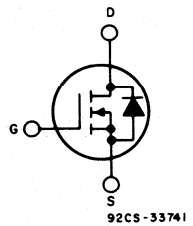
30 A, 120 V - 150 V

$r_{DS(on)}$ = 0.075 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



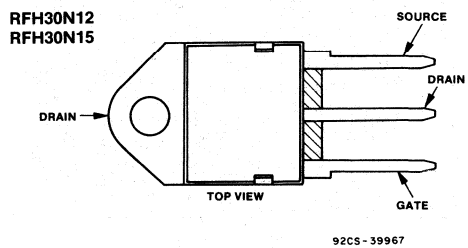
N-CHANNEL ENHANCEMENT MODE

The RFH30N12 and RFH30N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH30N12 and RFH30N15 types were formerly RCA developmental numbers TA9578A and TA9578B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH30N12	RFH30N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	30		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
On-State Gate Voltage	$V_{GS}(on)$[a]	V_{DS} = 5 V I_D = 15 A	—	8	—	8	V
		V_{DS} = 10 V I_D = 30 A	—	10	—	10	
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 30 A V_{GS} = 10 V	—	2.65	—	2.65	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 75 V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D = 15 A	420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	300(typ)	450	300(typ)	450	
Fall Time	t_f	V_{GS} = 10 V	250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH30N12, RFH30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 15A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH30N12, RFH30N15

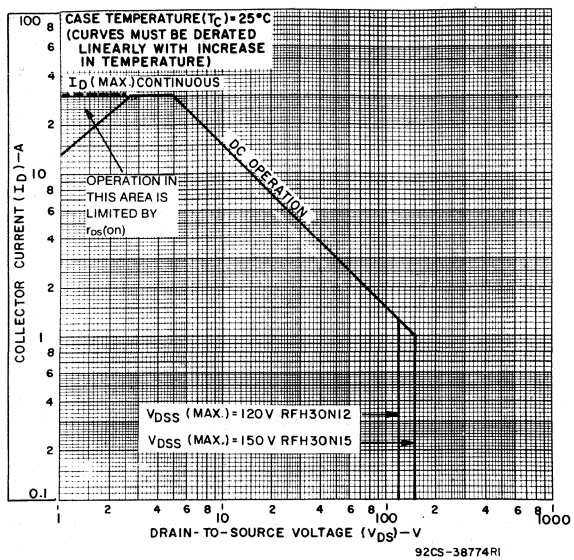


Fig. 1 - Maximum safe operating areas for all types.

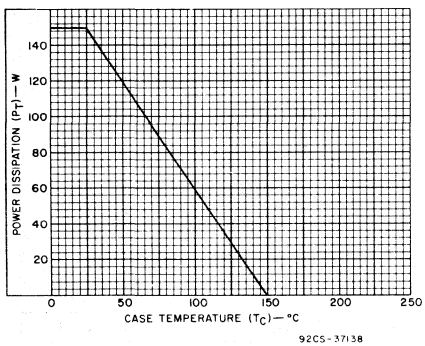


Fig. 2 - Power vs. temperature derating curve for all types.

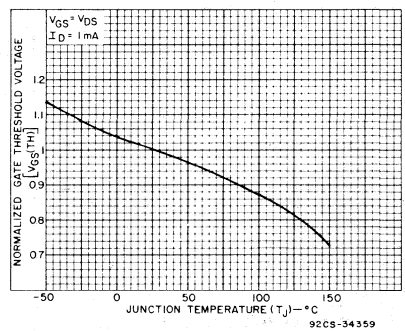


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

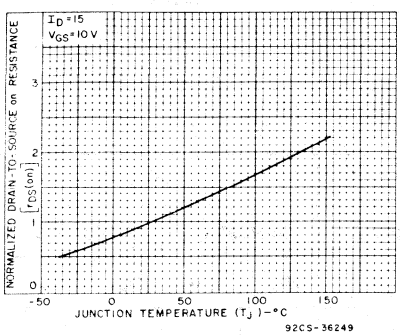


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

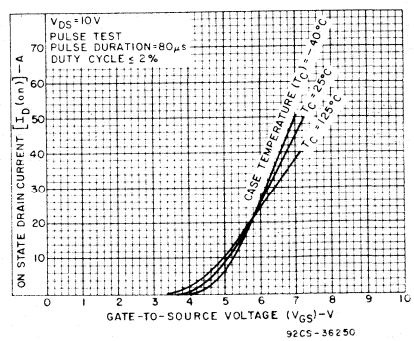


Fig. 5 - Typical transfer characteristics for all types.

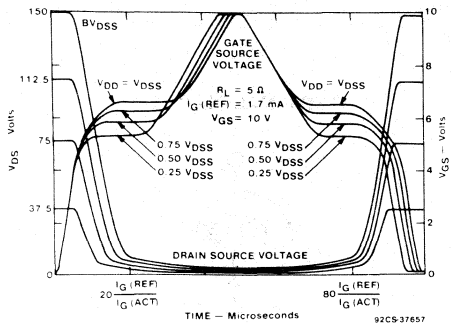


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

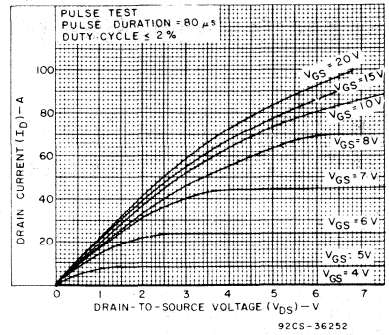


Fig. 7 - Typical saturation characteristics for all types.

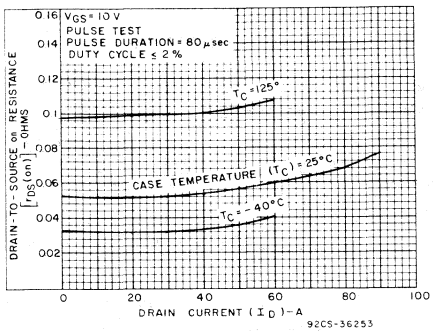


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

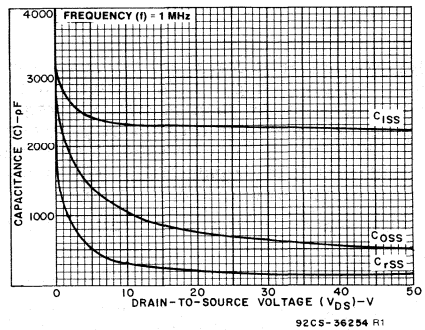


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

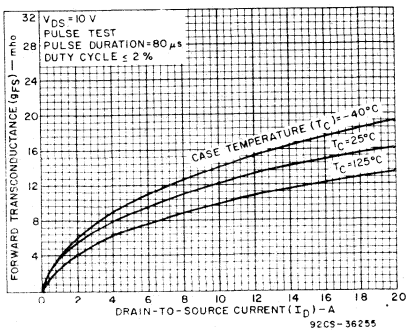


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

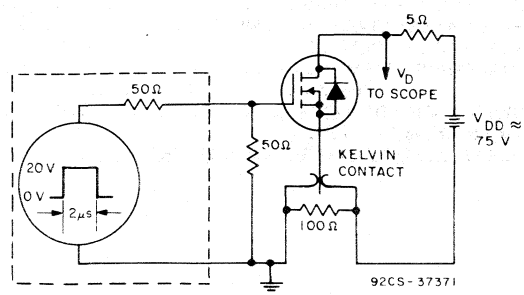


Fig. 11 - Switching Time Test Circuit.

RFH35N08, RFH35N10

File Number **1634**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

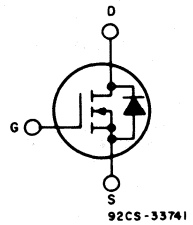
35 A, 80 V - 100 V

$r_{DS(on)}$ = 0.055 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



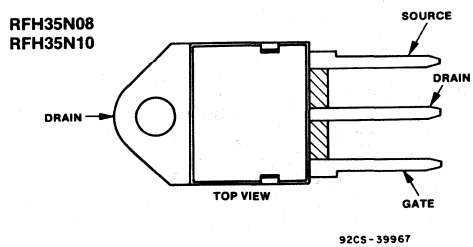
N-CHANNEL ENHANCEMENT MODE

The RFH35N08 and RFH35N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH35N08 and RFH35N10 types were formerly RCA developmental numbers TA9481A and TA9481B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH35N08	RFH35N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	35		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFH35N08, RFH35N10

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V	—	1	—	—	μA
		V_{DS} = 80 V	—	—	—	1	
		T_C = 125°C V_{DS} = 65 V	—	50	—	—	
		V_{DS} = 80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.963	—	0.963	V
		I_D = 35 A V_{GS} = 10 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	600	—	600	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r	I_D = 17.5 A	225(typ)	450	225(typ)	450	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	240(typ)	450	240(typ)	450	
Fall Time	t_f	V_{GS} = 10 V	165(typ)	350	165(typ)	350	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH35N08, RFH35N10 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 17.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{iF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFH35N08, RFH35N10

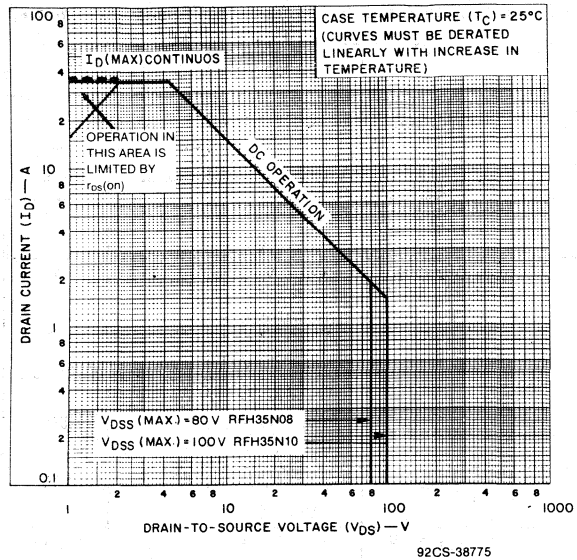


Fig. 1 - Maximum safe operating areas for all types.

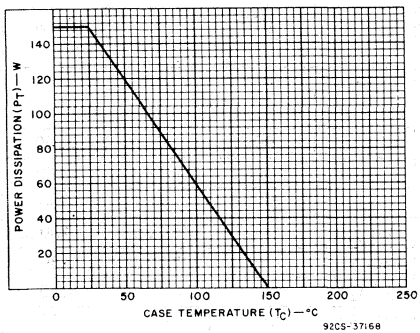


Fig. 2 - Power vs. temperature derating curve for all types.

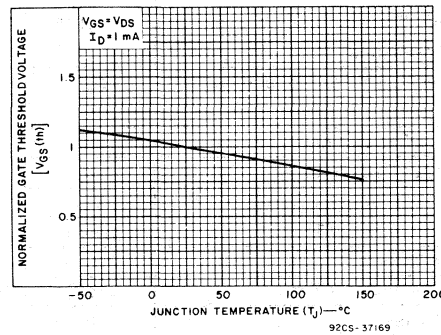


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

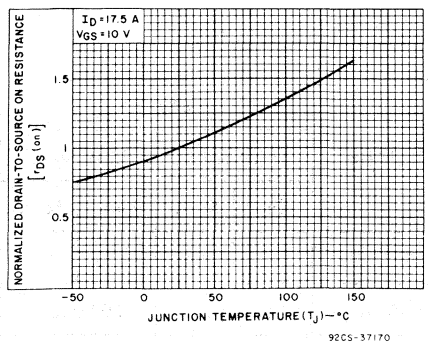


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

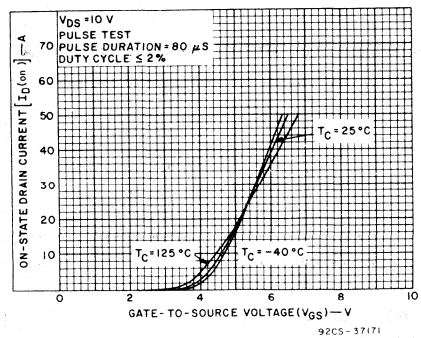


Fig. 5 - Typical transfer characteristics for all types.

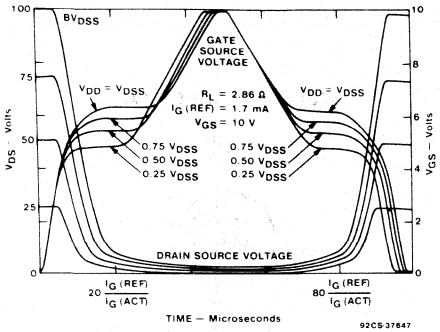


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

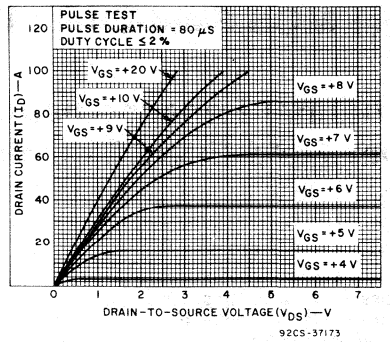


Fig. 7 - Typical saturation characteristics for all types.

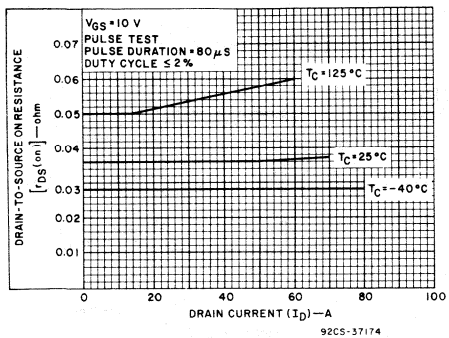


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

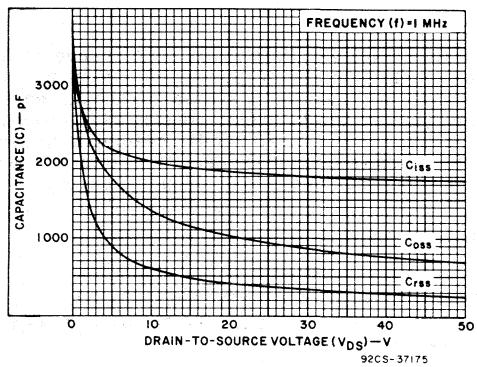


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

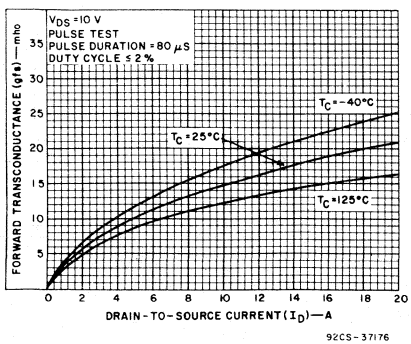


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

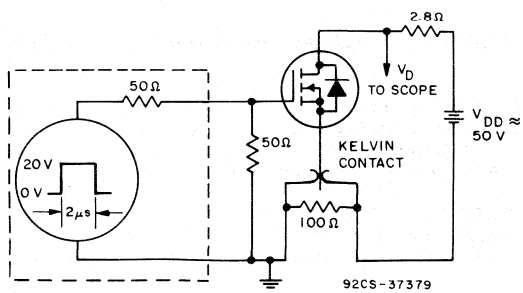


Fig. 11 - Switching Time Test Circuit.

RFH45N05, RFH45N06

File Number **1635**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

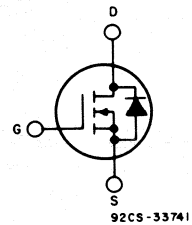
45 A, 50 V - 60 V

$r_{DS(on)}$ = 0.040 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



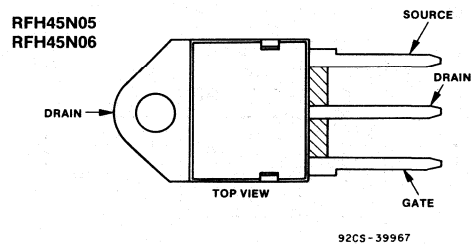
N-CHANNEL ENHANCEMENT MODE

The RFH45N05 and RFH45N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH45N05 and RFH45N06 types were formerly RCA developmental numbers TA9480A and TA9480B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH45N05	RFH45N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50	60	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	50	60	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	45		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		° C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125°C					
		V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	0.9	—	0.9	V
		I_D = 45 A V_{GS} = 10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1800	—	1800	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	750	—	750	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D = 22.5 A	310(typ)	475	310(typ)	475	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	220(typ)	350	220(typ)	350	
Fall Time	t_f	V_{GS} = 10 V	240(typ)	375	240(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH45N05, RFH45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}*	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH45N05, RFH45N06

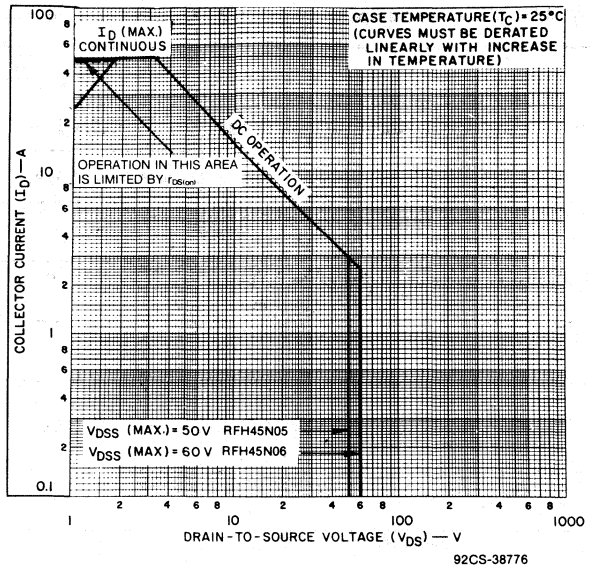


Fig. 1 - Maximum safe operating areas for all types.

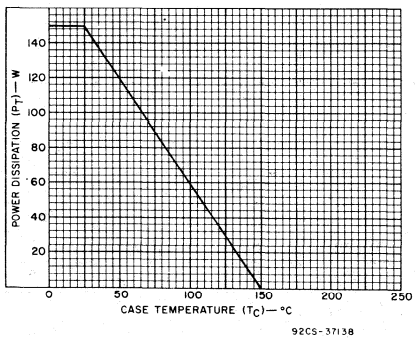


Fig. 2 - Power vs. temperature derating curve for all types.

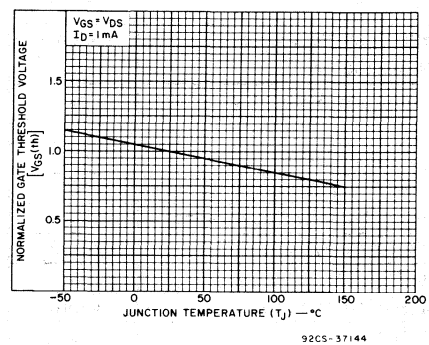


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

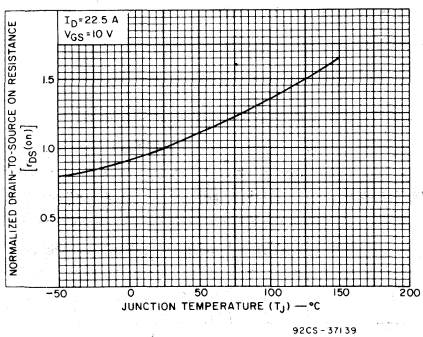


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

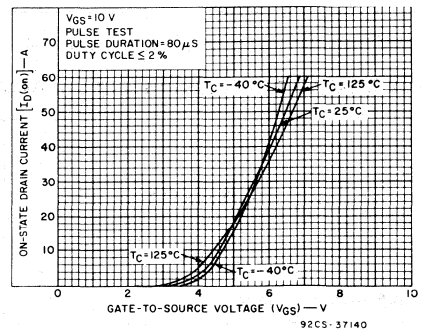


Fig. 5 - Typical transfer characteristics for all types.

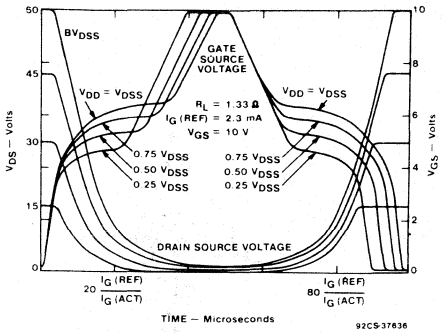


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

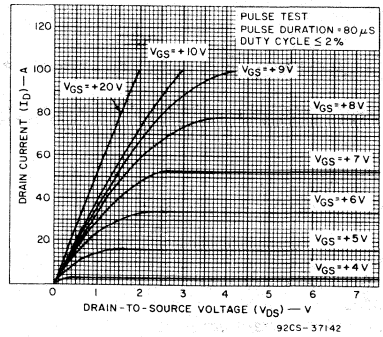


Fig. 7 - Typical saturation characteristics for all types.

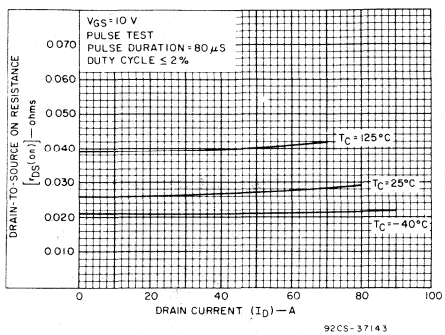


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

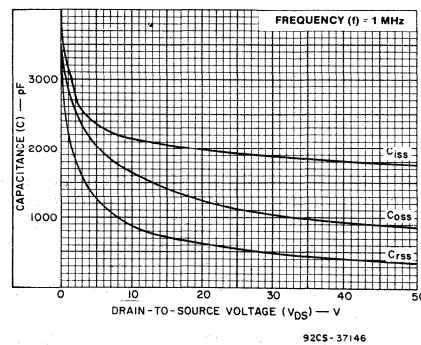


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

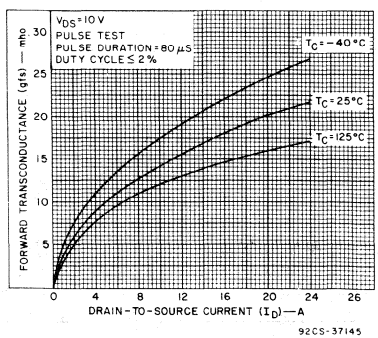


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

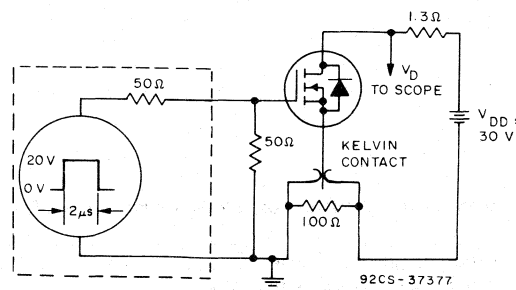


Fig. 11 - Switching Time Test Circuit.

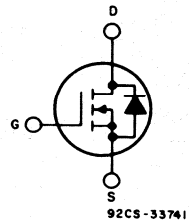
RFK25N18, RFK25N20

File Number **1500**

N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 180 V - 200 V
$r_{DS}(on)$ = 0.15 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



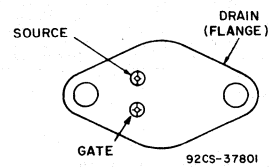
N-CHANNEL ENHANCEMENT MODE

The RFK25N18 and RFK25N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK25N18 and RFK25N20 types were formerly RCA developmental numbers TA9295A and TA9295B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK25N18		RFK25N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180		200	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	180		200	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		25		A
Pulsed	I_{DM}		60		A
POWER DISSIPATION @ T_C=25°C	P_T		150		W
Derate above T_C=25°C			1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

RFK25N18, RFK25N20

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	1.875	—	1.875	V
		I_D=25 A V_{GS}=10 V	—	5	—	5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	3500	—	3500	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V I_D=12.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		150(typ)	225	150(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$		300(typ)	400	300(typ)	400	ns
Fall Time	t_f		120(typ)	200	120(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK25N18, RFK25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300(typ)		300(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFK25N18, RFK25N20

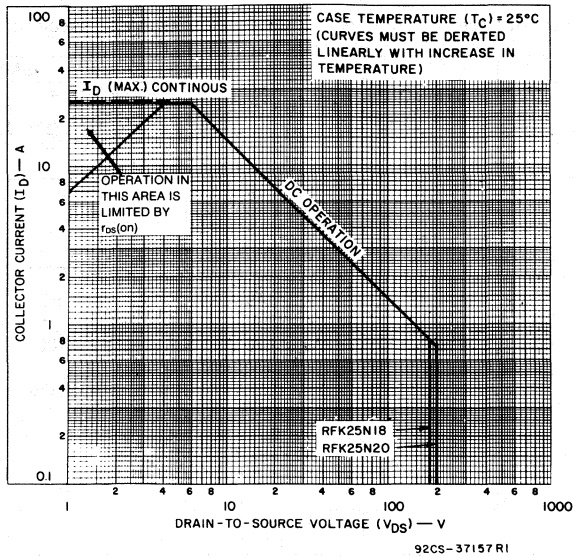


Fig. 1 — Maximum safe operating areas for all types.

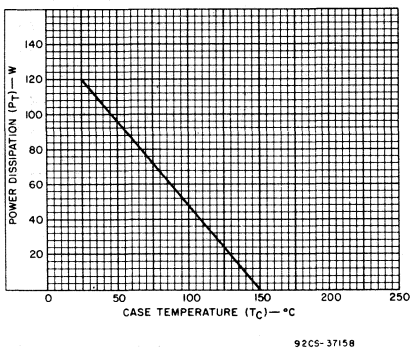


Fig. 2 — Power vs. temperature derating curve for all types.

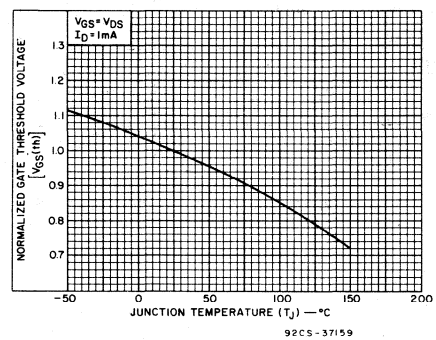


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

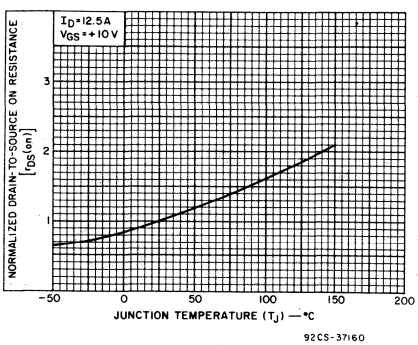


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

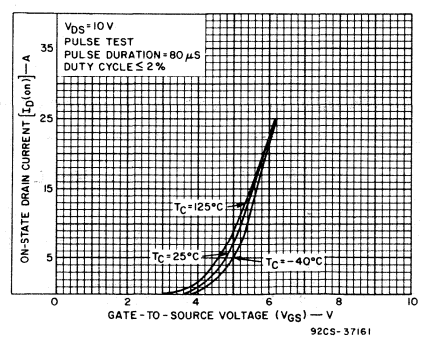


Fig. 5 — Typical transfer characteristics for all types.

RFK25N18, RFK25N20

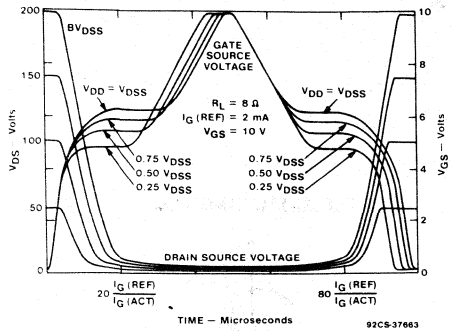


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

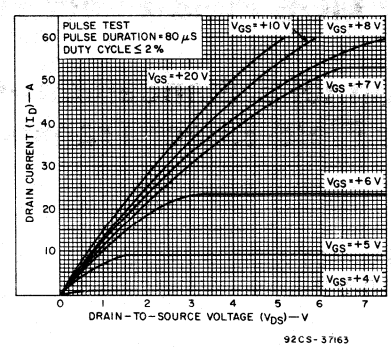


Fig. 7 — Typical saturation characteristics for all types.

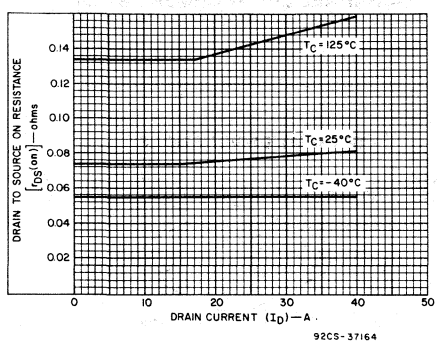


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

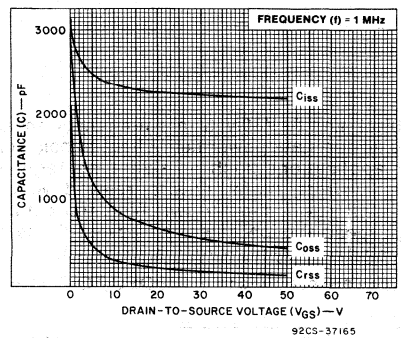


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

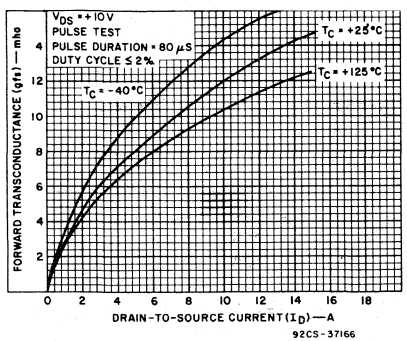


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

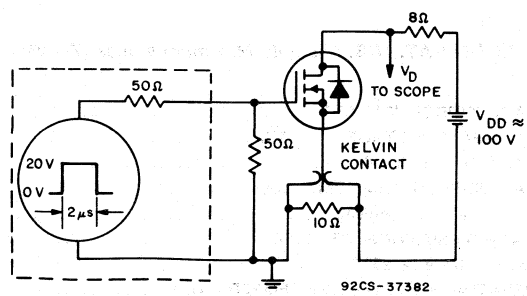


Fig. 11 — Switching Time Test Circuit

RFK30N12, RFK30N15

File Number **1455**

Power MOS Field-Effect Transistors

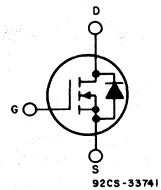
N-Channel Enhancement-Mode Power Field-Effect Transistors

30 A, 120 V - 150 V
$r_{DS}(on)$=0.075 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

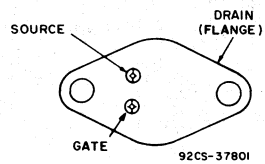
The RFK30N12 and RFK30N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK30N12 and RFK30N15 types were formerly RCA developmental numbers TA9188A and TA9188B, respectively.

TERMINAL DESIGNATIONS

RFK30N12
RFK30N15



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFK30N12	RFK30N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	30		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @T_C=25°C	P_T	120		W
Derate above T_C=25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125° C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ± 20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	1.125	—	1.125	V
		I_D=30 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}		—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75V I_D=15 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r		420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$		300(typ)	450	300(typ)	450	
Fall Time	t_f		250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK30N12, RFK30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=15 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFK30N12, RFK30N15

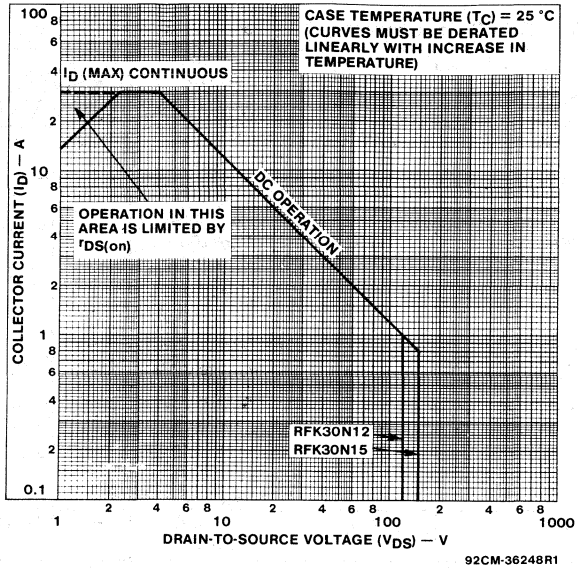


Fig. 1 - Maximum safe operating areas for all types.

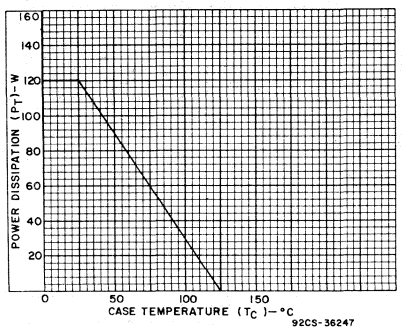


Fig. 2 - Power vs. temperature derating curve for all types.

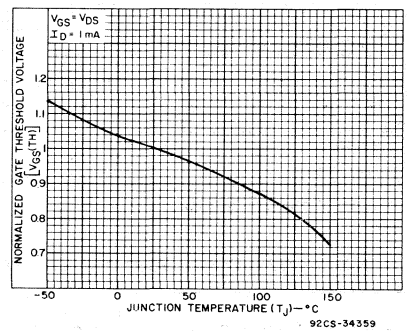


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

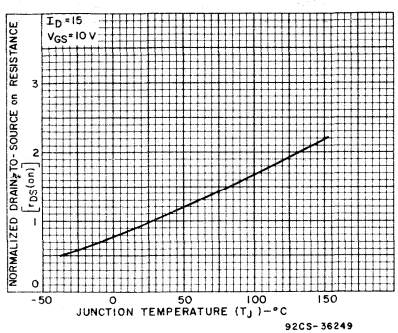


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

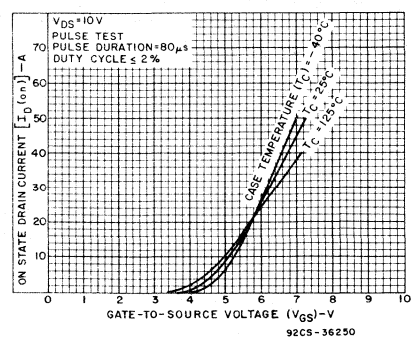


Fig. 5 - Typical transfer characteristics for all types.

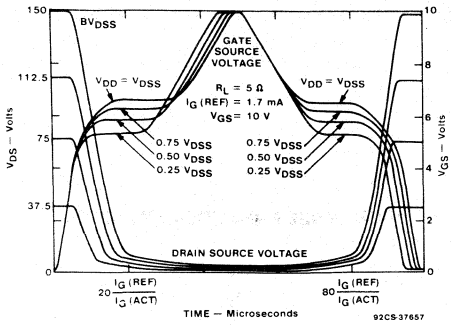


Fig. 6- Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

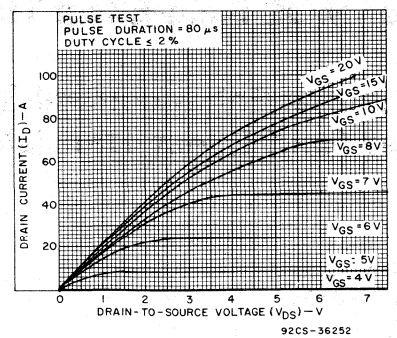


Fig. 7 - Typical saturation characteristics for all types.

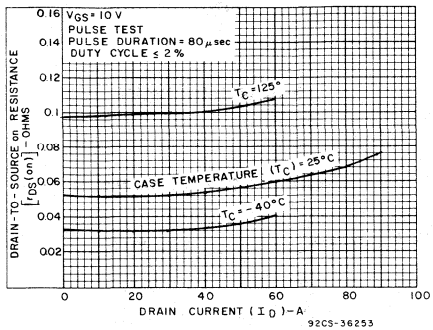


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

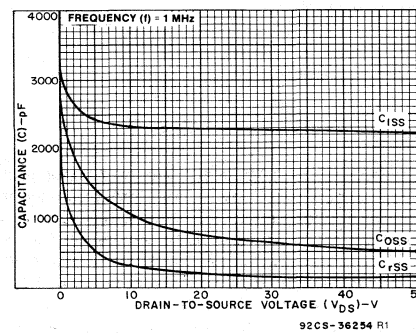


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

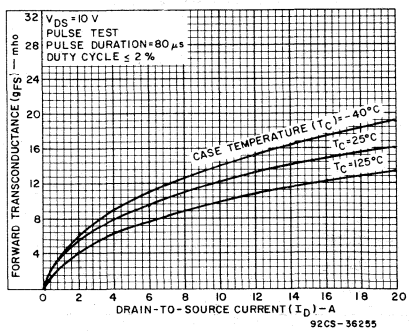


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

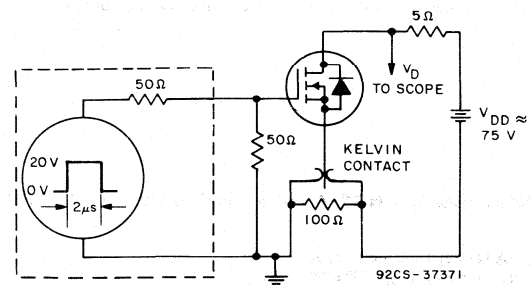


Fig. 11 — Switching Time Test Circuit

RFK35N08, RFK35N10

File Number **1499**

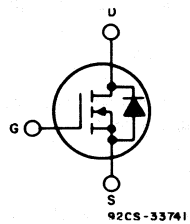
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

35 A, 80 V - 100 V
$r_{DS}(on)$ = 0.055 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

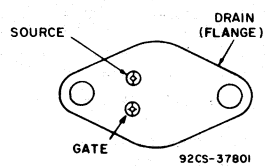
The RFK35N08 and RFK35N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK35N08 and RFK35N10 types were formerly RCA developmental numbers TA9288A and TA9288B, respectively.

TERMINAL DESIGNATIONS

RFK35N08
RFK35N10



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK35N08		RFK35N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80		100	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	80		100	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		35		A
Pulsed	I_{DM}		100		A
POWER DISSIPATION @ T_C=25°C	P_T		150		W
Derate above T_C=25°C			1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.9625	—	0.9625	V
		I_D=35 A V_{GS}=10 V	—	3.5	—	3.5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1500	—	1500	pF
Reverse Transfer Capacitance	C_{rss}		—	600	—	600	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=17.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r		225(typ)	450	225(typ)	450	ns
Turn-Off Delay Time	$t_d(off)$		240(typ)	450	240(typ)	450	ns
Fall Time	t_f		165(typ)	350	165(typ)	350	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK35N08, RFK35N10 Series	—	0.83	—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD} [a]	I_{SD}=17.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFK35N08, RFK35N10

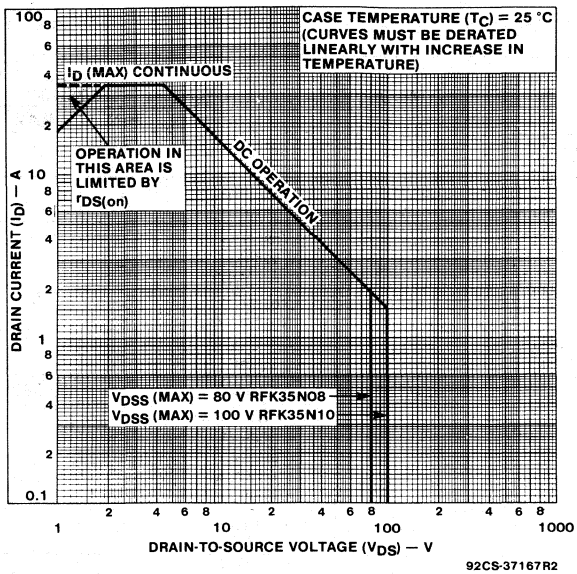


Fig. 1 — Maximum safe operating areas for all types.

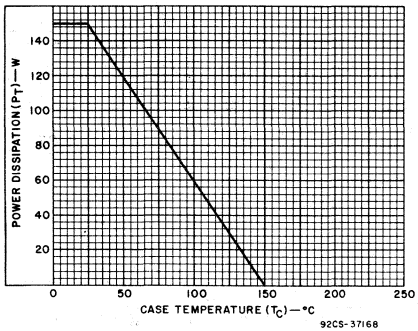


Fig. 2 — Power vs. temperature derating curve for all types.

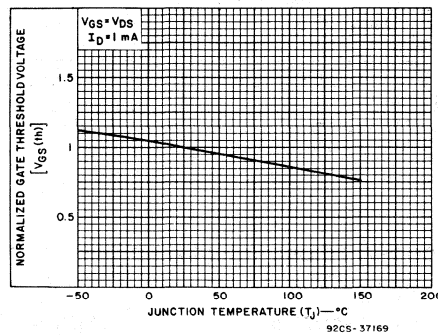


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

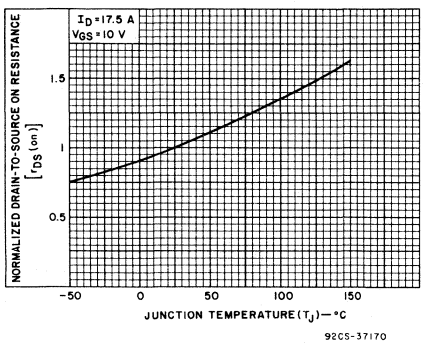


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

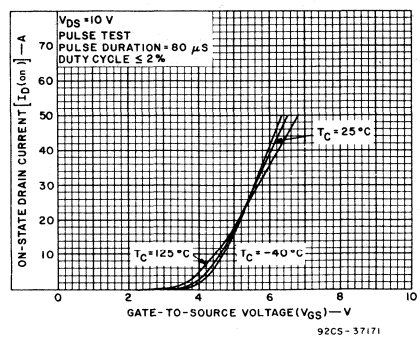


Fig. 5 — Typical transfer characteristics for all types.

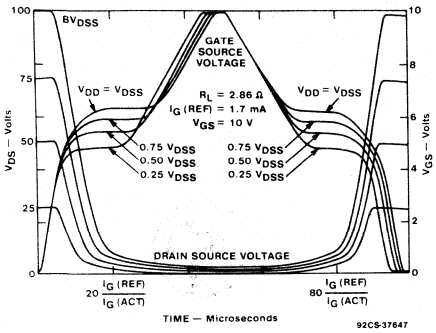


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

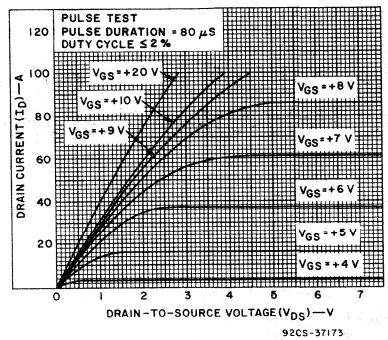


Fig. 7 — Typical saturation characteristics for all types.

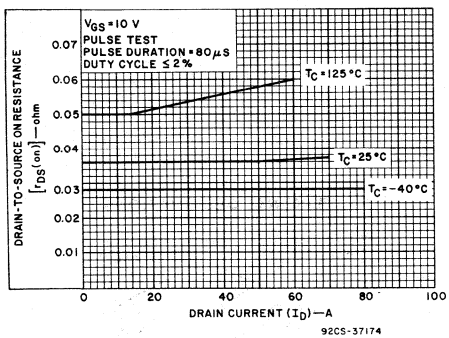


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

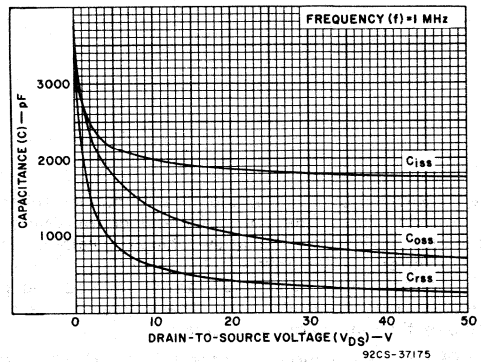


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

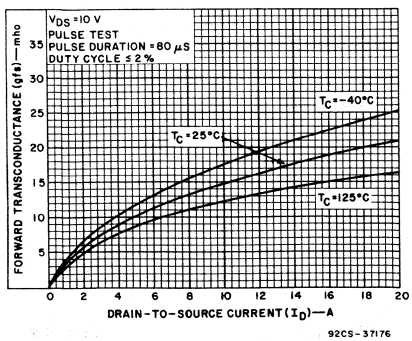


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

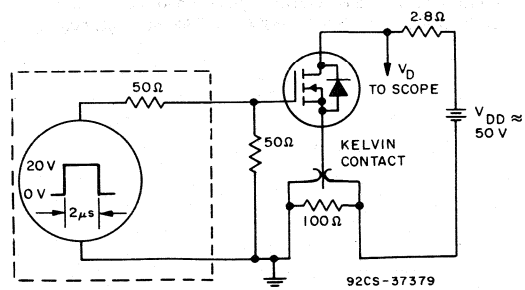


Fig. 11 — Switching Time Test Circuit.

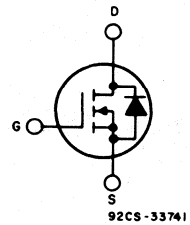
RFK45N05, RFK45N06

File Number **1498**

N-Channel Enhancement-Mode Power Field-Effect Transistors

45 A, 50 V - 60 V
$r_{DS}(on)$ = 0.040 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



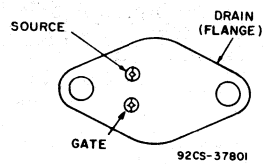
N-CHANNEL ENHANCEMENT MODE

The RFK45N05 and RFK45N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK45N05 and RFK45N06 types were formerly RCA developmental numbers TA9388A and TA9388B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK45N05		RFK45N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50		60	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	50		60	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		45		A
Pulsed	I_{DM}		100		A
POWER DISSIPATION @ T_C=25° C	P_T		150		W
Derate above T_C=25° C			1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		−55 to +150		° C

RFK45N05, RFK45N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V V_{DS}=50 V	— —	1 —	— —	— 1	μA
		T_C=125° c V_{DS}=40 V V_{DS}=50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	0.9	—	0.9	V
		I_D=45 A V_{GS}=10 V	—	3.6	—	3.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1800	—	1800	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	750	—	750	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=22.5 A	310(typ)	475	310(typ)	475	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	220(typ)	350	220(typ)	350	ns
Fall Time	t_f	V_{GS}=10 V	240(typ)	375	240(typ)	375	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK45N05, RFK45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	150(typ.)		150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFK45N05, RFK45N06

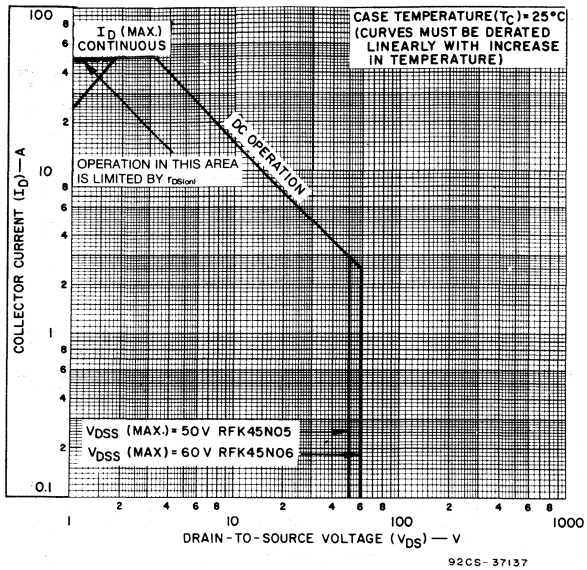


Fig. 1 — Maximum safe operating areas for all types.

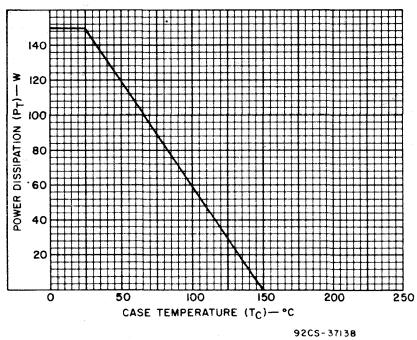


Fig. 2 — Power vs. temperature derating curve for all types.

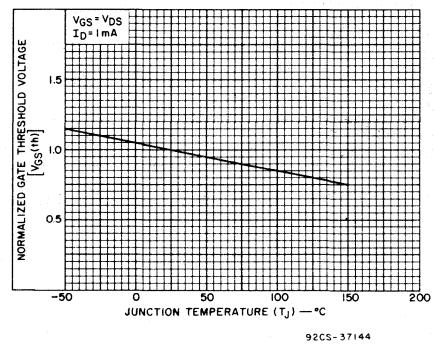


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

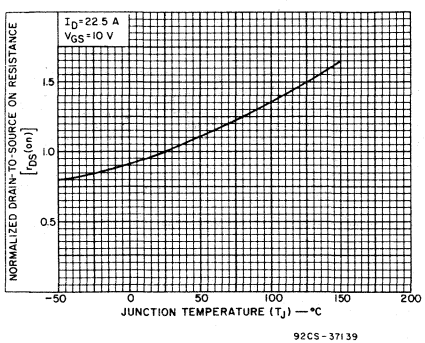


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

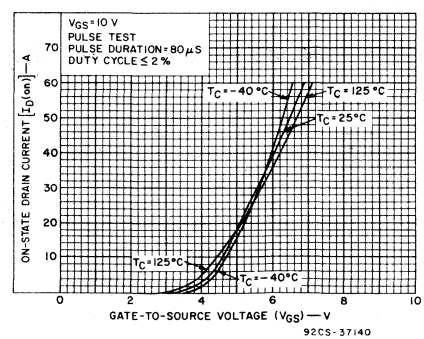


Fig. 5 — Typical transfer characteristics for all types.

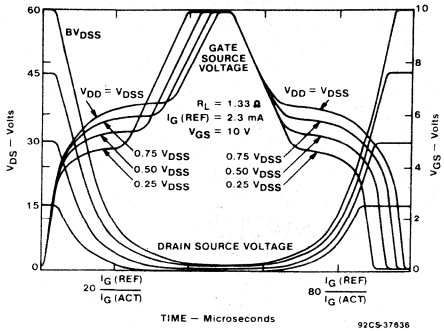


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

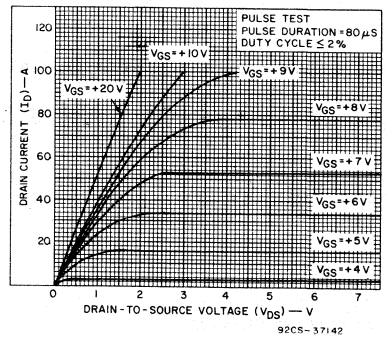


Fig. 7 — Typical saturation characteristics for all types.

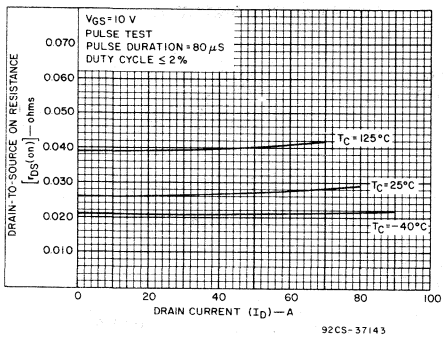


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

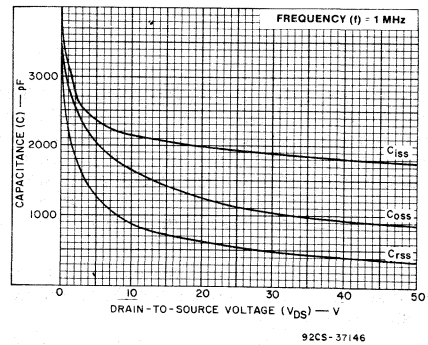


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

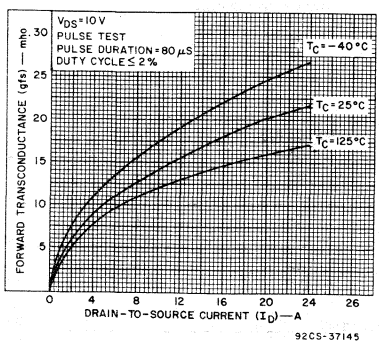


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

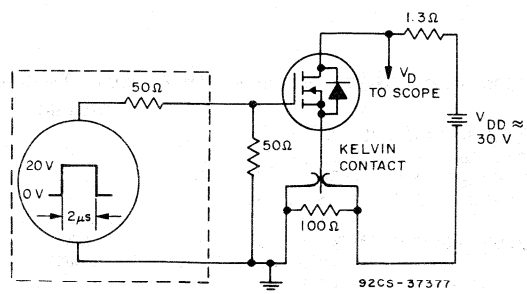


Fig. 11 - Switching Time Test Circuit.

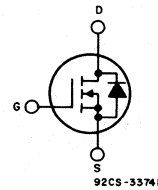
RFL1N08, RFL1N10, RFP2N08, RFP2N10

File Number **1385**

N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, 80 and 100 V
$r_{DS}(on)$: 1.05Ω and 1.2Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

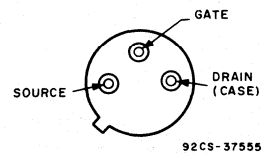
The RFL1N08 and RFL1N10 and the RFP2N08 and RFP2N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9282 and TA9283, respectively.

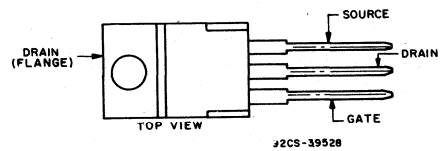
TERMINAL DESIGNATIONS

RFL1N08
RFL1N10



JEDEC TO-205AF

RFP2N08
RFP2N10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

		RFL1N08	RFL1N10	RFP2N08	RFP2N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100	80	100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	80	100	80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION @ T_C=25°C	P_T	8.33	8.33	25	25	W
Derate above T_C=25°C		0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFL1N08, RFL1N10, RFP2N08, RFP2N10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N08 RFP2N08 Min.	LIMITS RFL1N08 RFP2N08 Max.	LIMITS RFL1N10 RFP2N10 Min.	LIMITS RFL1N10 RFP2N10 Max.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0		80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA		2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V		—	1	—	—	μA
		V_{DS}=80 V		—	—	—	1	
		T_C=125° C, V_{DS}=65 V		—	50	—	—	
		T_C=125° C, V_{DS}=80 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V	RFP	—	1.05	—	1.05	V
			RFL	—	1.2	—	1.2	
		I_D=2 A, V_{GS}=10 V	RFP	—	3.0	—	3.0	
			RFL	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V	RFP	—	1.05	—	1.05	Ω
			RFL	—	1.4	—	1.4	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A		400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	80	—	80	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz		—	25	—	25	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V		17(Typ)	25	17(Typ)	25	ns
Rise Time	t_r	I_D=1 A		30(Typ)	45	30(Typ)	45	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω		30(Typ)	45	30(Typ)	45	
Fall Time	t_f	V_{GS}=10 V	RFP	17(Typ)	25	17(Typ)	25	
			RFL	30(Typ)	50	30(Typ)	50	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1N08, RFL1N10		—	15	—	15	°C/W
		RFP2N08, RFP2N10		—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N08 RFP2N08 Min.	LIMITS RFL1N08 RFP2N08 Max.	LIMITS RFL1N10 RFP2N10 Min.	LIMITS RFL1N10 RFP2N10 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	100(typ.)		100(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFL1N08, RFL1N10, RFP2N08, RFP2N10

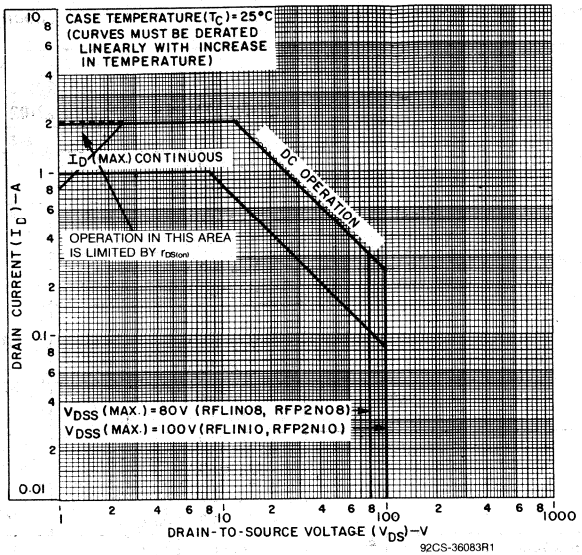


Fig. 1 - Maximum operating areas for all types.

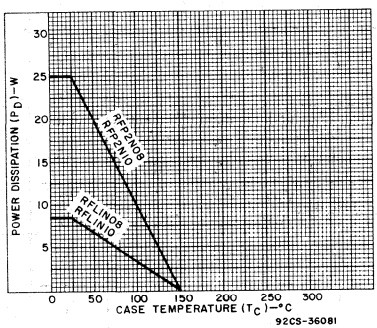


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

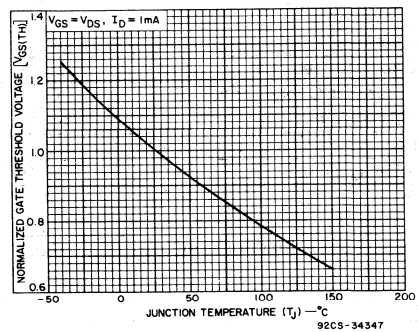


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

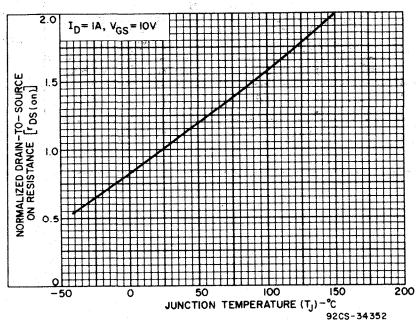


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

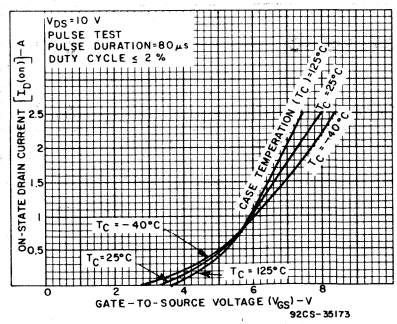


Fig. 5 - Typical transfer characteristics for all types.

RFL1N08, RFL1N10, RFP2N08, RFP2N10

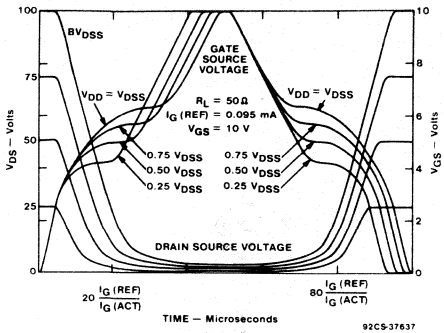


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

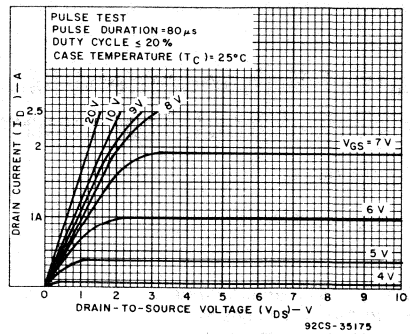


Fig. 7 - Typical saturation characteristics for all types.

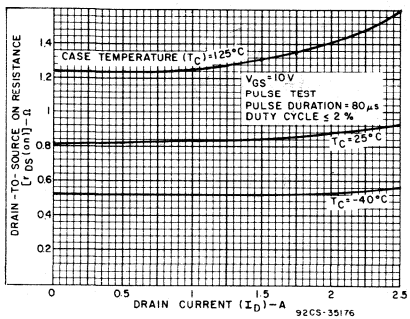


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

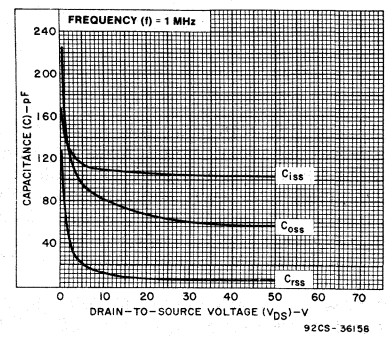


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

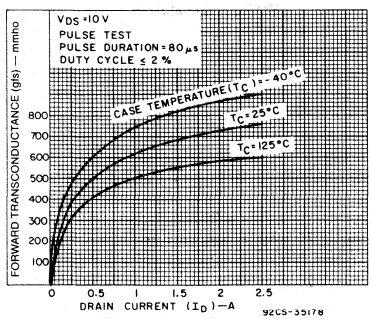


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

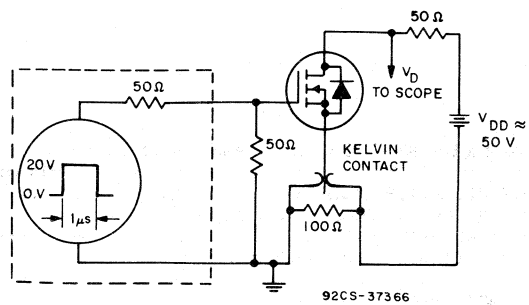


Fig. 11 - Switching Time Test Circuit.

RFL1N12, RFL1N15, RFP2N12, RFP2N15

File Number **1444**

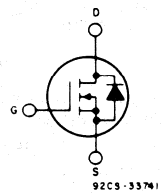
N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 Amperes 120 V — 150 V

$r_{DS}(on)$: 1.75Ω and 1.9Ω

Features:

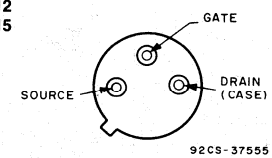
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

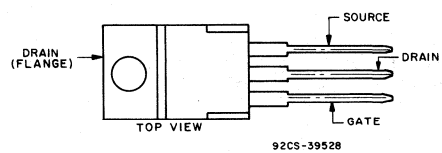
TERMINAL DESIGNATIONS

RFL1N12
RFL1N15



JEDEC TO-205AF

RFP2N12
RFP2N15



JEDEC TO-220AB

The RFL1N12 and RFL1N15 and the RFP2N12 and RFP2N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9196 and TA9213, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFL1N12	RFL1N15	RFP1N12	RFP2N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1A	1A	2A	2A	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION						
@ T_C=25°C	P_T	8.33	8.33	25	25	W
Derate above T_C=25°C		0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	−55 to +150				°C

RFL1N12, RFL1N15, RFP2N12, RFP2N15

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_c) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS RFL1N12 RFP2N12 MIN.	LIMITS RFL1N12 RFP2N12 MAX.	LIMITS RFL1N15 RFP2N15 MIN.	LIMITS RFL1N15 RFP2N15 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0		120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 2 mA		2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V		—	1	—	—	μA
		V_{DS} = 120 V		—	—	—	1	
		T_C = 125°C, V_{DS} = 100 V		—	50	—	—	
		T_C = 125°C, V_{DS} = 120 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm$ 20 V, V_{DS} = 0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 1 A, V_{GS} = 10 V	RFP	—	1.75	—	1.75	V
			RFL	—	1.9	—	1.9	
		I_D = 2 A, V_{GS} = 10 V	RFP	—	6.0	—	6.0	
			RFL	—	6.3	—	6.3	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 1 A, V_{GS} = 10 V	RFP	—	2	—	2	Ω
			RFL	—	2.15	—	2.15	
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 1 A		400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz		—	200	—	200	pF
Output Capacitance	C_{oss}			—	80	—	80	
Reverse Transfer Capacitance	C_{rss}			—	25	—	25	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 75 V, I_D = 1 A, $R_{gen} = R_{gs}$ = 50 Ω, V_{GS} = 10 V		17(typ.)	25	17(typ.)	25	ns
Rise Time	t_r			30(typ.)	45	30(typ.)	45	
Turn-Off Delay Time	$t_{d(off)}$			30(typ.)	45	30(typ.)	45	
Fall Time	t_f		RFP	17(typ.)	25	17(typ.)	25	
			RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	RθJC	RFL1N12, RFL1N15		—	15	—	15	°C/W
		RFP2N12, RFP2N15		—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N12 RFP2N12 Min.	LIMITS RFL1N12 RFP2N12 Max.	LIMITS RFL1N15 RFP2N15 Min.	LIMITS RFL1N15 RFP2N15 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	150(typ.)		150(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs duty cycle = 2%.

RFL1N12, RFL1N15, RFP2N12, RFP2N15

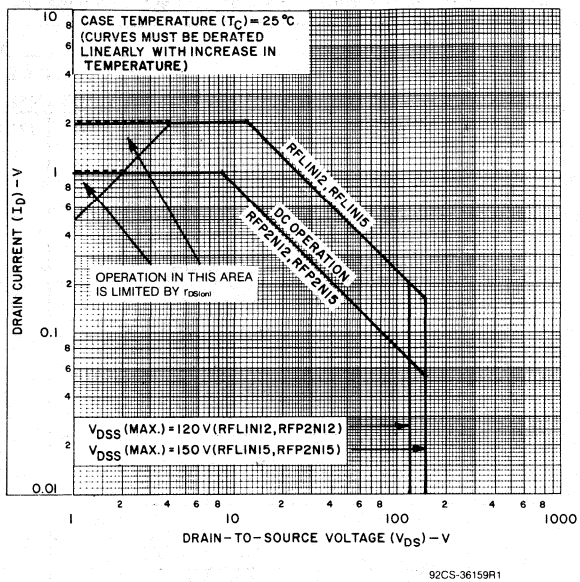


Fig. 1 — Maximum operating areas for all types.

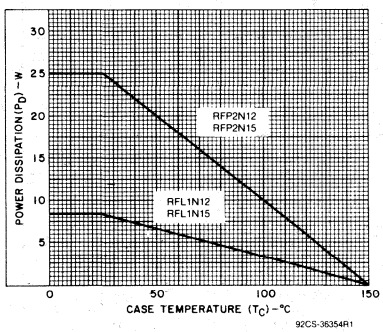


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

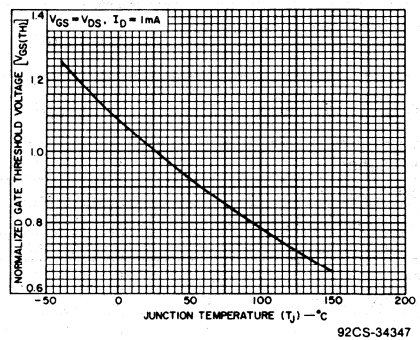


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

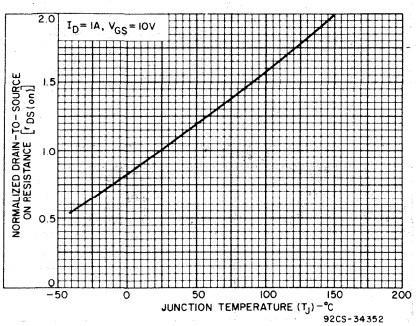


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

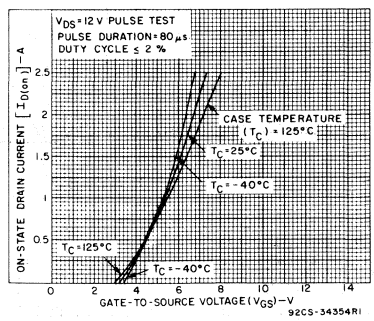


Fig. 5 — Typical transfer characteristics for all types.

RFL1N12, RFL1N15, RFP2N12, RFP2N15

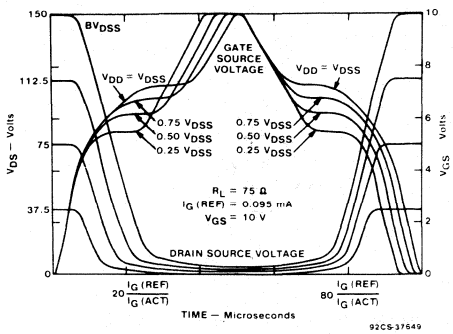


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

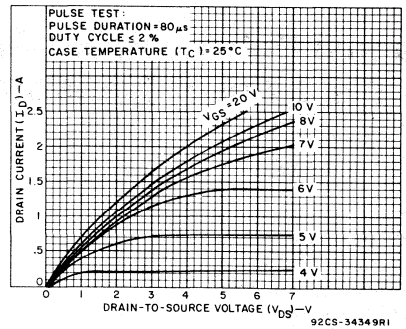


Fig. 7 — Typical saturation characteristics for all types.

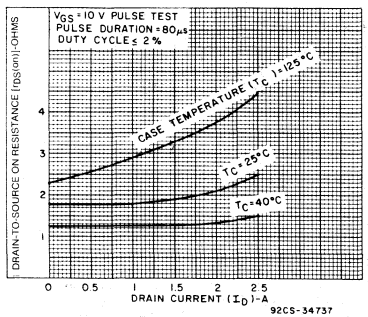


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

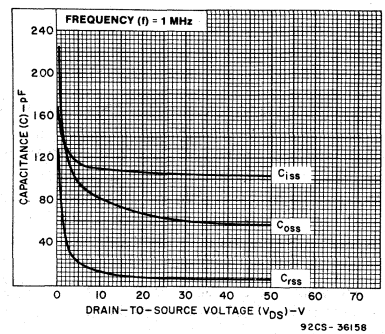


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

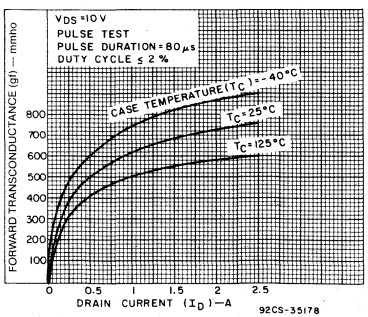


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

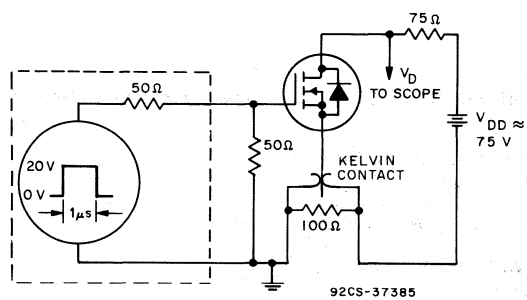


Fig. 11 — Switching Time Test Circuit.

RFL1N18, RFL1N20, RFP2N18, RFP2N20

File Number **1442**

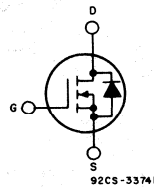
N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, 180 and 200 V

r_{DS}(on): 3.5Ω and 3.65Ω

Features:

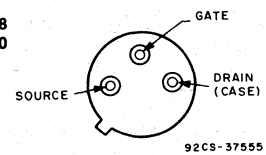
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

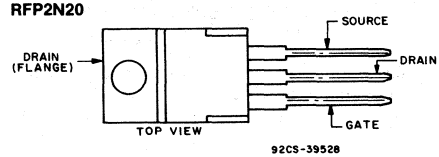
TERMINAL DESIGNATIONS

RFL1N18
RFL1N20



JEDEC TO-205AF

RFP2N18
RFP2N20



JEDEC TO-220AB

The RFL1N18 nd RFL1N20 and the RFP2N18 and RFP2N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9289 and TA9290, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

		RFL1N18	RFL1N20	RFP2N18	RFP2N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	180	200	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	180	200	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION	P_T					
@ T_C=25°C		8.33	8.33	25	25	W
Derate above T_C=25°C		0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFL1N18, RFL1N20, RFP2N18, RFP2N20

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18 RFP2N18		RFL1N20 RFP2N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0	180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125°C, V_{DS}=145 V	—	50	—	—	
		T_C=125°C, V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V RFP	—	3.5	—	3.5	V
		I_D=1 A, V_{GS}=10 V RFL	—	3.65	—	3.65	
		I_D=2 A, V_{GS}=10 V RFP	—	8.0	—	8.0	
		I_D=2 A, V_{GS}=10 V RFL	—	8.3	—	8.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V RFP	—	3.5	—	3.5	Ω
		I_D=1 A, V_{GS}=10 V RFL	—	3.65	—	3.65	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A	400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V, V_{GS}=0 V, f = 1MHz	—	200	—	200	pF
Output Capacitance	C_{oss}		—	60	—	60	
Reverse-Transfer Capacitance	C_{rss}		—	25	—	25	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V, I_D=1 A, R_{gen}=R_{gs}=50 Ω, V_{GS}=10 V RFP	15(Typ)	25	15(Typ)	25	ns
Rise Time	t_r		20(Typ)	30	20(Typ)	30	
Turn-Off Delay Time	$t_d(off)$		25(Typ)	40	25(Typ)	40	
Fall Time	t_f		15(Typ)	25	15(Typ)	25	
		RFL	30(Typ)	50	30(Typ)	50	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1N18, RFL1N20	—	15	—	15	°C/W
		RFP2N18, RFP2N20	—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18 RFP2N18		RFL1N20 RFP2N20		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	200(typ.)		200(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFL1N18, RFL1N20, RFP2N18, RFP2N20

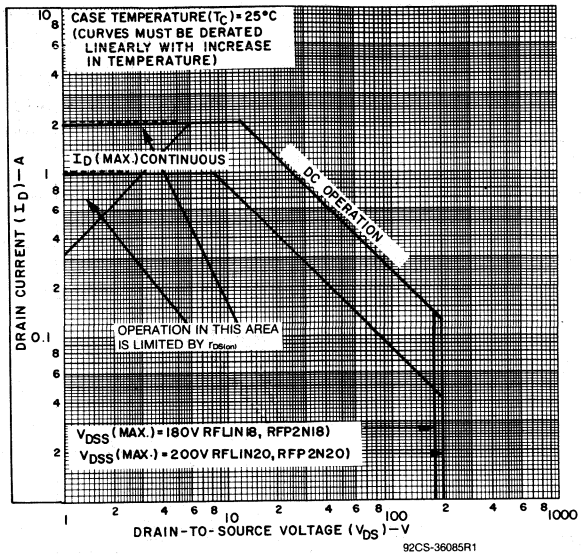


Fig. 1 - Maximum operating areas for all types.

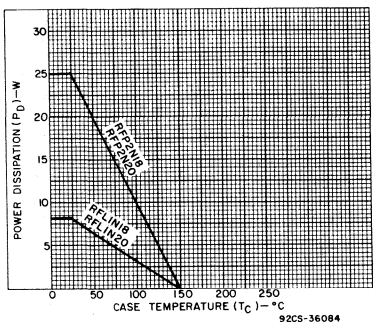


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

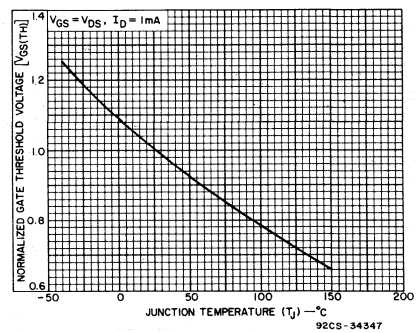


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

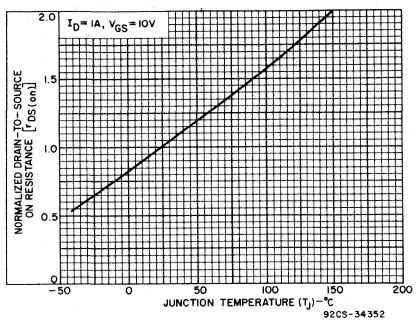


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

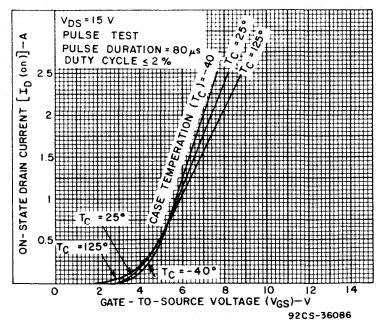


Fig. 5 - Typical transfer characteristics for all types.

RFL1N18, RFL1N20, RFP2N18, RFP2N20

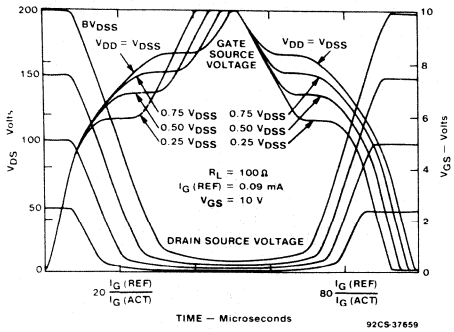


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

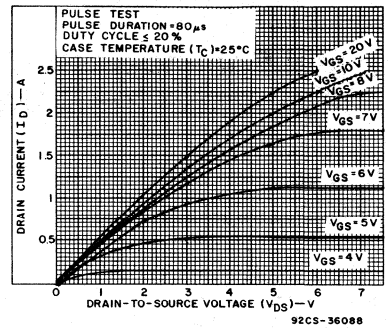


Fig. 7 - Typical saturation characteristics for all types.

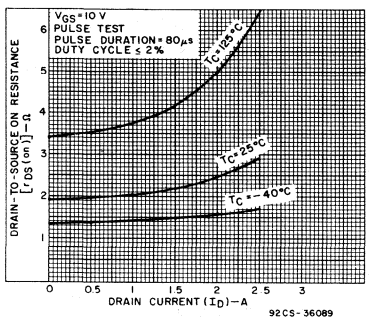


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

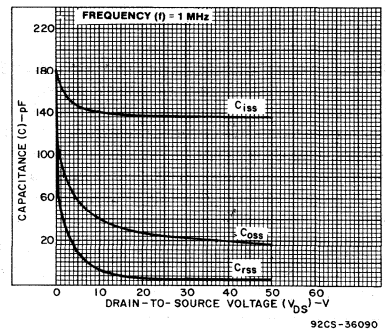


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

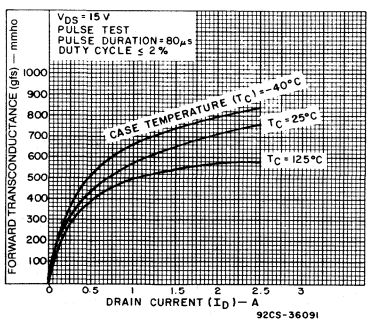


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

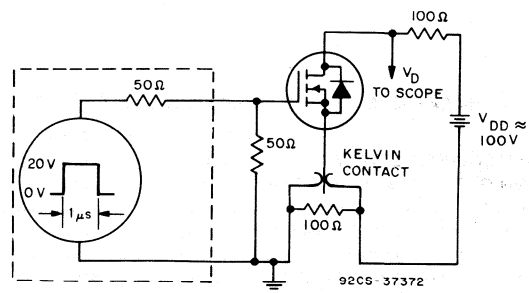


Fig. 11 — Switching Time Test Circuit.

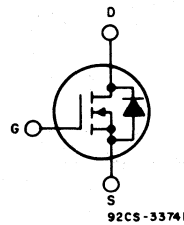
RFL2N05, RFL2N06, RFP4N05, RFP4N06

File Number **1497**

N-Channel Enhancement-Mode Power Field-Effect Transistors

2 and 4 Amperes, 50 V - 60 V
$r_{DS}(on)$ = 0.6Ω and 0.75Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

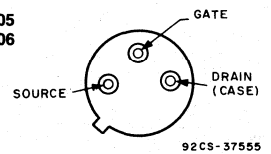
The RFL2N05 and RFL2N06 and the RFP4N05 and RFP4N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9378 and TA9379, respectively.

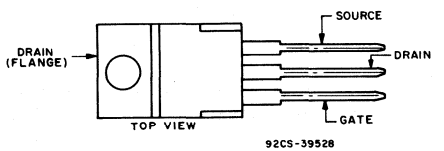
TERMINAL DESIGNATIONS

RFL2N05
RFL2N06



JEDEC TO-205AF

RFP4N05
RFP4N06



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL2N05	RFL2N06		RFP4N05	RFP4N06	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60		50	60	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	50	60		50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D	2	2		4	4	A
Pulsed ..... I_{DM}			10			A
POWER DISSIPATION @ T_C=25°C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25°C	0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL2N05, RFL2N06, RFP4N05, RFP4N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05 RFP4N05		RFL2N06 RFP4N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	μA
		V_{DS}=50 V	—	—	—	1	
		T_C=125°C, V_{DS}=40 V	—	50	—	—	
		T_C=125°C, V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V RFP	—	0.6	—	0.6	V
		I_D=1 A, V_{GS}=10 V RFL	—	0.75	—	0.75	
		I_D=2 A, V_{GS}=10 V	—	2.0	—	2.0	
		I_D=4 A, V_{DS}=15 V	—	4.8	—	4.8	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V RFP	—	0.6	—	0.6	Ω
		I_D=1 A, V_{GS}=10 V RFL	—	0.75	—	0.75	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A	400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V, V_{GS}=0 V, f = 1MHz	—	200	—	200	pF
Output Capacitance	C_{oss}		—	85	—	85	
Reverse Transfer Capacitance	C_{rss}		—	30	—	30	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V, I_D=1 A, R_{gen}=R_{gs}=50 Ω, V_{GS}=10 V RFP	6(typ)	15	6(typ)	15	ns
Rise Time	t_r		14(typ)	30	14(typ)	30	
Turn-Off Delay Time	$t_d(off)$		16(typ)	30	16(typ)	30	
Fall Time	t_f	V_{GS}=10 V RFP	14(typ)	25	14(typ)	25	
		V_{GS}=10 V RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL2N05, RFL2N06	—	15	—	15	°C/W
		RFP4N05, RFP4N06	—	5	—	5	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05 RFP4N05		RFL2N06 RFP4N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	100(typ.)		100(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFL2N05, RFL2N06, RFP4N05, RFP4N06

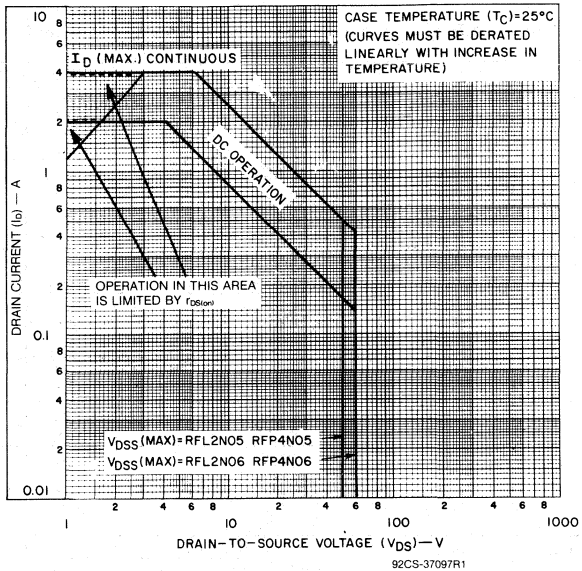


Fig. 1 — Maximum operating areas for all types.

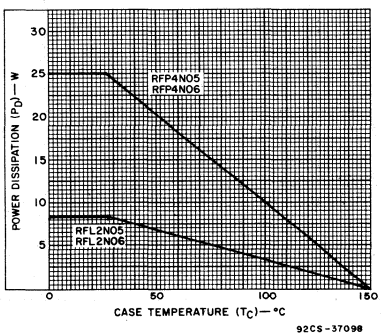


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

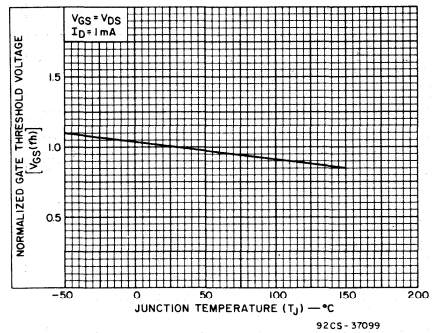


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

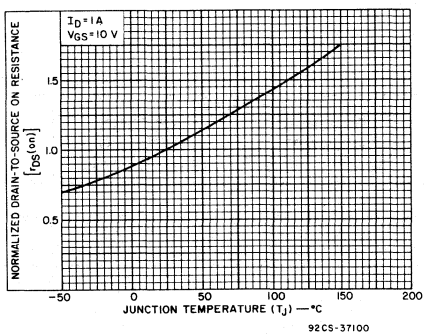


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

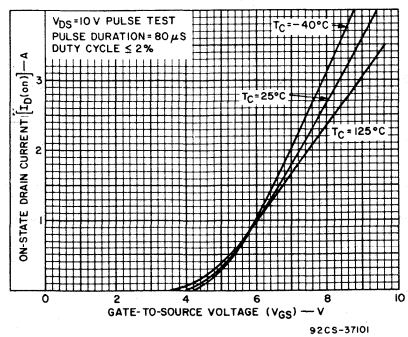


Fig. 5 — Typical transfer characteristics for all types.

RFL2N05, RFL2N06, RFP4N05, RFP4N06

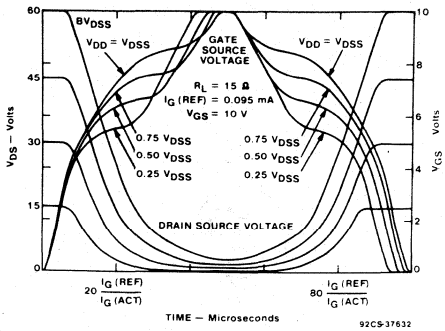


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

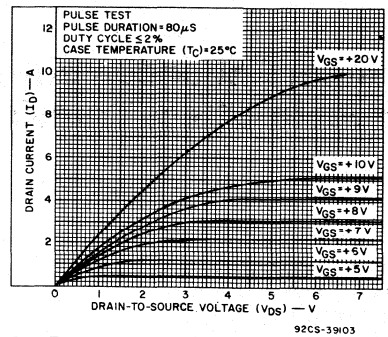


Fig. 7 — Typical saturation characteristics for all types.

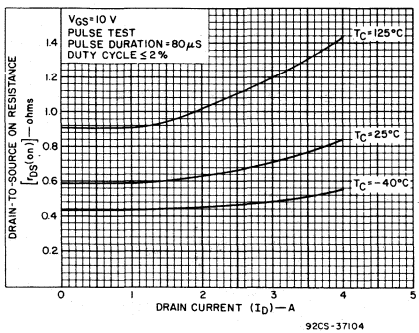


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

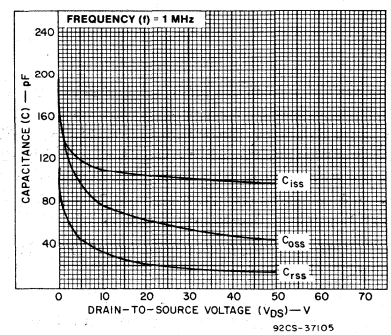


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

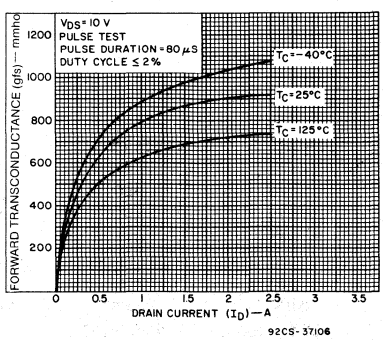


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

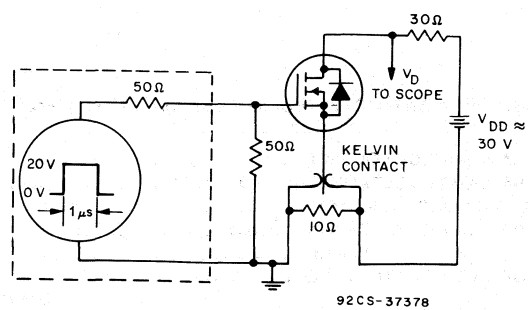


Fig. 11 — Switching Time Test Circuit.

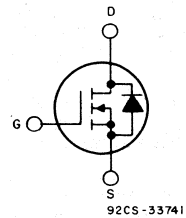
RFL4N12, RFL4N15

File Number **1462**

N-Channel Enhancement-Mode Power Field-Effect Transistors

4 A, 120 and 150 V
$r_{DS}(on)$: 0.4Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

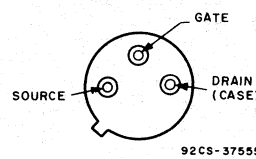
N-CHANNEL ENHANCEMENT MODE

The RFL4N12 and RFL4N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

*The RFL4N12 and RFL4N15 series were formerly RCA developmental numbers TA9256A and TA9256B, respectively.

TERMINAL DESIGNATIONS



92CS-37555

JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

		RFL4N12	RFL4N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	±20	V
DRAIN CURRENT RMS Continuous	I_D	4	4	A
Pulsed	I_{DM}	15	15	A
POWER DISSIPATION @ T_C=25°C	P_T	8.33	8.33	W
Derate above T_C=25°C		0.0667	0.0667	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	-55 to +150	°C

RFL4N12, RFL4N15

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125°C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	0.8	—	0.8	V
		I_D=4 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	0.40	—	0.40	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	850	—	850	pF
Output Capacitance	C_{oss}		—	230	—	230	
Reverse-Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 75 V I_D=2 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	40(typ)	60	40(typ)	60	ns
Rise Time	t_r		165(typ)	250	165(typ)	250	
Turn-Off Delay Time	$t_d(off)$		90(typ)	135	90(typ)	135	
Fall Time	t_f		90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL4N12, RFL4N15	—	15	—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 2A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFL4N12, RFL4N15

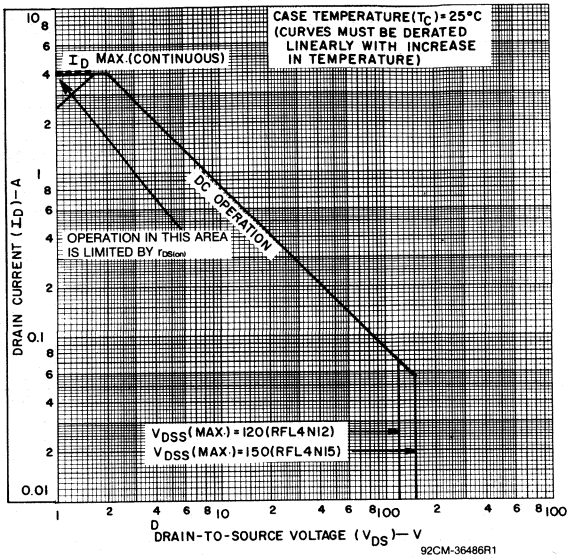


Fig. 1 - Maximum safe operating areas for all types.

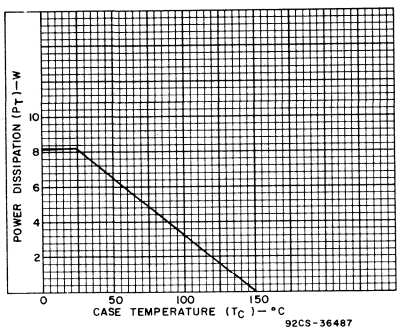


Fig. 2 - Power vs. temperature derating curve for all types.

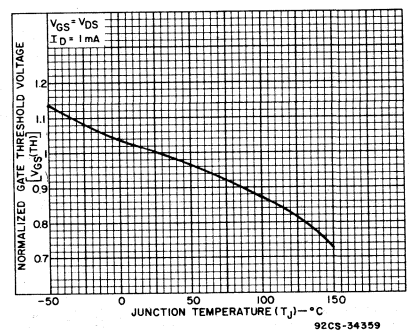


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

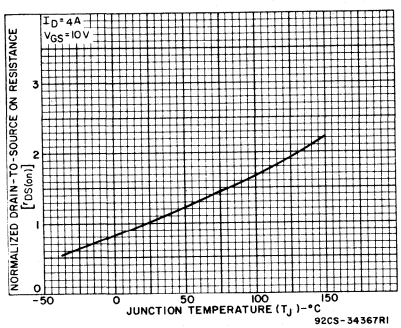


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

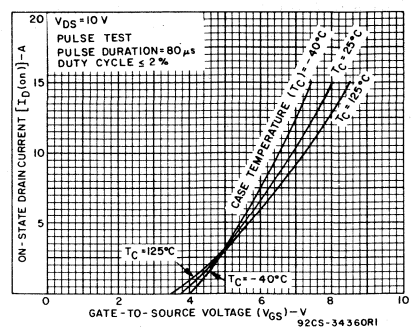


Fig. 5 - Typical transfer characteristics for all types.

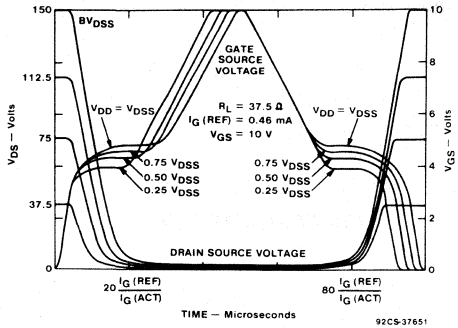


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

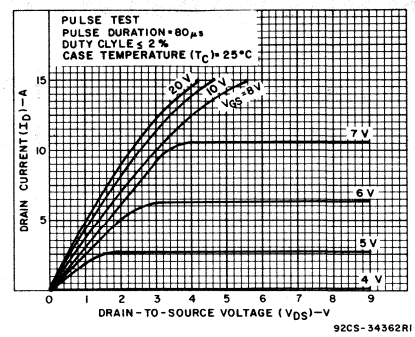


Fig. 7 - Typical saturation characteristics for all types.

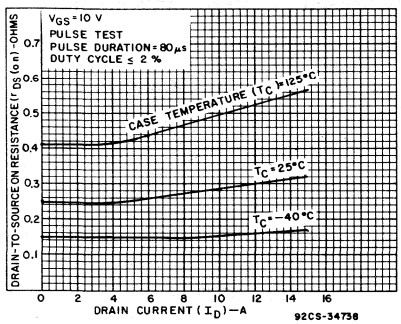


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

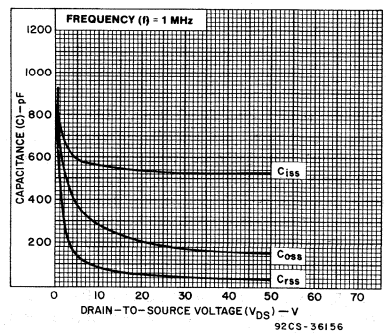


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

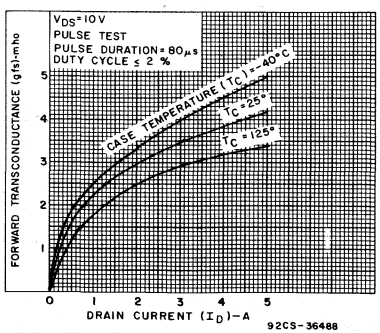


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

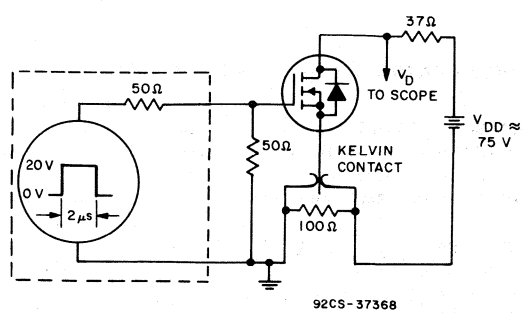


Fig. 11 - Switching Time Test Circuit.

RFM3N45, RFM3N50, RFP3N45, RFP3N50

File Number **1384**

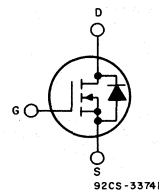
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3 A, 450 and 500 V
r_{DS}(on): 3Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

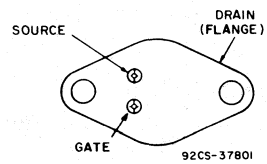
The RFM3N45 and RFM3N50 and the RFP3N45 and RFP3N50 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9193 and TA9232, respectively.

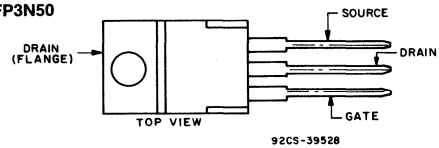
TERMINAL DESIGNATIONS

RFM3N45
RFM3N50



JEDEC TO 204AA

RFP3N45
RFP3N50



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM3N45	RFM3N50		RFP3N45	RFP3N50	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	450	500		450	500	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) ... V_{DGR}	450	500		450	500	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			3			A
Pulsed ..... I_{DM}			5			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM3N45, RFM3N50, RFP3N45, RFP3N50

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS}=0	450	—	500	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V	—	10	—	—	μA
		V_{DS}=400 V	—	—	—	10	
		T_C=125°C V_{DS}=360 V	—	50	—	—	
		V_{DS}=400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm$20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	4.5	—	4.5	V
		I_D=3 A V_{GS}=10 V	—	10.5	—	10.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	3	—	3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=1.5 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	750	—	750	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	150	—	150	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=250 V	30(Typ)	45	30(Typ)	45	ns
Rise Time	t_r	I_D=1.5 A	40(Typ)	60	40(Typ)	60	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	90(Typ)	135	90(Typ)	135	
Fall Time	t_f	V_{GS}=10 V	50(Typ)	75	50(Typ)	75	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM3N45, RFM3N50	—	1.67	—	1.67	°C/W
		RFP3N45, RFP3N50	—	2.083	—	2.083	

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM3N45, RFM3N50, RFP3N45, RFP3N50

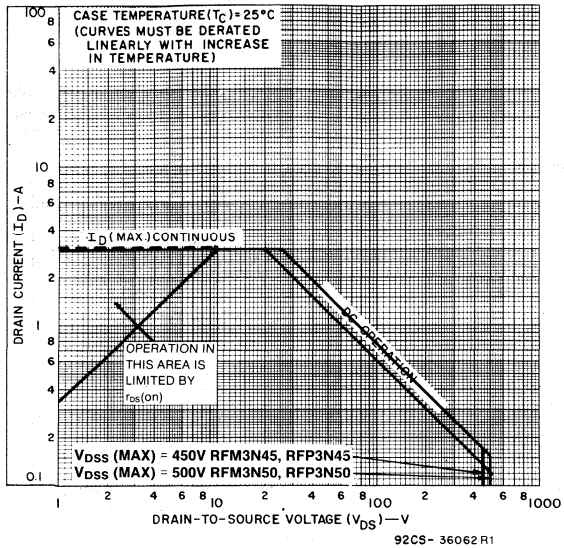


Fig. 1 - Maximum operating areas for all types.

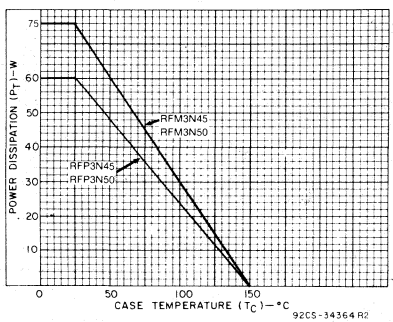


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

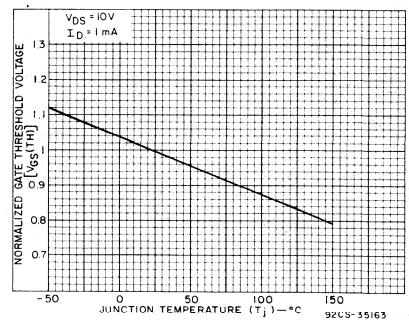


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

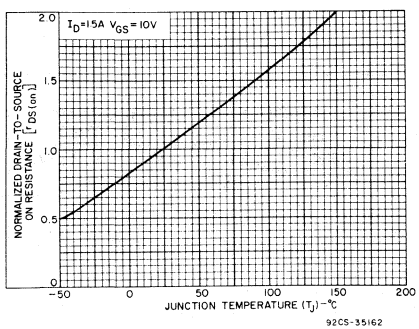


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

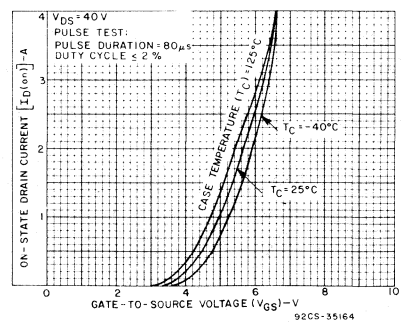


Fig. 5 - Typical transfer characteristics for all types.

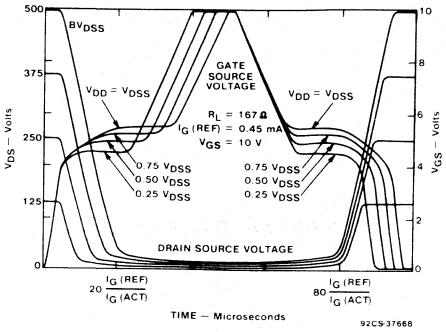


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

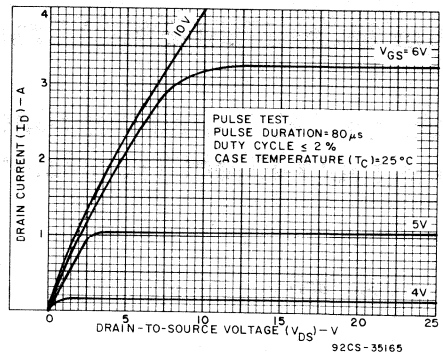


Fig. 7 - Typical saturation characteristics for all types.

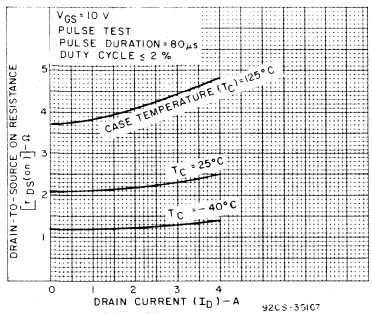


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

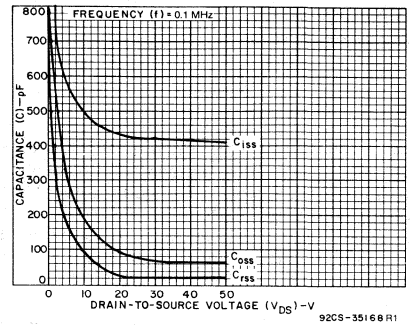


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

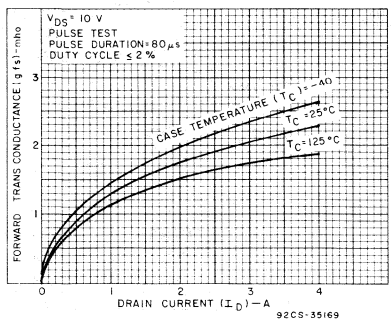


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

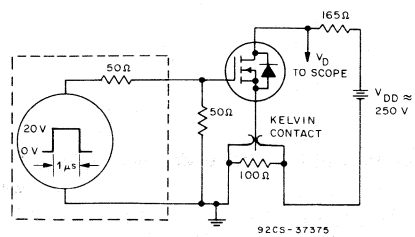


Fig. 11 — Switching Time Test Circuit

RFM4N35, RFM4N40, RFP4N35, RFP4N40

File Number **1491**

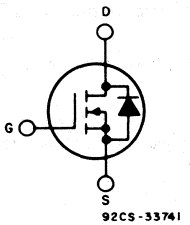
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

4 A, 350 V and 400 V
$r_{DS}(on)$: 2Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

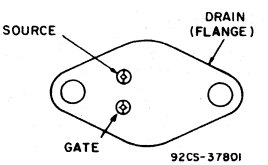
The RFM4N35 and RFM4N40 and the RFP4N35 and RFP4N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9393 and TA9394, respectively.

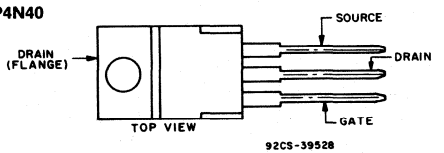
TERMINAL DESIGNATIONS

RFM4N35
RFM4N40



JEDEC TO-204AA

RFP4N35
RFP4N40



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM4N35	RFM4N40		RFP4N35	RFP4N40	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	350	400		350	400	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	350	400		350	400	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			4			A
Pulsed ..... I_{DM}			8			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM4N35, RFM4N40, RFP4N35, RFP4N40

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) 25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V V_{DS}=320 V	— —	10 —	— —	— 10	μA
		T_C=125°C V_{DS}=280 V V_{DS}=320 V	— —	100 —	— —	— 100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	4	—	4	V
		I_D=4 A V_{GS}=10 V	—	12	—	12	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	2	—	2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	750	—	750	pF
Output Capacitance	C_{oss}		—	150	—	150	
Reverse Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=200 V I_D=2 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	12(typ)	45	12(typ)	45	ns
Rise Time	t_r		42(typ)	60	42(typ)	60	
Turn-Off Delay Time	$t_d(off)$		130(typ)	200	130(typ)	200	
Fall Time	t_f		62(typ)	100	62(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM4N35, RFM4N40	—	1.67	—	1.67	°C/W
		RFP4N35, RFP4N40	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD} [a]	I_{SD}=2 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM4N35, RFM4N40, RFP4N35, RFP4N40

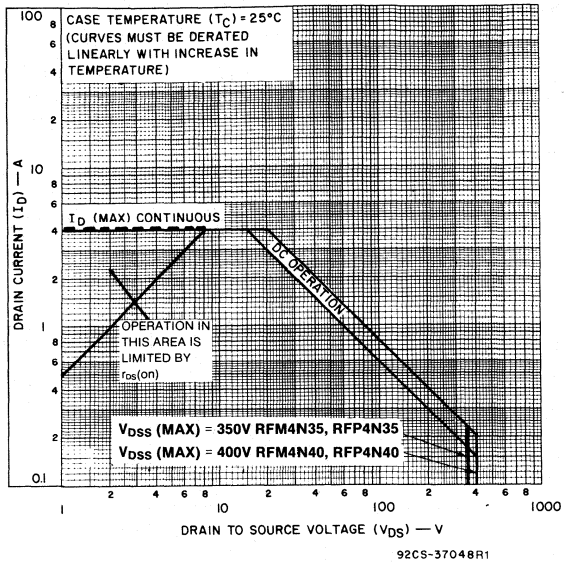


Fig. 1 — Maximum operating areas for all types.

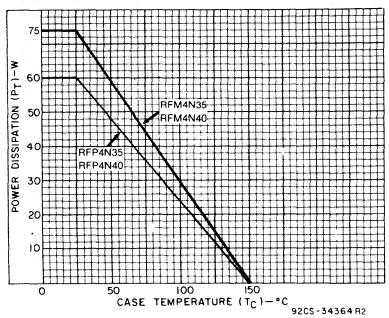


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

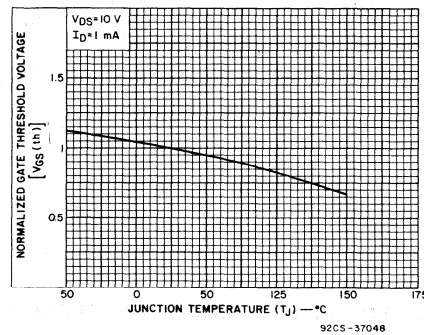


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

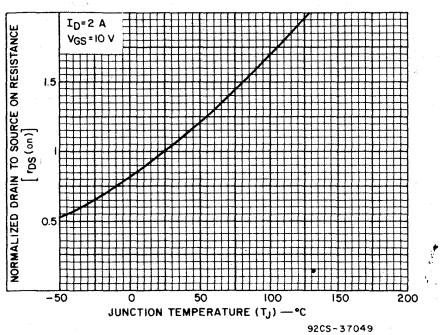


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

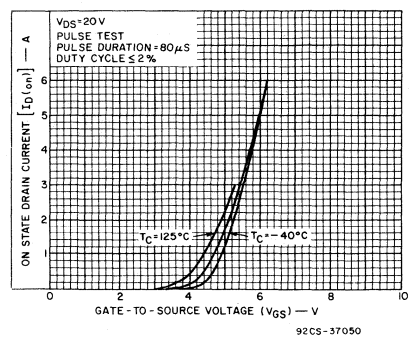


Fig. 5 — Typical transfer characteristics for all types.

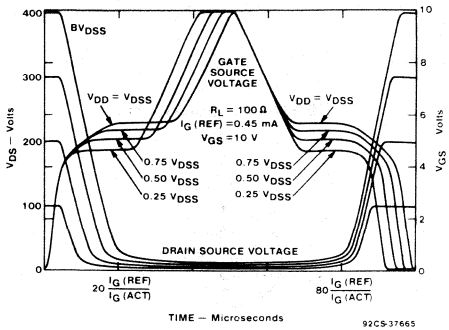


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

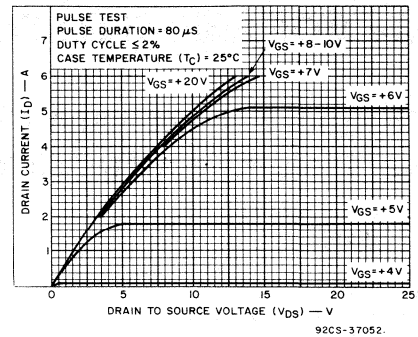


Fig. 7 — Typical saturation characteristics for all types.

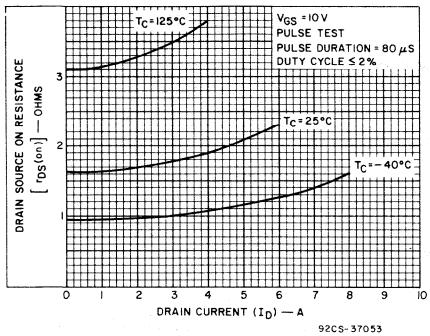


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

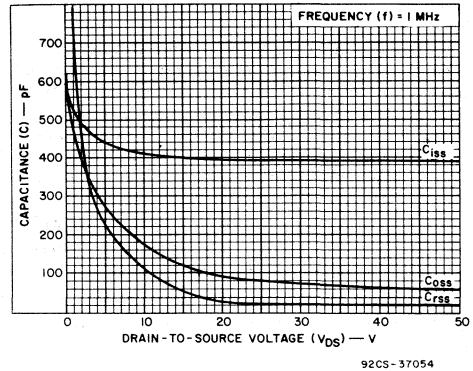


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

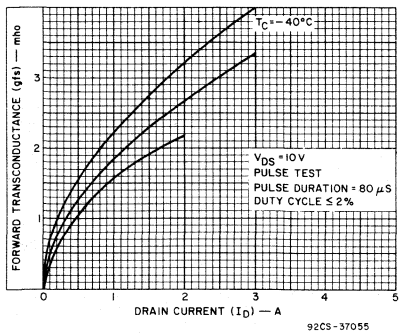


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

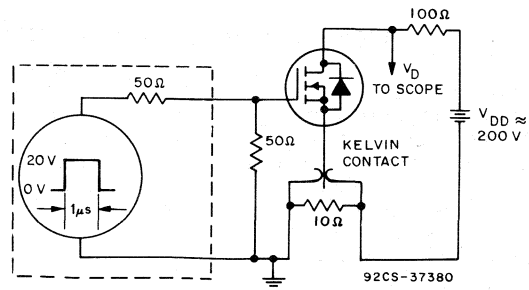


Fig. 11 — Switching Time Test Circuit

RFM6N45, RFM6N50, RFP6N45, RFP6N50

File Number **1494**

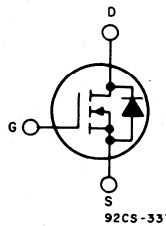
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

6 A, 450 V and 500 V
$r_{DS}(on)$ = 1.25Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

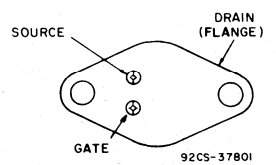
The RFM6N45 and RFM6N50 and the RFP6N45 and RFP6N50* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9191 and TA9231, respectively.

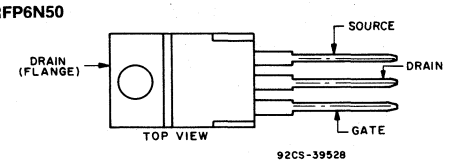
TERMINAL DESIGNATIONS

RFM6N45
RFM6N50



JEDEC TO-204AA

RFP6N45
RFP6N50



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM6N45	RFM6N50		RFP6N45	RFP6N50	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	450	500		450	500	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) .... V_{DGR}	450	500		450	500	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			6			A
Pulsed ..... I_{DM}			15			A
POWER DISSIPATION @ T_C 25°C ..... P_T	100	100		75	75	W
Derate above T_C 25° C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM6N45, RFM6N50, RFP6N45, RFP6N50

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V V_{DS}=400 V	— —	10 —	— —	— 10	μA
		T_C=125° C V_{DS}=360 V V_{DS}=400 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	3.75	—	3.75	V
		I_D=6 A V_{GS}=10 V	—	12	—	12	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	1.25	—	1.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	1500	—	1500	pF
Output Capacitance	C_{oss}		—	250	—	250	
Reverse Transfer Capacitance	C_{rss}		—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 250 V I_D=3 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r		40(typ)	80	40(typ)	80	
Turn-Off Delay Time	$t_d(off)$		190(typ)	300	190(typ)	300	
Fall Time	t_f		60(typ)	100	60(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6N45, RFM6N50	—	1.25	—	1.25	°C/W
		RFP6N45, RFP6N50	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} [a]	I_{SD} = 3A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	800(typ.)		800(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM6N45, RFM6N50, RFP6N45, RFP6N50

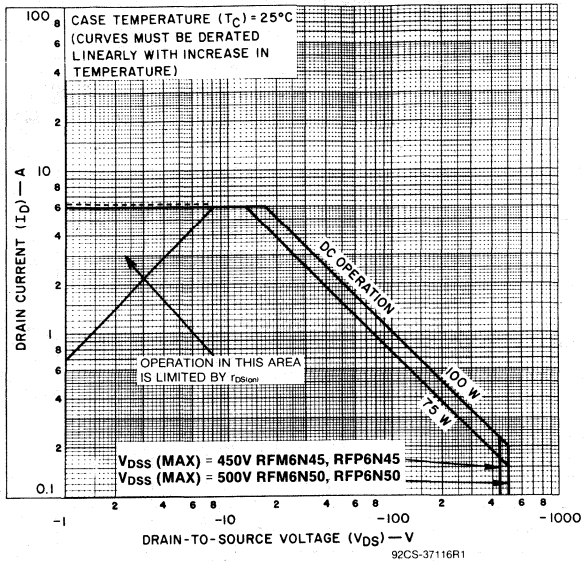


Fig. 1 — Maximum operating areas for all types.

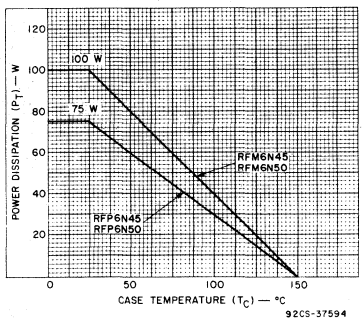


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

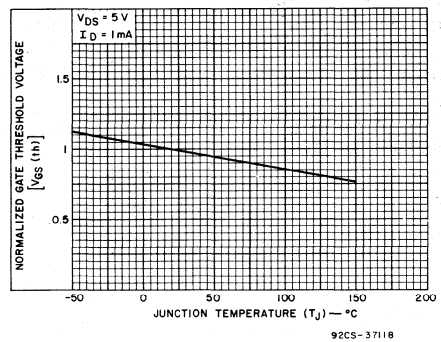


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

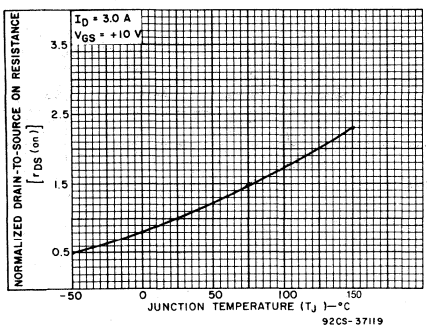


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

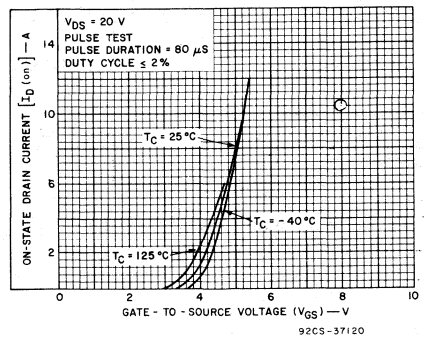


Fig. 5 — Typical transfer characteristics for all types.

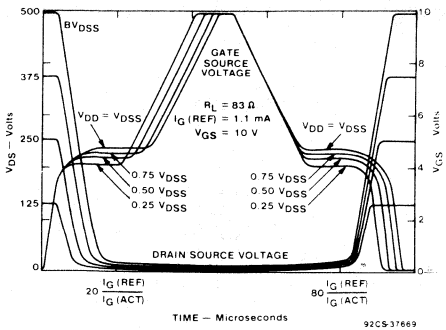


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

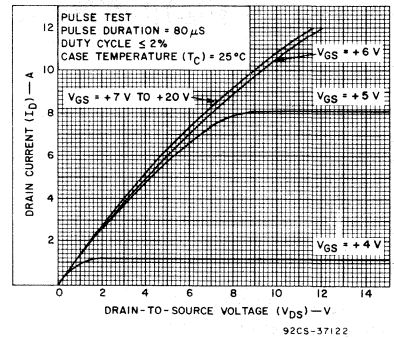


Fig. 7 — Typical saturation characteristics for all types.

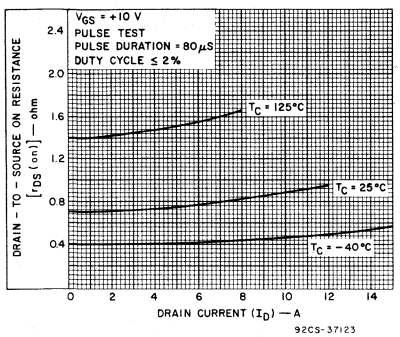


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

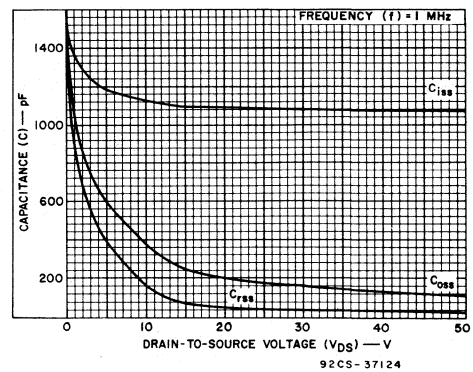


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

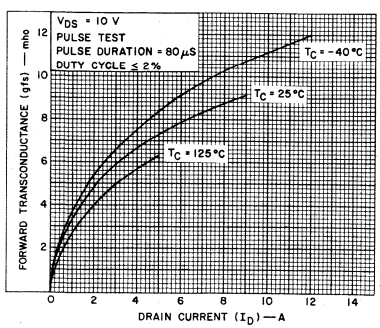


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

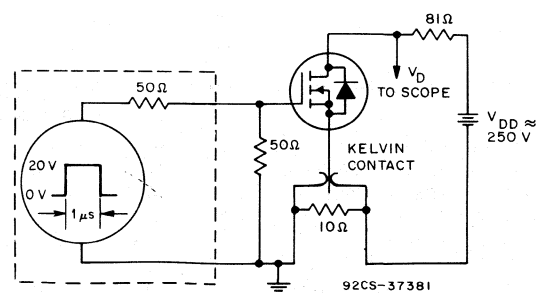


Fig. 11 — Switching Time Test Circuit.

RFM7N35, RFM7N40, RFP7N35, RFP7N40

File Number **1536**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

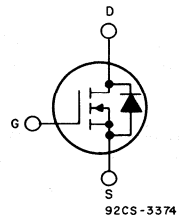
7 A, 350 V and 400 V

$r_{DS}(on)$: 0.75Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

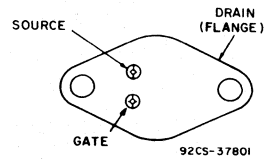
The RFM7N35 and RFM7N40 and the RFP7N35 and RFP7N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9397 and TA9398, respectively.

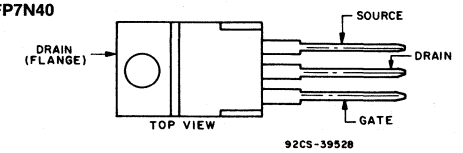
TERMINAL DESIGNATIONS

RFM7N35
RFM7N40



JEDEC TO-204AA

RFP7N35
RFP7N40



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

	RFM7N35	RFM7N40		RFP7N35	RFP7N40	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	350	400		350	400	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)..... V_{DGR}	350	400		350	400	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT						
Rms Continuous ..... I_D			7			A
Pulsed ..... I_{DM}			15			A
POWER DISSIPATION @ T_C=25°C ..... P_T	100	100		75	75	W
Derate above T_C=25°C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM7N35, RFM7N40, RFP7N35, RFP7N40

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V	—	1	—	—	μA
		V_{DS}=320 V	—	—	—	1	
		T_C=125° C V_{DS}=280 V	—	50	—	—	
		V_{DS}=320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3.5 A V_{GS}=10 V	—	2.63	—	2.63	V
		I_D=7 A V_{GS}=10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3.5 A V_{GS}=10 V	—	0.75	—	0.75	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1600	—	1600	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f= 1 MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS}=200 V	16(typ)	45	16(typ)	45	ns
Rise Time	t_r	I_D=3.5 A	54(typ)	75	54(typ)	75	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	170(typ)	250	170(typ)	250	
Fall Time	t_f	V_{GS}=10 V	62(typ)	100	62(typ)	100	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM7N35, RFM7N40	—	1.25	—	1.25	°C/W
		RFP7N35, RFP7N40	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=3.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A di_F/dt=100 A/μs	870 (typ)				ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFM7N35, RFM7N40, RFP7N35, RFP7N40

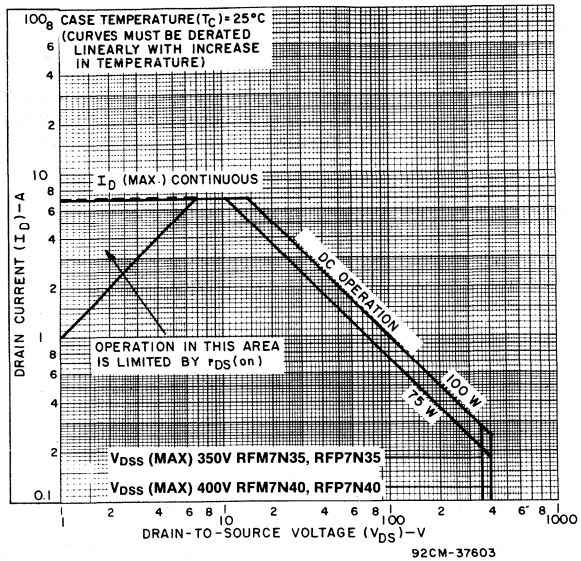


Fig. 1 - Maximum safe operating areas for all types.

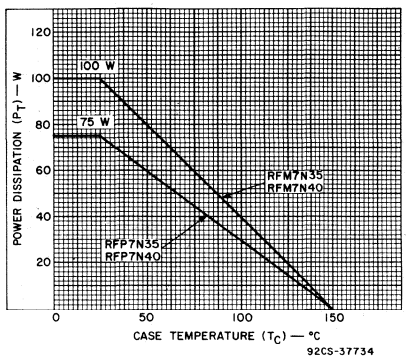


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

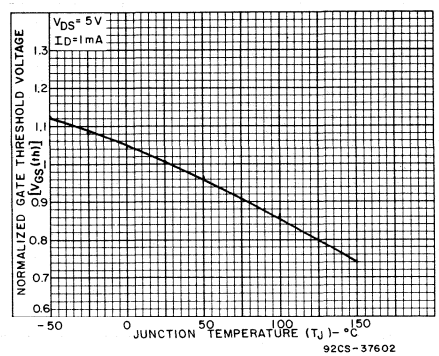


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

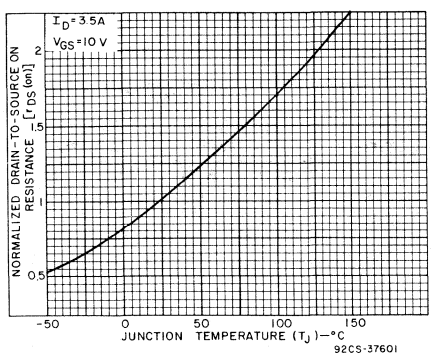


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

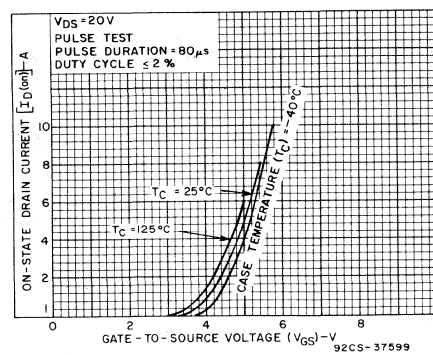


Fig. 5 - Typical transfer characteristics for all types.

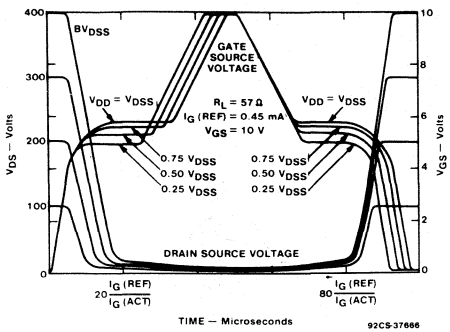


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

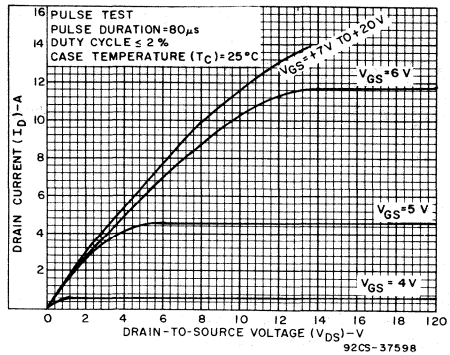


Fig. 7 - Typical saturation characteristics for all types.

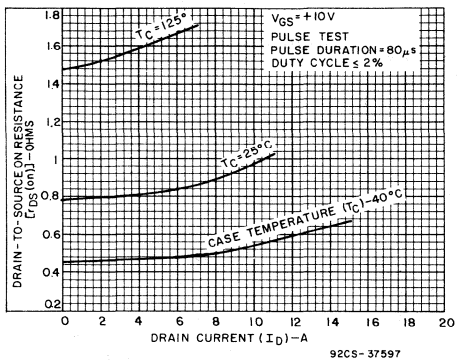


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

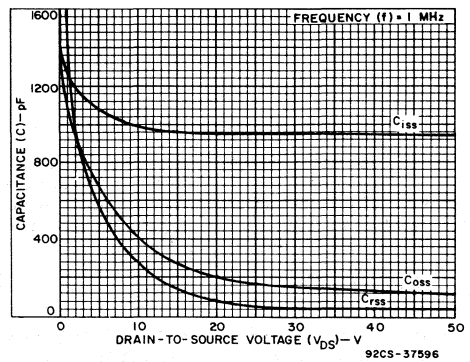


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

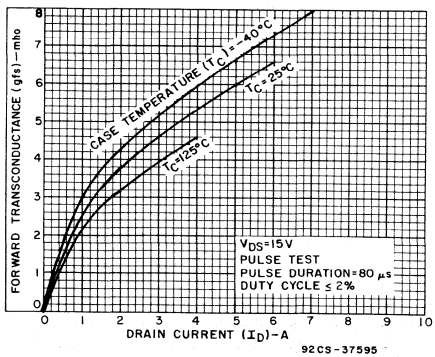


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

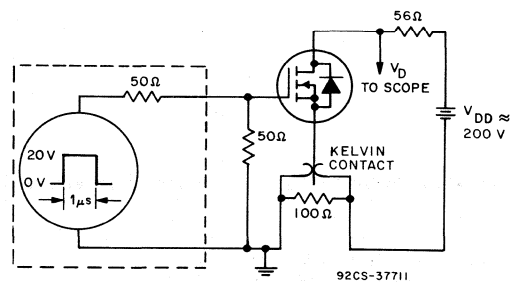


Fig. 11 - Switching time test circuit.

RFM8N18, RFM8N20, RFP8N18, RFP8N20

File Number **1447**

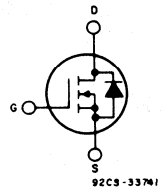
N-Channel Enhancement-Mode Power Field-Effect Transistors

8 A, 180 V — 200 V

$r_{DS}(on)$: 0.5 Ω

Features:

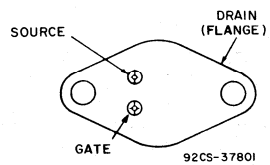
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

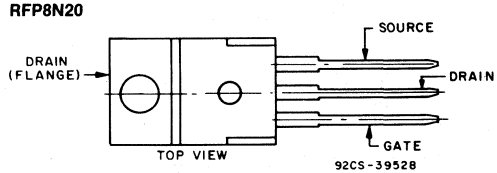
TERMINAL DESIGNATIONS

RFM8N18
RFM8N20



JEDEC TO-204AA

RFP8N18
RFP8N20



JEDEC TO-220AB

The RFM8N18 and RFM8N20 and the RFP8N18 and RFP8N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9291 and TA9292, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFM8N18	RFM8N20	RFP8N18	RFP8N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	180	200	V
DRAIN-GATE VOLTAGE (R_{GS} = 1MΩ)	V_{DGR}	180	200	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	8				A
Pulsed	I_{DM}	20				A
POWER DISSIPATION						
@ T_C = 25°C	P_T	75	75	60	60	W
Derate above T_C = 25°C		0.6	0.6	0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFM8N18, RFM8N20, RFP8N18, RFP8N20

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM8N18 RFP8N18 MIN.	LIMITS RFM8N18 RFP8N18 MAX.	LIMITS RFM8N20 RFP8N20 MIN.	LIMITS RFM8N20 RFP8N20 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145 V V_{DS} = 160 V	— —	1 —	— —	— 1	μA
		T_C = 125°C V_{DS} = 145 V V_{DS} = 160 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 4 A V_{GS} = 10 V	—	2.0	—	2.0	V
		I_D = 8 A V_{GS} = 10 V	—	5.5	—	5.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 4 A V_{GS} = 10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 4 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	750	—	750	pF
Output Capacitance	C_{oss}		—	250	—	250	
Reverse Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V I_D = 4 A R_{gen} = R_{gs} = 50 Ω V_{GS} = 10 V	30(typ.)	45	30(typ.)	45	ns
Rise Time	t_r		100(typ.)	150	100(typ.)	150	
Turn-Off Delay Time	$t_d(off)$		90(typ.)	135	90(typ.)	135	
Fall Time	t_f		70(typ.)	105	70(typ.)	105	
Thermal Resistance Junction-to-Case	RθJC	RFM8N18, RFM8N20	—	1.67	—	1.67	°C/W
		RFP8N18, RFP8N20	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM8N18 RFP8N18 Min.	LIMITS RFM8N18 RFP8N18 Max.	LIMITS RFM8N20 RFP8N20 Min.	LIMITS RFM8N20 RFP8N20 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	225(typ.)		225(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM8N18, RFM8N20, RFP8N18, RFP8N20

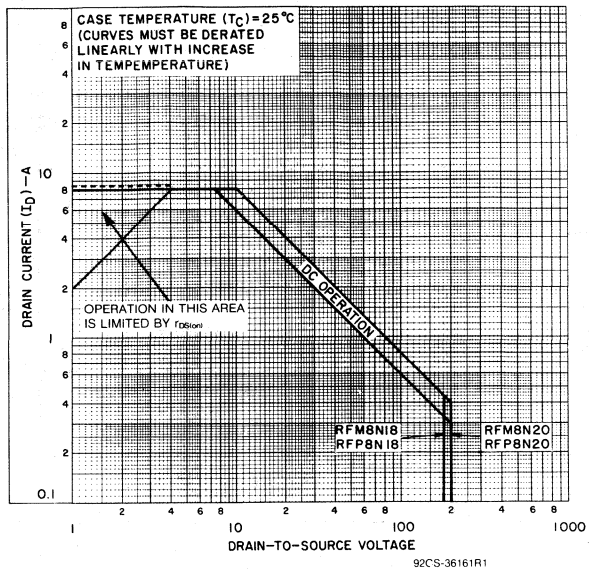


Fig. 1 — Maximum safe operating areas for all types.

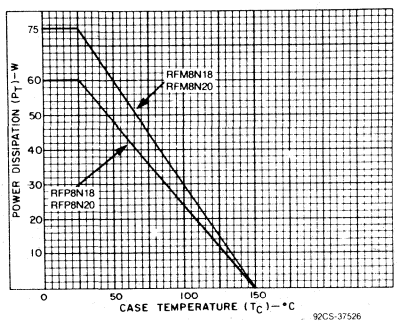


Fig. 2 — Power vs. temperature derating curve for all types.

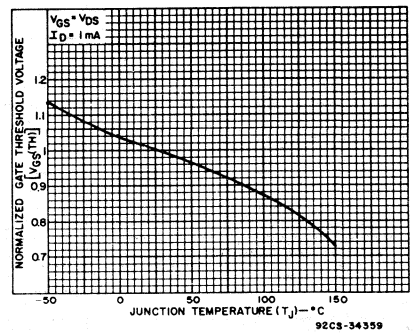


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

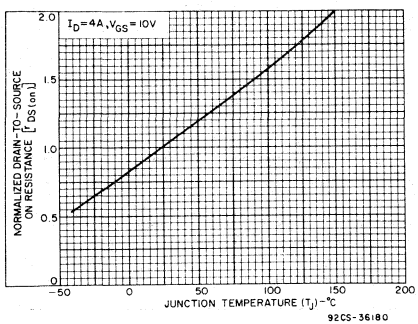


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

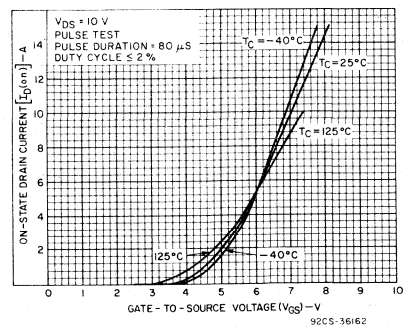


Fig. 5 — Typical transfer characteristics for all types.

RFM8N18, RFM8N20, RFP8N18, RFP8N20

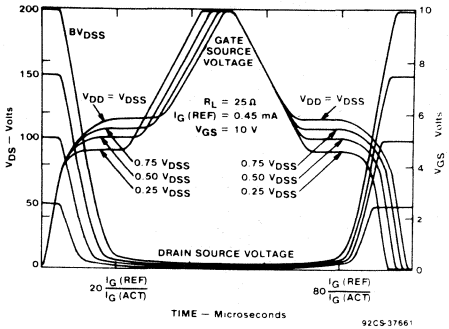


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

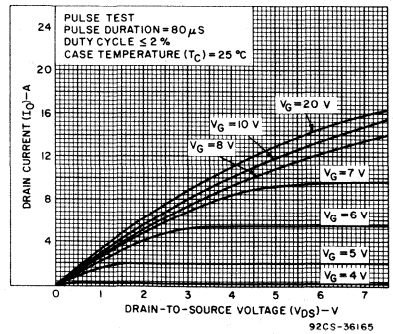


Fig. 7 — Typical saturation characteristics for all types.

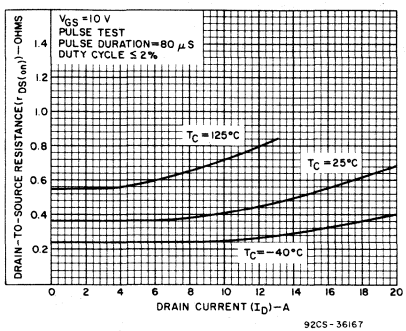


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

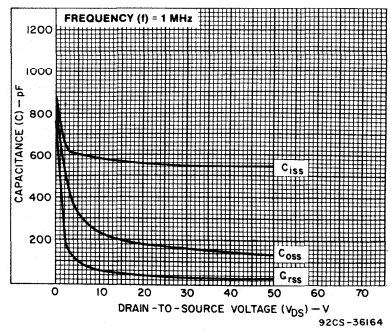


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

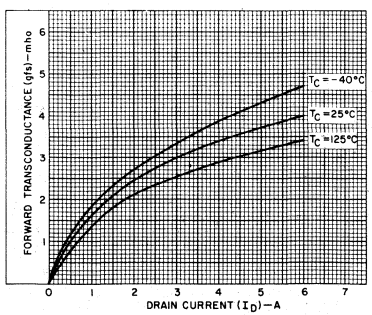


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

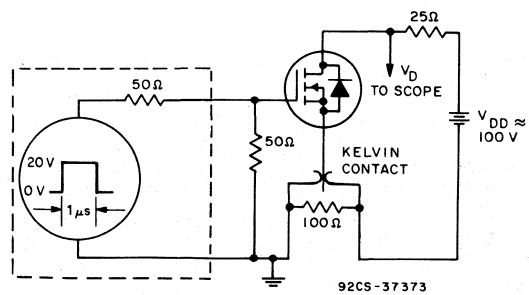


Fig. 11 — Switching Time Test Circuit.

RFM10N12, RFM10N15, RFP10N12, RFP10N15

File Number **1445**

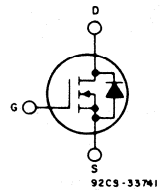
N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 120 V — 150 V

$r_{DS}(on)$: 0.3 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

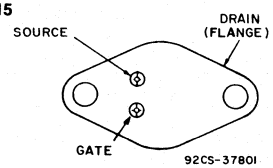
The RFM10N12 and RFM10N15 and the RFP10N12 and RFP10N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9192 and TA9212, respectively.

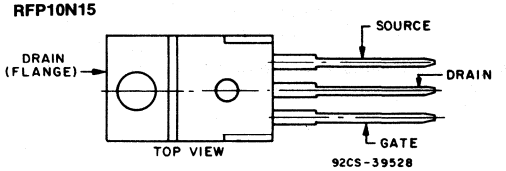
TERMINAL DESIGNATIONS

RFM10N12
RFM10N15



JEDEC TO-204AA

RFP10N12
RFP10N15



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM10N12	RFM10N15		RFP10N12	RFP10N15	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			10			A
Pulsed ..... I_{DM}			25			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM10N12, RFM10N15, RFP10N12, RFP10N15

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12 RFP10N12		RFM10N15 RFP10N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C					
		V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	1.5	—	1.5	V
		I_D = 10 A, V_{GS} = 10 V	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	230	—	230	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V	40(typ.)	60	40(typ.)	60	ns
Rise Time	t_r	I_D = 5 A	165(typ.)	250	165(typ.)	250	
Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	90(typ.)	135	90(typ.)	135	
Fall Time	t_f	V_{GS} = 10 V	90(typ.)	135	90(typ.)	135	
Thermal Resistance Junction-to-Case	RθJC	RFM10N12, RFM10N15	—	1.67	—	1.67	°C/W
		RFP10N12, RFP10N15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12 RFP10N12		RFM10N15 RFP10N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFM10N12, RFM10N15, RFP10N12, RFP10N15

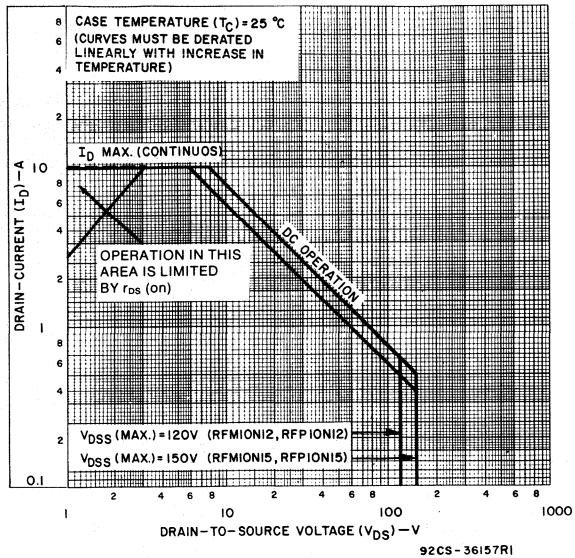


Fig. 1 — Maximum safe operating areas for all types.

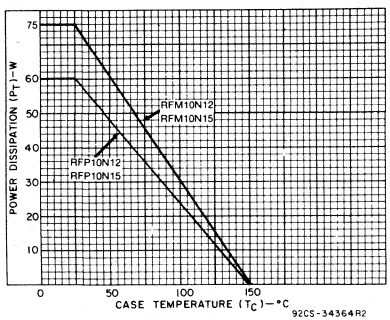


Fig. 2 — Power vs. temperature derating curve for all types.

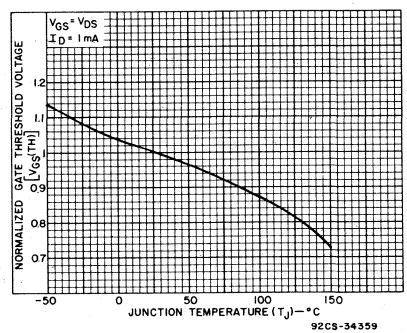


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

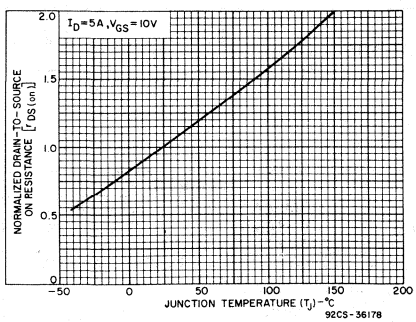


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

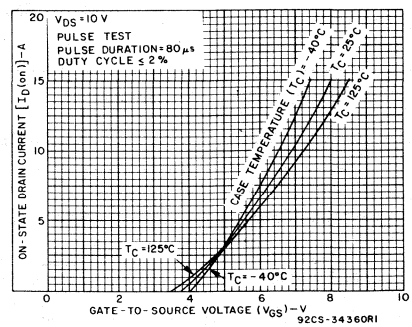


Fig. 5 — Typical transfer characteristics for all types.

RFM10N12, RFM10N15, RFP10N12, RFP10N15

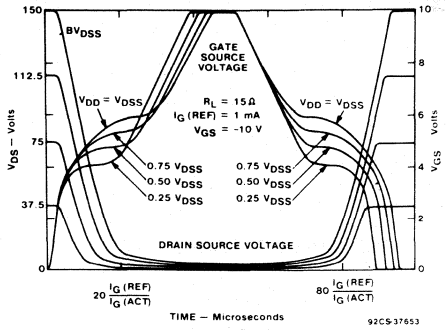


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

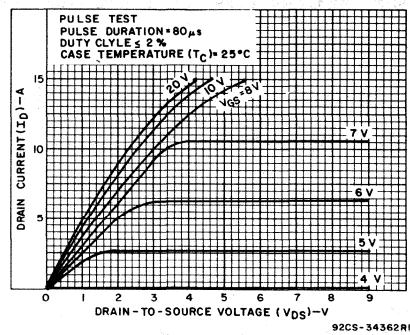


Fig. 7 — Typical saturation characteristics for all types.

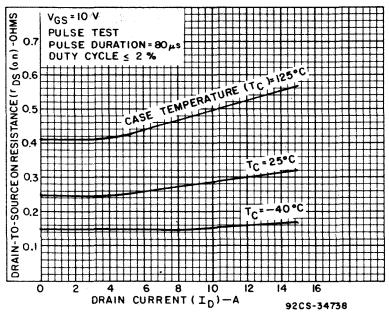


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

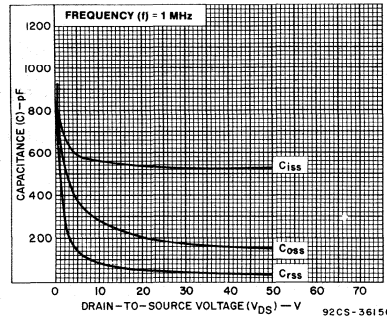


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

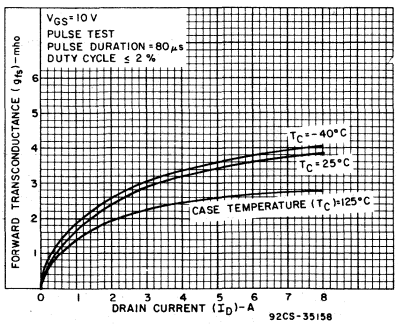


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

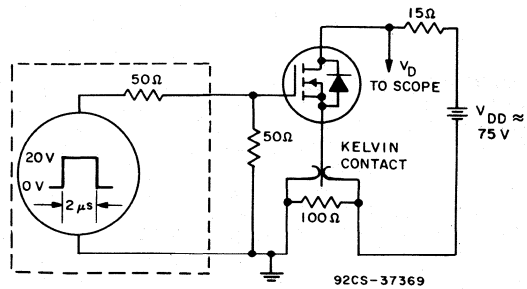


Fig. 11 — Switching Time Test Circuit

RFM10N45, RFM10N50

File Number **1788**

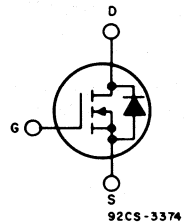
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 450 V - 500 V
$r_{DS(on)}$: 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

N-CHANNEL ENHANCEMENT MODE



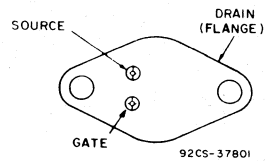
TERMINAL DIAGRAM

The RFM10N45 and RFM10N50* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package.

*The RFM10N45 and RFM10N50 types were formerly RCA developmental numbers TA9189A and TA9189B, respectively.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

		RFM10N45	RFM10N50	
DRAIN-SOURCE VOLTAGE	V_{DSS}	450	500	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	450	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	10		A
Pulsed	I_{DM}	20		A
POWER DISSIPATION @ T_C = 25°C	P_T	150		W
Derate above T_C = 25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V	—	1	—	—	μA
		V_{DS} = 400 V	—	—	—	1	
		T_C = 125°C V_{DS} = 360 V	—	50	—	—	
		V_{DS} = 400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	200	—	200	
Turn-On Delay Time	t_{d}(on)	V_{DS} = 250	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	t_{d}(off)	R_{gen}=R_{gs}=50Ω	525(typ)	900	525(typ)	900	
Fall Time	t_f	V_{GS} = 10 V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N45, RFM10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFM10N45, RFM10N50

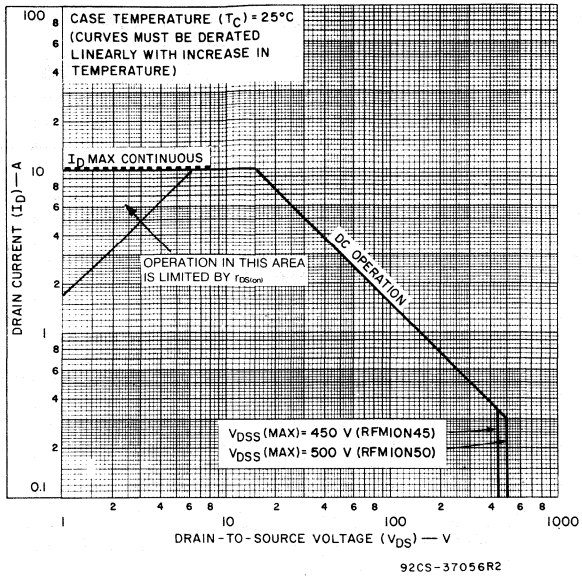


Fig. 1 - Maximum safe operating areas for all types.

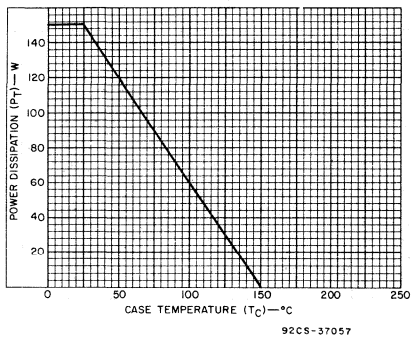


Fig. 2 - Power vs. temperature derating curve for all types.

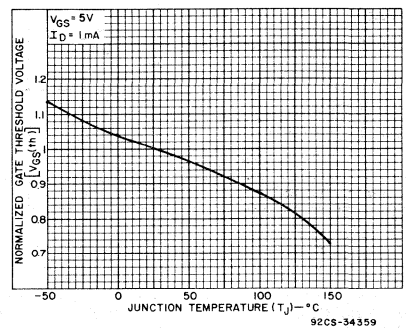


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

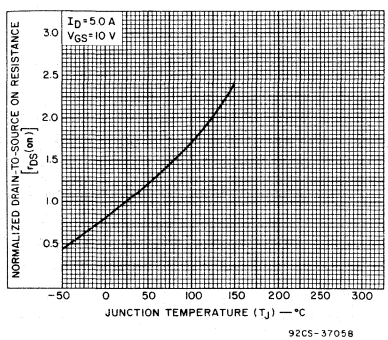


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

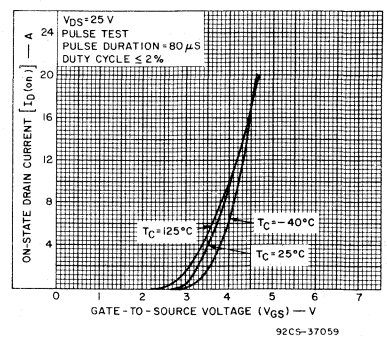


Fig. 5 - Typical transfer characteristics for all types.

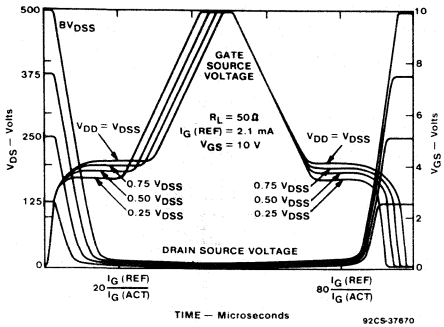


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

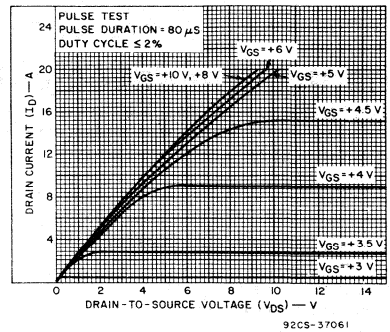


Fig. 7 - Typical saturation characteristics for all types.

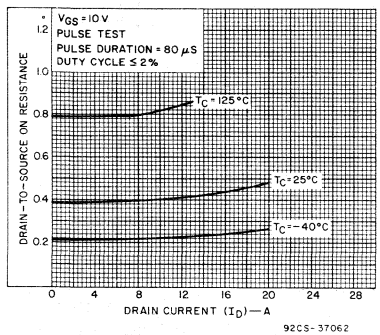


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

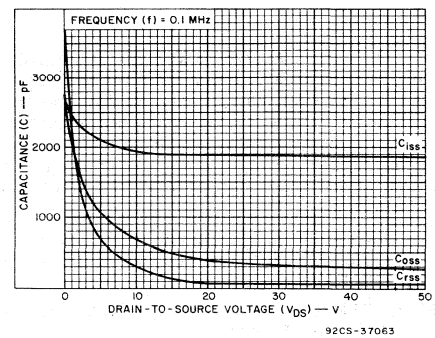


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

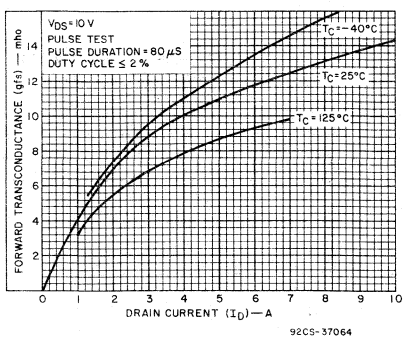


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

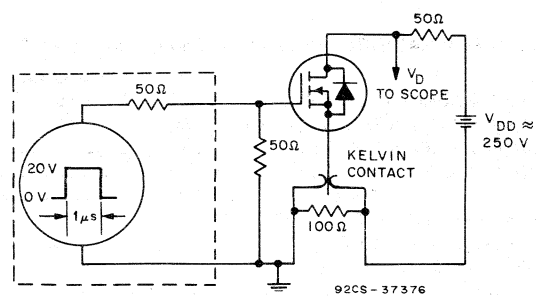


Fig. 11 - Switching Time Test Circuit.

RFM12N08, RFM12N10, RFP12N08, RFP12N10

File Number **1386**

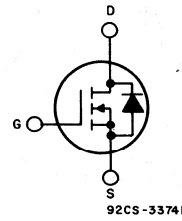
N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 80 and 100 V

$r_{DS\ (on)}$: 0.2 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

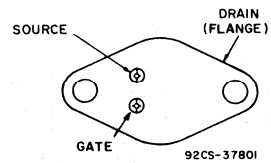
The RFM12N08 and RFM12N10 and the RFP12N08 and RFP12N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9284 and TA9285.

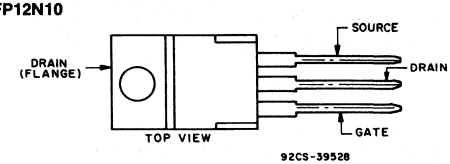
TERMINAL DESIGNATIONS

RFM12N08
RFM12N10



JEDEC TO-204AA

RFP12N08
RFP12N10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12N08	RFM12N10		RFP12N08	RFP12N10	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM12N08, RFM12N10, RFP12N08, RFP12N10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFP12N08		RFM12N10 RFP12N10		
			Min.	Max.	Min.	Max.	
Drain Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	μA
		V_{DS}=80 V	—	—	—	1	
		T_C=125° C V_{DS}=65 V	—	50	—	—	
		V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=10 V	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	150	—	150	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	45(Typ)	70	45(Typ)	70	ns
Rise Time	t_r	I_D=6 A	250(Typ)	375	250(Typ)	375	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	85(Typ)	130	85(Typ)	130	
Fall Time	t_f	V_{GS}=10 V	100(Typ)	150	100(Typ)	150	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N08, RFM12N10	—	1.67	—	1.67	°C/W
		RFP12N08, RFP12N10	—	2.083	—	2.083	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFM12N10		RFP12N08 RFP12N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM12N08, RFM12N10, RFP12N08, RFP12N10

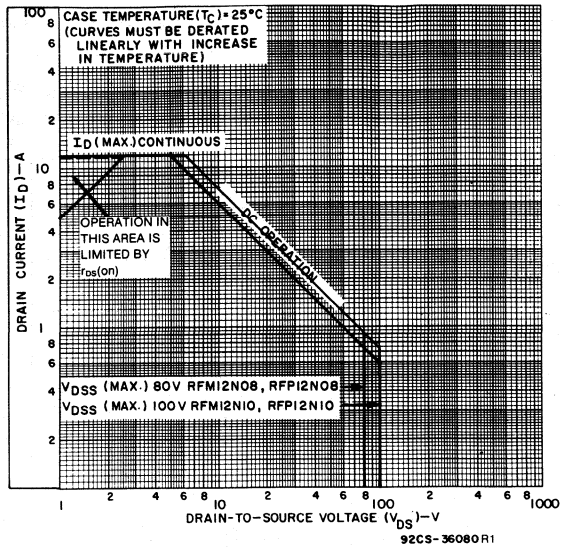


Fig. 1 - Maximum operating areas for all types.

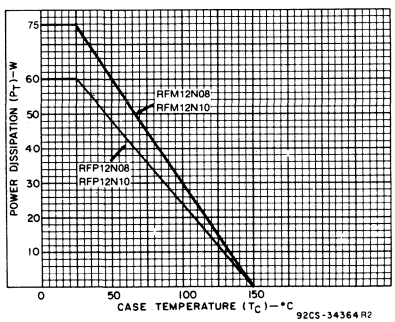


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

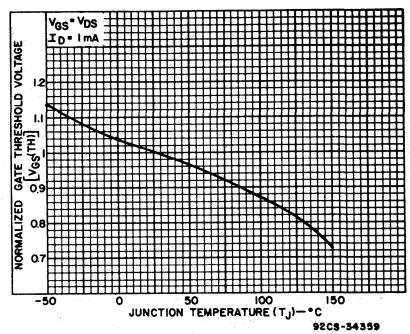


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

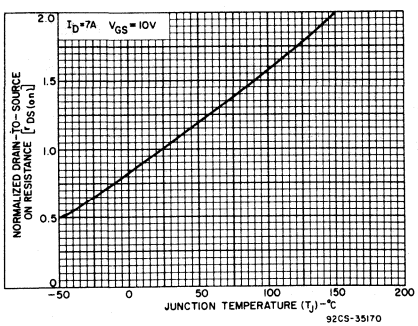


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

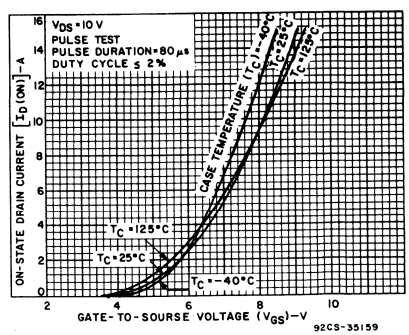


Fig. 5 - Typical transfer characteristics for all types.

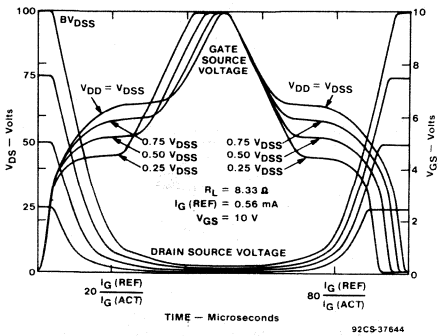


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

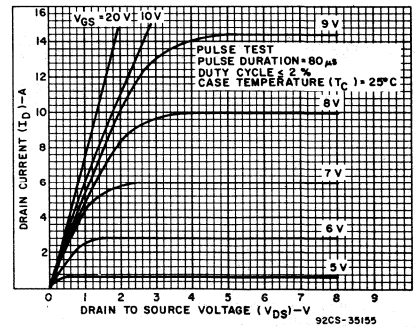


Fig. 7 - Typical saturation characteristics for all types.

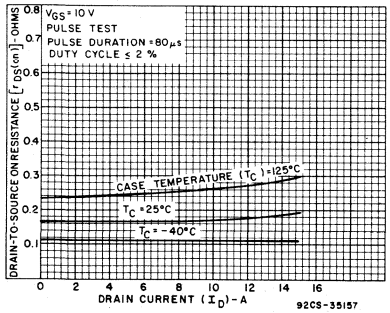


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

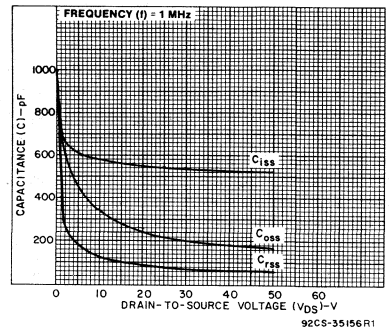


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

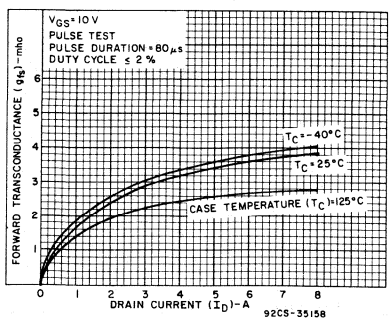


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

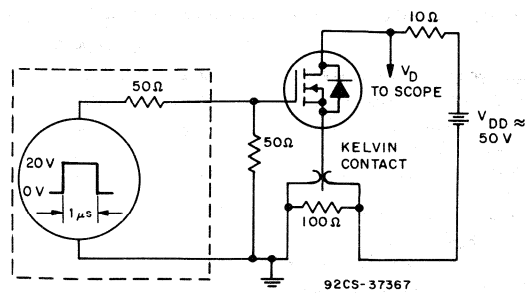


Fig. 11 — Switching Time Test Circuit

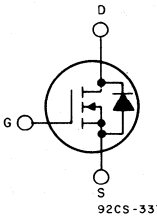
RFM12N18, RFM12N20, RFP12N18, RFP12N20

File Number **1461**

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 180 and 200 V
$r_{DS}(on)$: 0.25 Ω

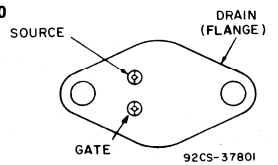
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

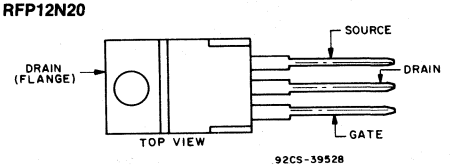
TERMINAL DESIGNATIONS

RFM12N18
RFM12N20



JEDEC TO-204AA

RFP12N18
RFP12N20



JEDEC TO-220AB

The RFM12N18 and RFM12N20 and the RFP12N18 and RFP12N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9293 and TA9294, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12N18	RFM12N20		RFP12N18	RFP12N20	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) .. V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT						
RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION						
@ T_C=25° C ..... P_T	100	100		75	75	W
Derate above T_C=25° C	0.8	0.8		0.6	0.6	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM12N18, RFM12N20, RFP12N18, RFP12N20

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125° C V_{DS}=145 V	—	50	—	—	
		V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.5	—	1.5	V
		I_D=12 A V_{GS}=10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.25	—	0.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1700	—	1700	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	600	—	600	
Reverse-Transfer Capacitance	C_{rss}	f=1 MHz	—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r	I_D=6 A	130(typ)	200	130(typ)	200	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	120(typ)	180	120(typ)	180	
Fall Time	t_f	V_{GS}=10 V	105(typ)	160	105(typ)	160	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N18, RFM12N20	—	1.25	—	1.25	°C/W
		RFP12N18, RFP12N20	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	325(typ)		325(typ)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFM12N18, RFM12N20, RFP12N18, RFP12N20

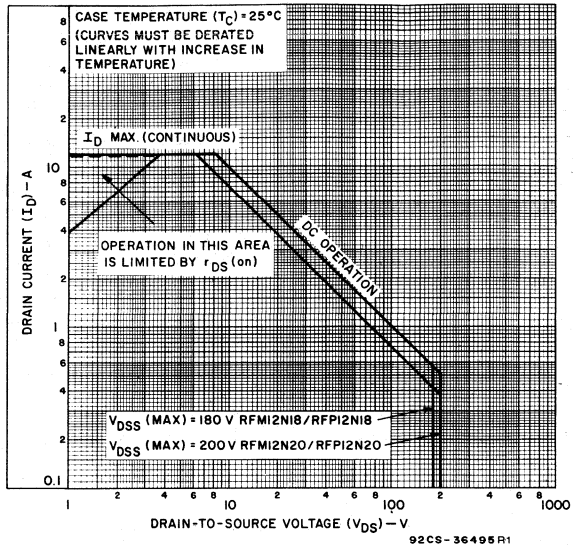


Fig. 1 - Maximum safe operating areas for all types.

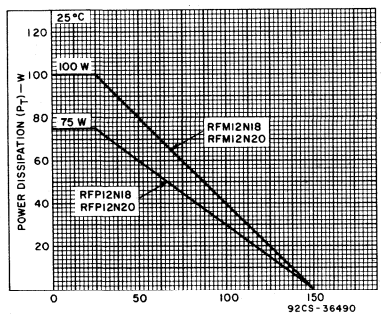


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

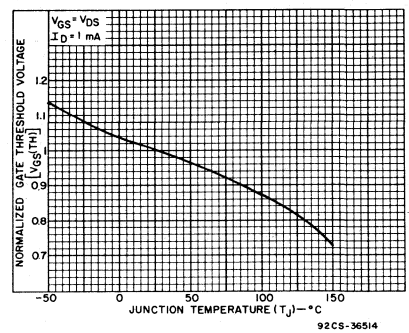


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

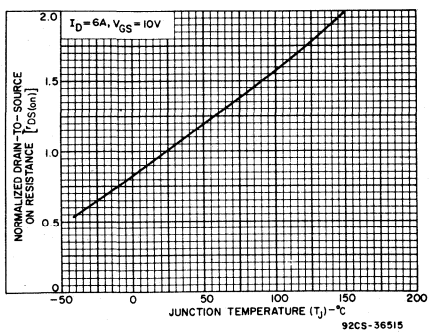


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

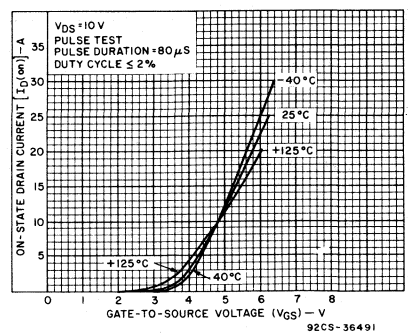


Fig. 5 - Typical transfer characteristics for all types.

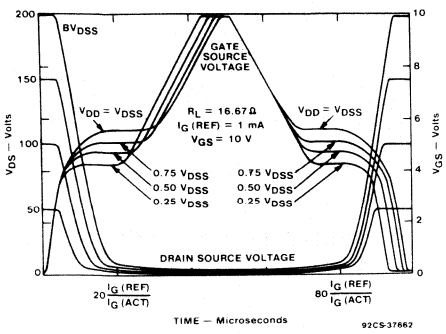


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

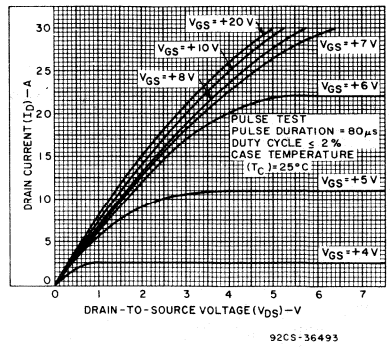


Fig. 7 - Typical saturation characteristics for all types.

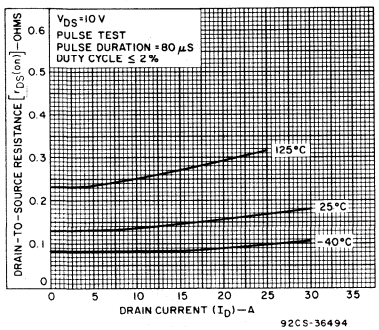


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

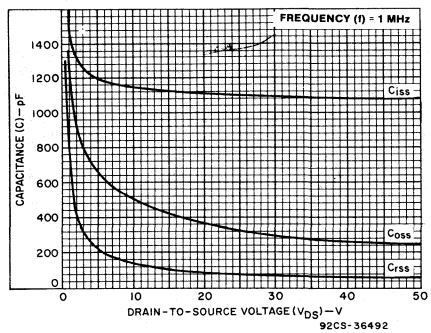


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

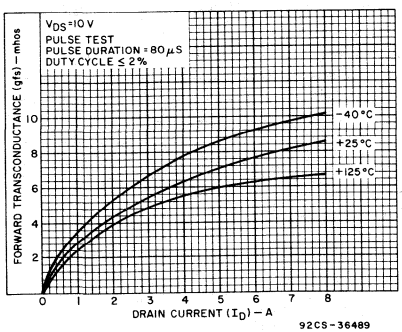


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

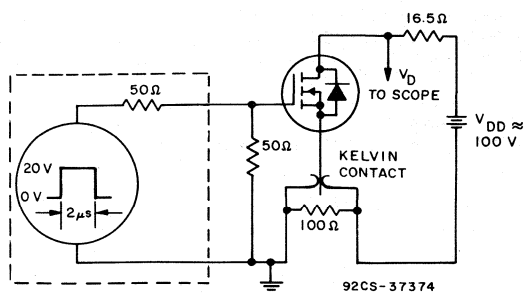


Fig. 11 — Switching Time Test Circuit

RFM12N35, RFM12N40

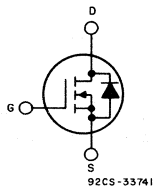
File Number **1787**

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 350 V - 400 V
$r_{DS}(on)$ = 0.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



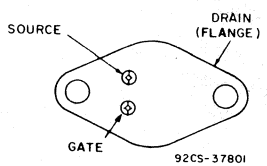
TERMINAL DIAGRAM

The RFM12N35 and RFM12N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package.

*The RFM12N35 and RFM12N40 types were formerly developmental numbers TA9399A and TA9399B, respectively.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		RFM12N35	RFM12N40	
DRAIN-SOURCE VOLTAGE	V_{DSS}	350	400	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	350	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	12		A
Pulsed	I_{DM}	24		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFM12N35, RFM12N40

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V V_{DS} = 320 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 280 V V_{DS} = 320 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	3	—	3	V
		I_D = 12 A V_{GS} = 10 V	—	10	—	10	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 200 I_D = 6 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	30(typ)	50	30(typ)	50	ns
Rise Time	t_r		105(typ)	150	105(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		480(typ)	750	480(typ)	750	ns
Fall Time	t_f		140(typ)	200	140(typ)	200	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N35, RFM12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4 A, dI_F/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFM12N35, RFM12N40

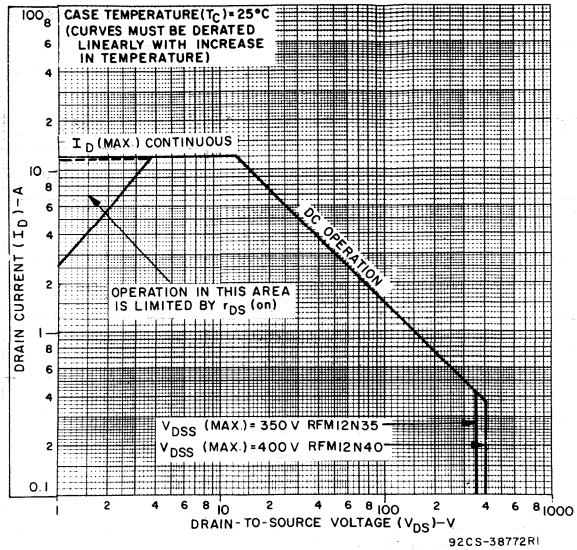


Fig. 1 - Maximum safe operating areas for all types.

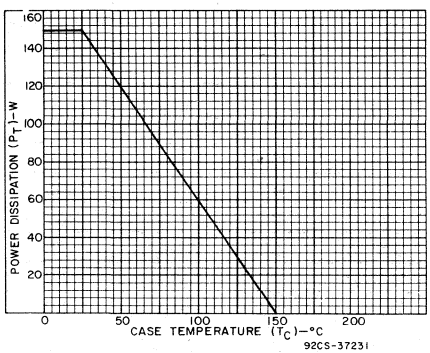


Fig. 2 - Power vs. temperature derating curve for all types.

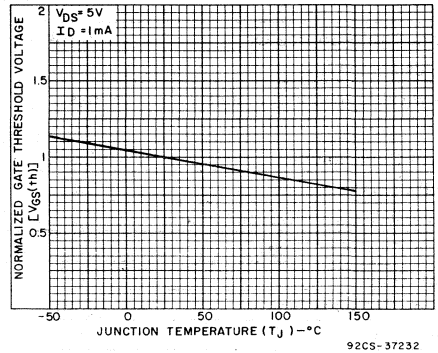


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

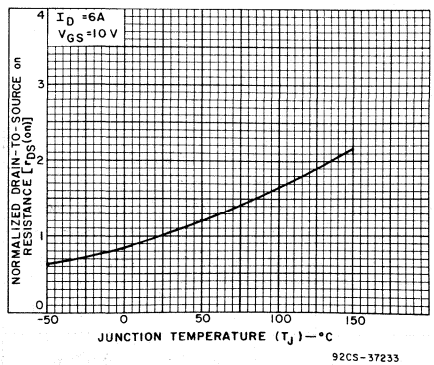


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

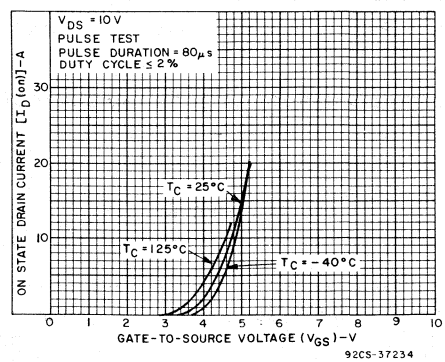


Fig. 5 - Typical transfer characteristics for all types.

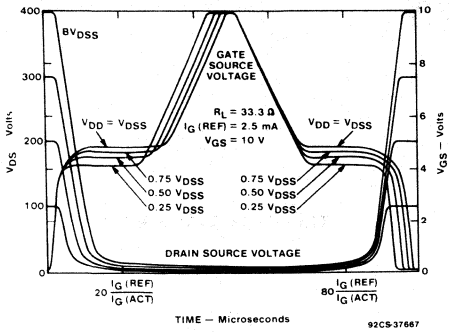


Fig. 6 - Normalized switching waveforms for constant gate-current drive. (Refer to RCA application notes AN-7254 and AN-7260.)

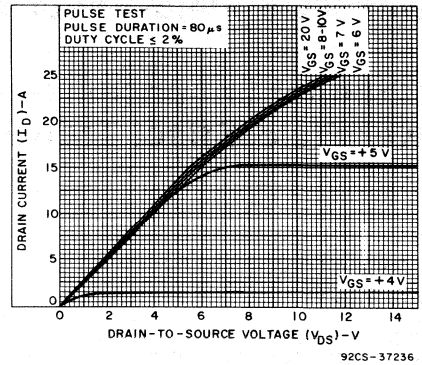


Fig. 7 - Typical saturation characteristics for all types.

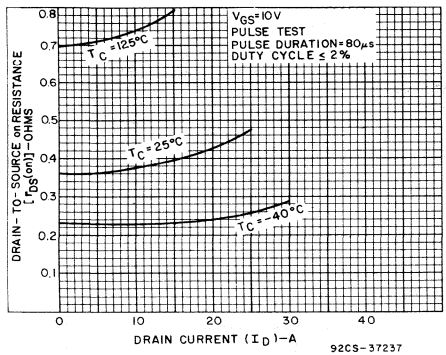


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

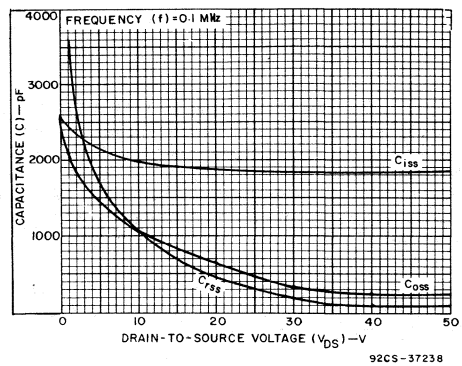


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

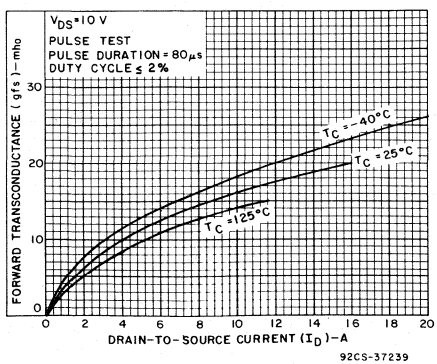


Fig. 10 - Typical forward transconductance as a function of drain for all types.

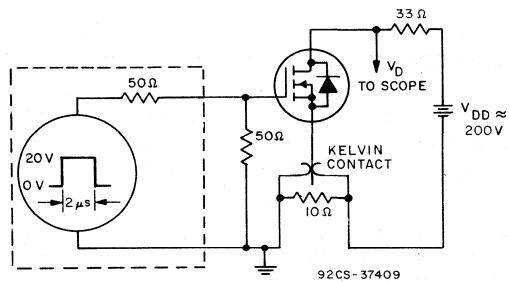


Fig. 11 - Switching Test Time Circuit.

RFM15N05, RFM15N06, RFP15N05, RFP15N06

File Number **1478**

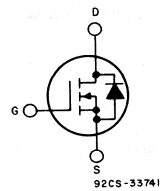
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

15 A, 50 and 60 V
$r_{DS}(on)$: 0.14 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

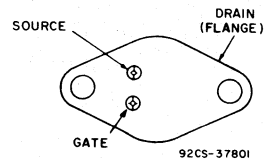
The RFM15N05 and RFM15N06 and the RFP15N05 and RFP15N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9382 and TA9383, respectively.

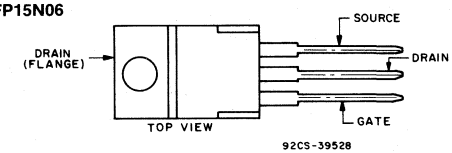
TERMINAL DESIGNATIONS

RFM15N05
RFM15N06



JEDEC TO-204AA

RFP15N05
RFP15N06



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM15N05	RFM15N06		RFP15N05	RFP15N06	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60		50	60	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	50	60		50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			15			A
Pulsed ..... I_{DM}			40			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM15N05, RFM15N06, RFP15N05, RFP15N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	μA
		V_{DS}=50 V	—	—	—	1	
		T_C=125°C V_{DS}=40 V	—	50	—	—	
		V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=7.5 A V_{GS}=10 V	—	1.05	—	1.05	V
		I_D=15 A V_{GS}=10 V	—	2.5	—	2.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=7.5 A V_{GS}=10 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=7.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	180	—	180	
Turn-On Delay Time	$t_d(on)$	V_{DD}=30 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r	I_D=7.5 A	100(typ)	175	100(typ)	175	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	72(typ)	175	72(typ)	175	
Fall Time	t_f	V_{GS}=10 V	66(typ)	140	66(typ)	140	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM15N05, RFM15N06	—	1.67	—	1.67	°C/W
		RFP15N05, RFP15N06	—	2.083	—	2.083	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	100 (typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM15N05, RFM15N06, RFP15N05, RFP15N06

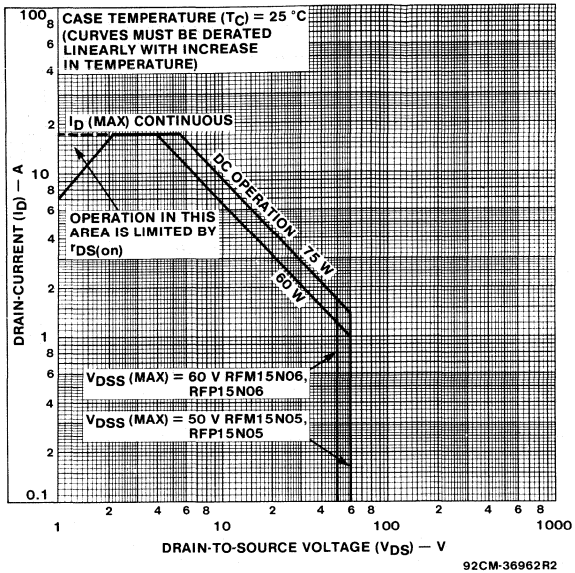


Fig. 1 - Maximum safe operating areas for all types.

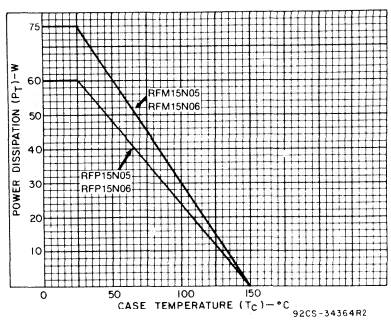


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

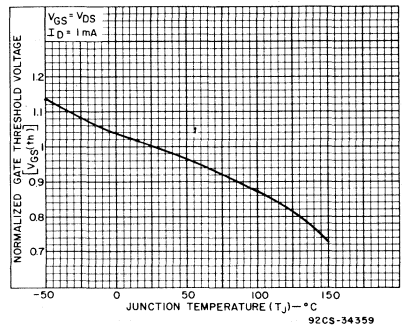


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

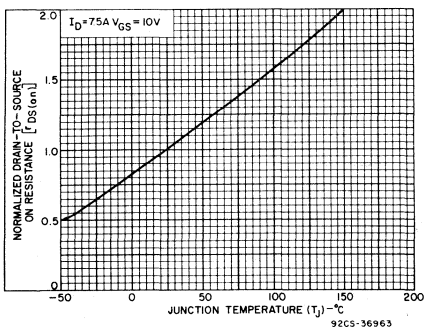


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

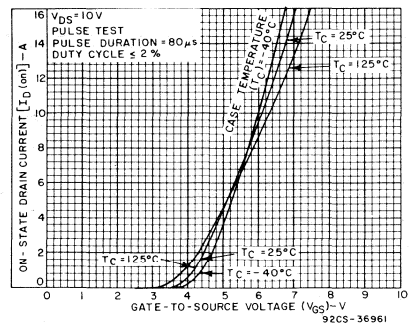


Fig. 5 - Typical transfer characteristics for all types.

RFM15N05, RFM15N06, RFP15N05, RFP15N06

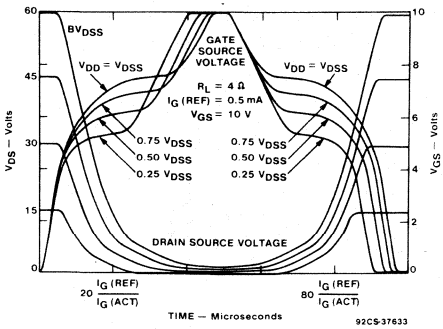


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

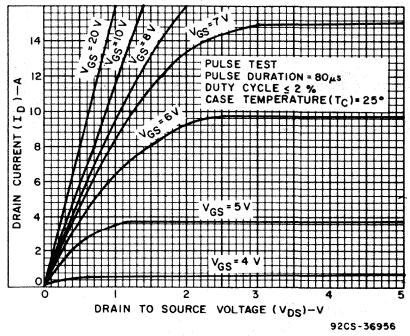


Fig. 7 - Typical saturation characteristics for all types.

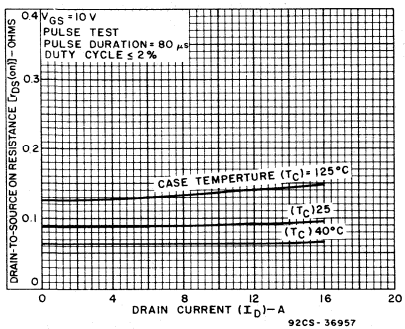


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

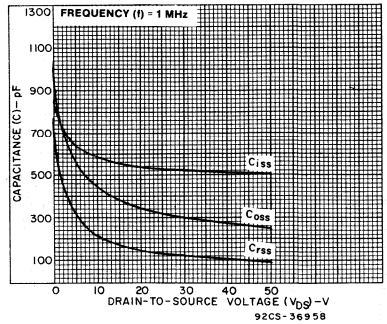


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

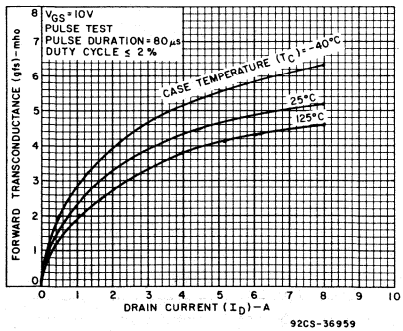


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

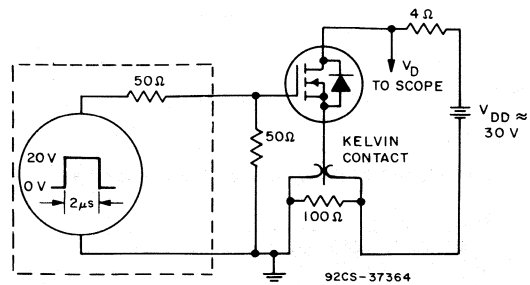


Fig. 11 — Switching Time Test Circuit

RFM15N12, RFM15N15, RFP15N12, RFP15N15

File Number **1443**

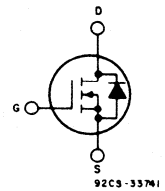
N-Channel Enhancement-Mode Power Field-Effect Transistors

15 A, 120 V — 150 V

$r_{DS}(on)$: 0.15 Ω

Features:

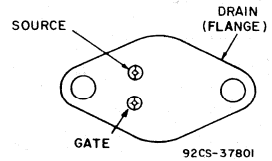
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

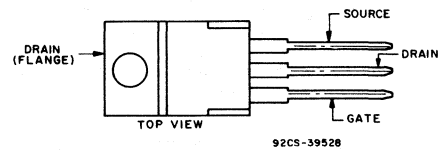
TERMINAL DESIGNATIONS

RFM15N12
RFM15N15



JEDEC TO-204AA

RFP15N12
RFP15N15



JEDEC TO-220AB

The RFM15N12 and RFM15N15 and the RFP15N12 and RFP15N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9195 and TA9230, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFM15N12	RFM15N15		RFP15N12	RFP15N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20					V
DRAIN CURRENT RMS Continuous	I_D	15					A
Pulsed	I_{DM}	40					A
POWER DISSIPATION @ T_C=25°C	P_T	100	100		75	75	W
Derate above T_C=25°C		0.80	0.80		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	−55 to +150					°C

RFM15N12, RFM15N15, RFP15N12, RFP15N15

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N12 RFP15N12		RFM15N15 RFP15N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125°C					
		V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.5 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 15 A V_{GS} = 10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.5 A V_{GS} = 10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 7.5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	750	—	750	
Reverse Transfer Capacitance	C_{rss}		—	350	—	350	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V I_D = 7.5 A R_{gen} = R_{gs} = 50 Ω V_{GS} = 10 V	50(typ.)	75	50(typ.)	75	ns
Rise Time	t_r		150(typ.)	225	150(typ.)	225	
Turn-Off Delay Time	$t_d(off)$		185(typ.)	280	185(typ.)	280	
Fall Time	t_f		125(typ.)	190	125(typ.)	190	
Thermal Resistance Junction-to-Case	RθJC	RFM15N12, RFM15N15	—	1.25	—	1.25	°C/W
		RFP15N12, RFP15N15	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N12 RFP15N12		RFM15N15 RFP15N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM15N12, RFM15N15, RFP15N12, RFP15N15

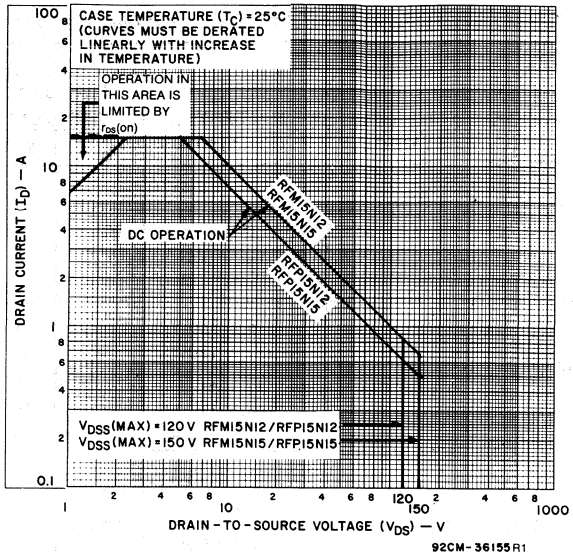


Fig. 1 — Maximum operating areas for all types.

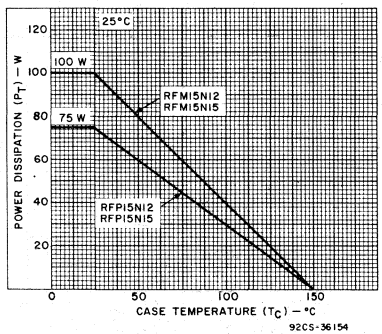


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

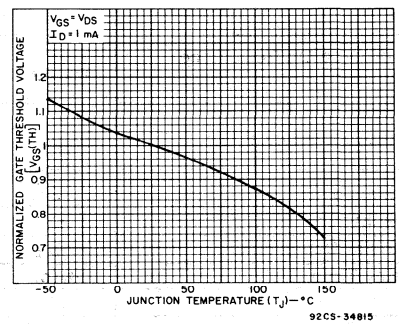


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

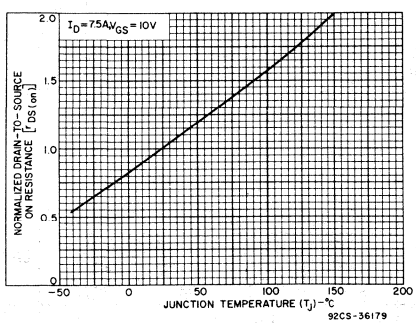


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

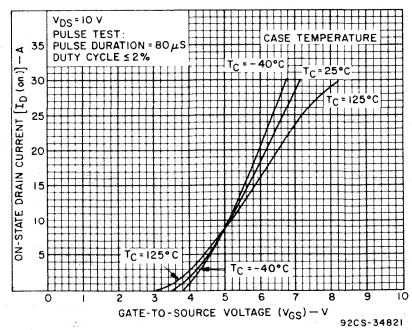


Fig. 5 — Typical transfer characteristics for all types.

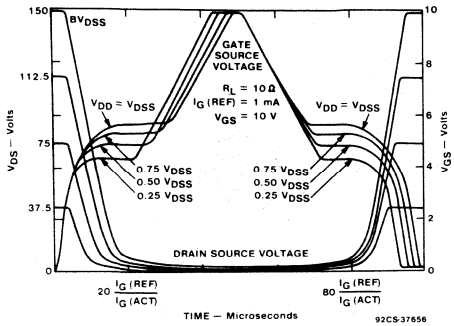


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

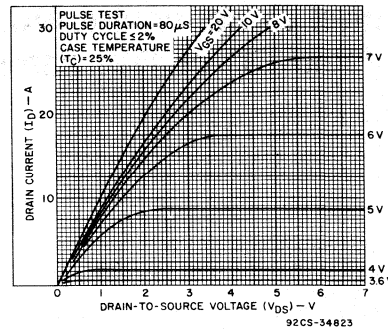


Fig. 7 — Typical saturation characteristics for all types.

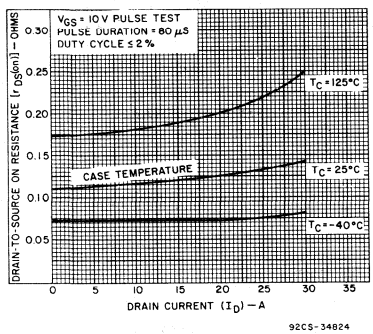


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

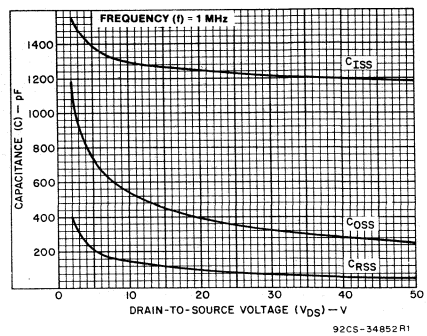


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

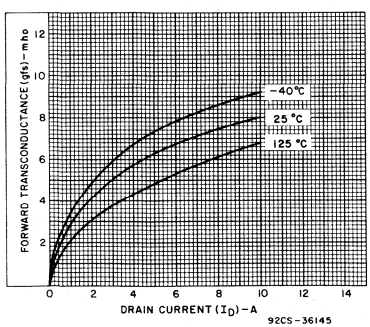


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

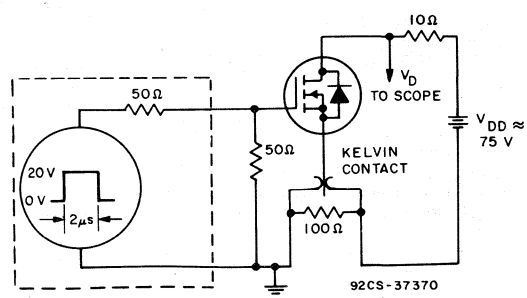


Fig. 11 — Switching Time Test Circuit

RFM18N08, RFM18N10, RFP18N08, RFP18N10

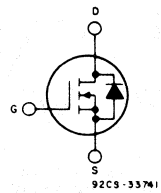
File Number **1446**

N-Channel Enhancment-Mode Power Field-Effect Transistors

18 A, 80 V — 100 V
$r_{DS}(on)$: 0.1Ω

Features:

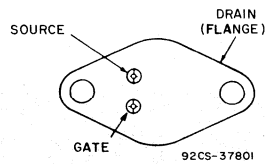
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

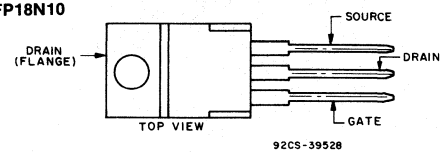
TERMINAL DESIGNATIONS

RFM18N08
RFM18N10



JEDEC TO-204AA

RFP18N08
RFP18N10



JEDEC TO-220AB

The RFM18N08 and RFM18N10 and the RFP18N08 and RFP18N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9286 and TA9287, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c=25°C):*

		RFM18N08	RFM18N10	RFP18N08	RFP18N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100	80	100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	80	100	80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	18				A
Pulsed	I_{DM}	45				A
POWER DISSIPATION						
@ T_C=25°C	P_T	100	100	75	75	W
Derate above T_C=25°C		0.8	0.8	0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	−55 to +150				°C

RFM18N08, RFM18N10, RFP18N08, RFP18N10

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFP18N08 MIN.	MAX.	LIMITS RFM18N10 RFP18N10 MIN.	MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V	—	1	—	—	μA
		V_{DS} = 80 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 65 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 9 A, V_{GS} = 10 V	—	1.08	—	1.08	V
		I_D = 18 A, V_{GS} = 10 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 9 A, V_{GS} = 10 V	—	0.10	—	0.10	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 9 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	1700	—	1700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	750	—	750	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	60(typ.)	90	60(typ.)	90	ns
Rise Time	t_r	I_D = 9 A	300(typ.)	450	300(typ.)	450	
Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	150(typ.)	225	150(typ.)	225	
Fall Time	t_f	V_{GS} = 10 V	150(typ.)	225	150(typ.)	225	
Thermal Resistance Junction-to-Case	RθJC	RFM18N08, RFM18N10	—	1.25	—	1.25	°C/W
		RFP18N08, RFP18N10	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFM18N10 MIN.	MAX.	LIMITS RFP18N08 RFP18N10 MIN.	MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=9 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM18N08, RFM18N10, RFP18N08, RFP18N10

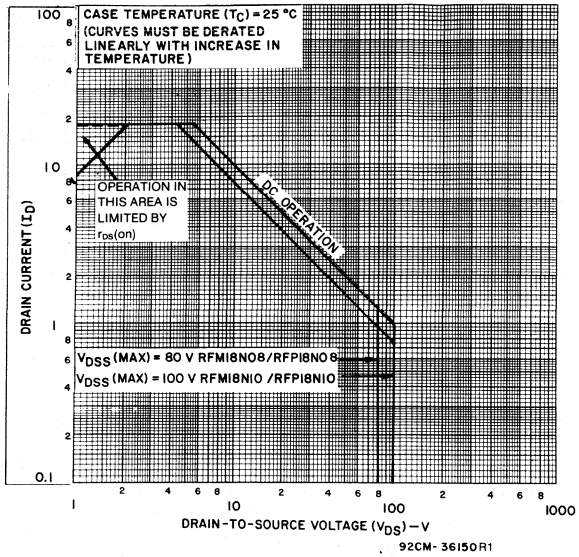


Fig. 1 — Maximum operating areas for all types.

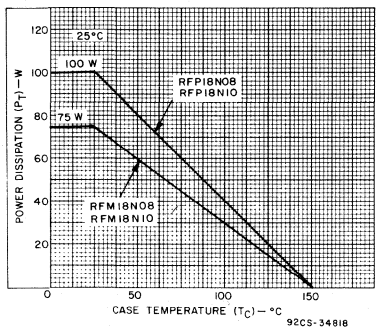


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

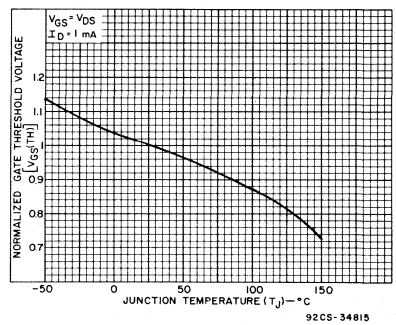


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

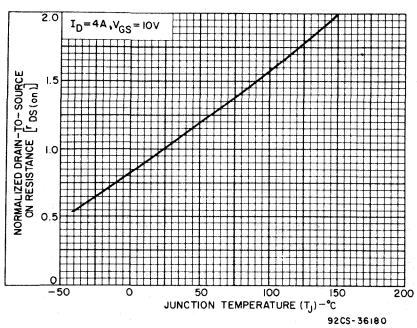


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

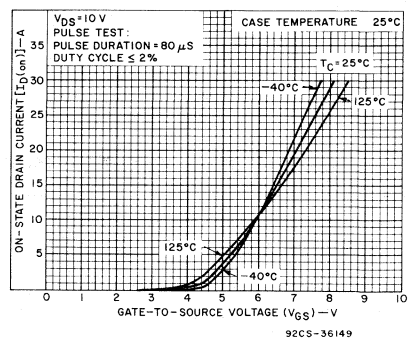


Fig. 5 — Typical transfer characteristics for all types.

RFM18N08, RFM18N10, RFP18N08, RFP18N10

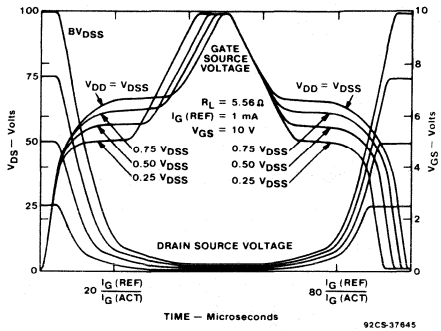


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

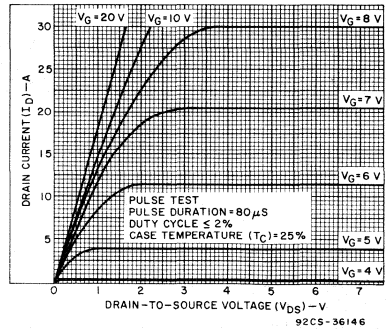


Fig. 7 — Typical saturation characteristics for all types.

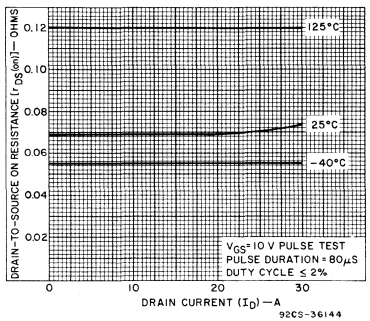


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

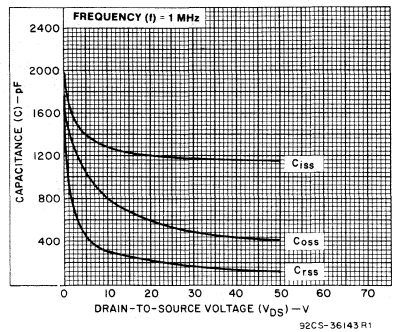


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

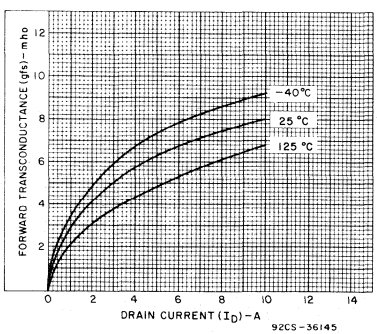


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

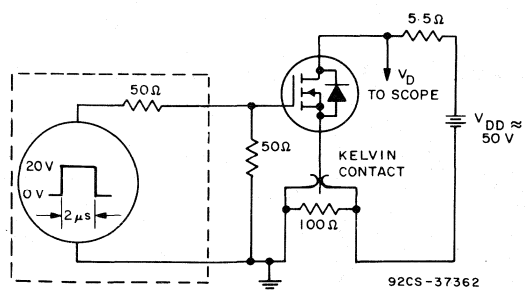


Fig. 11 — Switching Time Test Circuit

RFM25N06
RFP25N06

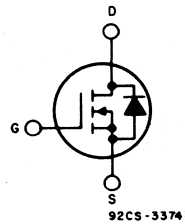
File Number **1492**

N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 50 V — 60 V
$r_{DS}(on)$ = 0.07 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



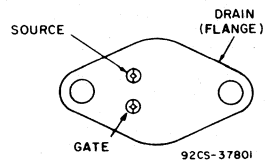
TERMINAL DIAGRAM

The RFM25N06 and the RFP25N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from ingegrated circuits.

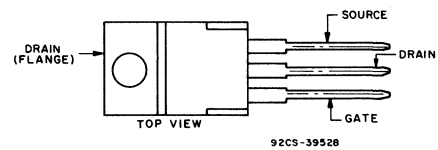
The RFM-type is supplied in the JEDEC TO-204AA steel package and the RFP-type in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9386 and TA9387, respectively.

TERMINAL DESIGNATION



JEDEC TO-204AA



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		RFM25N06		RFP25N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	60		60	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ)	V_{DGR}	60		60	V
GATE-SOURCE VOLTAGE	V_{GS}	———	±20	———	V
DRAIN CURRENT, RMS Continuous	I_D	———	25	———	A
Pulsed	I_{DM}	———	60	———	A
POWER DISSIPATION @ T_C = 25°C	P_T	100		75	W
Derate above T_C = 25 °C		0.8		0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	———	-55 to +150	———	°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM25N06 RFP25N06 MIN.	LIMITS RFM25N06 RFP25N06 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 1$ mA	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40$ V	—	—	μA
		$V_{DS} = 50$ V	—	1	
		$T_c = 125$ °C, $V_{DS} = 40$ V	—	—	
		$T_c = 125$ °C, $V_{DS} = 50$ V	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V, $V_{DS} = 0$	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 10$ V	—	0.875	V
		$I_D = 25$ A, $V_{GS} = 10$ V	—	2.5	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 10$ V	—	0.07	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 10$ V, $I_D = 12.5$ A	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 0.1 MHz	—	1700	pF
Output Capacitance	C_{oss}		—	900	
Reverse Transfer Capacitance	C_{rss}		—	400	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30$ V, $I_D = 12.5$ A, $R_{gen} = R_{gs} = 50\ \Omega$, $V_{GS} = 10$ V	18 (typ.)	60	ns
Rise Time	t_r		120 (typ.)	225	
Turn-Off Delay Time	$t_{d(off)}$		123 (typ.)	225	
Fall Time	t_f		123 (typ.)	200	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM25N06	—	1.25	°C/W
		RFP25N06	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM25N06 RFP25N06 MIN.	LIMITS RFM25N06 RFP25N06 MAX.	UNITS
Diode Forward Voltage	V_{SD}	$I_{SD} = 12.5$ A	—	1.4	V
Reverse Recovery Time	t_{rr}	$I_F = 4$ A, $dI_F/dt = 100$ A/μs	150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM25N06, RFP25N06

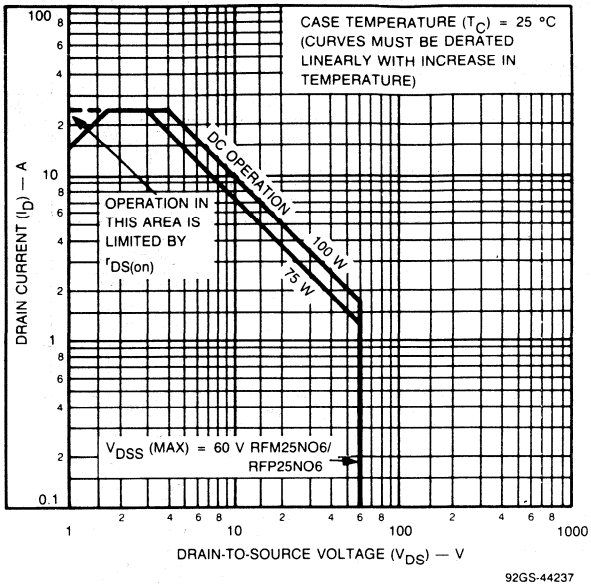


Fig. 1 — Maximum operating areas for all types.

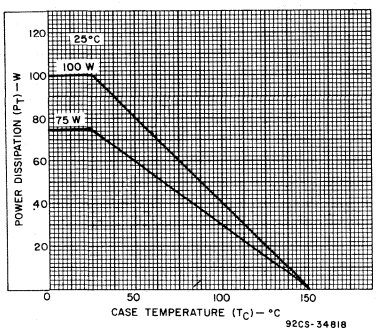


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

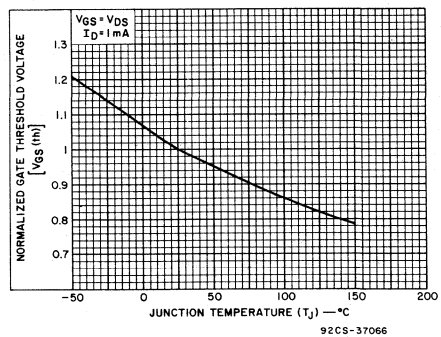


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

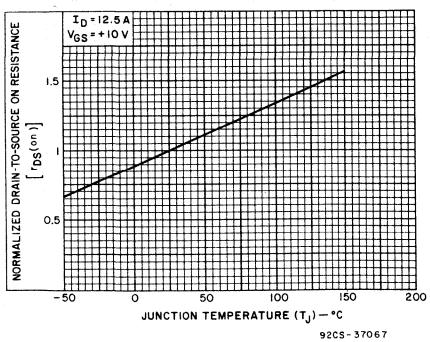


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

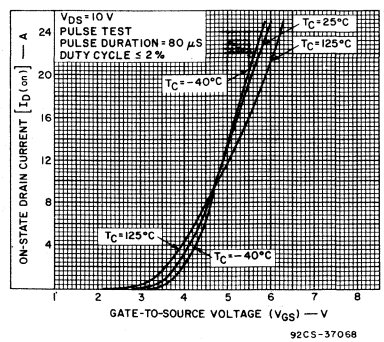


Fig. 5 — Typical transfer characteristics for all types.

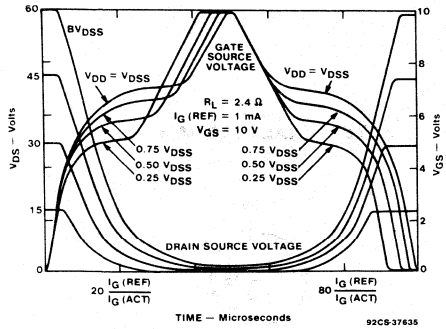


Fig. 6 - Normalized switching waveforms for constant gate-current drive. (Refer to RCA application notes AN7254 and AN7260.)

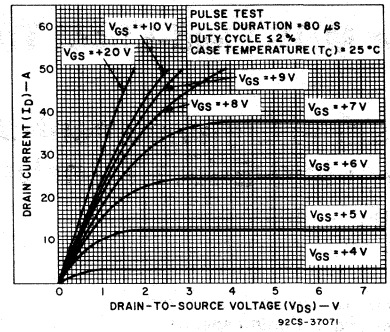


Fig. 7 — Typical saturation characteristics for all types.

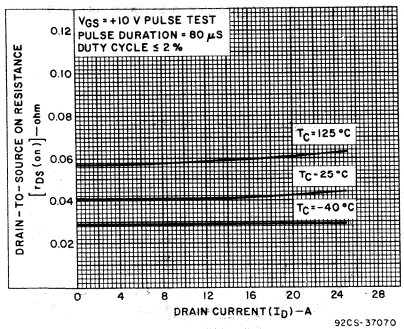


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

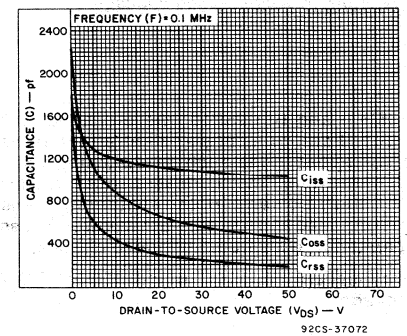


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

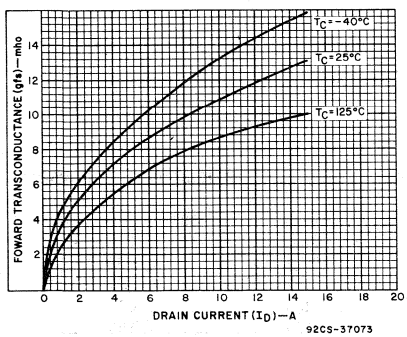


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

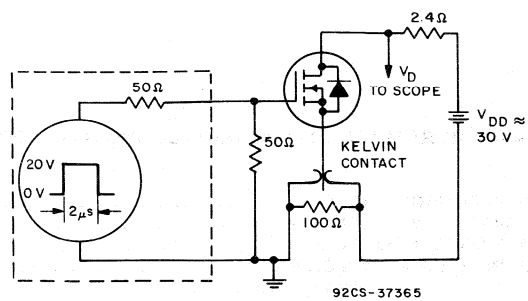


Fig. 11 — Switching Time Test Circuit

RFH25P08, RFH25P10

File Number **1632**

Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power Field-Effect Transistors

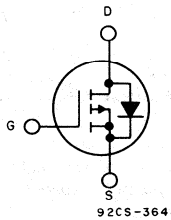
25 A, -80 V - -100 V

$r_{DS(on)}$ = 0.15 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



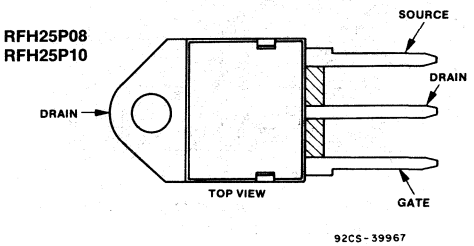
P-CHANNEL ENHANCEMENT MODE

The RFH25P08 and RFH25P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH25P08 and RFH25P10 types were formerly RCA developmental numbers TA9577A and TA9577B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH25P08	RFH25P10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	25		A
Pulsed	I_{DM}	60		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH25P08		RFH25P10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	—	—	1	μA
		V_{DS} = -65 V	—	1	—	—	
		T_C = 125° C V_{DS} = -80 V	—	—	—	50	
		V_{DS} = -65 V	—	50	—	—	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = -10 V	—	-1.88	—	-1.88	V
		I_D = 25 A V_{GS} = -10 V	—	-4.5	—	-4.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = -10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V I_D = 12.5 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	600	—	600	
Turn-On Delay Time	$t_d(on)$	V_{DD} = -50 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r	I_D = 12.5 A	165(typ)	250	165(typ)	250	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	270(typ)	400	270(typ)	400	
Fall Time	t_f	V_{GS} = -10 V	165(typ)	250	165(typ)	250	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH25P08, RFH25P10 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH25P08		RFH25P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 12.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	300 (typ.)		300 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH25P08, RFH25P10

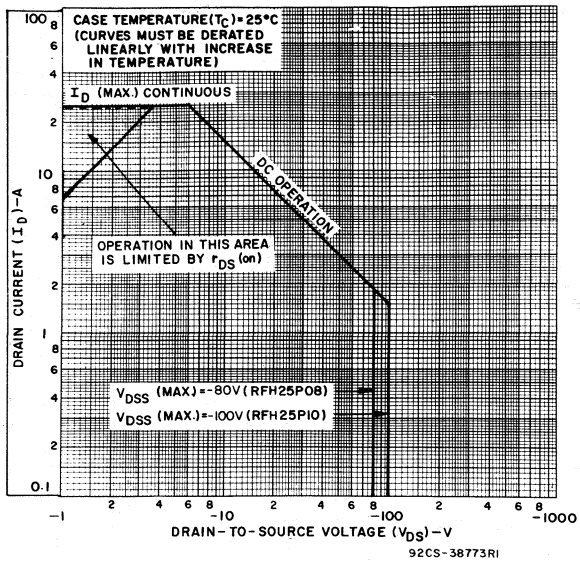


Fig. 1 - Maximum safe operating areas for all types.

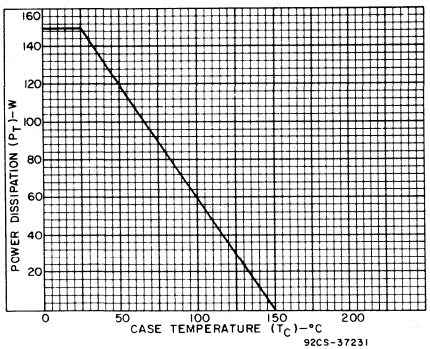


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

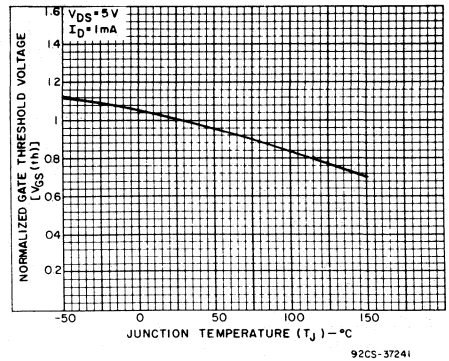


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

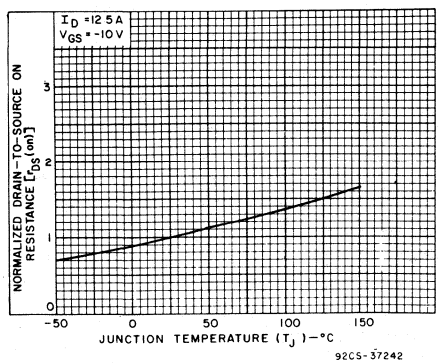


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

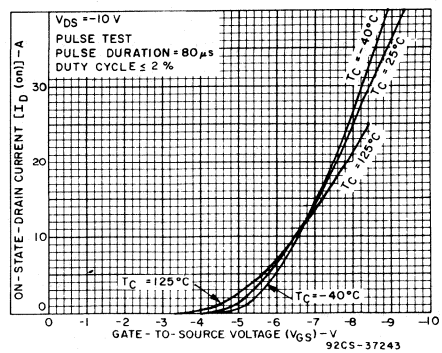


Fig. 5 - Typical transfer characteristics for all types.

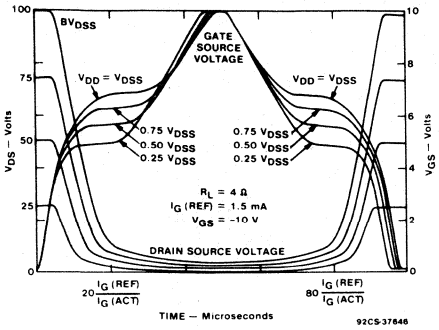


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

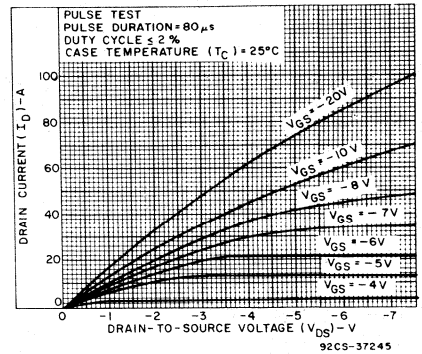


Fig. 7 - Typical saturation characteristics for all types.

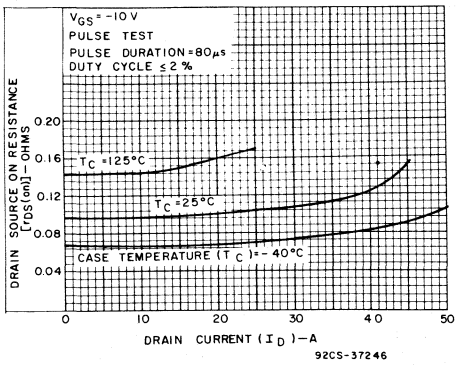


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

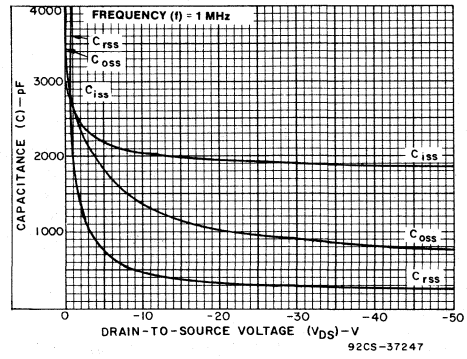


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

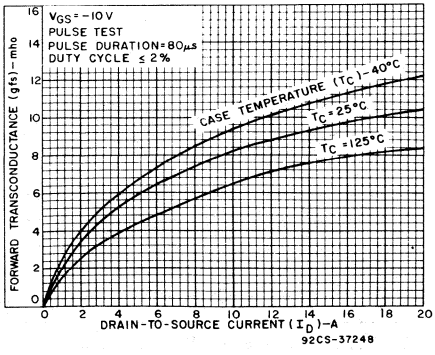


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

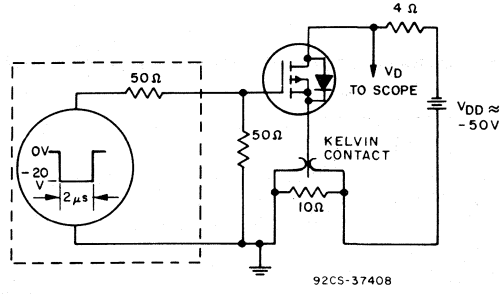


Fig. 11 - Switching Time Test Circuit.

RFK25P08, RFK25P10

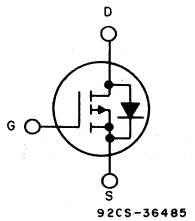
File Number **1516**

P-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, -100 V — -80 V
$r_{DS}(on)$: 0.15Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



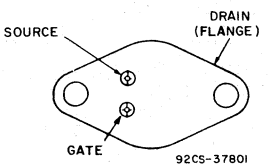
P-CHANNEL ENHANCEMENT MODE

The RFK25P10 and RFK25P08* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK25P10 and RFK25P08 types were formerly RCA developmental numbers TA9412A and TA9412B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFK25P10	RFK25P08	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-100	-80	V
DRAIN-GATE VOLTAGE, R_{GS}=1 MΩ)	V_{DGR}	-100	-80	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	25		A
Pulsed	I_{DM}	60		A
POWER DISSIPATION	P_T			
@ T_C = 25°C		150		W
Derate above T_C=25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFK25P08, RFK25P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25P10		RFK25P08		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-100	—	-80	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80 V V_{DS}=-65 V	— —	1 —	— —	— 1	μA
		T_C=125°C V_{DS}=-80 V V_{DS}=-65 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ± 20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=-10 V	—	-1.88	—	-1.88	V
		I_D=25 A V_{GS}=-10 V	—	-6	—	-6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=-10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=12.5 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V V_{GS}=0 V f = 1MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1500	—	1500	pF
Reverse Transfer Capacitance	C_{rss}		—	600	—	600	pF
Turn-On Delay Time	t_d (on)	V_{DD}=-50 V I_D=12.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=-10 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r		165(typ)	250	165(typ)	250	ns
Turn-Off Delay Time	t_d (off)		270(typ)	400	270(typ)	400	ns
Fall Time	t_f		165(typ)	250	165(typ)	250	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK25P10, RFK25P08	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25P10		RFK25P08		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage*	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300 typ.		300 typ.		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFK25P08, RFK25P10

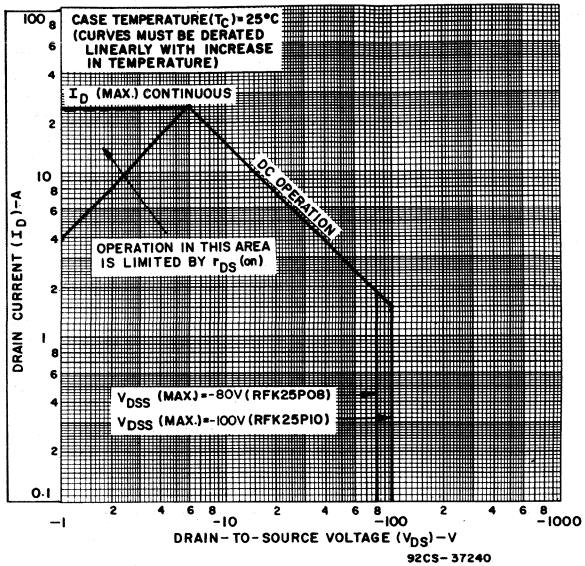


Fig. 1 - Maximum safe operating areas for all types.

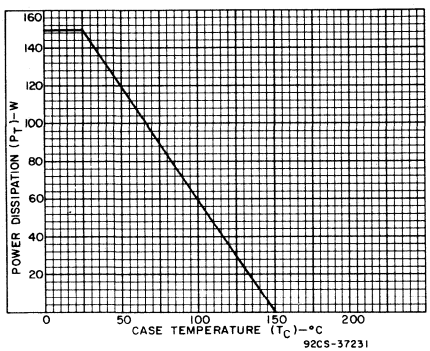


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

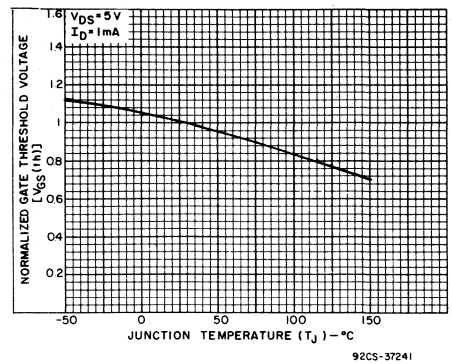


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

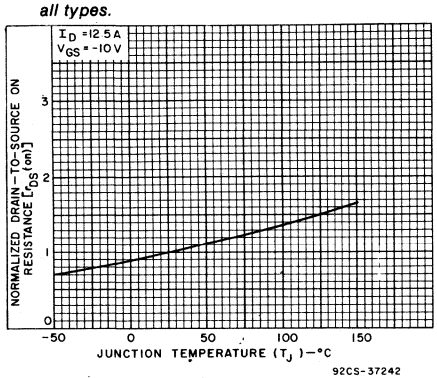


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

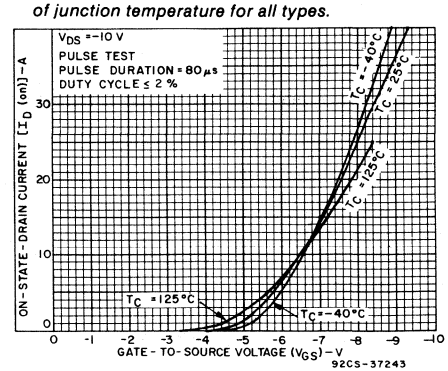


Fig. 5 - Typical transfer characteristics for all types.

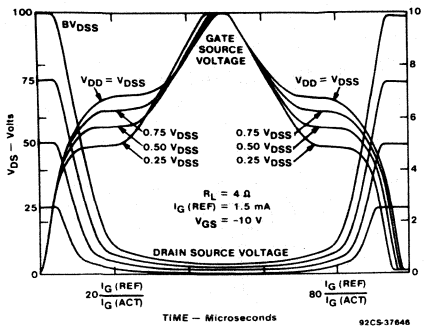


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

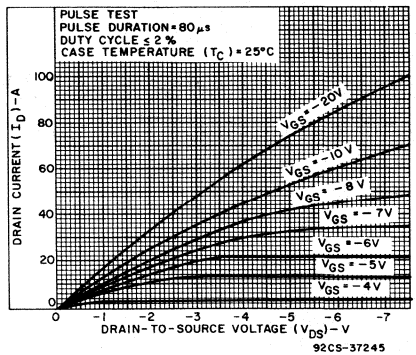


Fig. 7 - Typical saturation characteristics for all types.

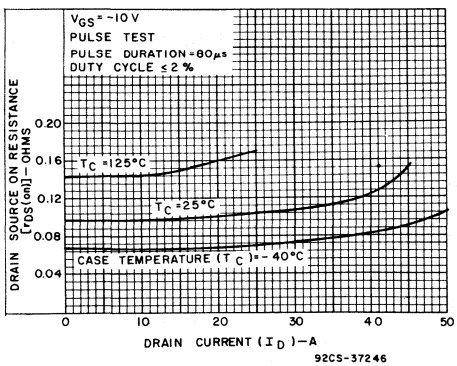


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

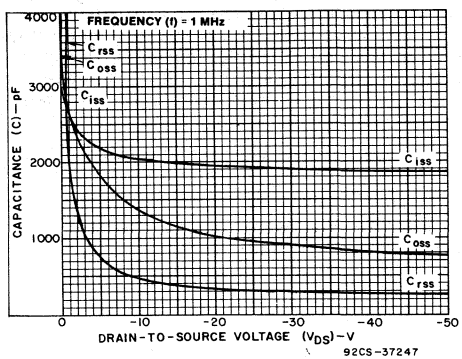


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

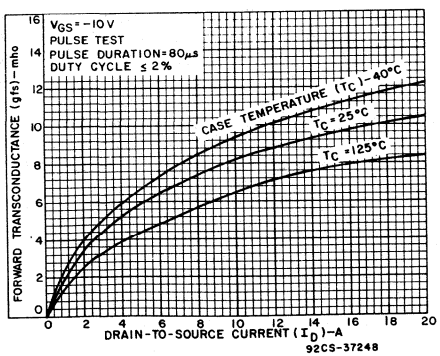


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

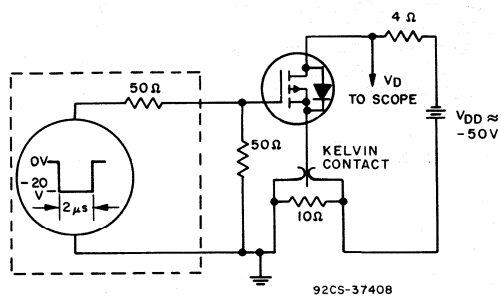


Fig. 11 - Switching time test circuit.

RFL1P08, RFL1P10, RFP2P08, RFP2P10

File Number **1535**

Power MOS Field-Effect Transistors

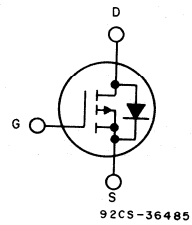
P-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, -80 V and -100 V
$r_{DS}(on)$: 3.0Ω and 3.15Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

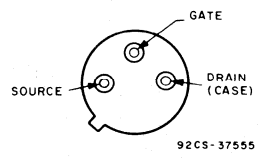
The RFL1P08 and RFL1P10 and the RFP2P08 and RFP2P10 are P-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9400 and TA9401, respectively.

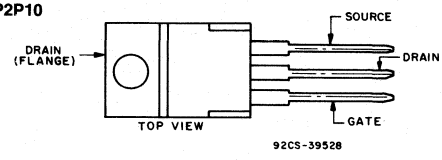
TERMINAL DESIGNATIONS

RFL1P08
RFL1P10



JEDEC TO-205AF

RFP2P08
RFP2P10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFL1P08	RFL1P10	RFP2P08	RFP2P10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100	-80	-100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	-80	-100	-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT Rms Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION	P_T					
@ T_C=25°C		8.33	8.33	25	25	W
Derate above T_C=25°C		0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFL1P08, RFL1P10, RFP2P08, RFP2P10

ELECTRICAL CHARACTERISTICS, at Case Temperature (TC) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
				RFL1P08 RFP2P08		RFL1P10 RFP2P10		
				Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0		-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA		-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65 V		—	1	—	—	µA
		V_{DS} = -80 V		—	—	—	1	
		T_C = 125° C V_{DS} = -65 V		—	50	—	—	
		V_{DS} = -80 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 1 A	RFP	—	-3.0	—	-3.0	V
		V_{GS} = -10 V	RFL	—	-3.15	—	-3.15	
		I_D = 2 A	RFP	—	-9	—	-9	
		V_{GS} = -10 V	RFL	—	-9.3	—	-9.3	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 1A	RFP	—	3.0	—	3.0	Ω
		V_{GS} = -10 V	RFL	—	3.15	—	3.15	
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V I_D = 1 A		200	—	200	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V		—	150	—	150	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		—	80	—	80	
Reverse Transfer Capacitance	C_{rss}	f=1 MHz		—	30	—	30	
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -50 V		7(typ)	25	7(typ)	25	ns
Rise Time	t_r	I_D = 1 A		15(typ)	45	15(typ)	45	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen}=R_{gs}=50Ω		14(typ)	45	14(typ)	45	
Fall Time	t_f	V_{GS} = -10 V	RFP	11(typ)	25	11(typ)	25	
			RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1P08, RFL1P10		—	15	—	15	°C/W
		RFP2P08, RFP2P10		—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFL1P08 RFP2P08		RFL1P10 RFP2P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, di_F/dt = 50 A/µs	135 (typ.)		135 (typ.)		ns

[a]Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

RFL1P08, RFL1P10, RFP2P08, RFP2P10

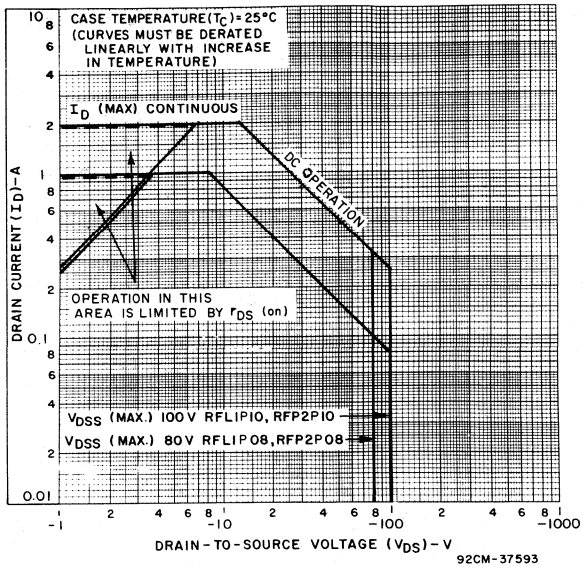


Fig. 1 - Maximum operating areas for all types.

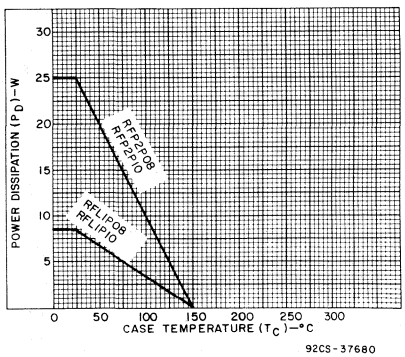


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

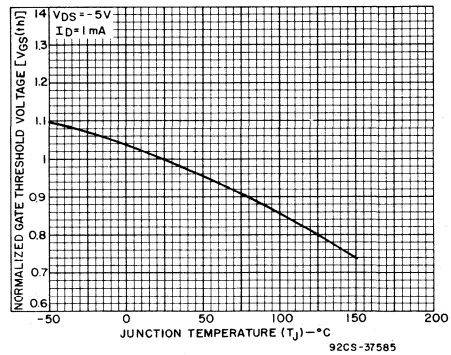


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

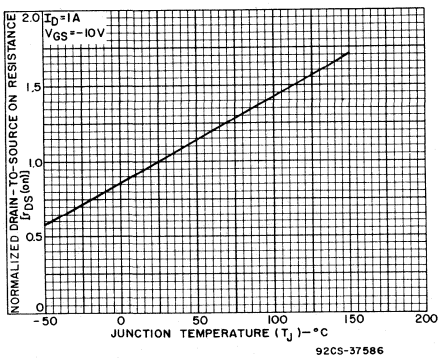


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

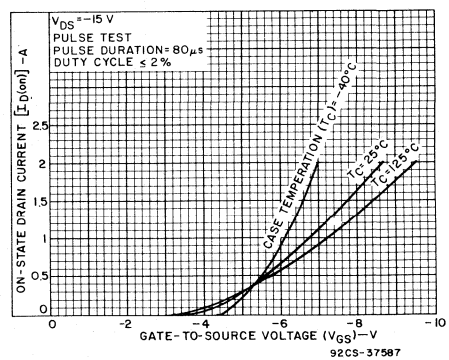


Fig. 5 - Typical transfer characteristics for all types.

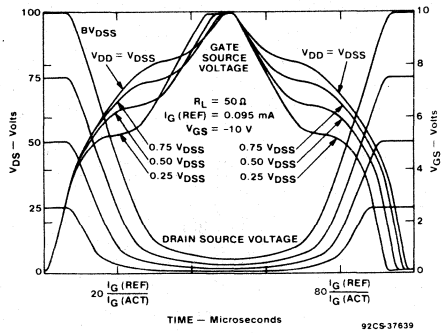


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

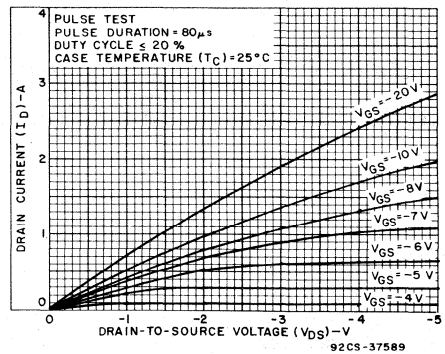


Fig. 7 - Typical saturation characteristics for all types.

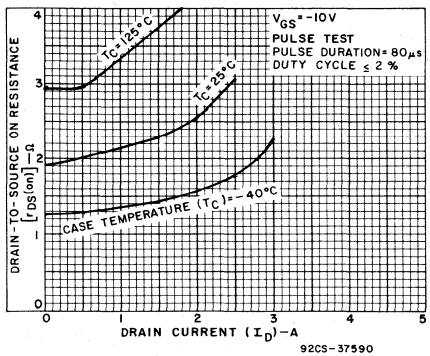


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

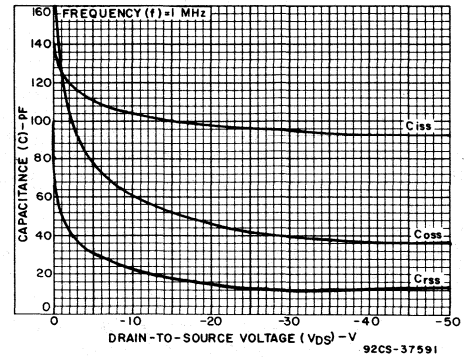


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

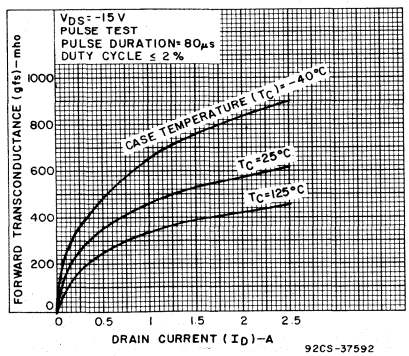


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

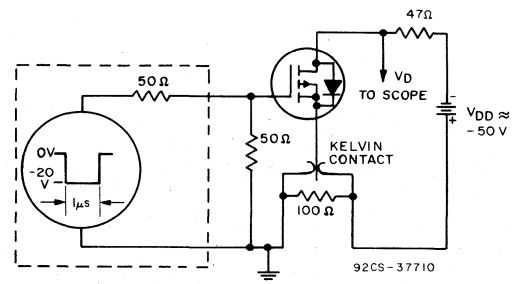


Fig. 11 - Switching time test circuit.

RFM5P12, RFM5P15, RFP5P12, RFP5P15

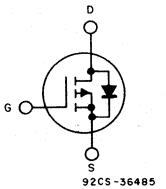
File Number **1463**

P-Channel Enhancement-Mode Power Field-Effect Transistors

5 A, 120 V — 150 V
$r_{DS}(on)$: 1Ω

Features:

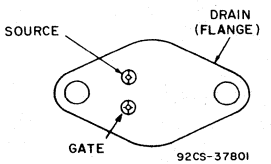
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



P-CHANNEL ENHANCEMENT MODE

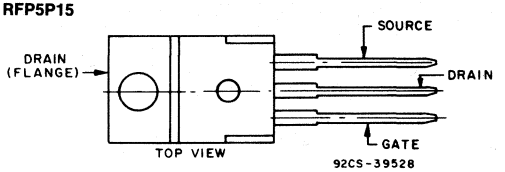
TERMINAL DESIGNATIONS

RFM5P12
RFM5P15



JEDEC TO-204AA

RFP5P12
RFP5P15



JEDEC TO-220AB

The RFM5P12 and RFM5P15 and the RFP5P12 and RFP5P15 * are P-Channel enhancement-mode silicon gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The RFM-Series types are supplied in the JEDEC TO-204AA metal package and the RFP-Series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate Zener diode.

* The RFM and RFP series were formerly RCA developmental numbers TA9320 and TA9321 respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (Tc = 25° C):*

		RFM5P12	RFM5P15		RFP5P12	RFP5P15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-120	-150		-120	-150	V
DRAIN-GATE VOLTAGE (R_{GS} = 1MΩ)	V_{DGR}	-120	-150		-120	-150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20					V
DRAIN CURRENT RMS Continuous	I_D	5					A
Pulsed	I_{DM}	15					A
POWER DISSIPATION	P_T						
@ T_C = 25°C		75	75		60	60	W
Derate above T_C = 25°C		0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150					°C

RFM5P12, RFM5P15, RFP5P12, RFP5P15

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V	—	1	—	—	μA
		V_{DS} = -120 V	—	—	—	1	
		T_C = 125°C V_{DS} = -100 V	—	50	—	—	
		V_{DS} = -120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 2.5 A V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 5A V_{GS} = -10 V	—	-8	—	-8	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 2.5 A V_{GS} = -10 V	—	1	—	1	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 2.5 A	0.75	—	0.75	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	700	—	700	pF
Output Capacitance	C_{oss}		—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1/2 BV_{DSS} I_D = 2.5 A R_{gen} = R_{gs} = 50Ω V_{GS} = 10 V	20(typ.)	60	20(typ.)	60	ns
Rise Time	t_r		36(typ.)	100	36(typ.)	100	
Turn-Off Delay Time	$t_{d(off)}$		63(typ.)	150	63(typ.)	150	
Fall Time	t_f		40(typ.)	100	40(typ.)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM5P12, RFM5P15	—	1.67	—	1.67	°C/W
		RFP5P12, RFP5P15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 2.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	300(typ.)		300(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFM5P12, RFM5P15, RFP5P12, RFP5P15

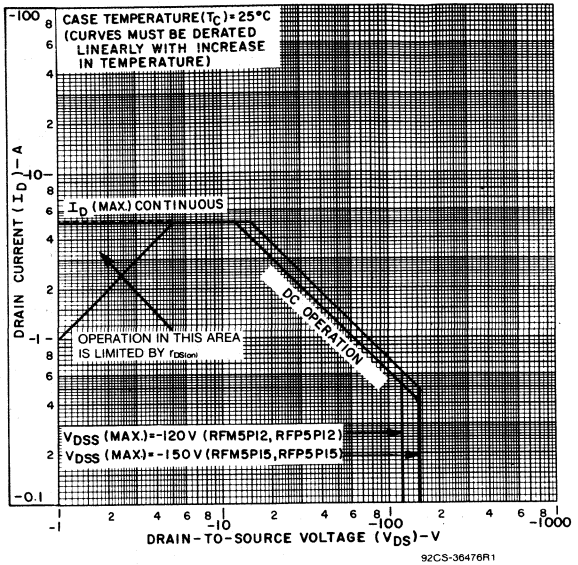


Fig. 1 - Maximum safe operating areas for all types.

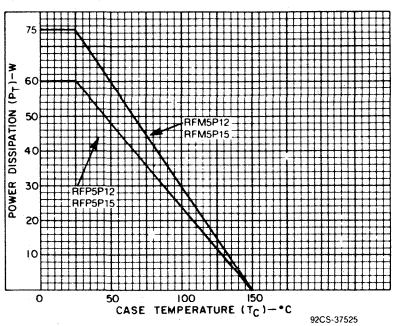


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

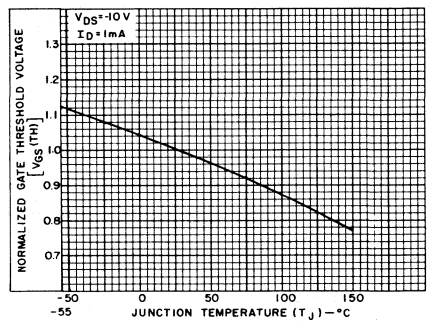


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

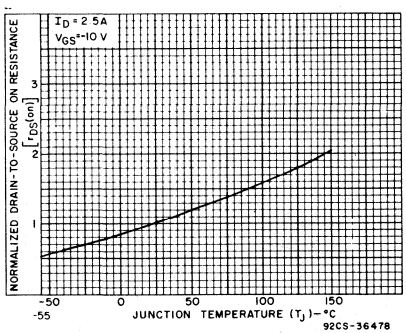


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

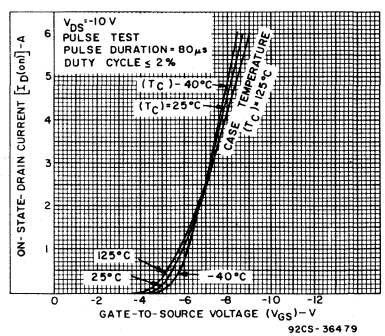


Fig. 5 - Typical transfer characteristics for all types.

RFM5P12, RFM5P15, RFP5P12, RFP5P15

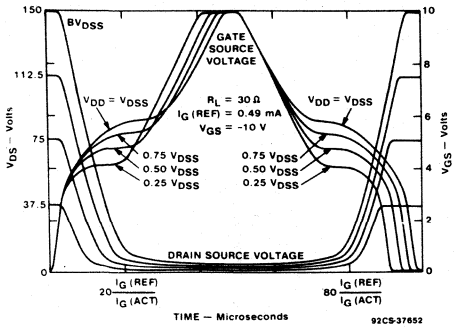


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

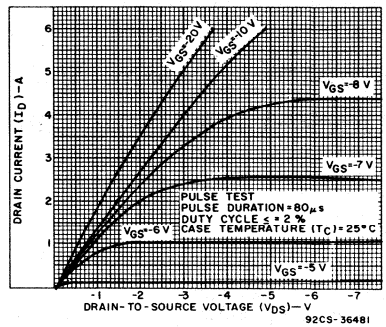


Fig. 7 - Typical saturation characteristics for all types.

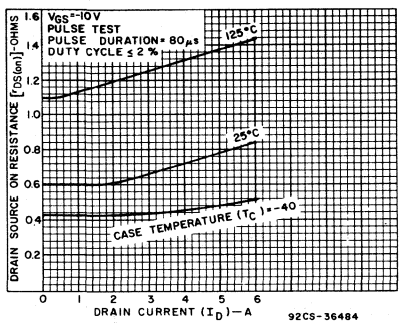


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

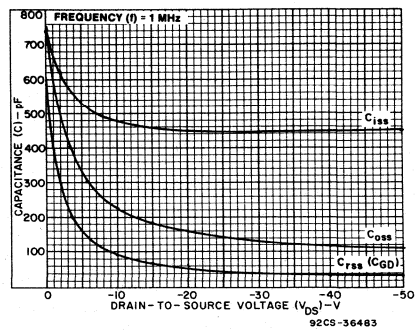


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

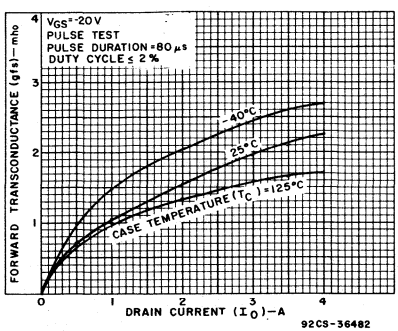


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

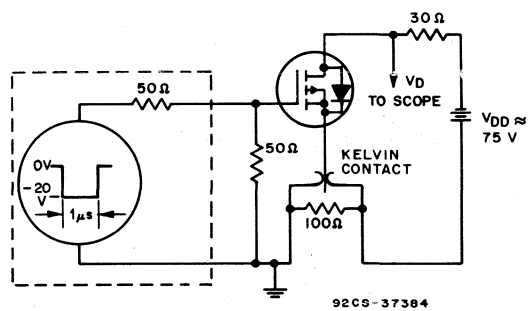


Fig. 11 - Switching Time Test Circuit.

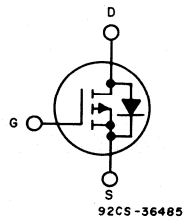
RFM6P08, RFM6P10, RFP6P08, RFP6P10

File Number **1490**

P-Channel Enhancement-Mode Power Field-Effect Transistors

6 A, 80 V — 100 V
$r_{DS}(on)$ = 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



P-CHANNEL ENHANCEMENT MODE

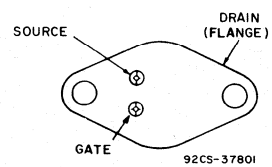
The RFM6P08 and RFM6P10 and the RFP6P08 and RFP6P10* are P-Channel enhancement-mode silicon-gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The RFM-Series types are supplied in the JEDEC TO-204AA metal package and the RFP-Series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate Zener diode.

*The RFM and RFP series were formerly RCA developmental numbers TA9406 and TA9407, respectively.

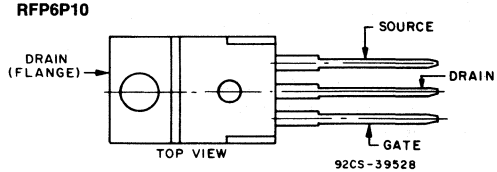
TERMINAL DESIGNATIONS

RFM6P08
RFM6P10



JEDEC TO-204AA

RFP6P08
RFP6P10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM6P08	RFM6P10		RFP6P08	RFP6P10	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			6			A
Pulsed ..... I_{DM}			20			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM6P08, RFM6P10, RFP6P08, RFP6P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125°C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=6 A V_{GS}=-10 V	—	-6	—	-6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	800	—	800	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	350	—	350	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	150	—	150	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	11(typ)	60	11(typ)	60	ns
Rise Time	t_r	I_D=3 A	48(typ)	100	48(typ)	100	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	102(typ)	150	102(typ)	150	ns
Fall Time	t_f	V_{GS}=10 V	70(typ)	100	70(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6P08, RFM6P10	—	1.67	—	1.67	°C/W
		RFP6P08, RFP6P10	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=3 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=50 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM6P08, RFM6P10, RFP6P08, RFP6P10

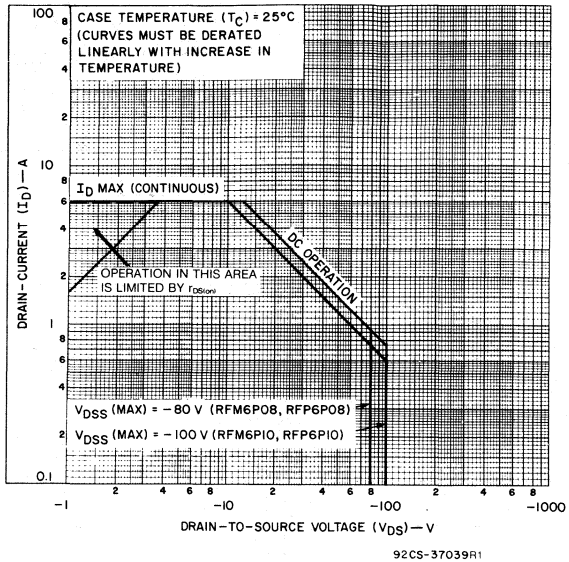


Fig. 1 — Maximum safe operating areas for all types.

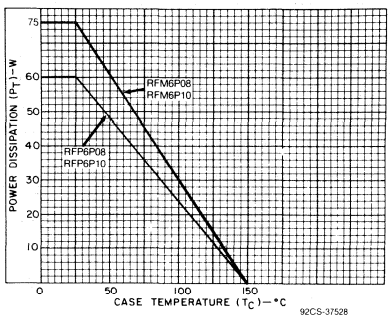


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

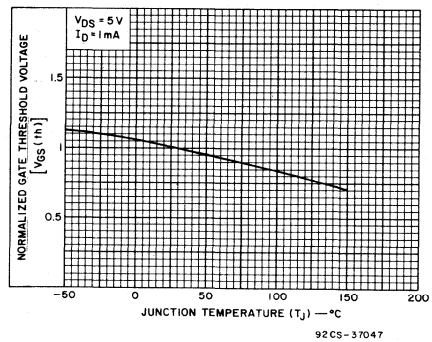


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

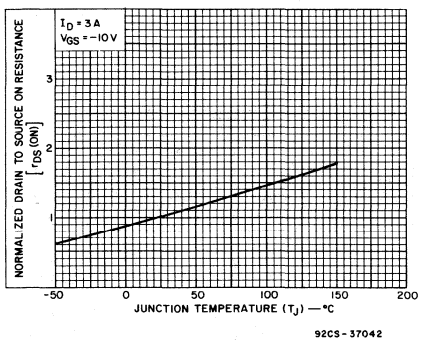


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

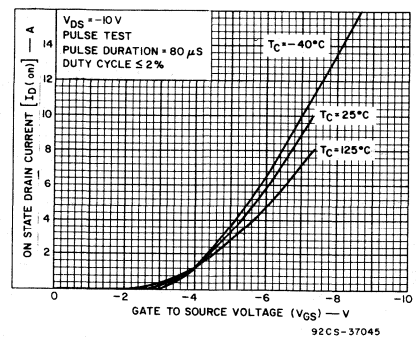


Fig. 5 — Typical transfer characteristics for all types.

RFM6P08, RFM6P10, RFP6P08, RFP6P10

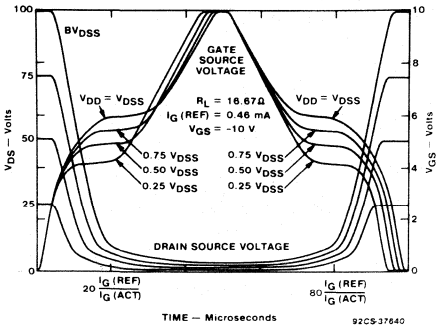


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

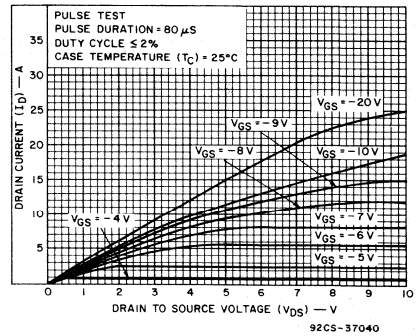


Fig. 7 — Typical saturation characteristics for all types.

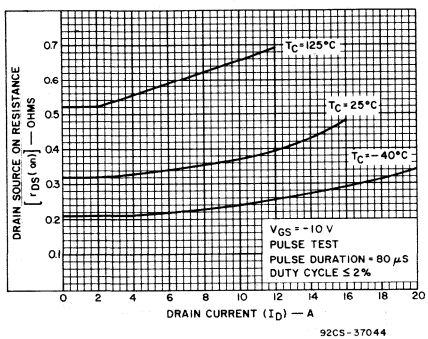


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

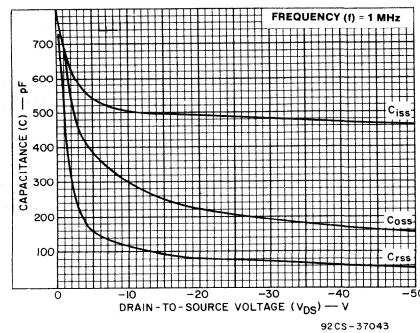


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

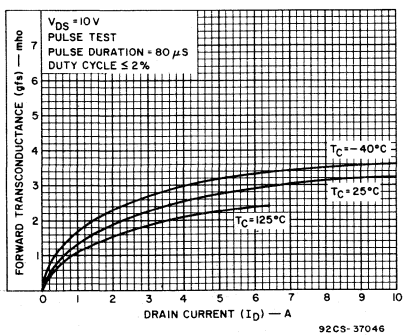


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

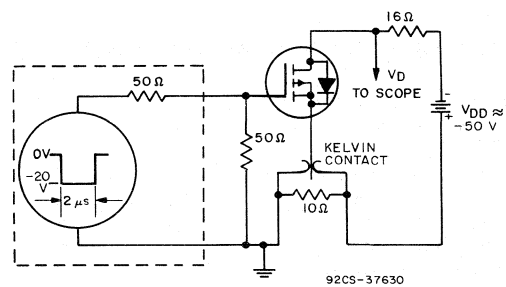


Fig. 11 - Switching Time Test Circuit.

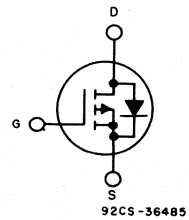
RFM8P08, RFM8P10, RFP8P08, RFP8P10

File Number **1496**

P-Channel Enhancement-Mode Power Field-Effect Transistors

8 A, -80 V and -100 V
$r_{DS}(on)$ = 0.4 Ω

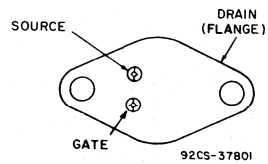
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



P-CHANNEL ENHANCEMENT MODE

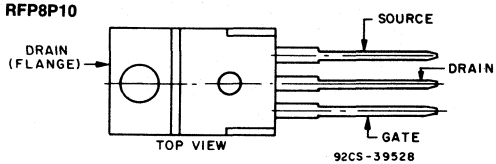
TERMINAL DESIGNATIONS

RFM8P08
RFM8P10



JEDEC TO-204AA

RFP8P08
RFP8P10



JEDEC TO-220AB

The RFM8P08 and RFM8P10 and the RFP8P08 and RFP8P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9410 and TA9411, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFM8P08	RFM8P10		RFP8P08	RFP8P10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100		-80	-100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	-80	-100		-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous	I_D			8			A
Pulsed	I_{DM}			20			A
POWER DISSIPATION @ T_C=25°C	P_T	100	100		75	75	W
Derate above T_C=25°C		0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

RFM8P08, RFM8P10, RFP8P08, RFP8P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	-1.6	—	-1.6	V
		I_D=8 A V_{GS}=-10 V	—	-4.0	—	-4.0	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	.4	—	.4	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=4 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	1500	—	1500	pF
Output Capacitance	C_{oss}		—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}		—	300	—	300	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V I_D=4 A R_{gen}=R_{gs}=50 Ω V_{GS}=-10 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r		70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		166(typ)	275	166(typ)	275	ns
Fall Time	t_f		94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8P08, RFM8P10	—	1.25	—	1.25	°C/W
		RFP8P08, RFP8P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFM8P08, RFM8P10, RFP8P08, RFP8P10

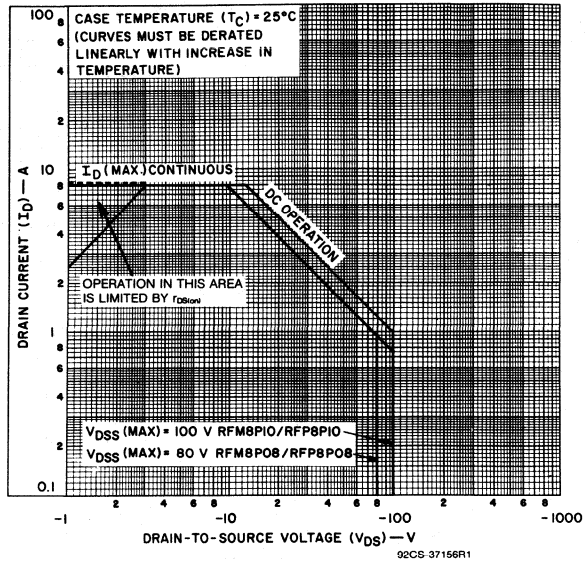


Fig. 1 — Maximum operating areas for all types.

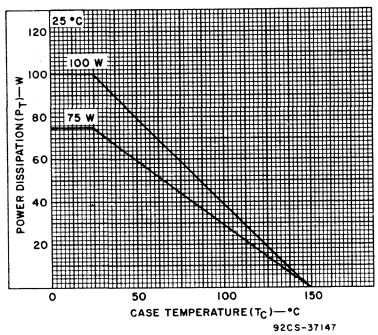


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

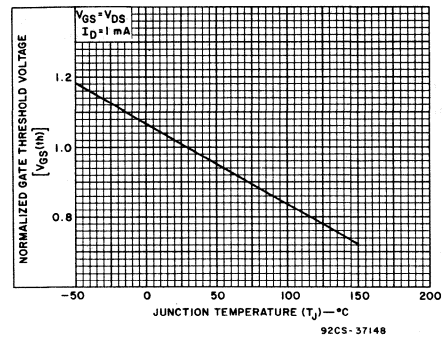


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

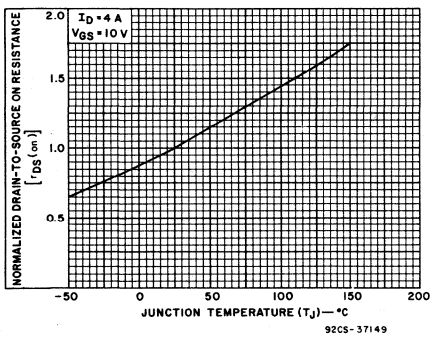


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

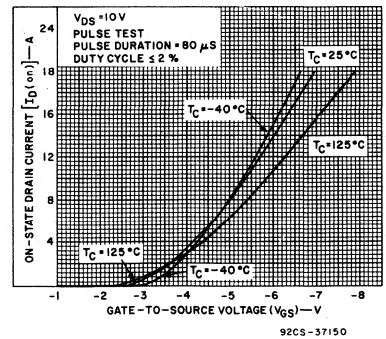


Fig. 5 — Typical transfer characteristics for all types.

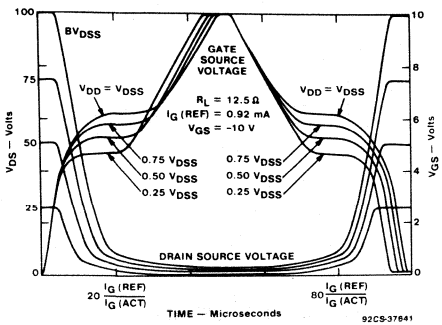


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

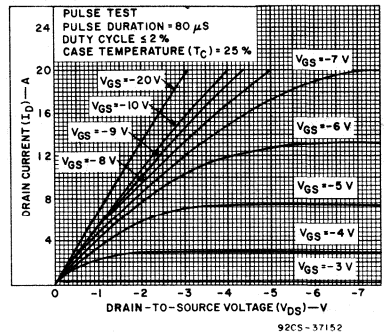


Fig. 7 — Typical saturation characteristics for all types.

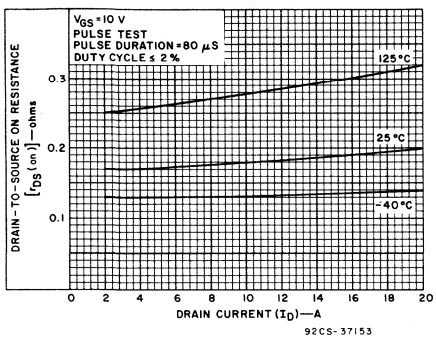


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

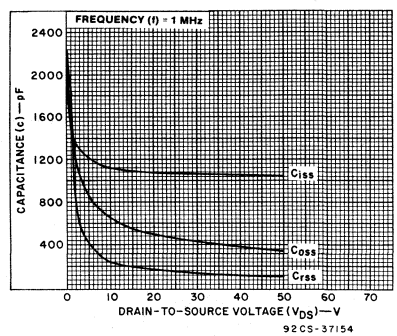


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

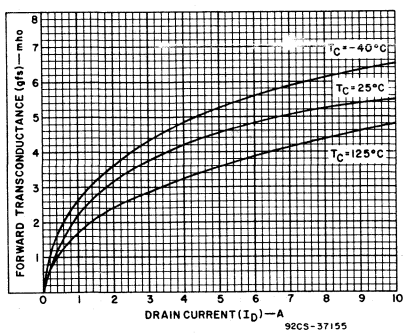


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

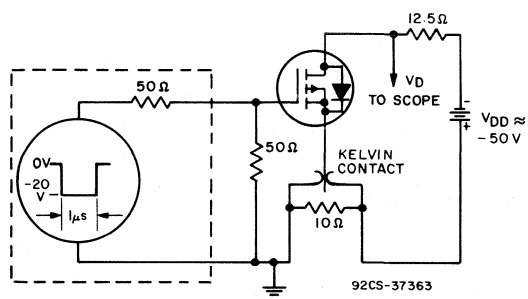


Fig. 11 — Switching Time Test Circuit.

RFM10P12, RFM10P15, RFP10P12, RFP10P15

File Number **1595**

P-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, -120V and -150 V
$r_{DS(on)}$ = 0.5 Ω

Features:

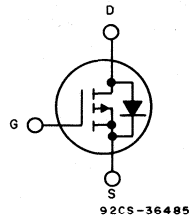
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFM10P12 and RFM10P15 and the RFP10P12 and RFP10P15* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

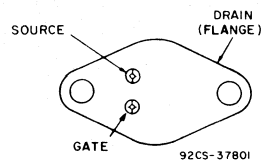
*The RFM and RFP series were formerly developmental TA9404 and TA9405, respectively.

TERMINAL DIAGRAM



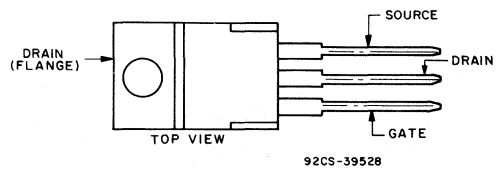
P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

	RFM10P12	RFM10P15	RFP10P12	RFP10P15	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	-120	-150	-120	-150	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ) ..... V_{DGR}	-120	-150	-120	-150	V
GATE-SOURCE VOLTAGE ..... V_{GS}	±20				V
DRAIN CURRENT, RMS Continuous ..... I_D	10				A
Pulsed ..... I_{DM}	30				A
POWER DISSIPATION @ T_C = 25°C ..... P_T	100	100	75	75	W
Derate above T_C = 25°C	0.8	0.8	0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}	-55 to +150				°C

RFM10P12, RFM10P15, RFP10P12, RFP10P15

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V V_{DS} = -120 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = -100 V V_{DS} = -120 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 10 A V_{GS} = -10 V	—	-6.0	—	-6.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V	—	1700	—	1700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	350	—	350	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -75 V	24(typ)	50	24(typ)	50	ns
Rise Time	t_r	I_D = 5 A	74(typ)	150	74(typ)	150	ns
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = R_{gs} = 50 Ω	138(typ)	225	138(typ)	225	ns
Fall Time	t_f	V_{GS} = -10 V	61(typ)	100	61(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10P12, RFM10P15	—	1.25	—	1.25	°C/W
		RFP10P12, RFP10P15	—	1.67	—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, dI_F/d_t = 100 A/μs	210 (typ.)		210 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM10P12, RFM10P15, RFP10P12, RFP10P15

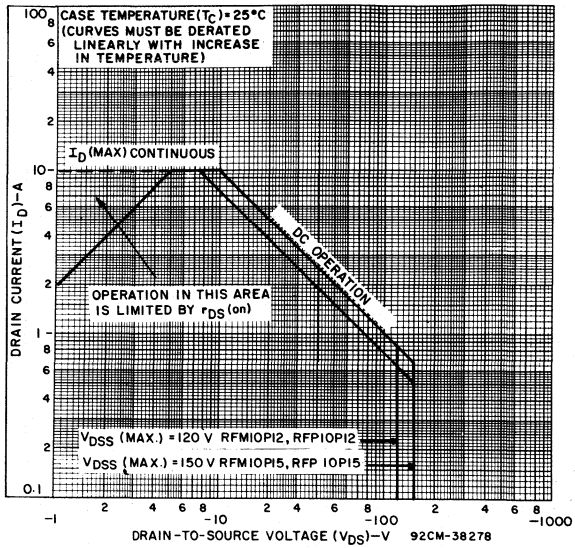


Fig. 1 - Maximum safe operating areas for all types.

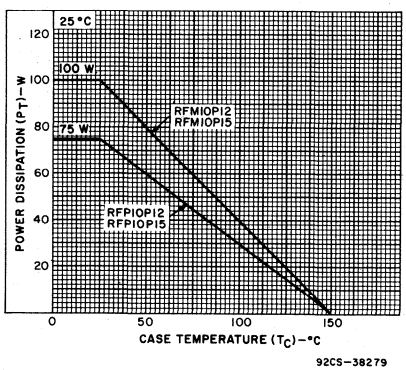


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

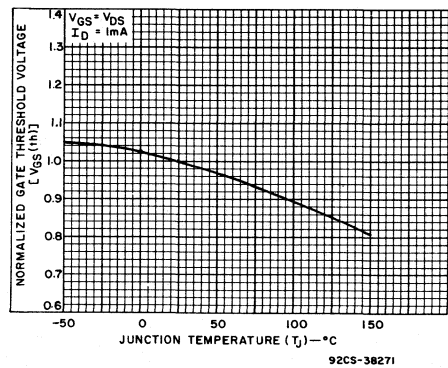


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

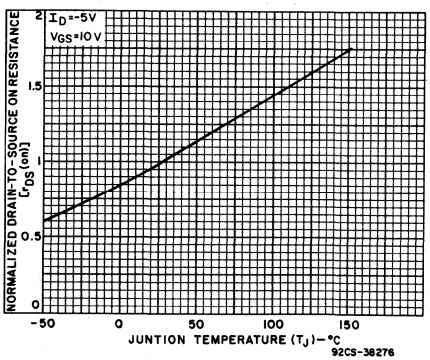


Fig. 4 - Normalized drain-to-source on resistance as as function of junction temperature for all types.

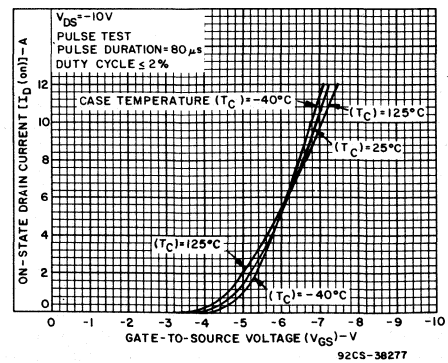


Fig. 5 - Typical transfer characteristics for all types.

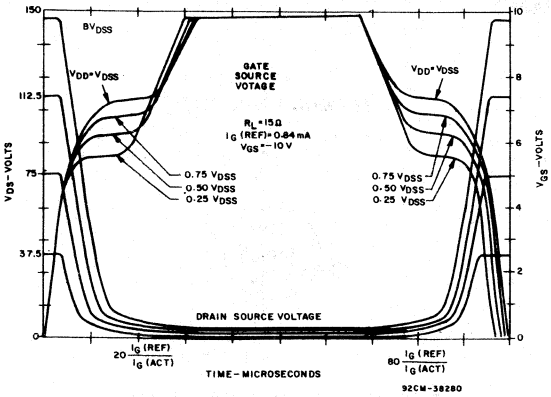


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA application notes AN-7254 and AN-7260.

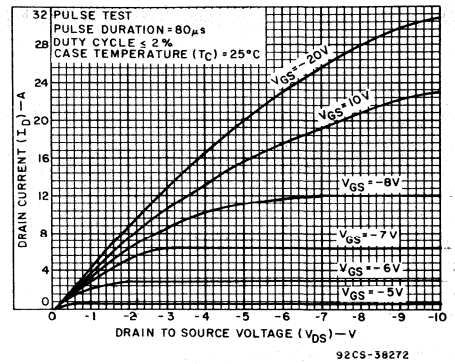


Fig. 7 - Typical saturation characteristics for all types.

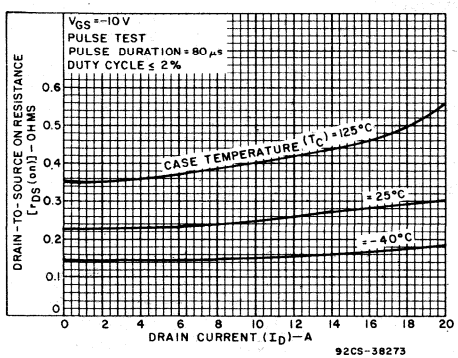


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

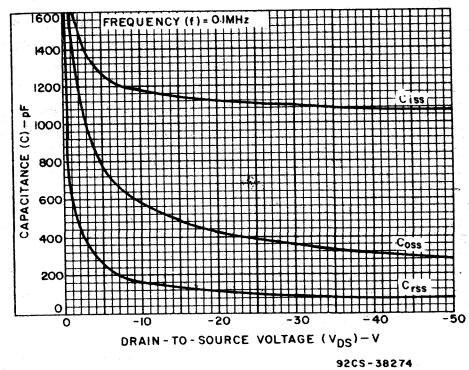


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

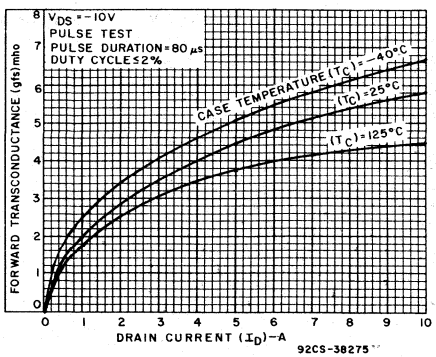


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

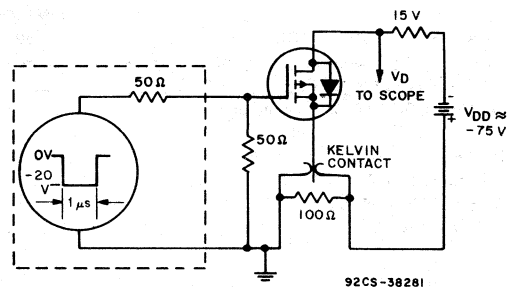


Fig. 11 - Switching Time Test Circuit.

RFM12P08, RFM12P10, RFP12P08, RFP12P10

File Number **1495**

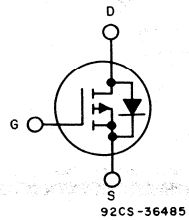
Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, -80 V and -100 V
$r_{DS}(on)$ = 0.3 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

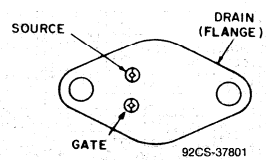
TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

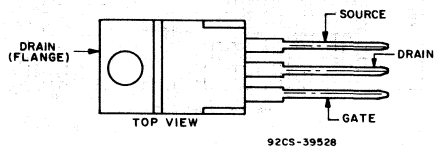
TERMINAL DESIGNATIONS

RFM12P08
RFM12P10



JEDEC TO-204AA

RFP12P08
RFP12P10



JEDEC TO-220AB

The RFM12P08 and RFM12P10 and the RFP12P08 and RFP12P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9410 and TA9411, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12P08	RFM12P10		RFP12P08	RFP12P10	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	-80	-100		-80	-100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	-80	-100		-80	-100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C ..... P_T	100	100		75	75	W
Derate above T_C=25°C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM12P08, RFM12P10, RFP12P08, RFP12P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=12 A V_{GS}=-10 V	—	-4.8	—	-4.8	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	.3	—	.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V V_{GS}=0 V f = 1MHz	—	1500	—	1500	pF
Output Capacitance	C_{oss}		—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}		—	300	—	300	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=6 A R_{gen}=R_{gs}=50 Ω V_{GS}=-10 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r		90(typ)	175	90(typ)	175	ns
Turn-Off Delay Time	$t_d(off)$		144(typ)	275	144(typ)	275	ns
Fall Time	t_f		94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12P08, RFM12P10	—	1.25	—	1.25	°C/W
		RFP12P08, RFP12P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM12P08, RFM12P10, RFP12P08, RFP12P10

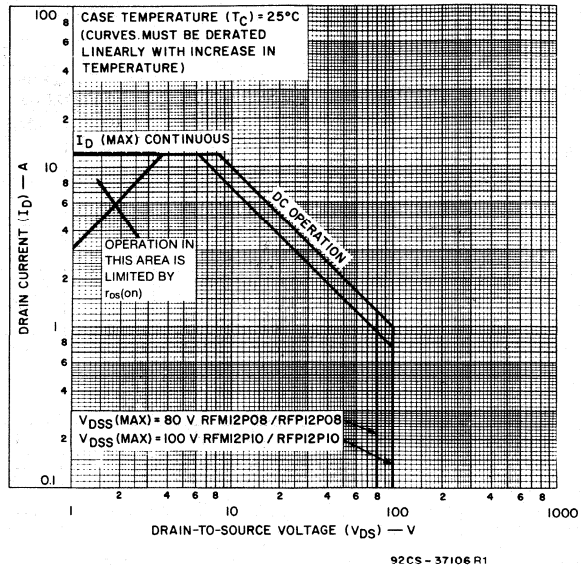


Fig. 1 — Maximum safe operating areas for all types.

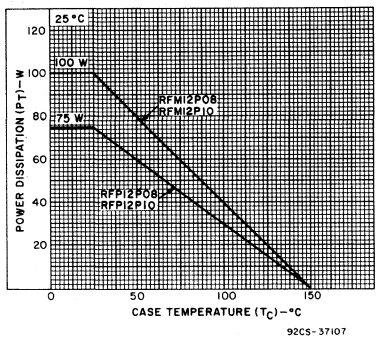


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

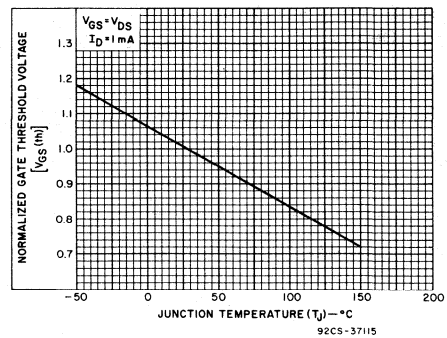


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

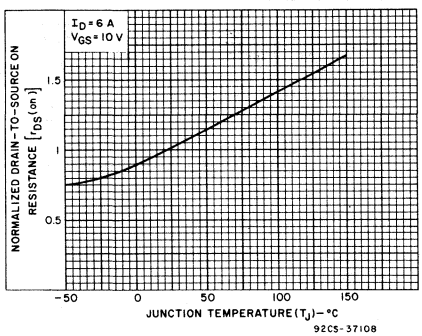


Fig. 4 — Normalized drain-to-source on resistance as a function of junction temperature for all types.

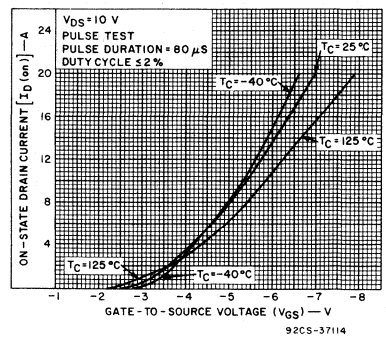


Fig. 5 — Typical transfer characteristics for all types.

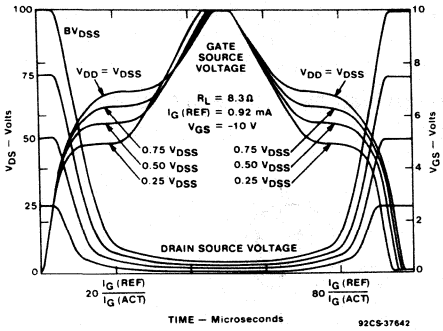


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

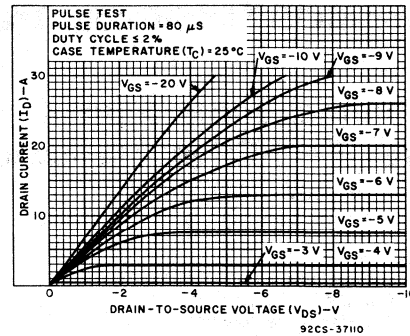


Fig. 7 — Typical saturation characteristics for all types.

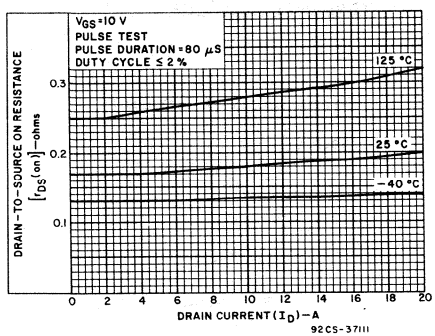


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

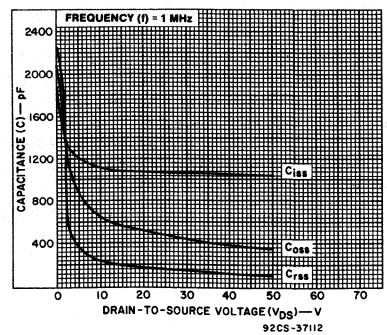


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

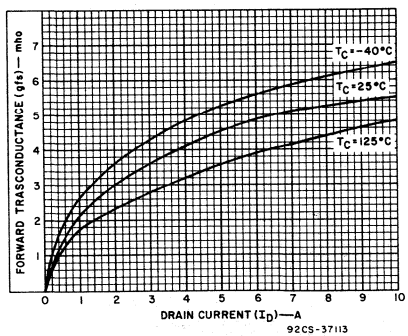


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

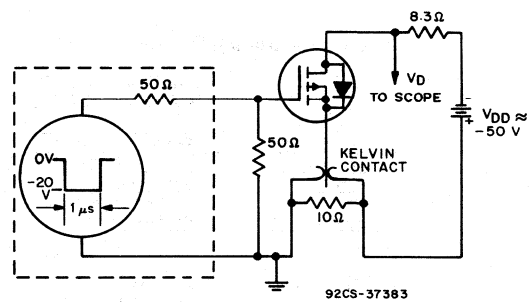


Fig. 11 — Switching Time Test Circuit

2N6755, 2N6756

File Number **1586**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

12A and 14A, 60V - 100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

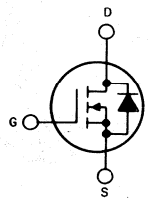
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6755 and 2N6756 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

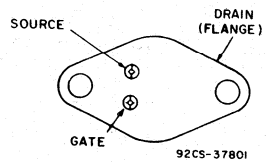
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6755	2N6756	Units
V_{DS}	Drain – Source Voltage	60*	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ)	60*	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	12*	14*	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0*	9.0*	A
I_{DM}	Pulsed Drain Current	25	30	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		25	30	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, T_C = 125°C
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 36V, I_D = 9A, Z_o = 15Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	
t_f	Fall Time	ALL	–	–	45*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage ①	2N6755	0.85*	–	1.7*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	T_C 25°C, I_S = 14A, V_{GS} 0
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

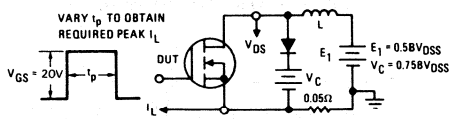


Fig. 1 — Clamped Inductive Test Circuit

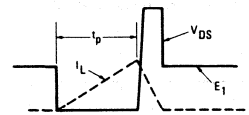


Fig. 2 — Clamped Inductive Waveforms

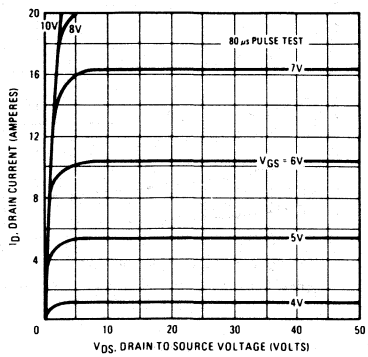


Fig. 3 — Typical Output Characteristics

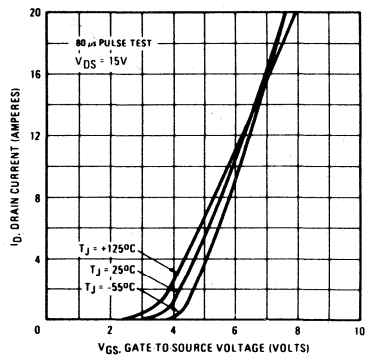


Fig. 4 — Typical Transfer Characteristics

2N6755, 2N6756

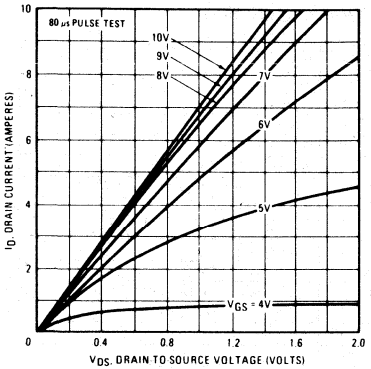


Fig. 5— Typical Saturation Characteristics (2N6755)

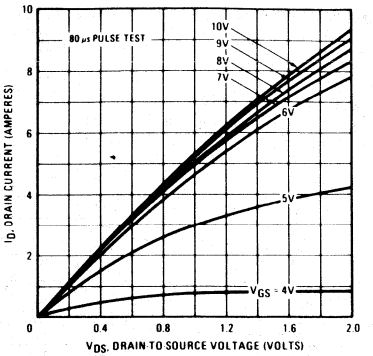


Fig. 6— Typical Saturation Characteristics (2N6756)

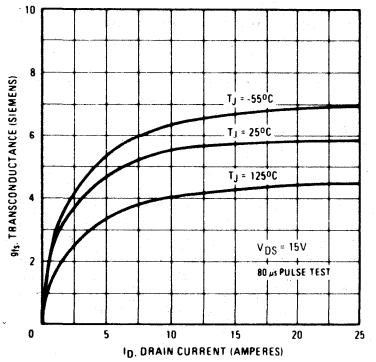


Fig. 7 — Typical Transconductance Vs. Drain Current

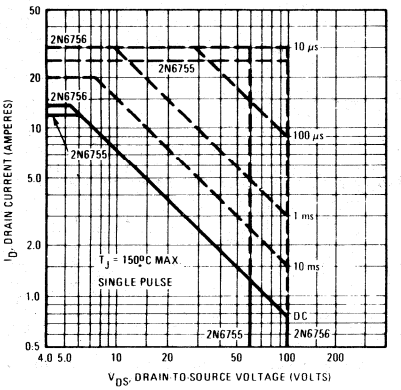


Fig. 8 — Maximum Safe Operating Area

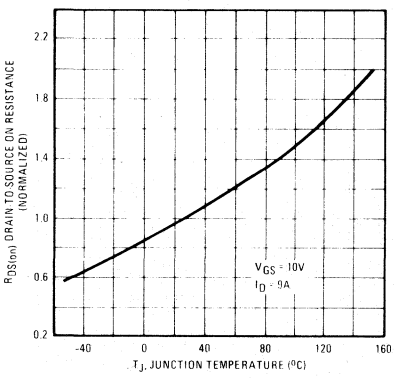


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

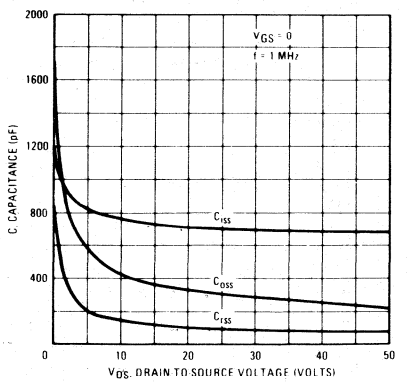


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

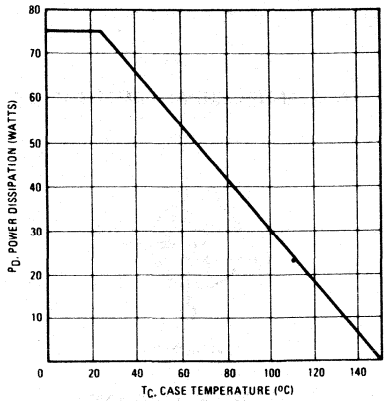


Fig. 11 — Power Vs. Temperature Derating Curve

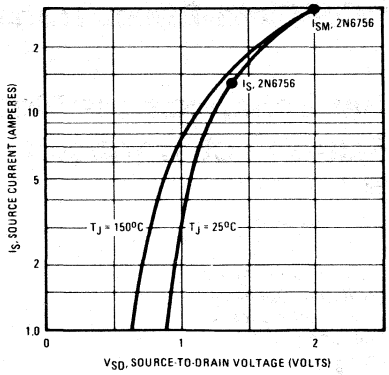


Fig. 12 — Typical Body-Drain Diode Forward Voltage

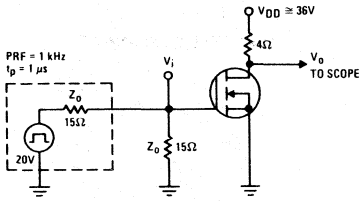


Fig. 13 — Switching Time Test Circuit

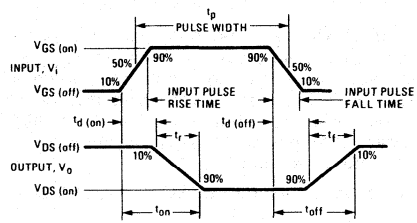


Fig. 14 — Switching Time Waveforms

2N6757, 2N6758

File Number **1587**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8A and 9A, 150V - 200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

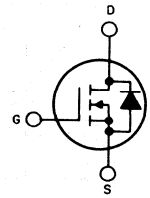
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6757 and 2N6758 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

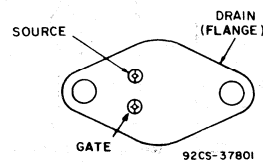
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6757	2N6758	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	9.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	6.0*	A
I_{DM}	Pulsed Drain Current	12	15	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		12	15	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	V_{GS} = 0
		2N6758	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6757	–	–	4.6*	V	V_{GS} = 10V, I_D = 8A
		2N6758	–	–	3.6*	V	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	0.4	0.6*	Ω	V_{GS} = 10V, I_D = 5A
		2N6758	–	0.25	0.4*	Ω	V_{GS} = 10V, I_D = 6A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	–	1.13*	Ω	V_{GS} = 10V, I_D = 5A, T_C = 125°C
		2N6758	–	–	0.75*	Ω	V_{GS} = 10V, I_D = 6A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	3.0*	5.0	9.0*	S (℧)	V_{DS} = 15V, I_D = 6A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	100*	250	450*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 90V$, I_D = 6A, Z_o = 15Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50*	ns	
t_f	Fall Time	ALL	–	–	40*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6758	–	–	9.0*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V_{SD}	Diode Forward Voltage ①	2N6757	0.75*	–	1.50*	V	T_C = 25°C, I_S = 8A, V_{GS} = 0
		2N6758	0.80*	–	1.60*	V	T_C = 25°C, I_S = 9A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

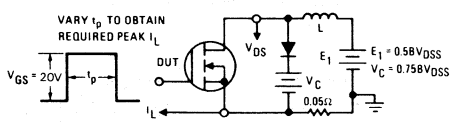


Fig. 1 – Clamped Inductive Test Circuit

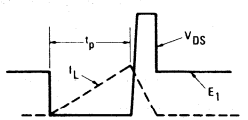


Fig. 2 – Clamped Inductive Waveforms

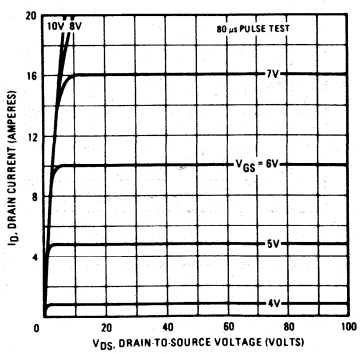


Fig. 3 – Typical Output Characteristics

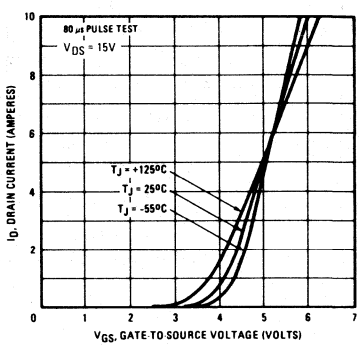


Fig. 4 – Typical Transfer Characteristics

2N6757, 2N6758

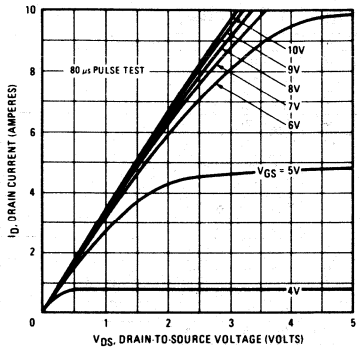


Fig. 5— Typical Saturation Characteristics (2N6757)

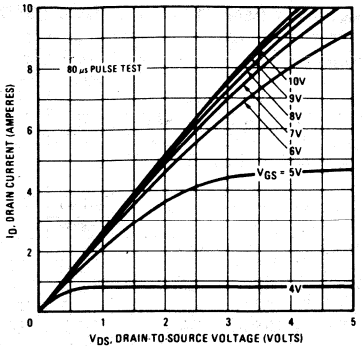


Fig. 6— Typical Saturation Characteristics (2N6758)

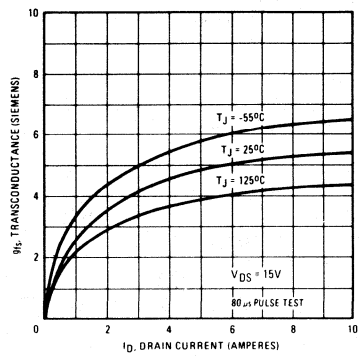


Fig. 7 — Typical Transconductance Vs. Drain Current

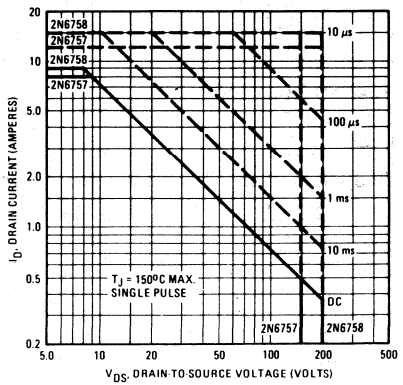


Fig. 8 — Maximum Safe Operating Area

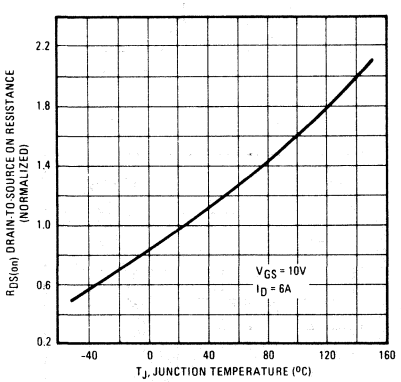


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

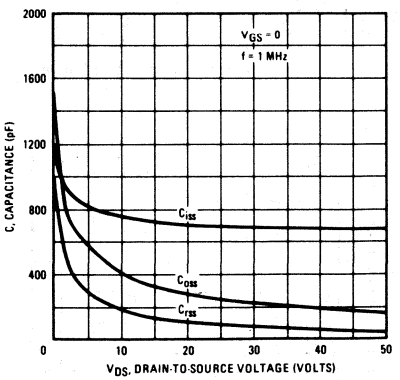


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

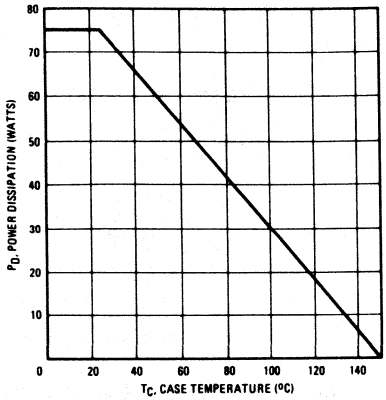


Fig. 11 – Power Vs. Temperature Derating Curve

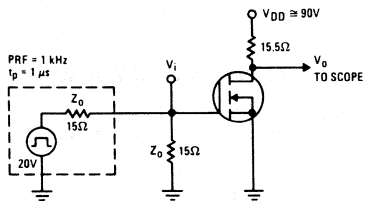


Fig. 13 – Switching Time Test Circuit

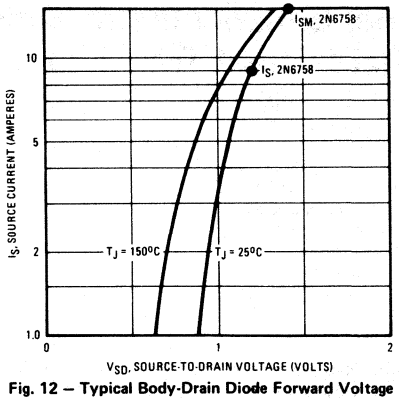


Fig. 12 – Typical Body-Drain Diode Forward Voltage

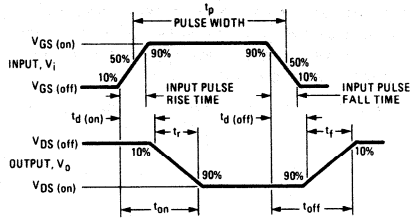


Fig. 14 – Switching Time Waveforms

2N6759, 2N6760

File Number **1588**

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5A and 5.5A, 350V - 400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

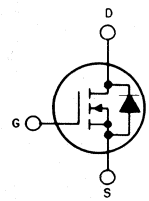
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6759 and 2N6760 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

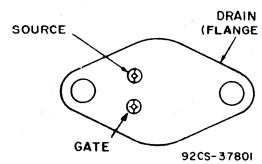
TERMINAL DIAGRAM



92CS-33741

N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6759	2N6760	Units
V_{DS}	Drain – Source Voltage	350*	400*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	350*	400*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5*	5.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0*	3.5*	A
I_{DM}	Pulsed Drain Current	7.0	8.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH	7.0 | 8.0	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6759	350	–	–	V	V_{GS} = 0
		2N6760	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6759	–	–	7.0*	V	V_{GS} = 10V, I_D = 4.5A
		2N6760	–	–	6.7*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 3A
		2N6760	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3A, T_C = 125°C
		2N6760	–	–	2.2*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	3.0*	4.5	9.0*	S (℧)	V_{DS} = 15V, I_D = 3.5A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	50*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 175V, I_D = 3.5A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	35*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6760	–	–	5.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
		2N6760	–	–	8.0		
V_{SD}	Diode Forward Voltage ①	2N6759	0.70*	–	1.4*	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0
		2N6760	0.75*	–	1.5*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

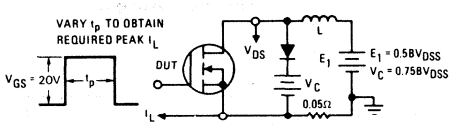


Fig. 1 – Clamped Inductive Test Circuit

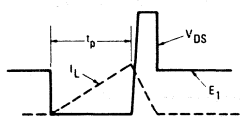


Fig. 2 – Clamped Inductive Waveforms

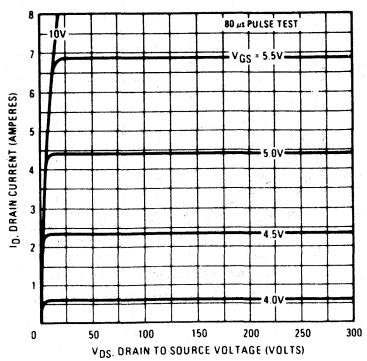


Fig. 3 – Typical Output Characteristics

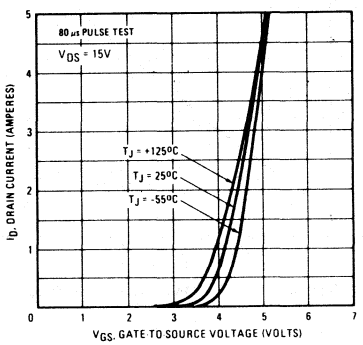


Fig. 4 – Typical Transfer Characteristics

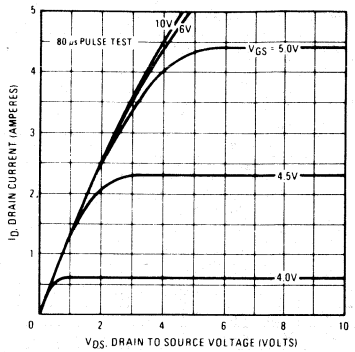


Fig. 5— Typical Saturation Characteristics (2N6759)

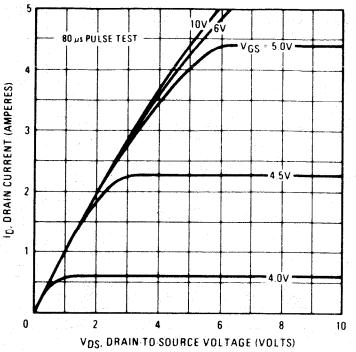


Fig. 6— Typical Saturation Characteristics (2N6760)

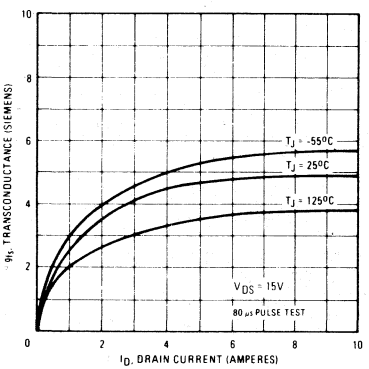


Fig. 7 — Typical Transconductance Vs. Drain Current

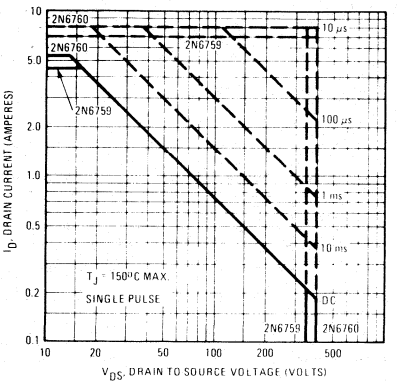


Fig. 8 — Maximum Safe Operating Area

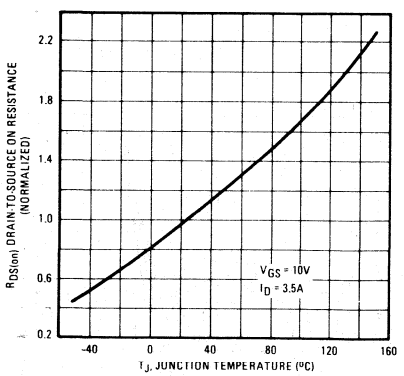


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

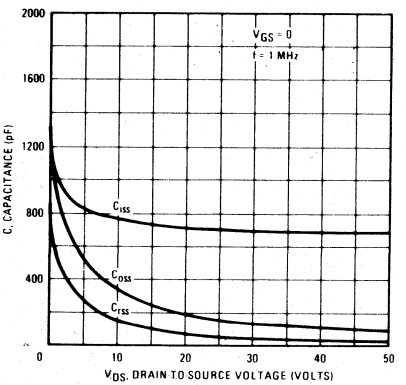


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

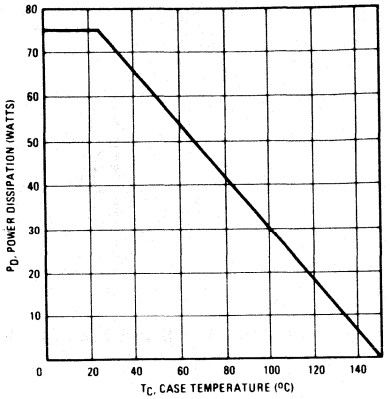


Fig. 11 — Power Vs. Temperature Derating Curve

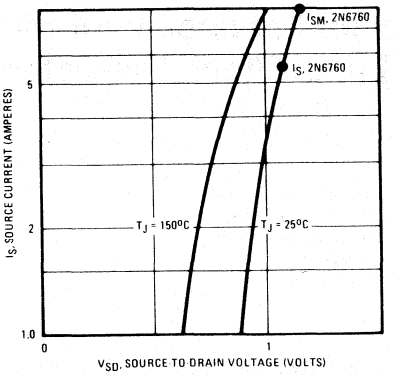


Fig. 12 — Typical Body-Drain Diode Forward Voltage

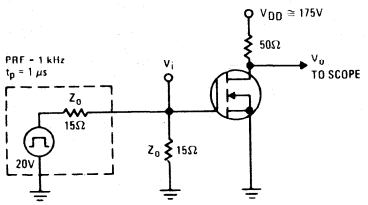


Fig. 13 — Switching Time Test Circuit

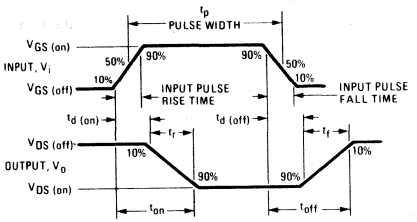


Fig. 14 — Switching Time Waveforms

2N6761, 2N6762

File Number **1589**

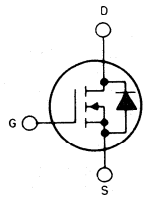
N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 4.5A, 450V - 500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



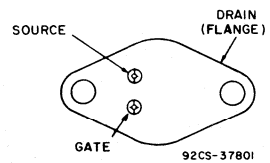
92CS-33741

N-CHANNEL ENHANCEMENT MODE

The 2N6761 and 2N6762 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6761	2N6762	Units
V_{DS}	Drain – Source Voltage	450*	500*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	450*	500*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0*	4.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5*	3.0*	A
I_{DM}	Pulsed Drain Current	6.0	7.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		6.0	7.0	
T_J	Operating and	-55* to 150*		°C
T_{stg}	Storage Temperature Range			
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6761	450	–	–	V	V_{GS} = 0
		2N6762	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 25°C to 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6761	–	–	8.0*	V	V_{GS} = 10V, I_D = 4A
		2N6762	–	–	7.7*	V	V_{GS} = 10V, I_D = 4.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	1.5	2.0*	Ω	V_{GS} = 10V, I_D = 2.5A
		2N6762	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	–	4.4*	Ω	V_{GS} = 10V, I_D = 2.5A, T_C = 125°C
		2N6762	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3.0A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	2.5*	3.5	7.5*	S (℧)	V_{DS} = 16V, I_D = 3A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	25*	100	200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 225V, I_D = 3A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	30*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	30*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6762	–	–	4.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
		2N6762	–	–	7.0		
V_{SD}	Diode Forward Voltage ①	2N6761	0.65*	–	1.3*	V	T_C = 25°C, I_S = 4A, V_{GS} = 0
		2N6762	0.7*	–	1.4*	V	T_C = 25°C, I_S =4.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

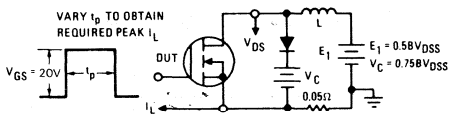


Fig. 1 – Clamped Inductive Test Circuit

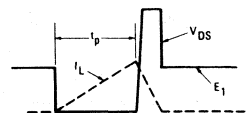


Fig. 2 – Clamped Inductive Waveforms

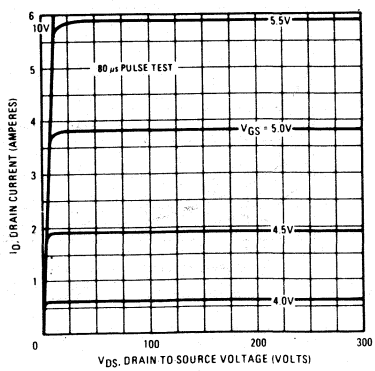


Fig. 3 – Typical Output Characteristics

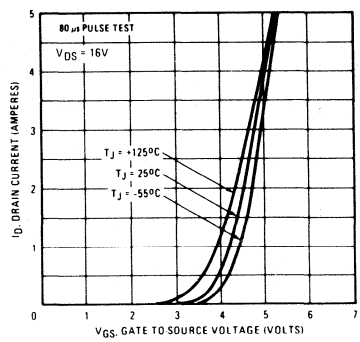


Fig. 4 – Typical Transfer Characteristics

2N6761, 2N6762

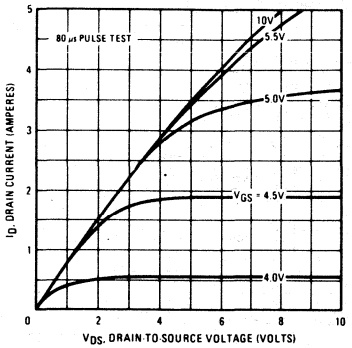


Fig. 5— Typical Saturation Characteristics (2N6761)

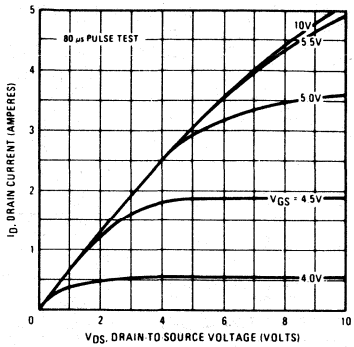


Fig. 6— Typical Saturation Characteristics (2N6762)

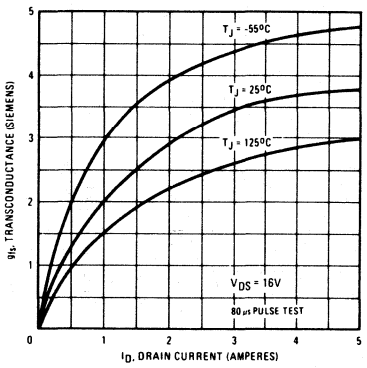


Fig. 7 — Typical Transconductance Vs. Drain Current

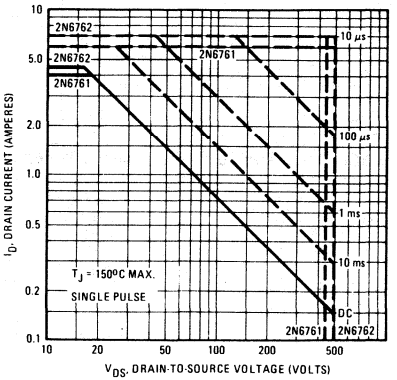


Fig. 8 — Maximum Safe Operating Area

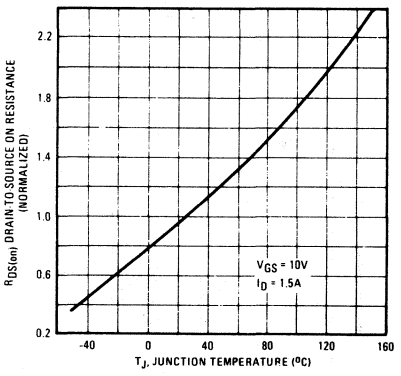


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

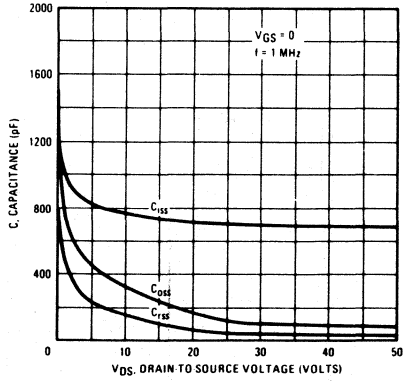


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

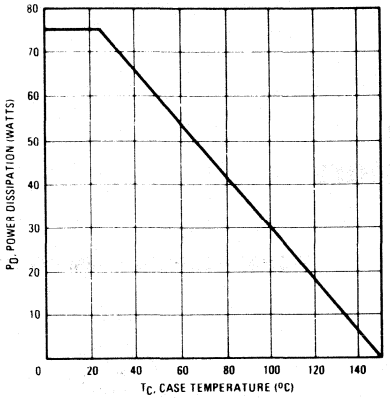


Fig. 11 – Power Vs. Temperature Derating Curve

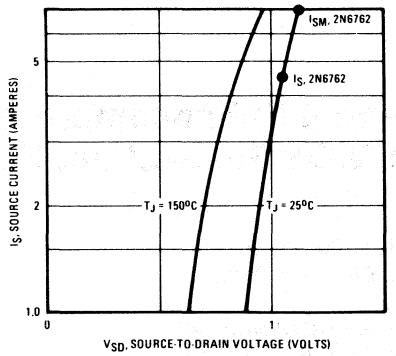


Fig. 12 – Typical Body-Drain Diode Forward Voltage

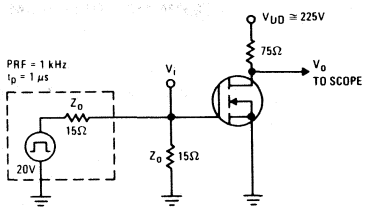


Fig. 13 – Switching Time Test Circuit

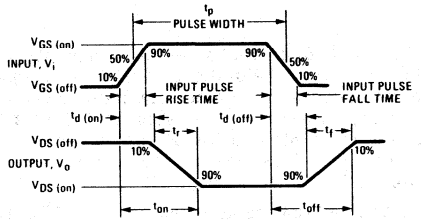


Fig. 14 – Switching Time Waveforms

2N6763, 2N6764

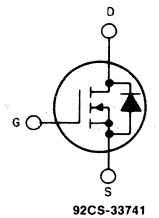
File Number **1590**

N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

31A and 38A, 60V-100V
$r_{DS}(on)$ = 0.08 Ω and 0.055 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



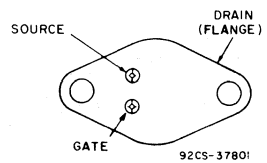
92CS-33741

TERMINAL DIAGRAM

The 2N6763 and 2N6764 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6763 and 2N6764 are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	2N6763	2N6764	
* DRAIN-SOURCE VOLTAGE, V_{DS}	60	100	V
* DRAIN-GATE VOLTAGE, V_{DGR} (R_{GS} = 20 kΩ)	60	100	V
* GATE-SOURCE VOLTAGE, V_{GS}	±20		V
DRAIN CURRENT, I_D, RMS Continuous			
At T_C = 25°C	31	38	A
At T_C = 100°C	20	24	A
DRAIN CURRENT, I_{DM}, Pulsed	60	70	A
* POWER DISSIPATION, P_T			
At T_C = 25°C	150		W
At T_C = 100°C	60		W
Above T_C = 25°C, Derate Linearly	1.2		W/°C
INDUCTIVE CURRENT, I_{LM}, Clamped (L = 100 μH)	60	70	A
* OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150		°C
* LEAD TEMPERATURE, T_L			
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300		°C

*JEDEC registered data.

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6763	60	–	–	V	V_{GS} = 0
		2N6764	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6763	–	–	2.48*	V	V_{GS} = 10V I_D = 31A
		2N6764	–	–	2.09*	V	V_{GS} = 10V, I_D = 38A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	0.06	0.08*	Ω	V_{GS} = 10V, I_D = 20A
		2N6764	–	0.045	0.055*	Ω	V_{GS} = 10V, I_D = 24A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	–	0.136*	Ω	V_{GS} = 10V, I_D = 20A, T_C = 125°C
		2N6764	–	–	0.094*	Ω	V_{GS} = 10V, I_D = 24A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	12.5	27*	S (℧)	V_{DS} = 15V, I_D = 24A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	500*	1000	1500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 24V, I_D = 24A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6763	–	–	31*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6764	–	–	38*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6763	–	–	60	A	
		2N6764	–	–	70		
V_{SD}	Diode Forward Voltage ①	2N6763	0.90*	–	1.8*	V	T_C = 25°C, I_S = 31A, V_{GS} = 0
		2N6764	0.95*	–	1.9*	V	T_C = 25°C, I_S = 38A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

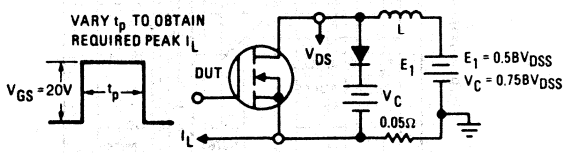


Fig. 1 - Clamped inductive test circuit.

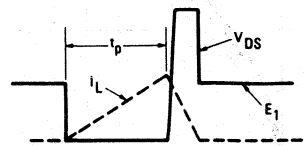


Fig. 2 - Clamped inductive waveforms.

2N6763, 2N6764

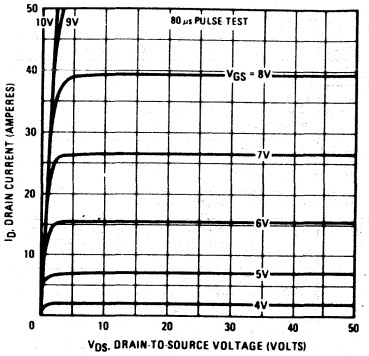


Fig. 3 - Typical output characteristics.

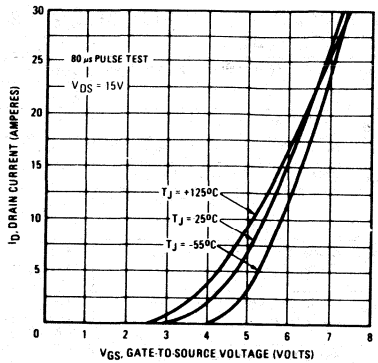


Fig. 4 - Typical transfer characteristics.

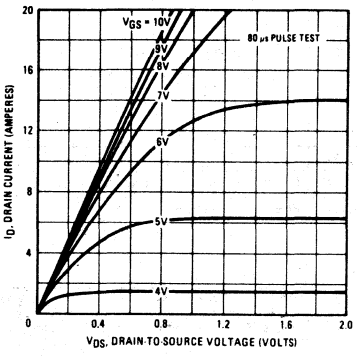


Fig. 5 - Typical saturation characteristics for the 2N6763.

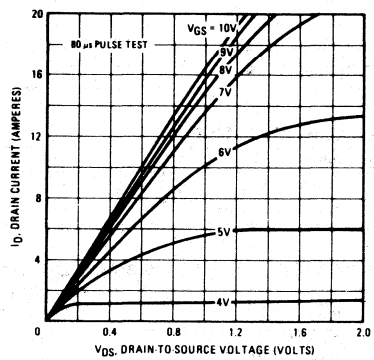


Fig. 6 - Typical saturation characteristics for the 2N6764.

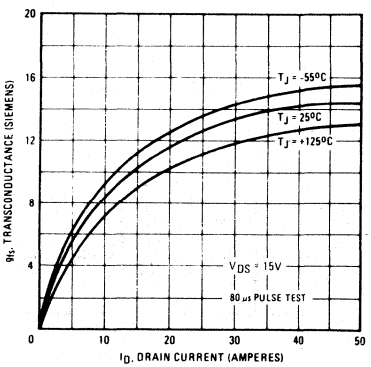


Fig. 7 - Typical transconductance vs. drain current.

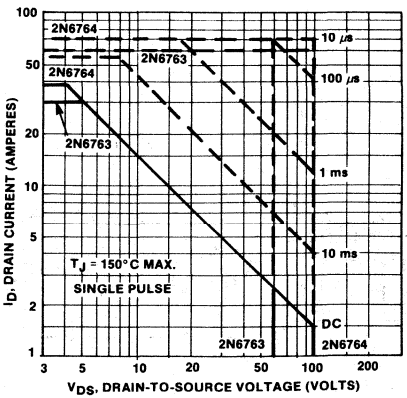


Fig. 8 - Maximum safe operating areas.

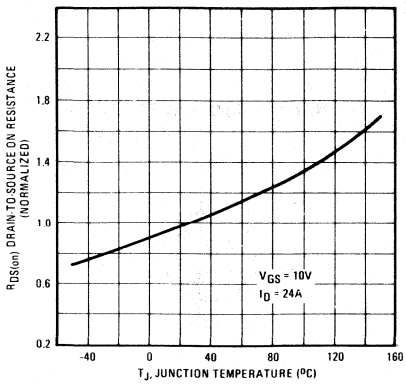


Fig. 9 - Typical normalized on-resistance vs. temperature.

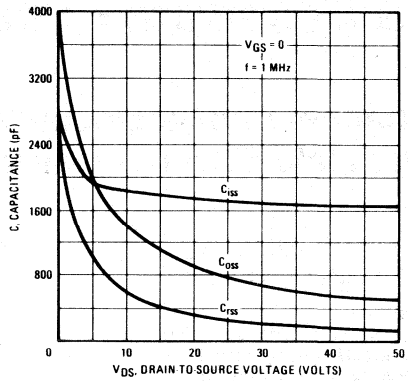


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

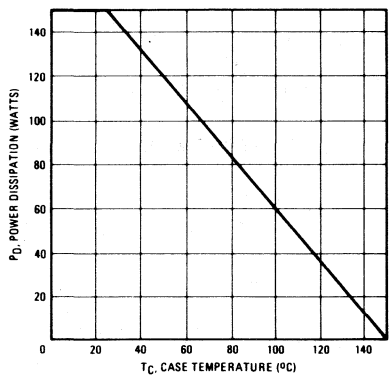


Fig. 11 - Power vs. temperature derating curve.

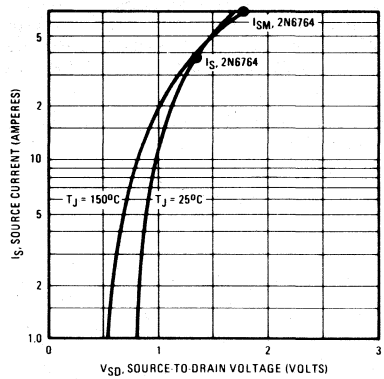


Fig. 12 - Typical body-drain diode forward voltage.

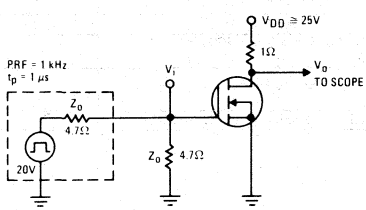


Fig. 13 - Switching time test circuit.

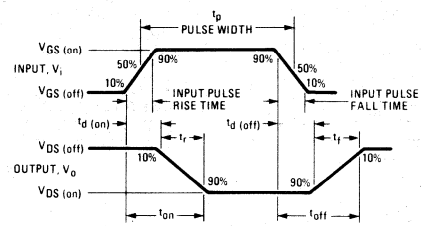


Fig. 14 - Switching time waveforms.

2N6765, 2N6766

File Number **1591**

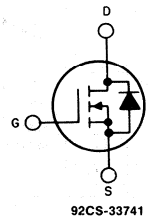
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A and 30 A, 150 V and 200 V
$r_{DS(on)}$ = 0.085 Ω and 0.12 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

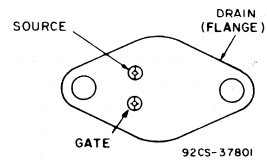
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

The 2N6765 and 2N6766 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6765 and 2N6766 are supplied in the JEDEC TO-204AE steel package.

Absolute Maximum Ratings

Parameter		2N6765	2N6766	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	25*	30*	A
I_D @ T_C = 100°C	Continuous Drain Current	16*	19*	A
I_{DM}	Pulsed Drain Current	50	60	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		50	60	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherside Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6765	150	–	–	V	V_{GS} = 0
		2N6766	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6765	–	–	3.0*	V	V_{GS} = 10V, I_D = 25A
		2N6766	–	–	2.7*	V	V_{GS} = 10V, I_D = 30A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	0.09	0.12*	Ω	V_{GS} = 10V, I_D = 16A
		2N6766	–	0.07	0.085*	Ω	V_{GS} = 10V, I_D = 19A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	–	0.216*	Ω	V_{GS} = 10V, I_D = 16A, T_C = 125°C
		2N6766	–	–	0.153*	Ω	V_{GS} = 10V, I_D = 19A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	15.5	27*	S (℧)	V_{DS} = 15V, I_D = 19A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	450*	800	1200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 95V, I_D = 19A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Typical socket mount

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6765	–	–	25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6766	–	–	30*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6765	–	–	50	A	
		2N6766	–	–	60		
V_{SD}	Diode Forward Voltage ①	2N6765	0.85*	–	1.7*	V	T_C = 25°C, I_S = 25A, V_{GS} = 0
		2N6766	0.9*	–	1.8*	V	T_C = 25°C, I_S = 30A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

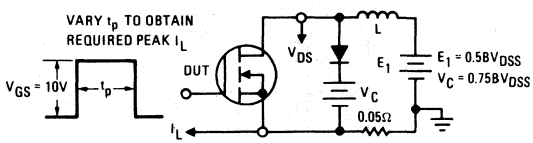


Fig. 1 – Clamped Inductive Test Circuit

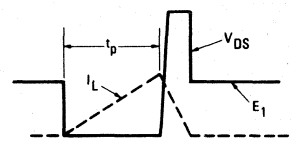


Fig. 2 – Clamped Inductive Waveforms

2N6765, 2N6766

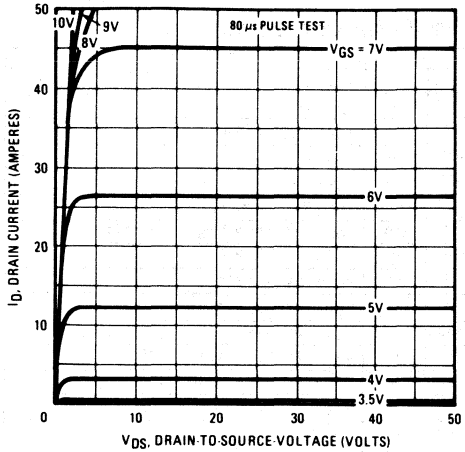


Fig. 3 — Typical Output Characteristics

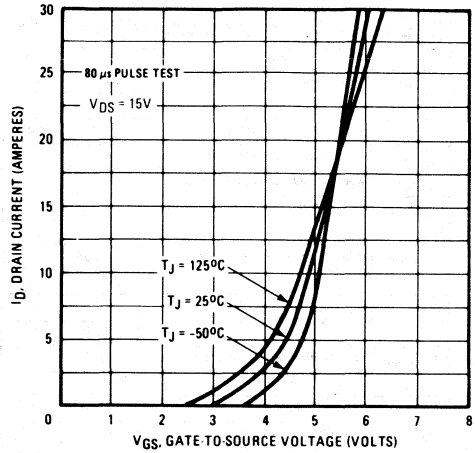


Fig. 4 — Typical Transfer Characteristics

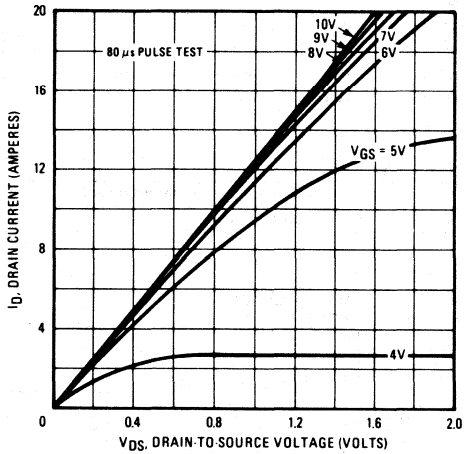


Fig. 5— Typical Saturation Characteristics (2N6765)

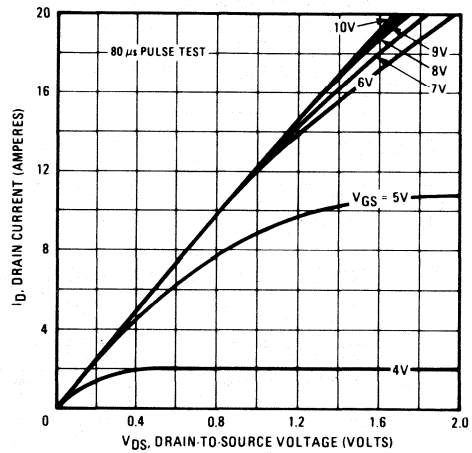


Fig. 6— Typical Saturation Characteristics (2N6766)

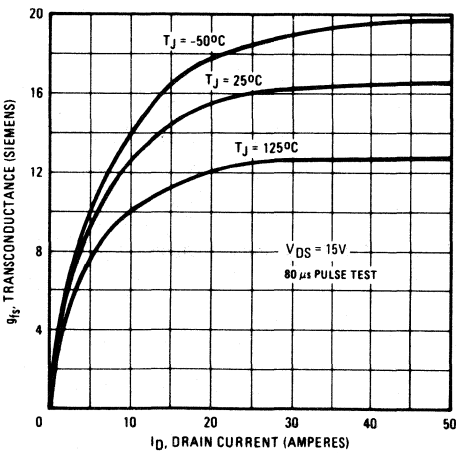


Fig. 7 — Typical Transconductance Vs. Drain Current

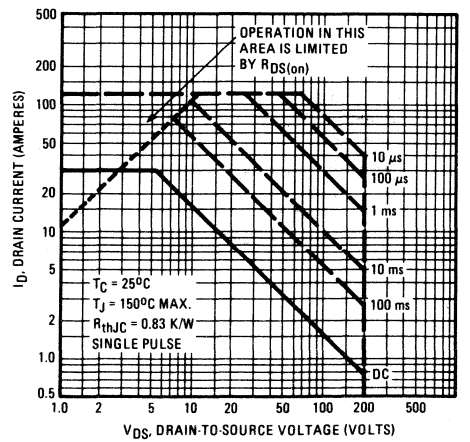


Fig. 8 — Maximum Safe Operating Area

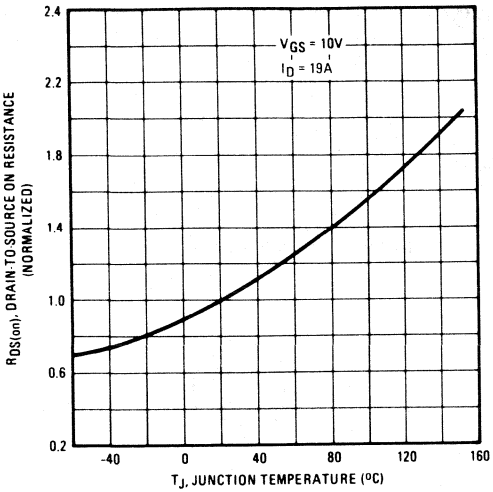


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

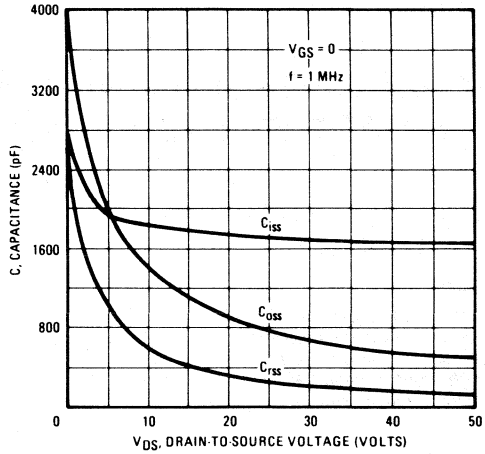


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

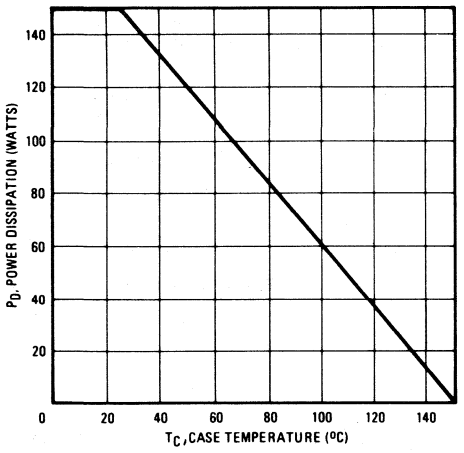


Fig. 11 – Power Vs. Temperature Derating Curve

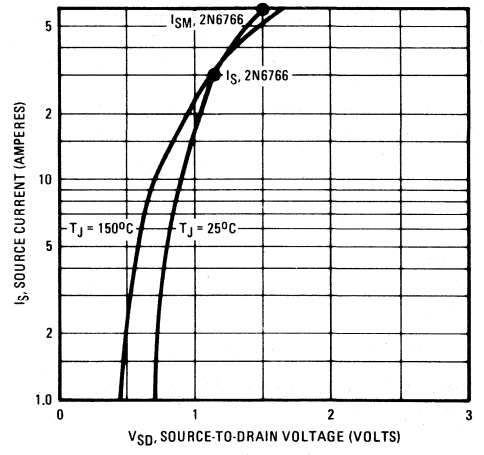


Fig. 12 – Typical Body-Drain Diode Forward Voltage

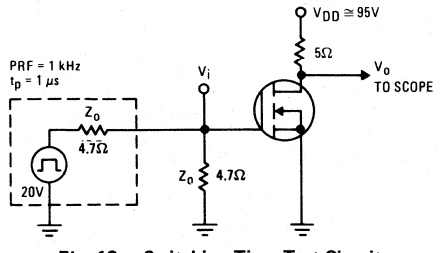


Fig. 13 – Switching Time Test Circuit

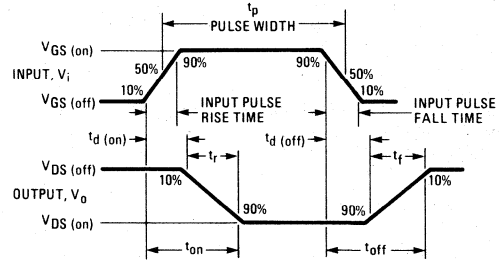


Fig. 14 – Switching Time Waveforms

2N6767, 2N6768

File Number **1898**

Power MOS Field-Effect Transistors

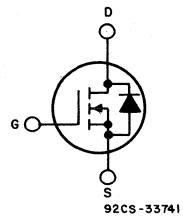
N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

12A and 14A, 350V - 400V
$r_{DS(on)}$ = 0.4Ω and 0.3Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

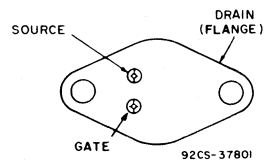


The 2N6767 and 2N6768 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6767 and 2N6768 are supplied in the JEDEC TO-204AA steel package.

TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6767		2N6768	
*DRAIN-SOURCE VOLTAGE	V_{DSS}	350		400	V
*DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	350		400	V
*GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D				
At T_C = 25°C		12		14	A
At T_C = 100°C		7.75		9	A
Pulsed	I_{DM}	20		25	A
*POWER DISSIPATION	P_T				
At T_C = 25°C			150		W
Above T_C = 25°C, Derate Linearly			1.2		W/°C
INDUCTIVE CURRENT, CLAMPED (L = 100μH)	I_{LM}	20		25	A
*OPERATING AND STORAGE TEMPERATURE	T_i, T_{stg}		-55 to +150		°C
*LEAD TEMPERATURE (0.063 in. or 1.6 mm from case for 10 s)	T_L		300		°C

*JEDEC REGISTERED DATA

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6767	350	–	–	V	V_{GS} = 0
		2N6768	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6767	–	–	5.4*	V	V_{GS} = 10V, I_D = 12A
		2N6768	–	–	5.6*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
		2N6768	–	0.25	0.3*	Ω	V_{GS} = 10V, I_D = 9.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
		2N6768	–	–	0.66*	Ω	V_{GS} = 10V, I_D = 9.0A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	8.0*	11.0	24*	S (℧)	V_{DS} = 15V, I_D = 9.0A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 180V, I_D = 9.0A, Z_o = 4.7Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	65*	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	
t_f	Fall Time	ALL	–	–	75*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6767	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6768	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6767	–	–	20	A	
		2N6768	–	–	25		
V_{SD}	Diode Forward Voltage ①	2N6767	0.8*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6768	0.85*	–	1.7*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	25	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

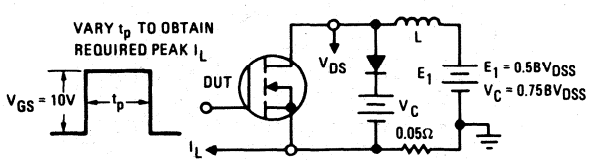


Fig. 1 - Clamped inductive test circuit.

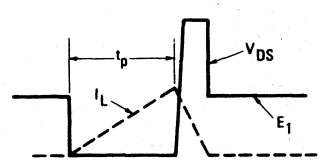


Fig. 2 - Clamped inductive waveforms.

2N6767, 2N6768

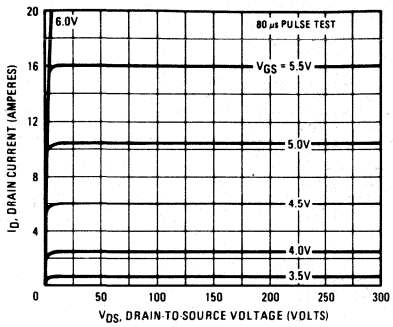


Fig. 3 - Typical output characteristics for both types.

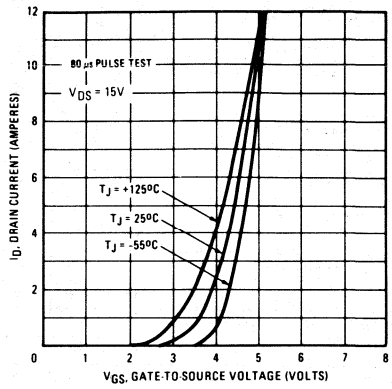


Fig. 4 - Typical transfer characteristics for both types.

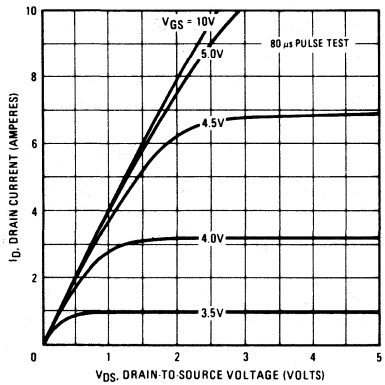


Fig. 5 - Typical saturation characteristics for the 2N6767.

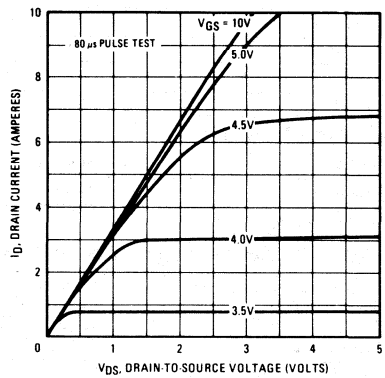


Fig. 6. - Typical saturation characteristics for the 2N6768.

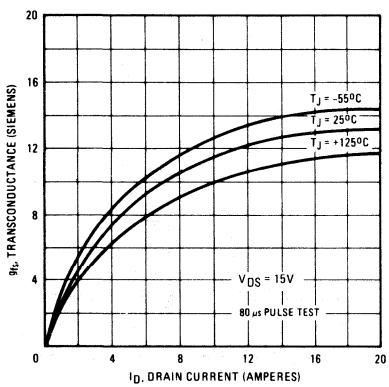


Fig. 7 - Typical transconductance versus drain current for both types.

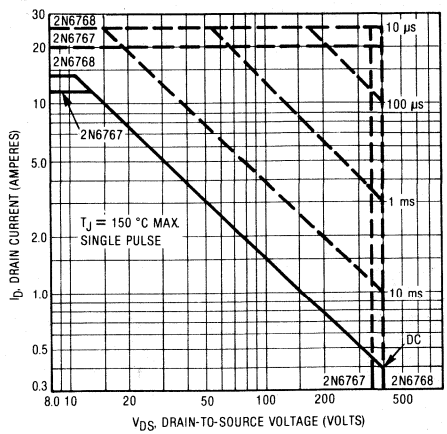


Fig. 8 - Maximum safe operating area for both types.

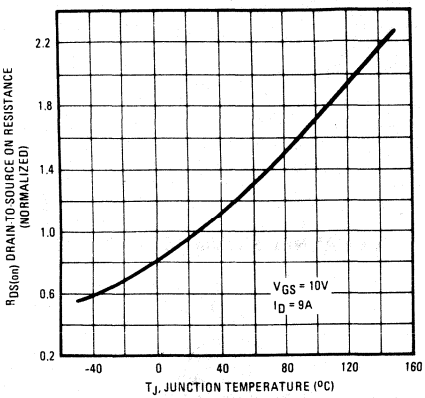


Fig. 9 - Typical normalized on-resistance versus temperature for both types.

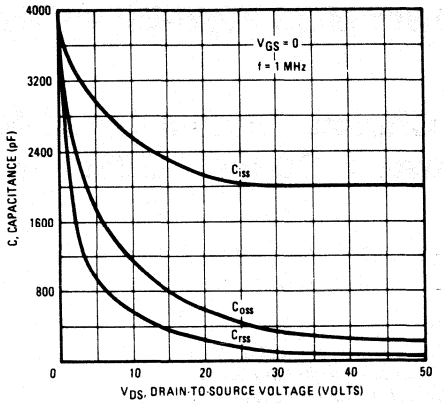


Fig. 10 - Typical capacitance versus drain-to-source voltage for both types.

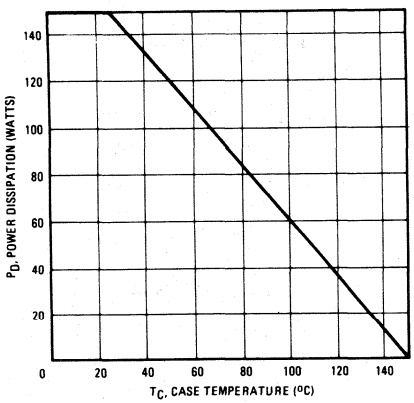


Fig. 11 - Power versus temperature derating curve for both types.

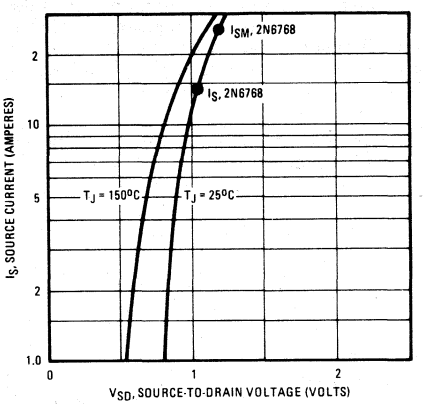


Fig. 12 - Typical body-drain diode forward voltage for both types.

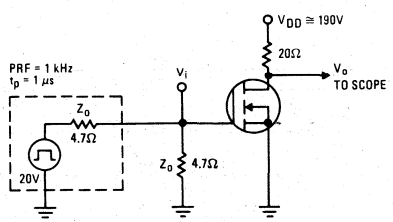


Fig. 13 - Switching time test circuit.

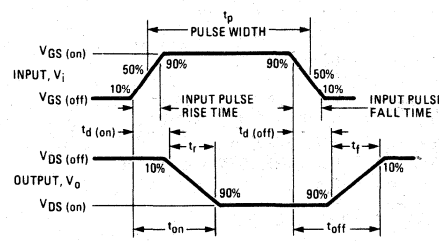


Fig. 14 - Switching time waveforms

2N6769, 2N6770

File Number **1899**

Power MOS Field-Effect Transistors

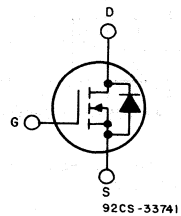
N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

11A and 12A, 450V - 500V
$r_{DS(on)}$ = 0.5Ω and 0.4Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

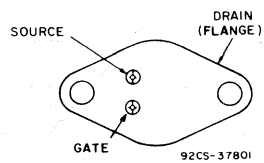


TERMINAL DIAGRAM

The 2N6769 and 2N6770 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6769 and 2N6770 are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6769		2N6770	
*DRAIN-SOURCE VOLTAGE	V_{DSS}	450		500	V
*DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	450		500	V
*GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D				
At T_C = 25°C		11		12	A
At T_C = 100°C		7		7.75	A
Pulsed	I_{DM}	20		25	A
*POWER DISSIPATION	P_T				
At T_C = 25°C			150		W
Above T_C = 25°C, Derate Linearly			1.2		W/°C
INDUCTIVE CURRENT, CLAMPED (L = 100μH)	I_{LM}	20		25	A
*OPERATING AND STORAGE TEMPERATURE	T_i, T_{stg}		-55 to +150		°C
*LEAD TEMPERATURE (0.063 in. or 1.6 mm from case for 10 s)	T_L		300		°C

*JEDEC REGISTERED DATA

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6769	450	–	–	V	V_{GS} = 0
		2N6770	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 25°C to 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6769	–	–	6.0*	V	V_{GS} = 10V, I_D = 11A
		2N6770	–	–	6.0*	V	V_{GS} = 10V, I_D = 12A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6769	–	0.4	0.5*	Ω	V_{GS} = 10V, I_D = 7A
		2N6770	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6769	–	–	1.1*	Ω	V_{GS} = 10V, I_D = 7.0A, T_C = 125°C
		2N6770	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	8.0*	12.0	24*	S (℧)	V_{GS} = 10V I_D = 7.75A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong 210V$, I_D = 7.75A, $Z_o = 4.7\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50*	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	
t_f	Fall Time	ALL	–	–	70*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6769	–	–	11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6770	–	–	12*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6769	–	–	20	A	
		2N6770	–	–	25		
V_{SD}	Diode Forward Voltage ①	2N6769	0.75*	–	1.5*	V	T_C = 25°C, I_S = 11A, V_{GS} = 0
		2N6770	0.80*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1300	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.4	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

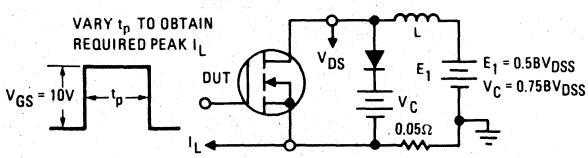


Fig. 1 - Clamped inductive test circuit.

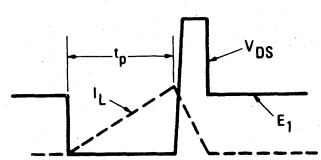


Fig. 2 - Clamped inductive waveforms.

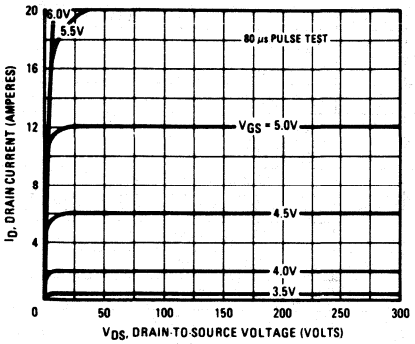


Fig. 3 - Typical output characteristics for both types.

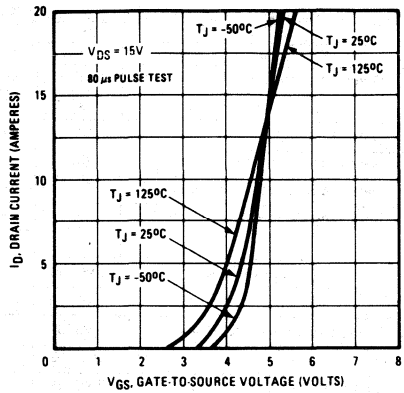


Fig. 4 - Typical transfer characteristics for both types.

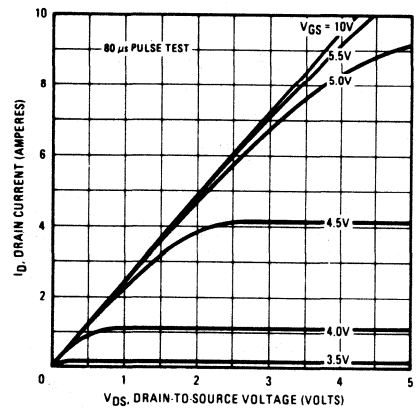


Fig. 5 - Typical saturation characteristics for the 2N6769.

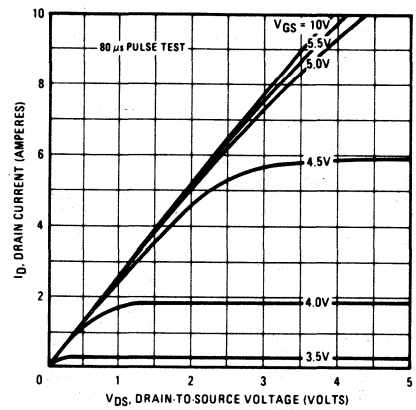


Fig. 6. - Typical saturation characteristics for the 2N6770.

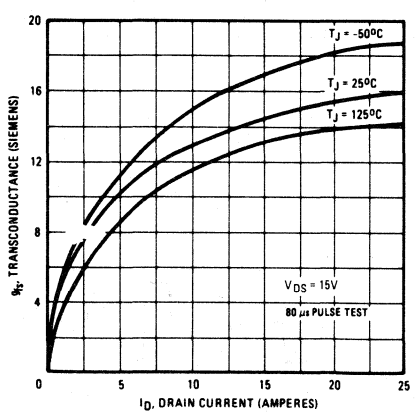


Fig. 7 - Typical transconductance versus drain current for both types.

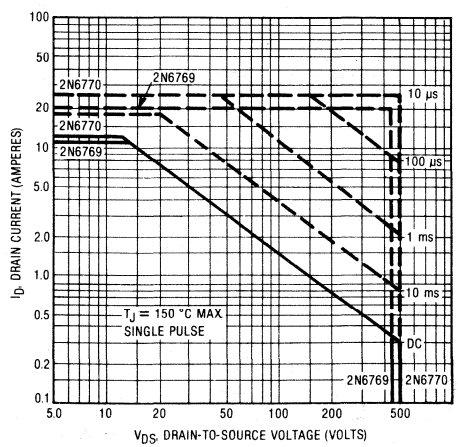


Fig. 8 - Maximum safe operating area for both types.

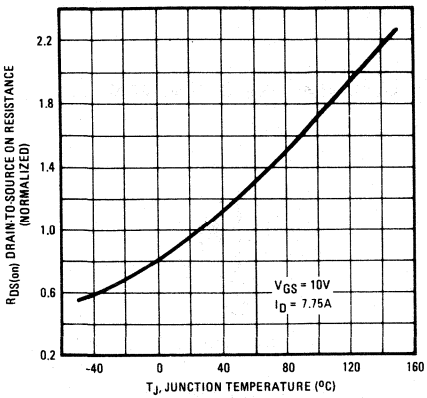


Fig. 9 - Typical normalized on-resistance versus temperature for both types.

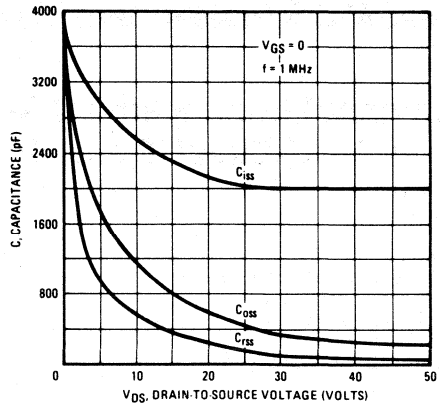


Fig. 10 - Typical capacitance versus drain-to-source voltage for both types.

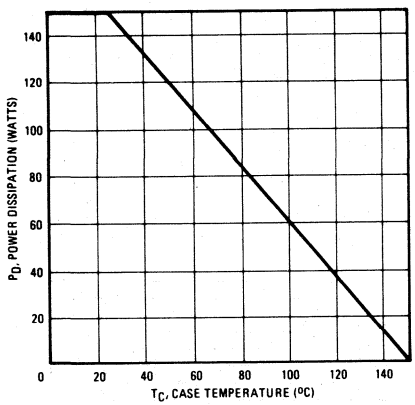


Fig. 11 - Power versus temperature derating curve for both types.

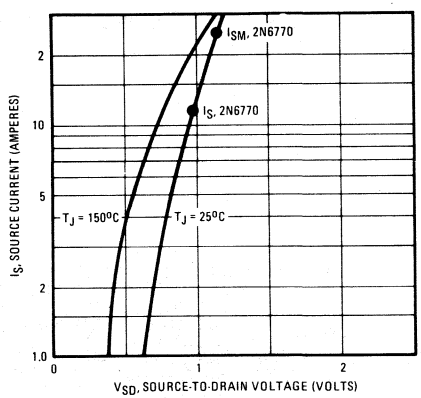


Fig. 12 - Typical body-drain diode forward voltage for both types.

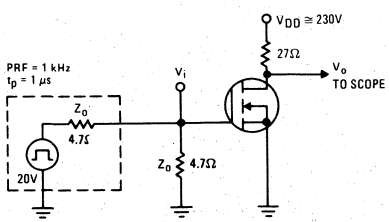


Fig. 13 - Switching time test circuit.

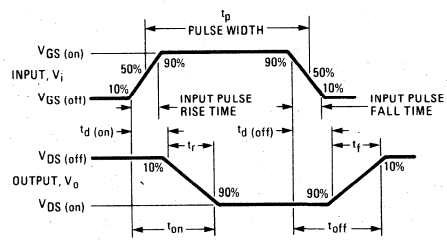


Fig. 14 - Switching time waveforms

2N6782

File Number **1592**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3.5A, 100V

$r_{DS}(on)$ = 0.6 Ω

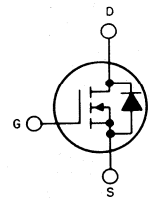
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6782 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6782 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

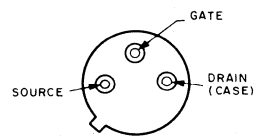
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

Absolute Maximum Ratings

Parameter		2N6782	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.25*	A
I_{DM}	Pulsed Drain Current ③	14*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	3.50*	A
I_{SM}	Pulse Source Current (Body Diode) ③	14*	A
P_D @ T_C = 25°C	Max. Power Dissipation	15* (See Fig. 14)	W
	Linear Derating Factor	0.12* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 14	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	—	—	2.1*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	—	0.5	0.6*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 25°C
		—	—	1.08*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	—	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.0*	1.5	3.0*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	80	100*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	10*	20	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	15*	ns	V_{DD} ≅ 34V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	—	—	25*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	25*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	20*	ns	of operating temperature.)
SOA	Safe Operating Area	15	—	—	W	V_{DS} = 80V, I_D = 188 mA, See Fig. 16.
		15	—	—	W	V_{DS} = 4.28V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	200	ns	T_J = 150°C, I_F = 3.5A, di_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.0	μC	T_J = 150°C, I_F = 3.5A, di_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

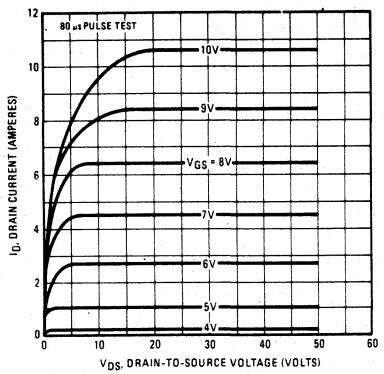


Fig. 1 — Typical Output Characteristics

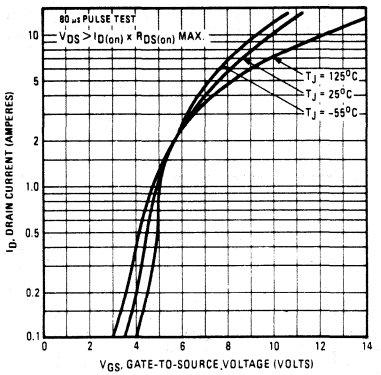


Fig. 2 — Typical Transfer Characteristics

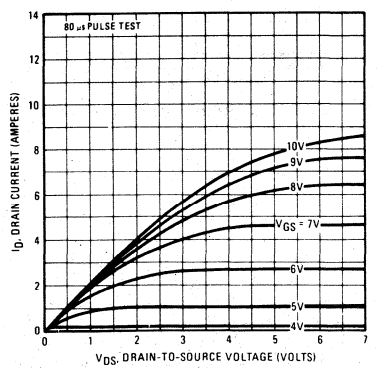


Fig. 3 — Typical Saturation Characteristics

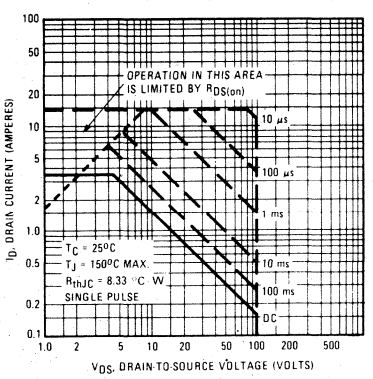


Fig. 4 — Maximum Safe Operating Area

2N6782

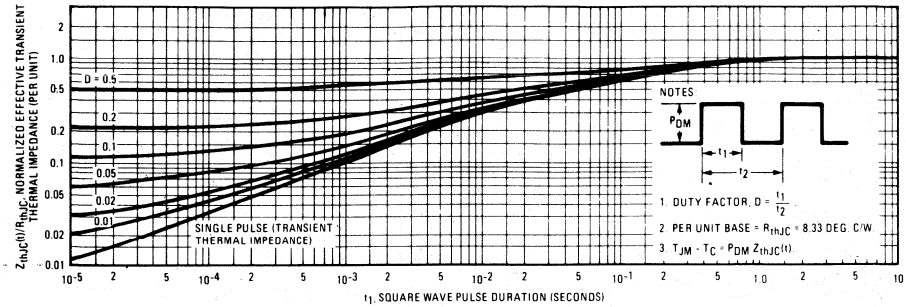


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

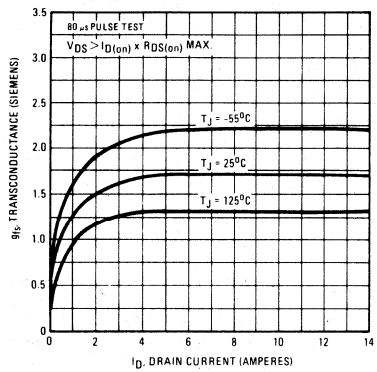


Fig. 6 – Typical Transconductance Vs. Drain Current

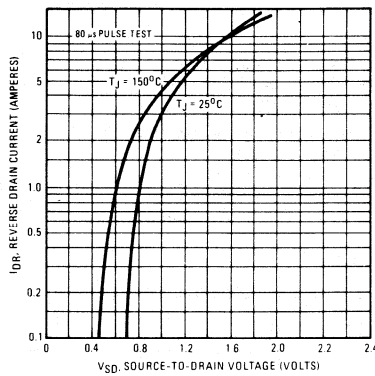


Fig. 7 – Typical Source-Drain Diode Forward Voltage

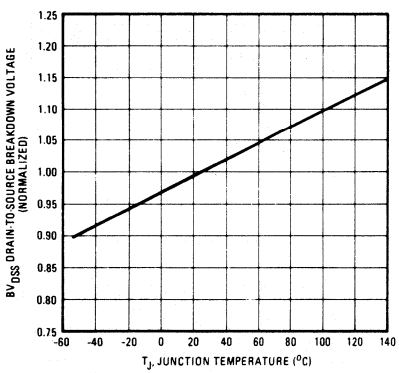


Fig. 8 – Breakdown Voltage Vs. Temperature

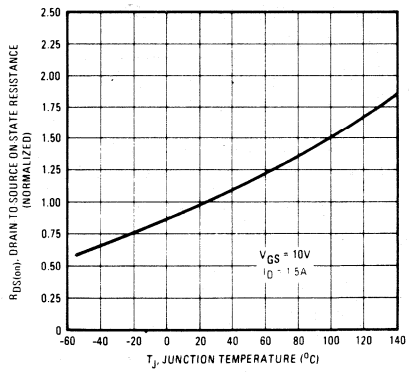


Fig. 9 – Normalized On-Resistance Vs. Temperature

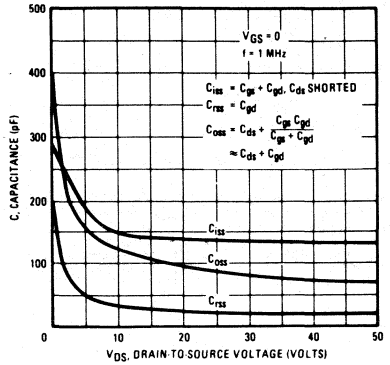


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

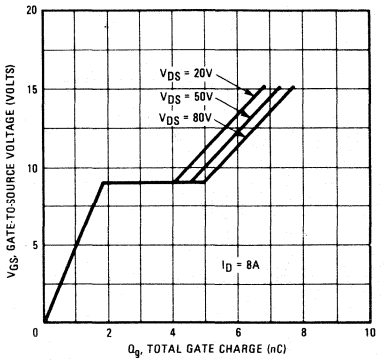


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

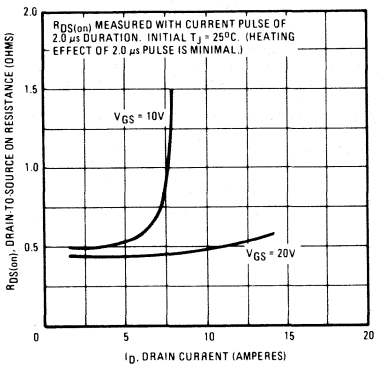


Fig. 12 – Typical On-Resistance Vs. Drain Current

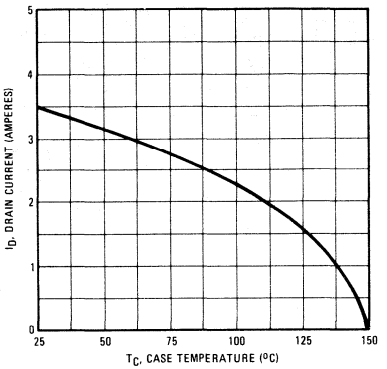


Fig. 13 – Maximum Drain Current Vs. Case Temperature

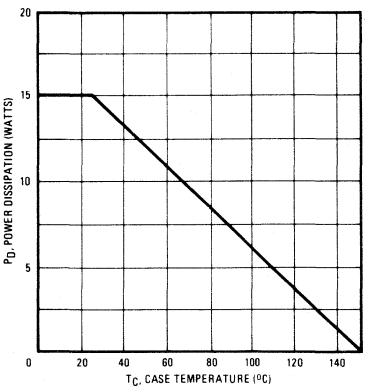
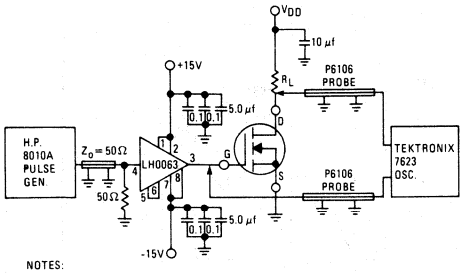
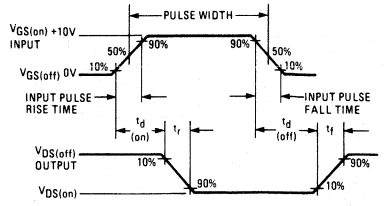


Fig. 14 – Power Vs. Temperature Derating Curve

2N6782

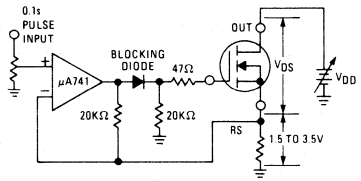


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

File Number **1906**

2N6784

Power MOS Field-Effect Transistors

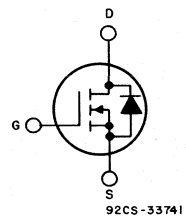
N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

2.25A, 200V
$r_{DS(on)}$ = 1.5Ω

Features:

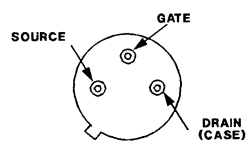
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The 2N6784 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6784 is supplied in the JEDEC TO-205AF metal package.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

*DRAIN-SOURCE VOLTAGE, V_{DS}	200V
*DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ), V_{DGR}	200V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
*DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	2.25A
At T_C = 100°C	1.5A
Pulsed, I_{DM}	9A
*SOURCE CURRENT:	
Continuous, I_S	2.25A
Pulsed, I_{SM}	9A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	15W
Above T_C = 25°C	Derate linearly 0.12 W/°C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	9A
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

2N6784

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	3.37*	V	V_{GS} = 10V, I_D = 2.25A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 25°C
		–	–	2.81*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.7*	–	1.5*	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	0.9*	1.3	2.7*	S(℧)	V_{DS} = 5V, I_D = 1.5A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	20*	60	80*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	16	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	15*	ns	V_{DD} ≅ 75V, I_D = 1.5A, Z_o = 50Ω
t_r	Rise Time	–	–	20*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	30*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	20*	ns	of operating temperature.)
SOA	Safe Operating Area	15	–	–	W	V_{DS} = 160V, I_D = 94 mA, See Fig. 16.
		15	–	–	W	V_{DS} = 6.67V, I_D = 2.25A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	290	ns	T_J = 150°C, I_F = 2.25A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	2.0	μC	T_J = 150°C, I_F = 2.25A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

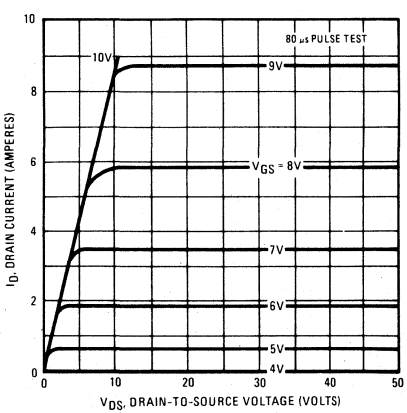


Fig. 1 - Typical output characteristics.

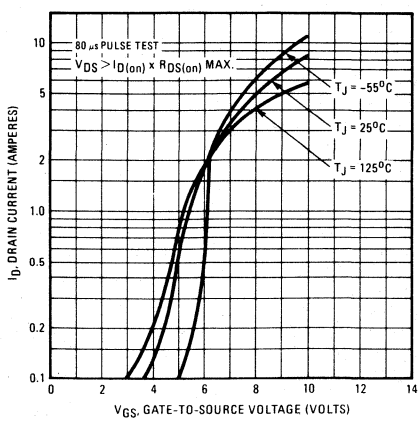


Fig. 2 - Typical transfer characteristics.

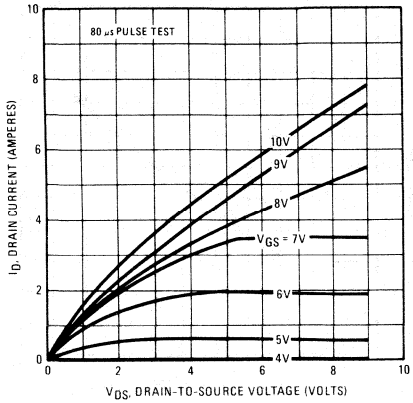


Fig. 3 - Typical saturation characteristics.

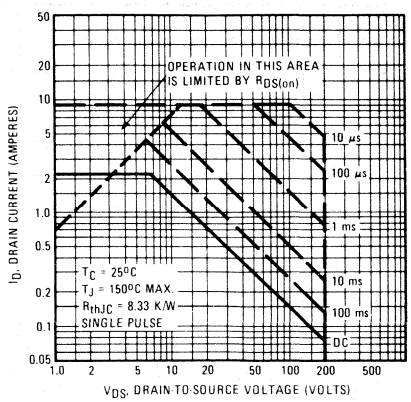


Fig. 4 - Maximum safe operating area.

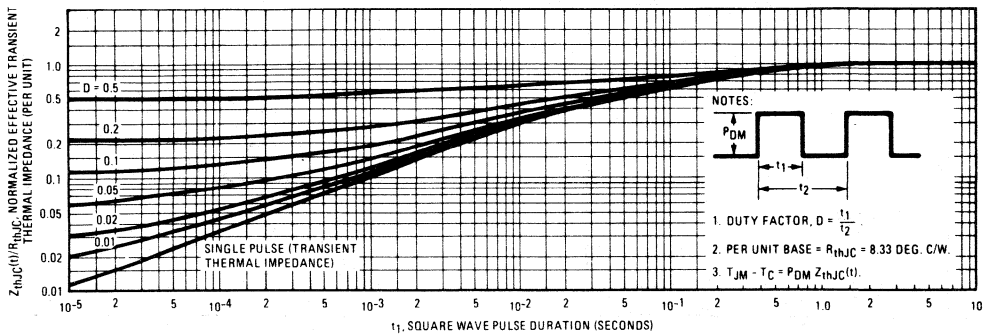


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

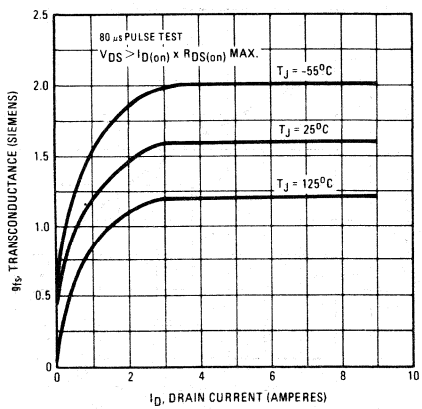


Fig. 6 - Typical transconductance versus drain current.

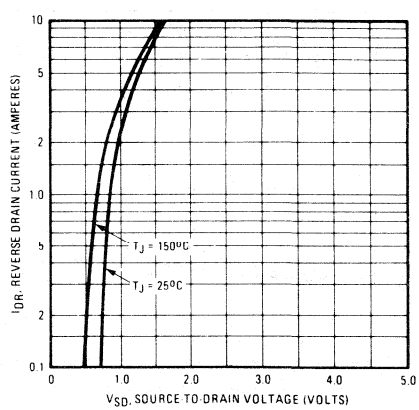


Fig. 7 - Typical source-drain diode forward voltage.

2N6784

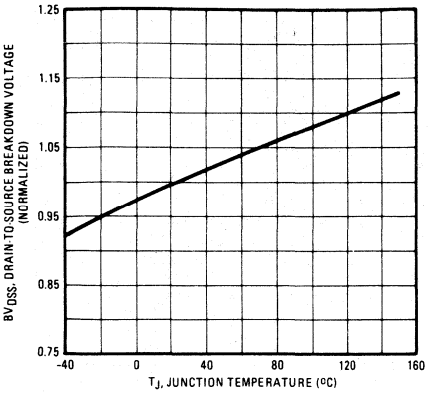


Fig. 8 - Breakdown voltage versus temperature.

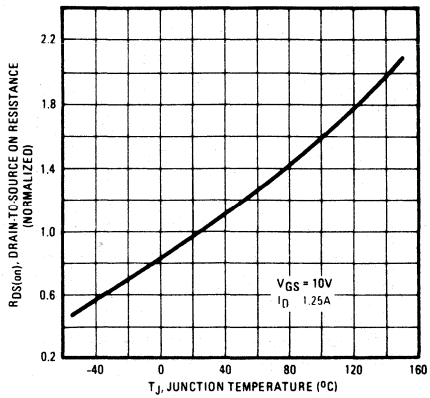


Fig. 9 - Typical normalized on-resistance versus temperature.

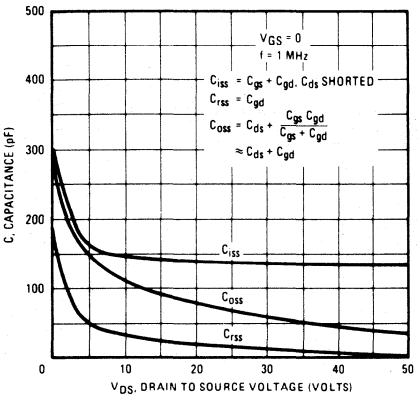


Fig. 10 - Typical capacitance versus drain-to-source voltage.

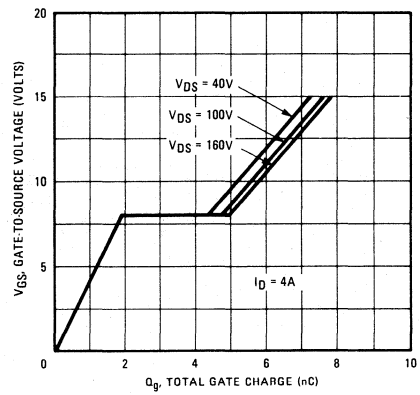


Fig. 11 - Typical gate charge versus gate-to-source voltage.

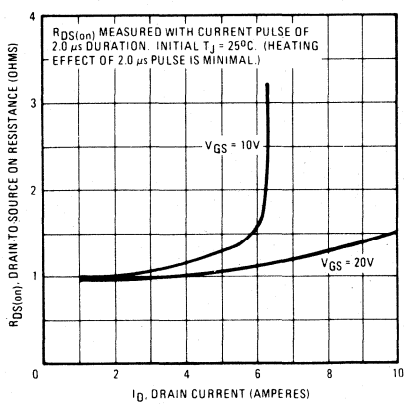


Fig. 12 - Typical on-resistance versus drain current.

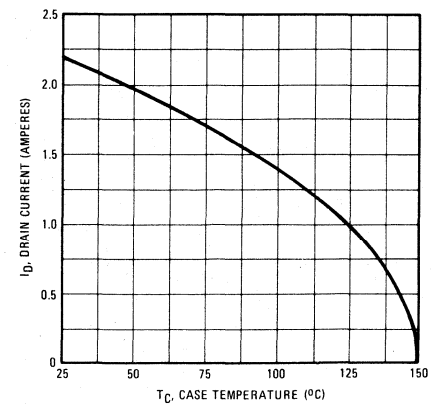


Fig. 13 - Maximum drain current versus case temperature.

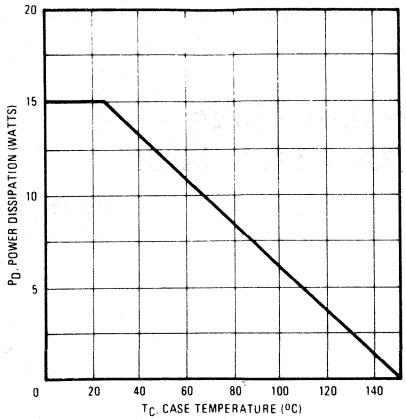
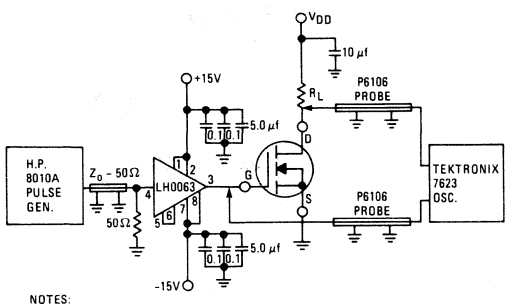
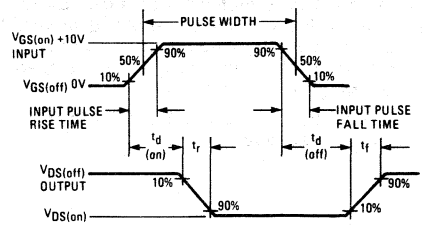


Fig. 14 - Power versus temperature derating curve.

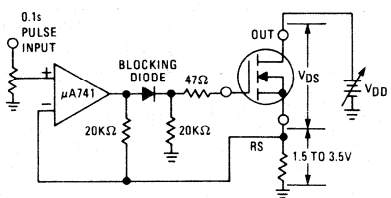


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

2N6786

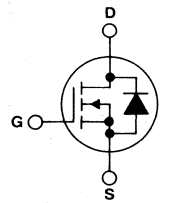
File Number **2207**

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

1.25 A, 400 V
$r_{DS}(on)$: 3.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



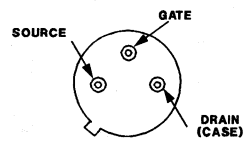
92CS-43357

TERMINAL DIAGRAM

The 2N6786 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6786 is supplied in the JEDEC TO-205AF (Low-Profile TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

*DRAIN-SOURCE VOLTAGE, V_{DS}	400 V
*DRAIN-GATE VOLTAGE (R_{GS} = 20 kΩ), V_{DGR}	400 V
*GATE-SOURCE VOLTAGE, V_{GS}	±20 V
*DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	1.25 A
At T_C = 100°C	0.8 A
Pulsed, I_{DM}	5.5 A
*SOURCE CURRENT:	
Continuous, I_S	1.25 A
Pulsed, I_{SM}	5.5 A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	15 W
Above T_C = 25°C	Derate linearly 0.12 W/°C
INDUCTIVE CURRENT, Clamped (L = 100 μH), I_{LM}	5.5 A
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

ELECTRICAL CHARACTERISTICS at T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	400*	—	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.5 mA	2.0*	—	4.0*	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	—	100*	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	—	—	100*	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	—	—	250*	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_C = 125°C	—	—	1000*	μA
On-State Voltage[a]	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 1.25 A	—	—	4.5*	V
Static Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 0.8 A, T_A = 25°C	—	3.3	3.6*	Ω
		V_{GS} = 10 V, I_D = 0.8 A, T_A = 125°C	—	—	7.92*	Ω
Diode Forward Voltage[a]	V_{SD}	T_C = 25°C, I_S = 1.25 A, V_{GS} = 0 V	0.6*	—	1.4*	V
Forward Transconductance[a]	g_{fs}	V_{DS} = 5 V, I_D = 0.8 A	0.7*	1.2	2.1*	S(℧)
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	60*	135	200*	pF
Output Capacitance	C_{oss}	See Fig. 10	15*	35	50*	pF
Reverse Transfer Capacitance	C_{rss}		2*	8	15*	pF
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} \cong$ 170 V, I_D = 0.8 A, Z_O = 50 Ω	—	—	15*	ns
Rise Time	t_r	See Fig. 15. (MOSFET switching	—	—	20*	ns
Turn-Of Delay Time	$t_{d(off)}$	times are essentially independent	—	—	35*	ns
Fall Time	t_f	of operating temperature.)	—	—	30*	ns
Safe Operating Area	SOA	V_{DS} = 200 V, I_D = 75 mA, See Fig. 16.	15	—	—	W
		V_{DS} = 12 V, I_D = 1.25 A, See Fig. 16.	15	—	—	W

THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$		—	—	8.33*	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	175	°C/W

SOURCE-DRAIN DIODE SWITCHING CHARACTERISTICS (TYPICAL)

Reverse Recovery Time	t_{rr}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	380	ns
Reverse Recovered Charge	Q_{RR}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	2.7	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value.

[a]Pulse Test: Pulse width ≤ 300 μs, duty cycle ≤ 2%.

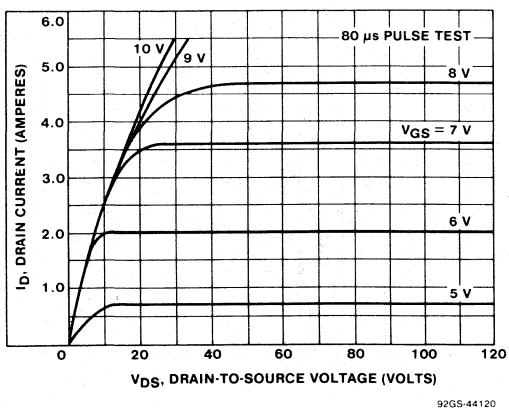


Fig. 1 - Typical output characteristics.

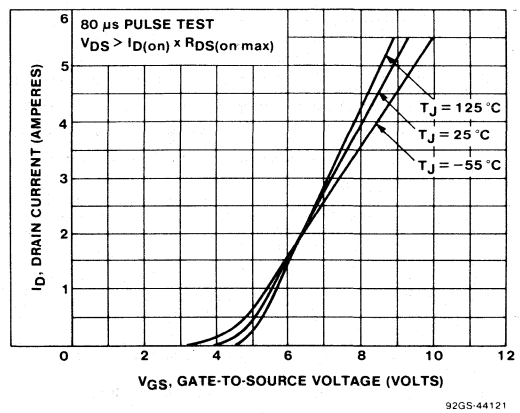


Fig. 2 - Typical transfer characteristics.

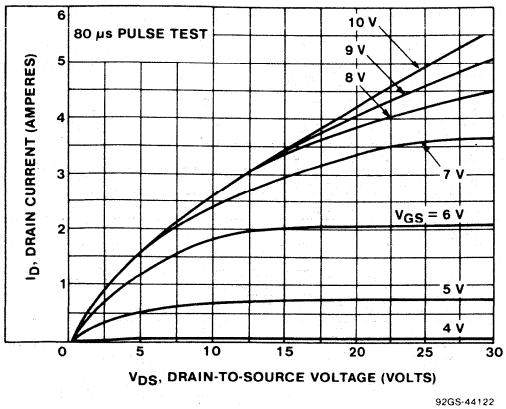


Fig. 3 - Typical saturation characteristics.

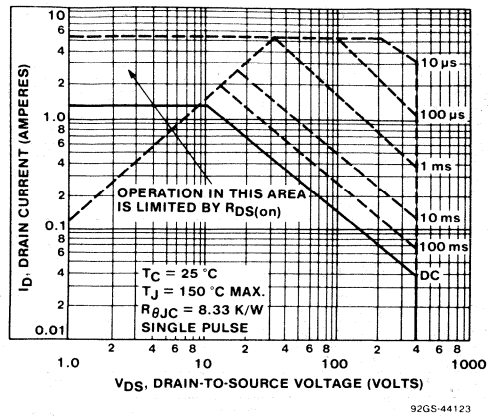


Fig. 4 - Maximum safe operating area.

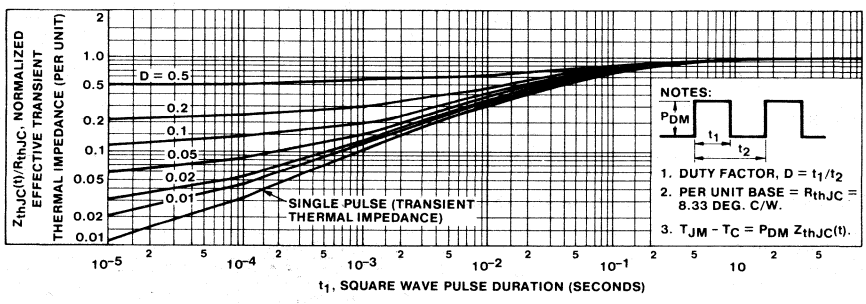


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

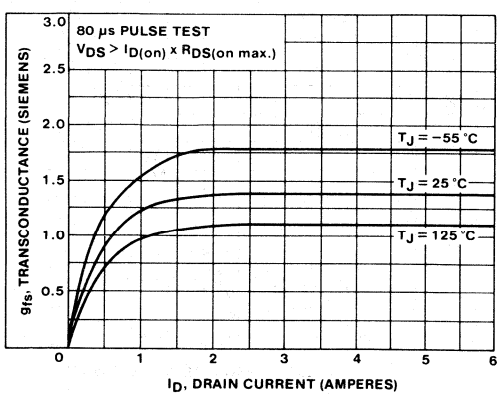


Fig. 6 - Typical transconductance vs. drain current.

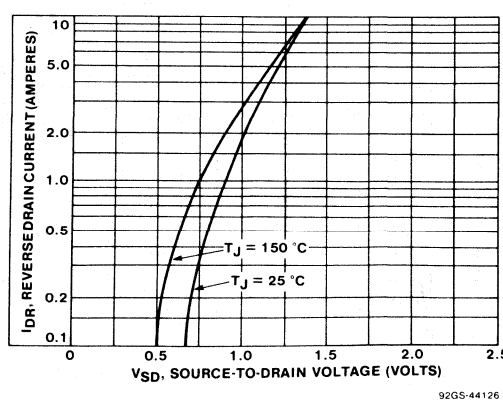


Fig. 7 - Typical source-drain diode forward voltage.

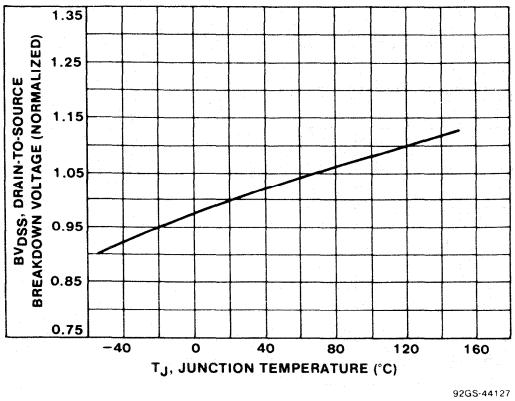


Fig. 8 - Breakdown voltage vs. temperature.

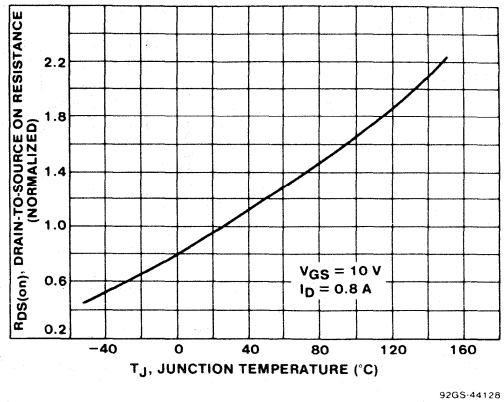


Fig. 9 - Normalized on-resistance vs. temperature.

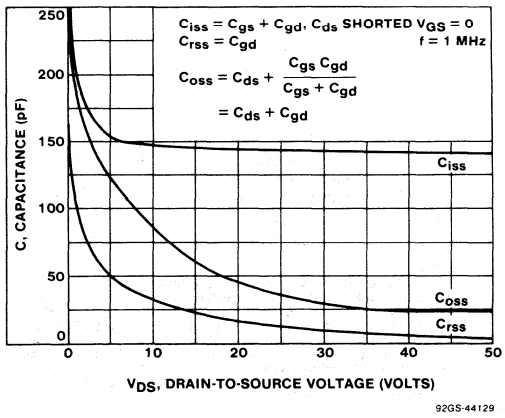


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

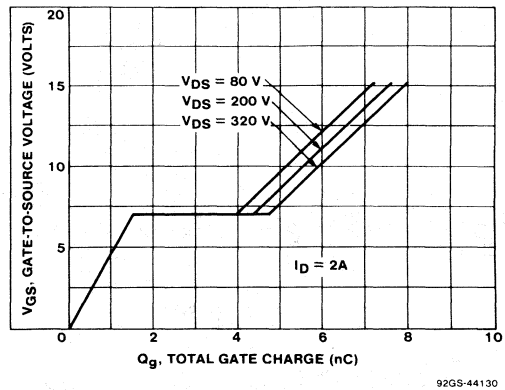


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

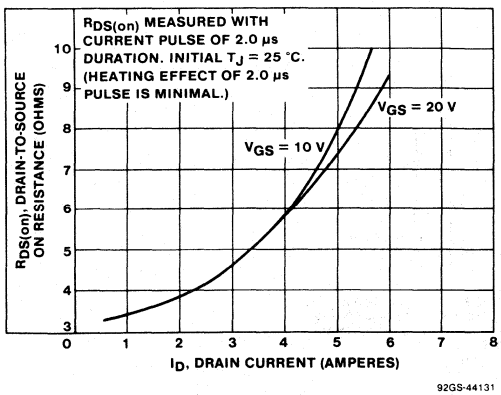


Fig. 12 - Typical on-resistance vs. drain current.

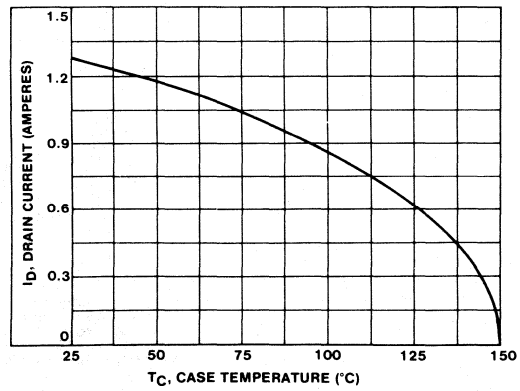


Fig. 13 - Maximum drain current vs. case temperature.

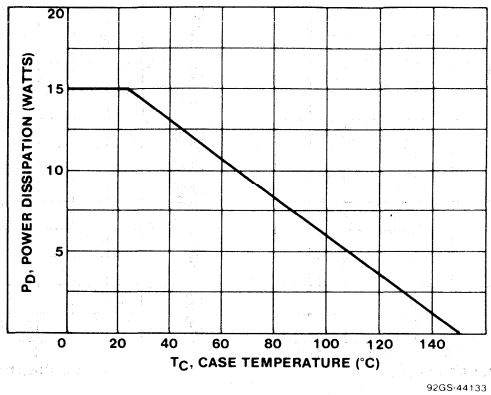
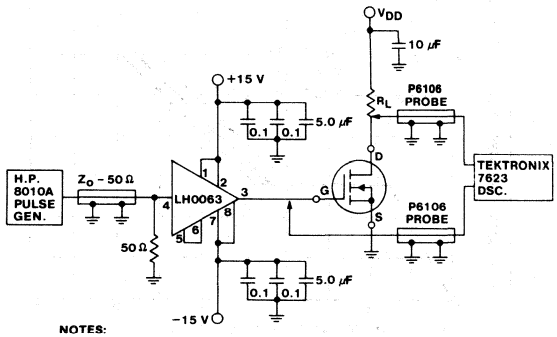


Fig. 14 - Power vs. temperature derating curve.



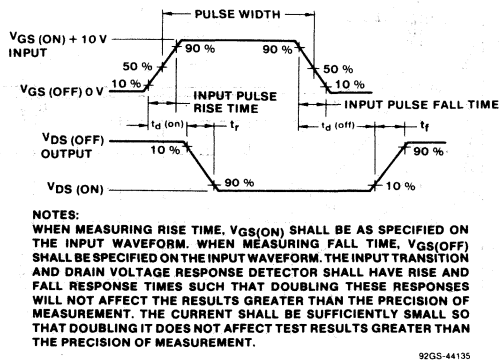


Fig. 15 - Switching time test circuit.

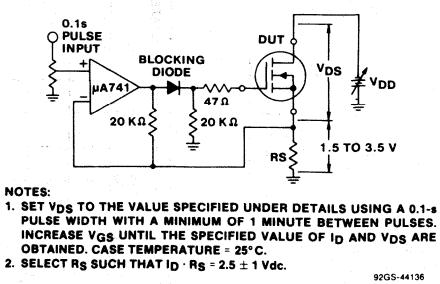


Fig. 16 - Safe operating test circuit.

File Number **1593**

2N6788

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

6.0A, 100V

$r_{DS}(on)$ = 0.30 Ω

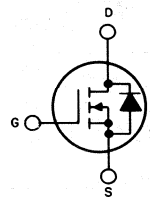
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6788 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6788 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

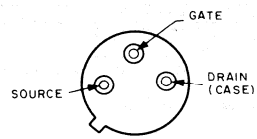
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

Absolute Maximum Ratings

Parameter		2N6788	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5*	A
I_{DM}	Pulsed Drain Current ③	24*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	6.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	24*	A
P_D @ T_C = 25°C	Max. Power Dissipation	20* (See Fig. 14)	W
	Linear Derating Factor	0.16* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 24	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

2N6788

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	2.10*	V	V_{GS} = 10V, I_D = 6.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.25	0.30*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 25°C
		–	–	0.54*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.8*	–	1.8*	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.5*	2.9	4.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	200	400*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	50	100*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 35V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	–	–	70*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	70*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 80V, I_D = 250 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 3.3V, I_D = 60A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	C W	
R_{thJA}	Junction-to-Ambient	–	–	175	C W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	230	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.2	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

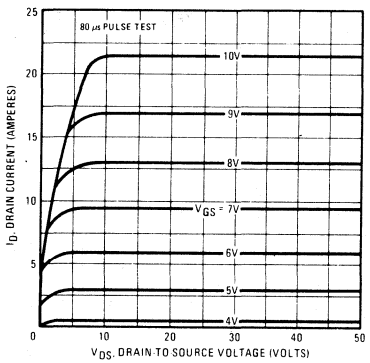


Fig. 1 – Typical Output Characteristics

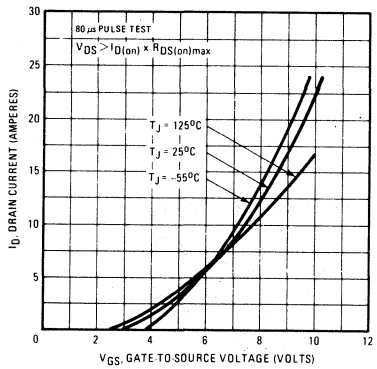


Fig. 2 – Typical Transfer Characteristics

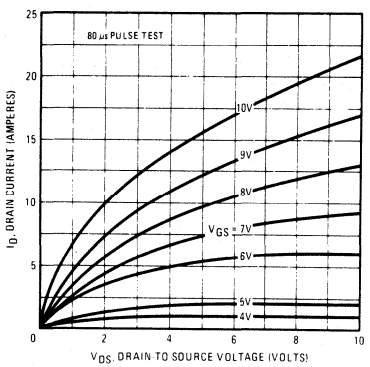


Fig. 3 – Typical Saturation Characteristics

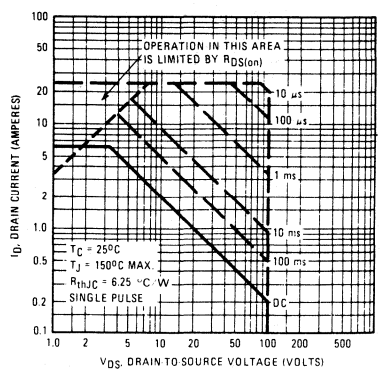


Fig. 4 – Maximum Safe Operating Area

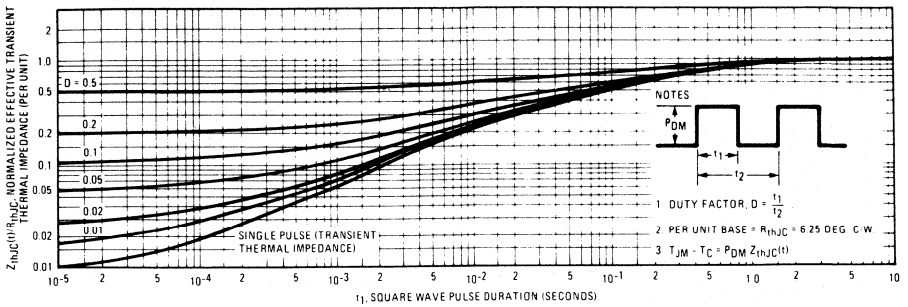


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

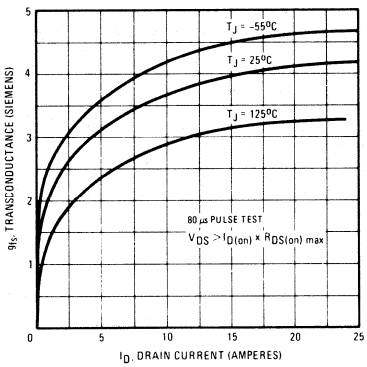


Fig. 6 – Typical Transconductance Vs. Drain Current

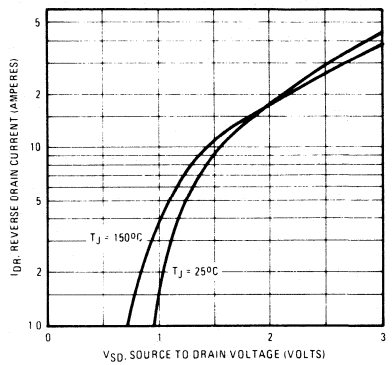


Fig. 7 – Typical Source-Drain Diode Forward Voltage

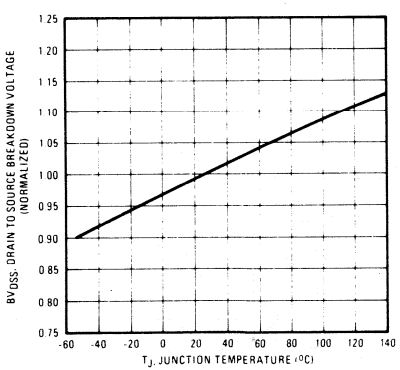


Fig. 8 – Breakdown Voltage Vs. Temperature

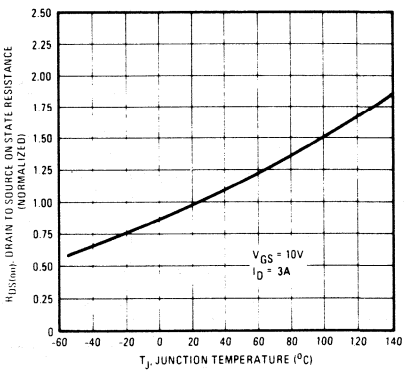


Fig. 9 – Normalized On-Resistance Vs. Temperature

2N6788

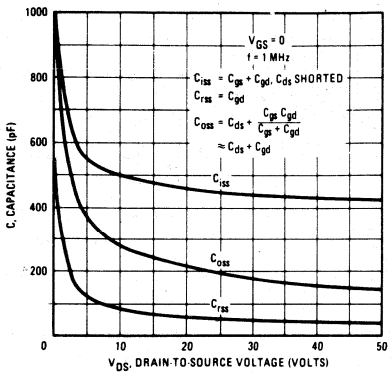


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

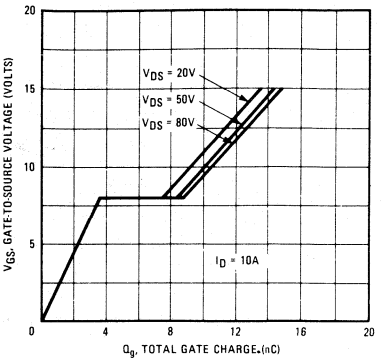


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

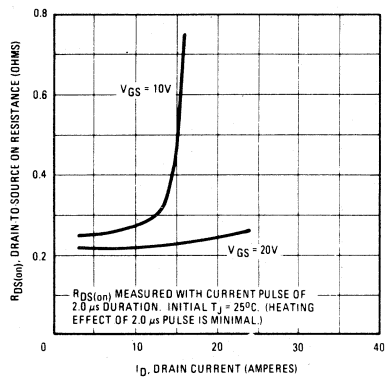


Fig. 12 – Typical On-Resistance Vs. Drain Current

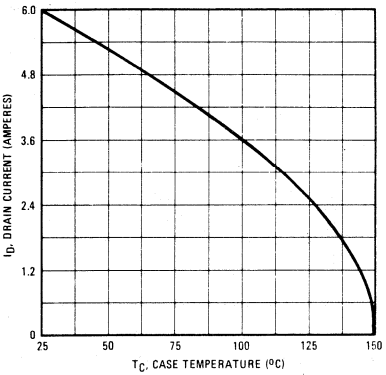


Fig. 13 – Maximum Drain Current Vs. Case Temperature

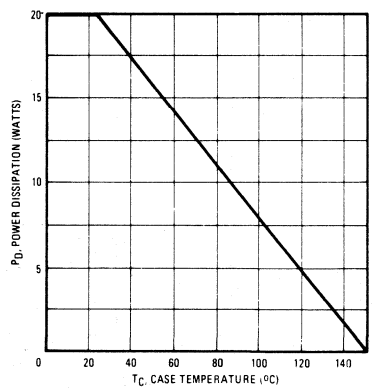
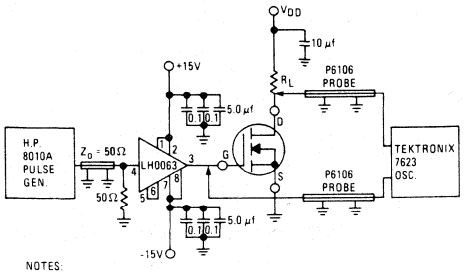
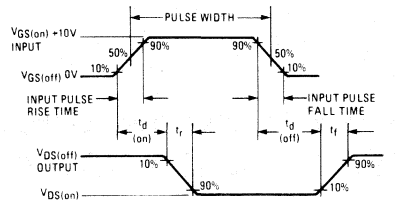


Fig. 14 – Power Vs. Temperature Derating Curve

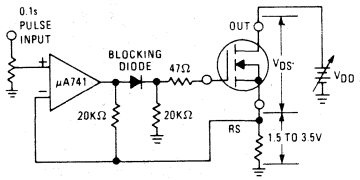


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

2N6790

File Number **1900**

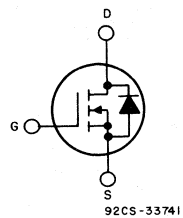
N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

3.5 A, 200V
$r_{DS(on)}$ = 0.8Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

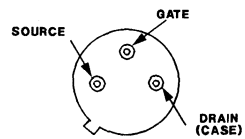


TERMINAL DIAGRAM

The 2N6790 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6790 is supplied in the JEDEC TO-205AF metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

*DRAIN-SOURCE VOLTAGE, V_{DSS}	200V
*DRAIN-GATE VOLTAGE, (R_{GS} = 20 KΩ), V_{DGR}	200V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	3.5A
At T_C = 100°C	2.25A
Pulsed, I_{DM}	14A
*SOURCE CURRENT:	
Continuous, I_S	3.5A
Pulsed, I_{SM}	14A
*POWER DISSIPATION, P_T	
At T_C = 25°C	20W
Above T_C = 25°C	Derate Linearly 0.16 W/°C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	14A
*OPERATING AND STORAGE TEMPERATURE, T_i, T_{stg}	−55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	2.8*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	0.50	0.80*	Ω	V_{GS} = 10V, I_D = 2.25A, T_A = 25°C
		–	–	1.50*	Ω	V_{GS} = 10V, I_D = 2.25A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.7*	–	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.5*	2.25	4.5*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	60*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	15*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	$V_{DD} \cong$ 74V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	–	–	50*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	50*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	50*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 160V, I_D = 125 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 5.7V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	350	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	2.3	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

aPulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

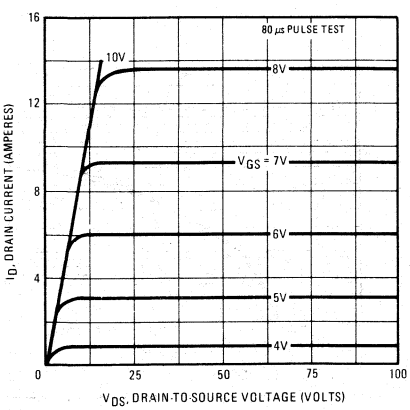


Fig. 1 - Typical output characteristics.

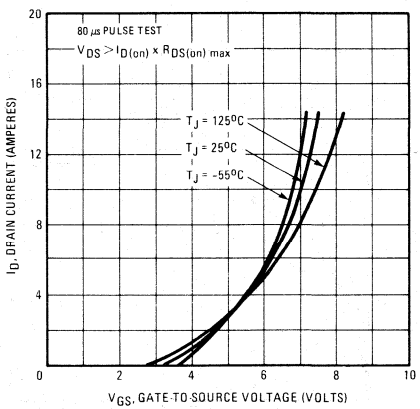


Fig. 2 - Typical transfer characteristics.

2N6790

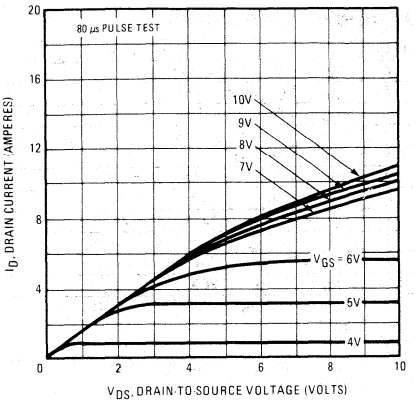


Fig. 3 - Typical saturation characteristics.

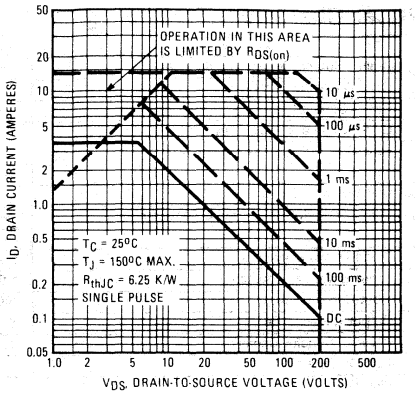


Fig. 4 - Maximum safe operating area.

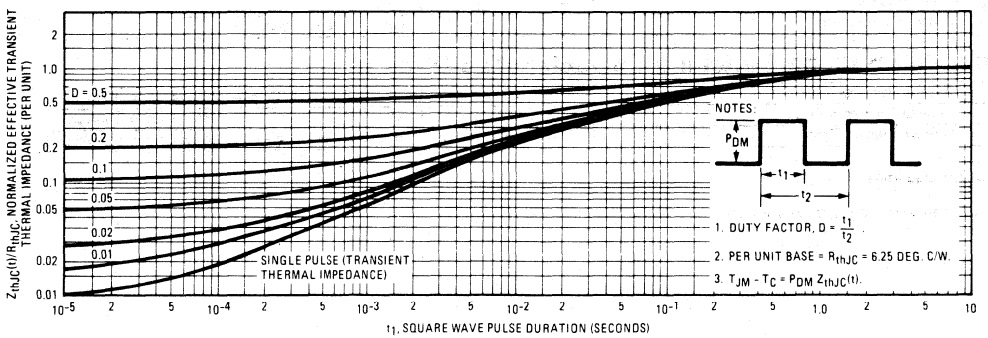


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

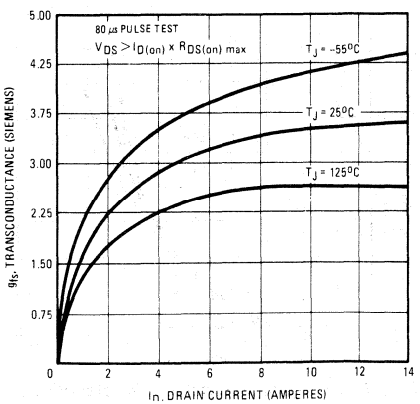


Fig. 6 - Typical transconductance versus drain current.

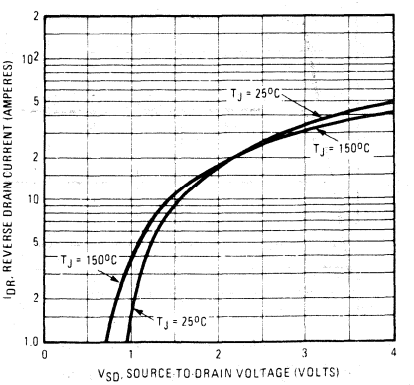


Fig. 7 - Typical source-drain diode forward voltage.

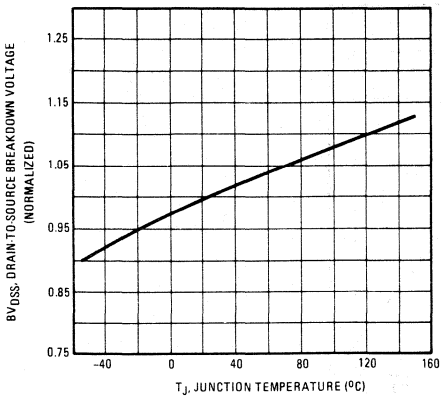


Fig. 8 - Breakdown voltage versus temperature.

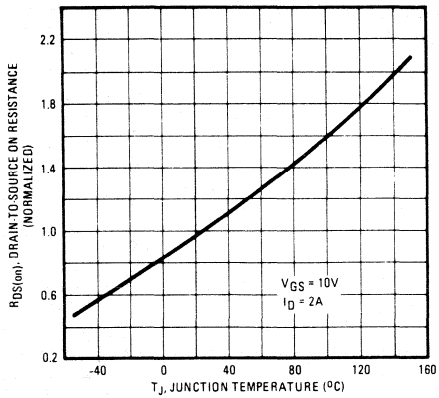


Fig. 9 - Typical normalized on-resistance versus temperature.

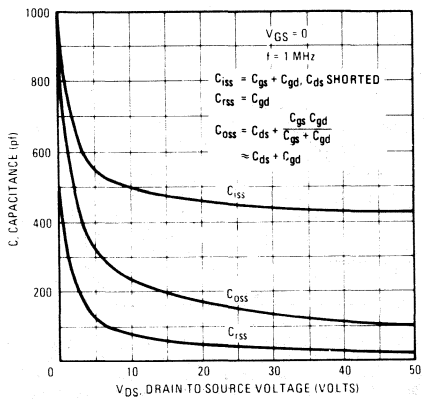


Fig. 10 - Typical capacitance versus drain-to-source voltage.

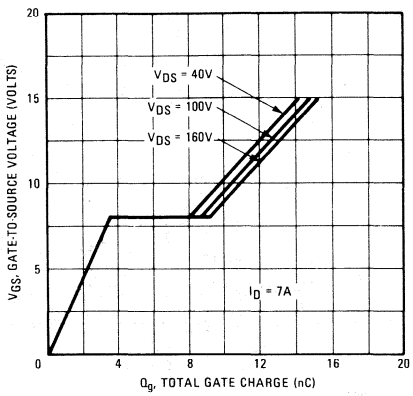


Fig. 11 - Typical gate charge versus gate-to-source voltage.

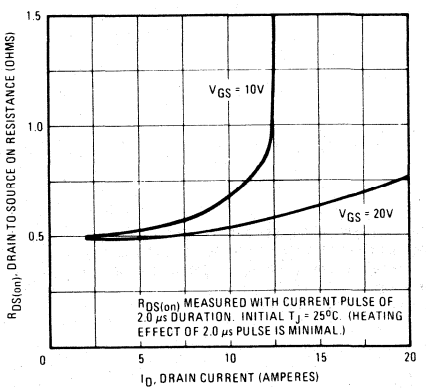


Fig. 12 - Typical on-resistance versus drain current.

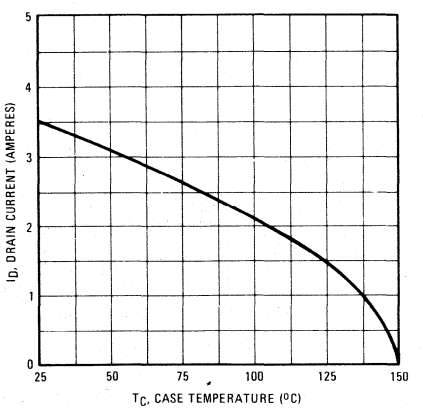


Fig. 13 - Maximum drain current versus case temperature.

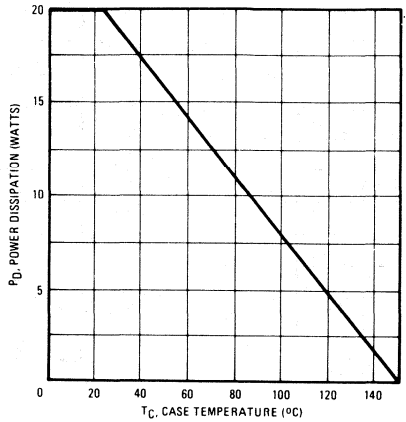


Fig. 14 - Power versus temperature derating curve.

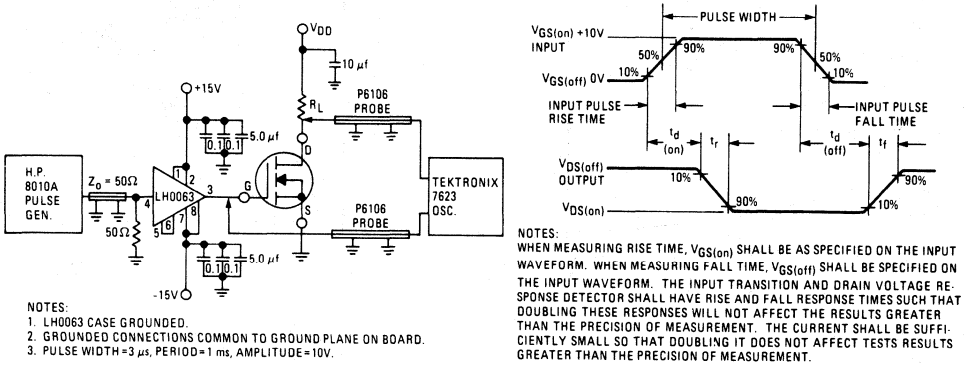
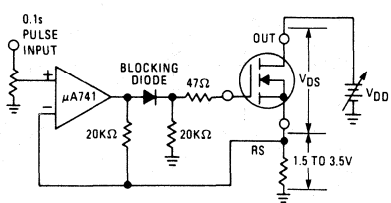


Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating area test circuit.

File Number **1901**

2N6792

Power MOS Field-Effect Transistors

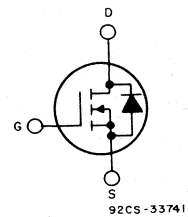
N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

2 A, 400V
$r_{DS(on)}$ = 1.8Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

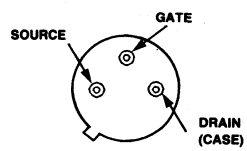
N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

The 2N6792 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6792 is supplied in the JEDEC TO-205AF metal package.



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

*DRAIN-SOURCE VOLTAGE, V_{DSS}	400V
*DRAIN-GATE VOLTAGE, R_{GS} = 20 KΩ), V_{DGR}	400V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	2A
At T_C = 100°C	1.25A
Pulsed, I_{DM}	10A
*SOURCE CURRENT:	
Continuous, I_S	2A
Pulsed, I_{SM}	10A
*POWER DISSIPATION, P_T	
At T_C = 25°C	20W
Above T_C = 25°C	Derate Linearly 0.16 W/°C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	10A
*OPERATING AND STORAGE TEMPERATURE, T_i, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

2N6792

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage [a]	–	–	3.6*	V	V_{GS} = 10V, I_D = 2.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance [a]	–	1.50	1.80*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 25°C
		–	–	4.00*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 125°C
V_{SD}	Diode Forward Voltage [a]	0.6*	–	1.4*	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance [a]	1.0*	2.0	3.0*	S(℧)	V_{DS} = 5V, I_D = 1.25A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	20	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 175V, I_D = 1.25A, Z_o = 50Ω
t_r	Rise Time	–	–	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	60*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	–	–	35*	ns	
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 200V, I_D = 100 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 10V, I_D = 2.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	450	ns	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.1	μC	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

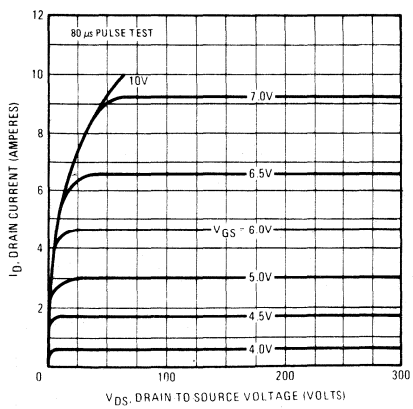


Fig. 1 - Typical output characteristics.

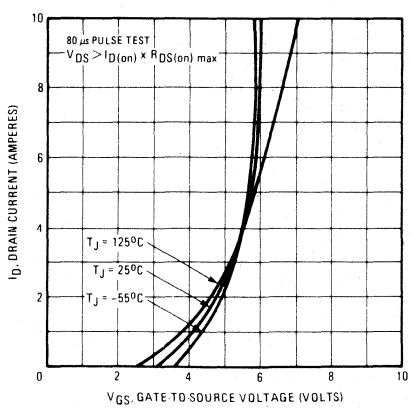


Fig. 2 - Typical transfer characteristics.

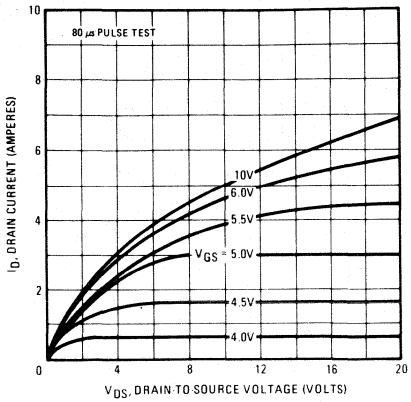


Fig. 3 - Typical saturation characteristics.

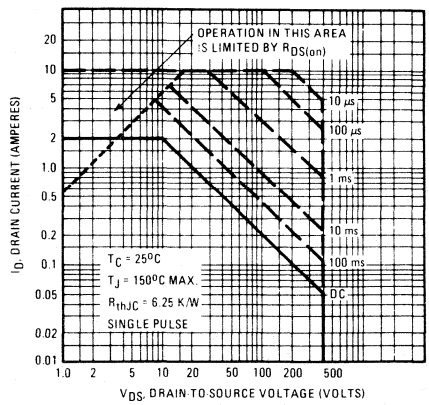


Fig. 4 - Maximum safe operating area.

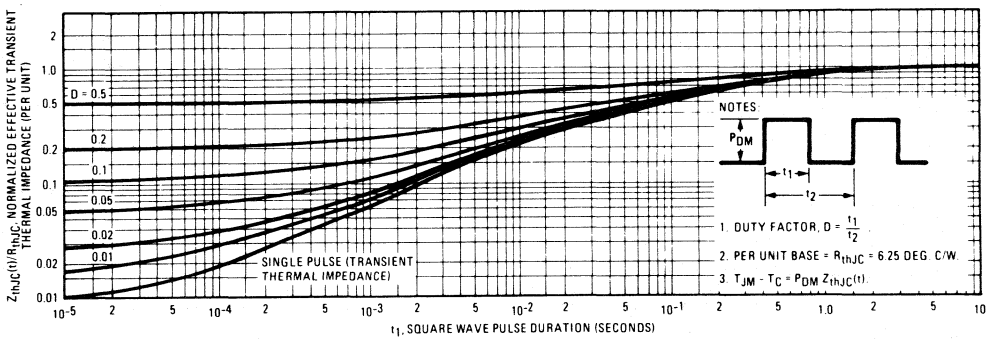


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

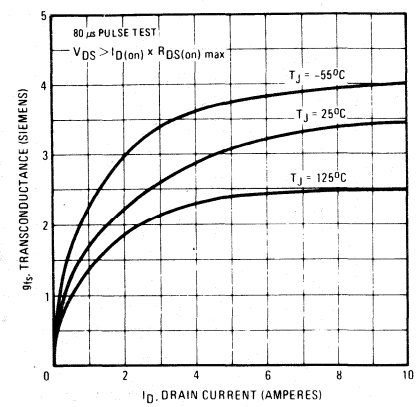


Fig. 6 - Typical transconductance versus drain current.

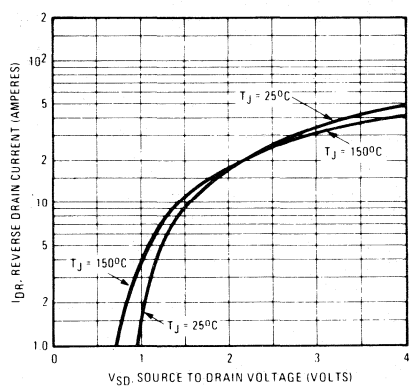


Fig. 7 - Typical source-drain diode forward voltage.

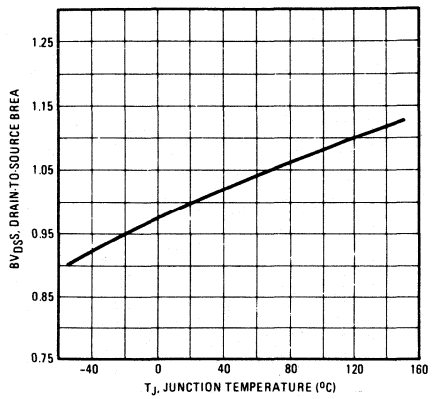


Fig. 8 - Breakdown voltage versus temperature.

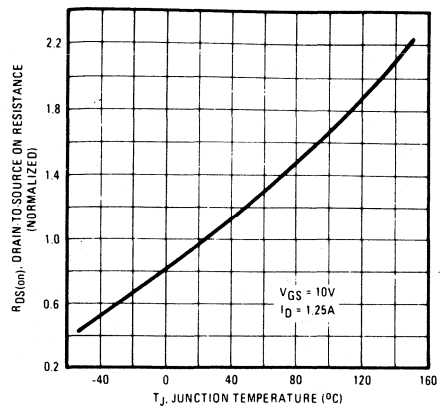


Fig. 9 - Typical normalized on-resistance versus. temperature.

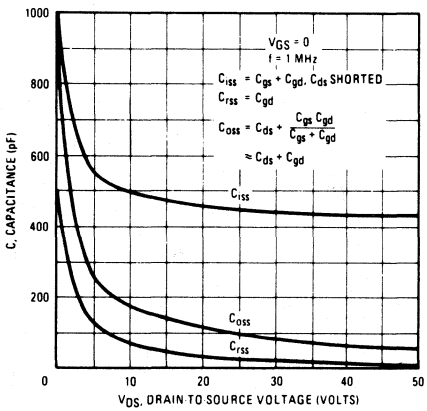


Fig. 10 - Typical capacitance versus drain-to-source. voltage.

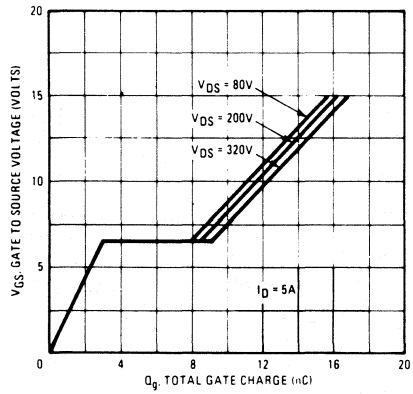


Fig. 11 - Typical gate charge versus gate-to-source. voltage.

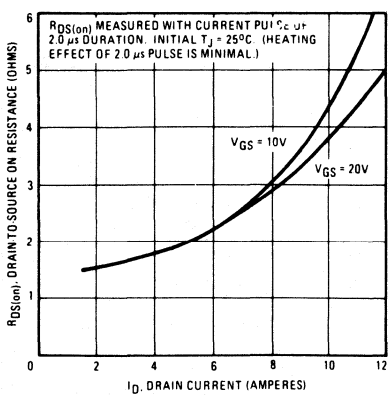


Fig. 12 - Typical on-resistance versus drain current.

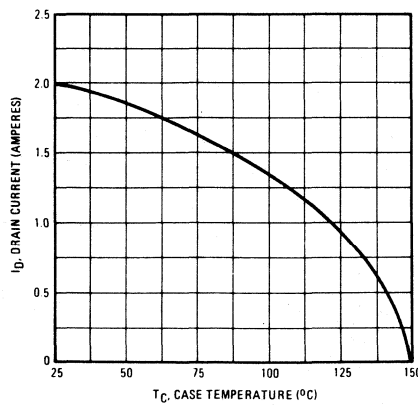


Fig. 13 - Maximum drain current versus case. temperature.

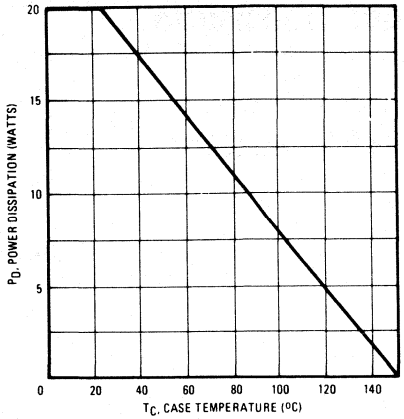
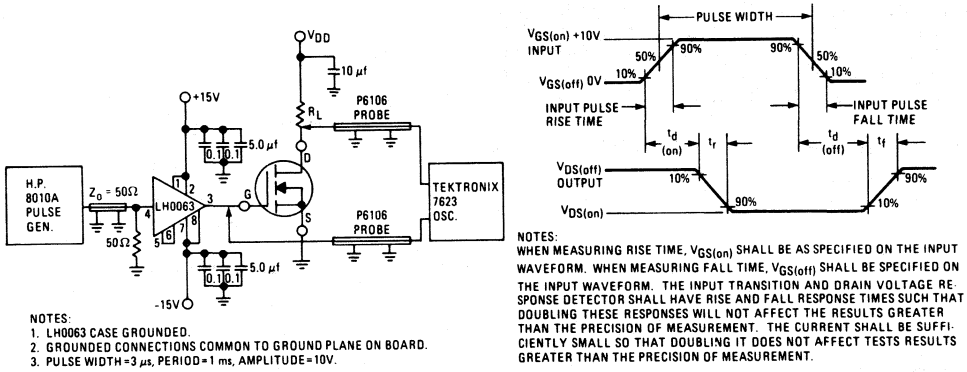


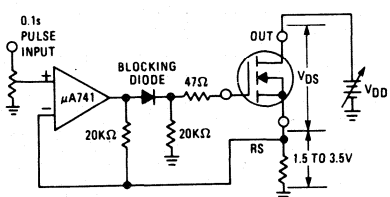
Fig. 14 - Power versus temperature derating curve.



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.

NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating area test circuit.

2N6794 File Number **1902**

Power MOS Field-Effect Transistors

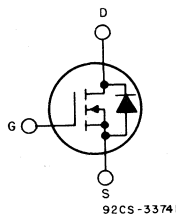
N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

1.5A, 500V
$r_{DS(on)} = 3\Omega$

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

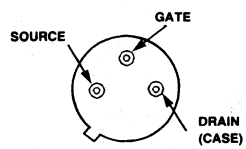
N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

The 2N6794 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6794 is supplied in the JEDEC TO-205AF metal package.



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

*DRAIN-SOURCE VOLTAGE, V_{DS}	500V
*DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ), V_{DGR}	500V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
*DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25° C	1.5A
At T_C = 100° C	1A
Pulsed, I_{DM}	6.5A
*SOURCE CURRENT:	
Continuous, I_S	1.5A
Pulsed, I_{SM}	6.5A
*POWER DISSIPATION, P_T:	
At T_C = 25° C	20W
Above T_C = 25° C	Derate linearly 0.16 W/° C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	6.5A
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150° C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300° C

*In accordance with JEDEC registration data.

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	500*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 500V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	4.5*	V	V_{GS} = 10V, I_D = 1.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	2.5	3.0*	Ω	V_{GS} = 10V, I_D = 1.0A, T_A = 25°C
		–	–	6.6*	Ω	V_{GS} = 10V, I_D = 1.0A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.6*	–	1.2*	V	T_C = 25°C, I_S = 1.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.0*	1.75	3.0*	S(℧)	V_{DS} = 5V, I_D = 1.00A
C_{iss}	Input Capacitance	200*	300	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	30*	75	150*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	20	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 225V, I_D = 1.0A, Z_o = 50Ω
t_r	Rise Time	–	–	30*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	60*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	30*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 200V, I_D = 100 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 13.3V, I_D = 1.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	600	ns	T_J = 150°C, I_F = 1.50A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.5	μC	T_J = 150°C, I_F = 1.50A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

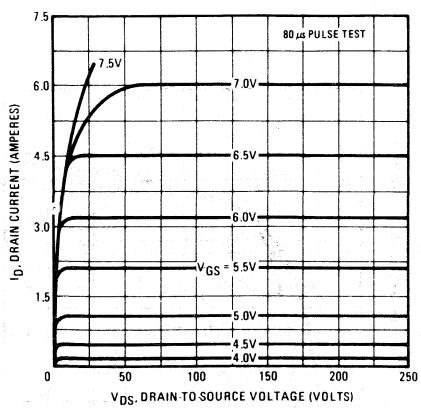


Fig. 1 - Typical output characteristics.

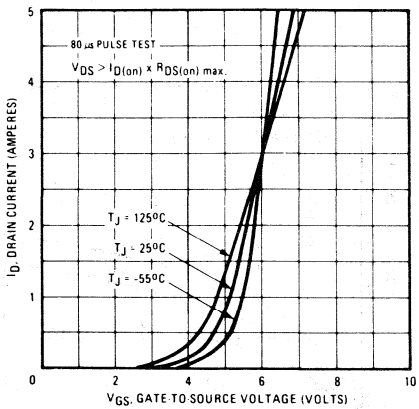


Fig. 2 - Typical transfer characteristics.

2N6794

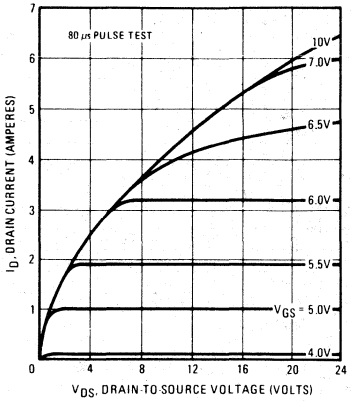


Fig. 3 - Typical saturation characteristics.

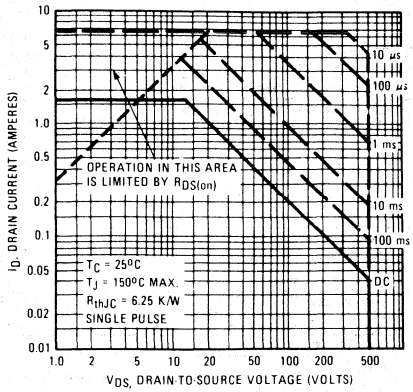


Fig. 4 - Maximum safe operating area.

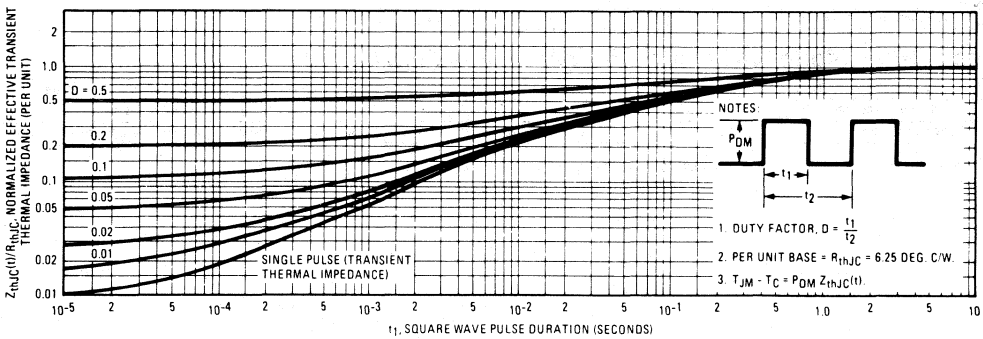


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

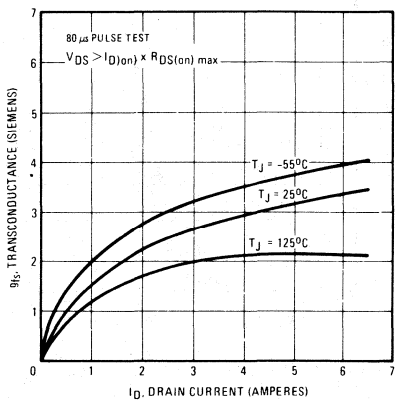


Fig. 6 - Typical transconductance versus drain current.

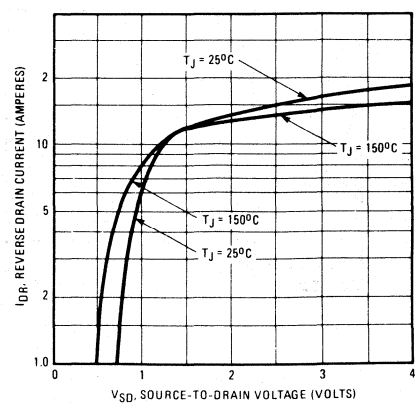


Fig. 7 - Typical source-drain diode forward voltage.

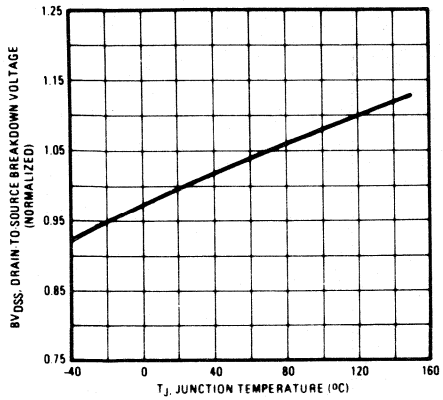


Fig. 8 - Breakdown voltage versus temperature.

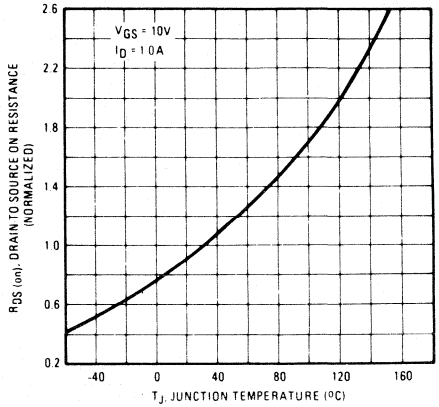


Fig. 9 - Typical normalized on-resistance versus temperature.

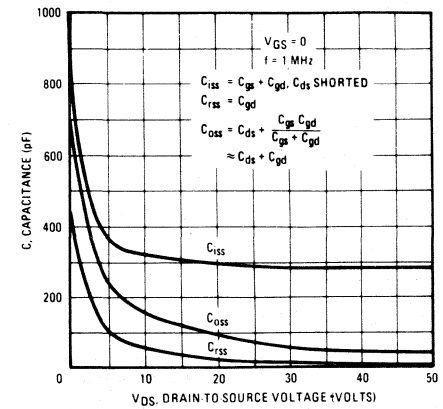


Fig. 10 - Typical capacitance versus drain-to-source voltage.

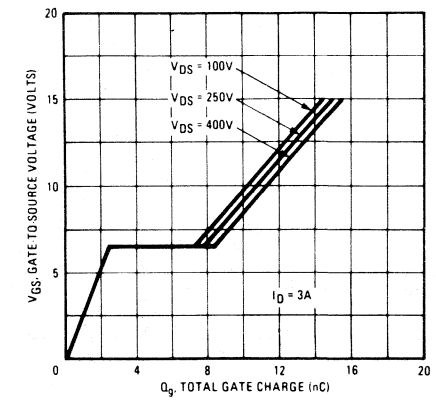


Fig. 11 - Typical gate charge versus gate-to-source voltage.

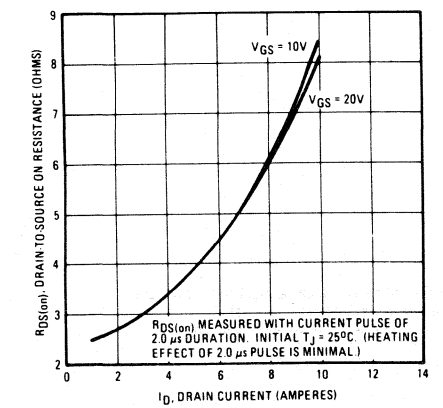


Fig. 12 - Typical on-resistance versus drain current.

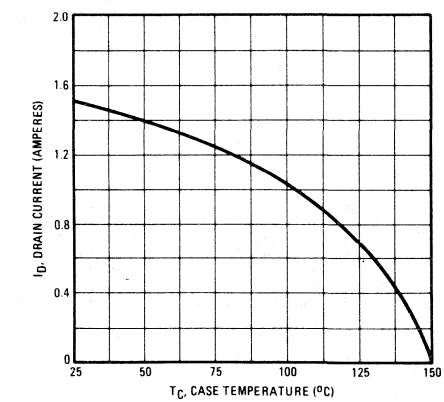


Fig. 13 - Maximum drain current versus case temperature.

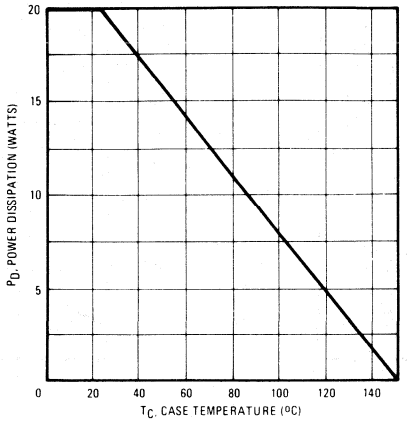
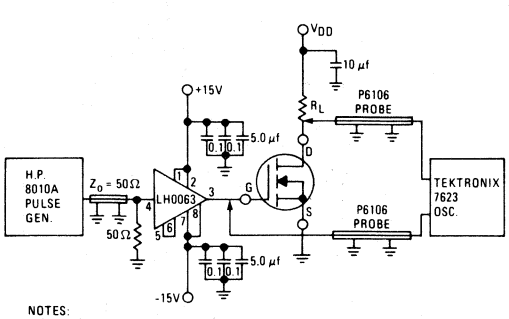
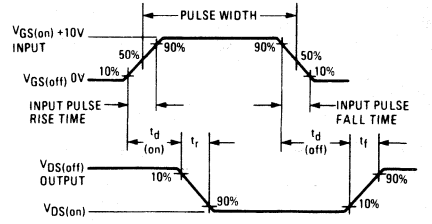


Fig. 14 - Power versus temperature derating curve.



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
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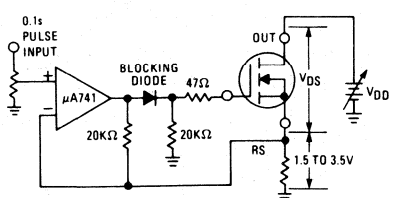
Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

File Number **1594**

2N6796

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8.0A, 100V

$r_{DS}(on)$ = 0.18 Ω

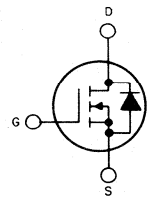
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6796 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6796 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

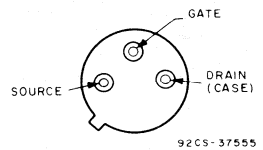
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

Absolute Maximum Ratings

Parameter		2N6796	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	A
I_{DM}	Pulsed Drain Current ③	32*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	8.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	32*	A
P_D @ T_C = 25°C	Max. Power Dissipation	25* (See Fig. 14)	W
	Linear Derating Factor	0.20* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

2N6796

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	1.56*	V	V_{GS} = 10V, I_D = 8.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 25°C
		–	–	0.35*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	3.0*	5.5	9.0*	S(℧)	V_{DS} = 5V, I_D = 5.0A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	150*	300	500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 30V, I_D = 5.0A, Z_o = 50Ω
t_r	Rise Time	–	–	75*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	45*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 80V, I_D = 310 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 3.12V, I_D = 8.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	300	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.5	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

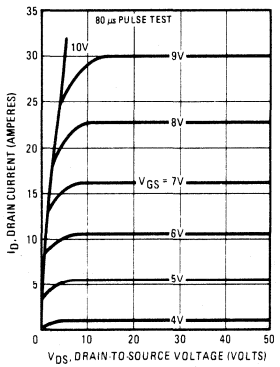


Fig. 1 — Typical Output Characteristics

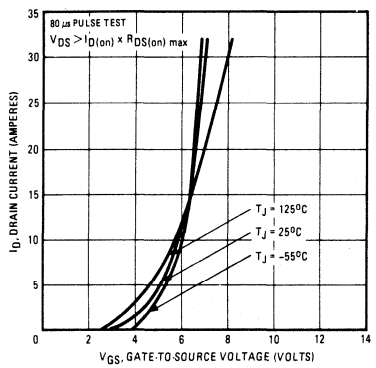


Fig. 2 — Typical Transfer Characteristics

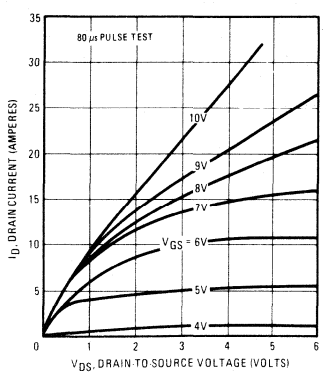


Fig. 3 — Typical Saturation Characteristics

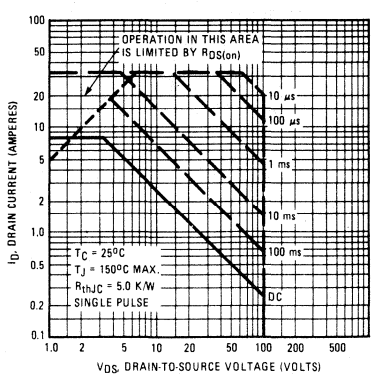


Fig. 4 — Maximum Safe Operating Area

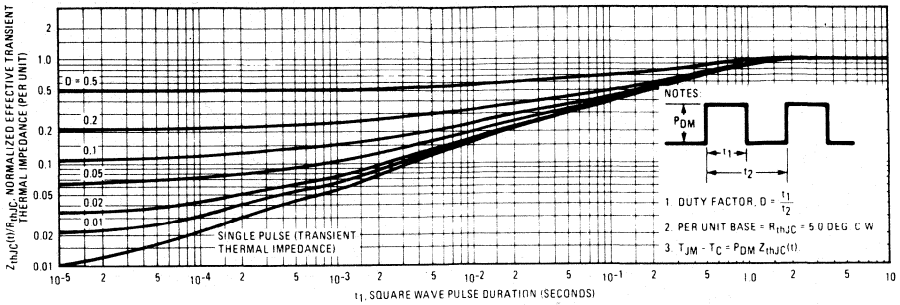


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

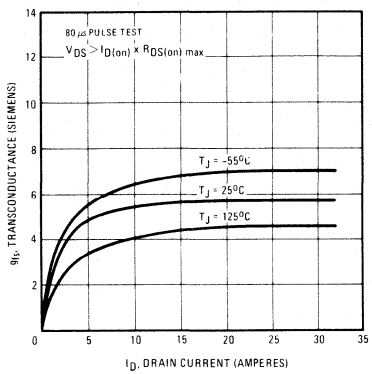


Fig. 6 – Typical Transconductance Vs. Drain Current

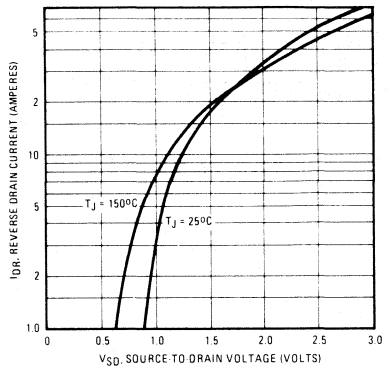


Fig. 7 – Typical Source-Drain Diode Forward Voltage

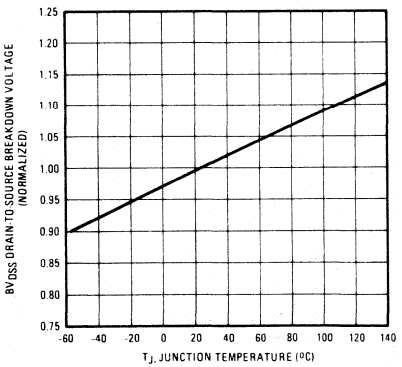


Fig. 8 – Breakdown Voltage Vs. Temperature

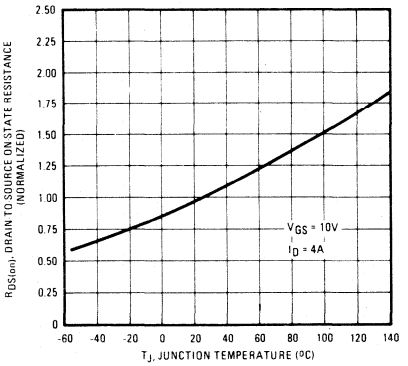


Fig. 9 – Normalized On-Resistance Vs. Temperature

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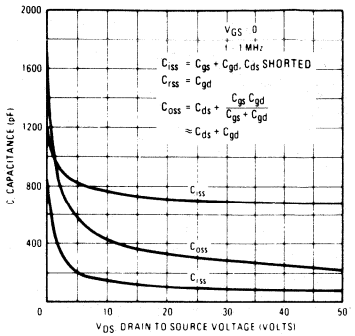


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

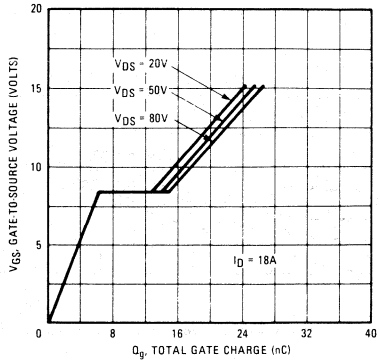


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

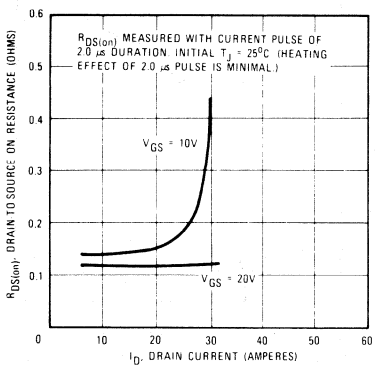


Fig. 12 – Typical On-Resistance Vs. Drain Current

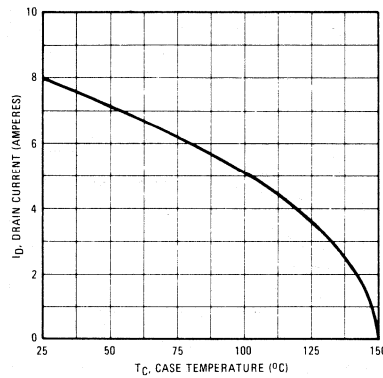


Fig. 13 – Maximum Drain Current Vs. Case Temperature

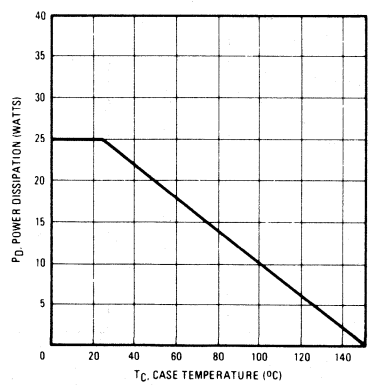
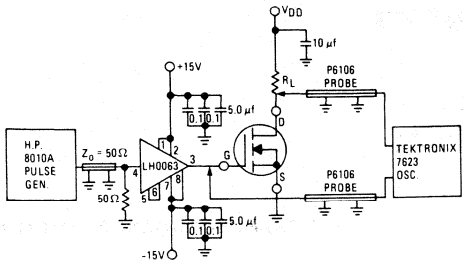
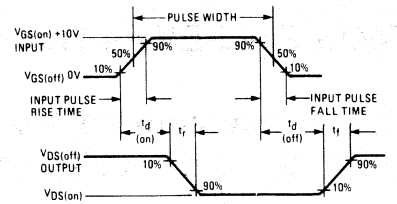


Fig. 14 – Power Vs. Temperature Derating Curve

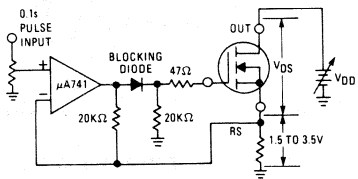


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 – Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 – Safe Operating Area Test Circuit

2N6798

File Number **1903**

Power MOS Field-Effect Transistors

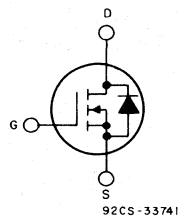
N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

5.5A, 200V
$r_{DS(on)} = 0.4\Omega$

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

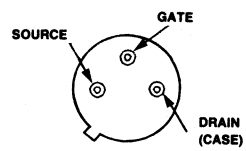
N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

The 2N6798 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6798 is supplied in the JEDEC TO-205AF metal package.



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

*DRAIN-SOURCE VOLTAGE, V_{DS}	200V
*DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ), V_{DGR}	200V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
*DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	5.5A
At T_C = 100°C	3.5A
Pulsed, I_{DM}	22A
*SOURCE CURRENT:	
Continuous, I_S	5.5A
Pulsed, I_{SM}	22A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	25W
Above T_C = 25°C	Derate linearly 0.20 W/°C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	22A
*OPERATING AND STORAGE TEMPERATURE, T_J, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	2.20*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	0.25	0.4*	Ω	V_{GS} = 10V, I_D = 3.5A, T_A = 25°C
		–	–	0.75*	Ω	V_{GS} = 10V, I_D = 3.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	–	1.4*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	2.5*	4.5	7.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	250	450*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 77V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	–	–	50*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	50*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	40*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 160V, I_D = 155 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 4.5V, I_D = 5.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	450	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.0	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

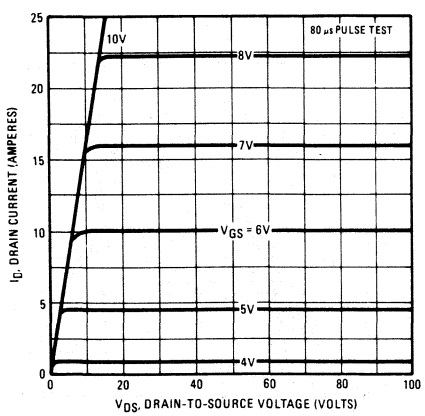


Fig. 1 - Typical output characteristics.

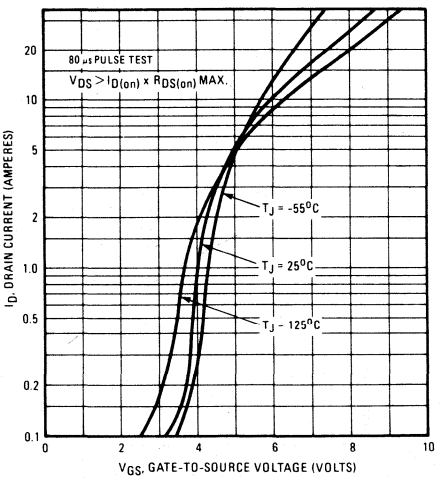


Fig. 2 - Typical transfer characteristics.

2N6798

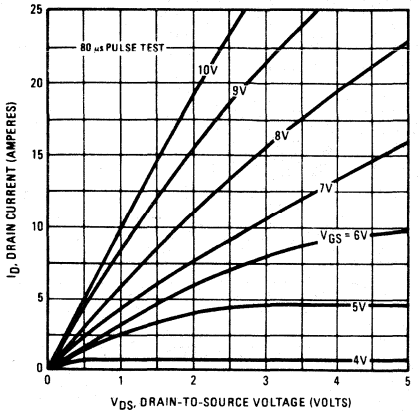


Fig. 3 - Typical saturation characteristics.

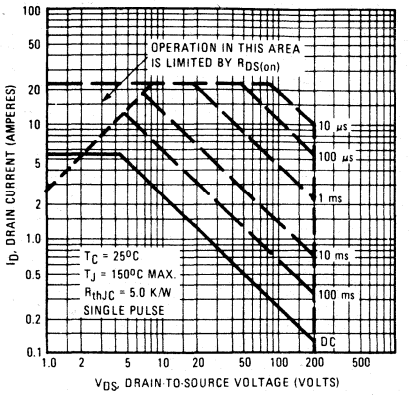


Fig. 4 - Maximum safe operating area.

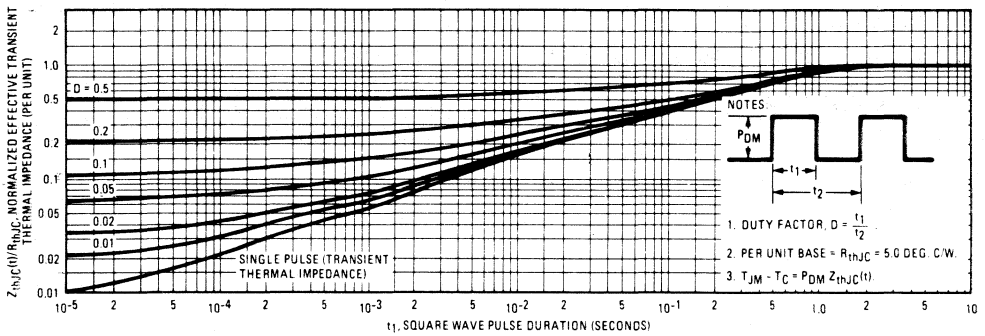


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

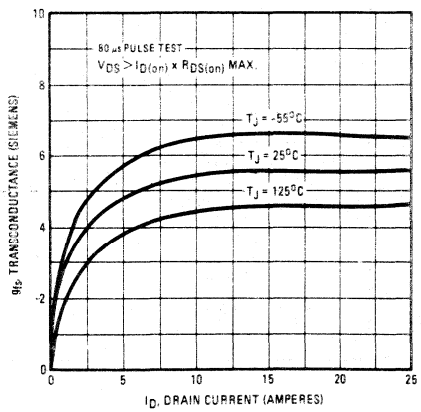


Fig. 6 - Typical transconductance versus drain current.

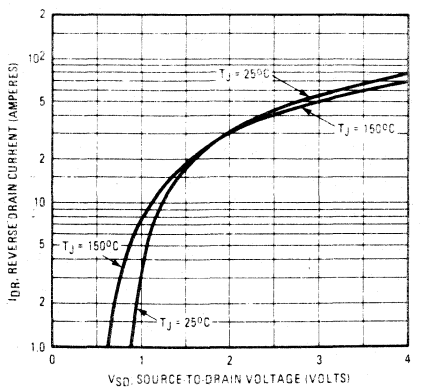


Fig. 7 - Typical source-drain diode forward voltage.

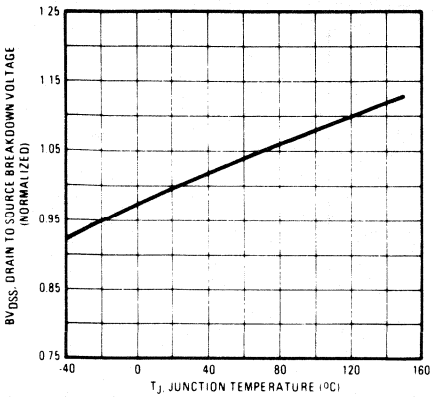


Fig. 8 - Breakdown voltage versus temperature.

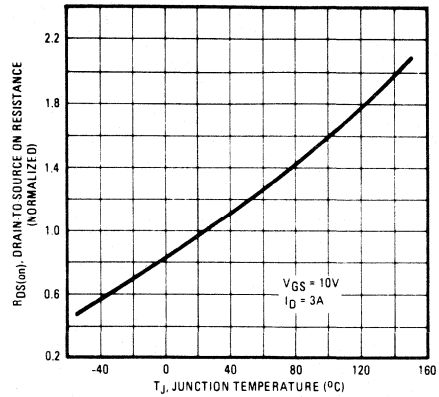


Fig. 9 - Typical normalized on-resistance versus temperature.

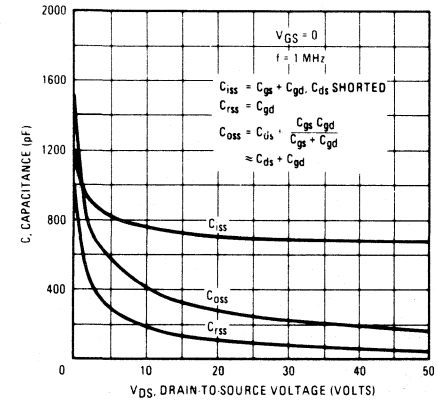


Fig. 10 - Typical capacitance versus drain-to-source voltage.

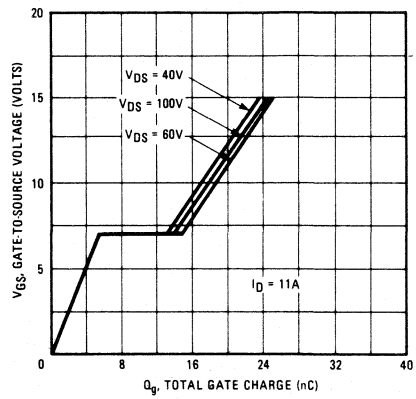


Fig. 11 - Typical gate charge versus gate-to-source voltage.

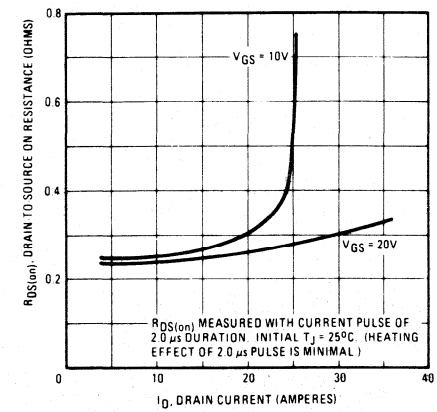


Fig. 12 - Typical on-resistance versus drain current.

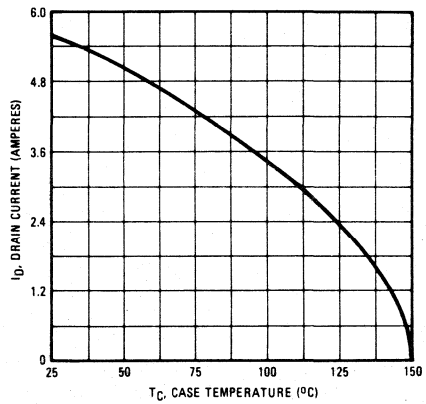


Fig. 13 - Maximum drain current versus case temperature.

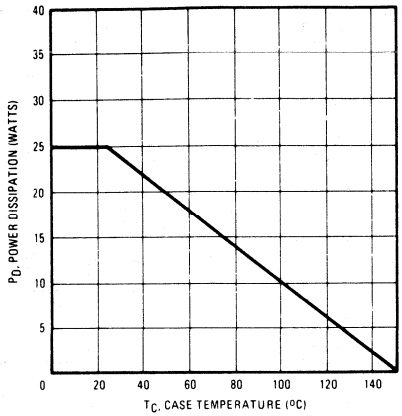
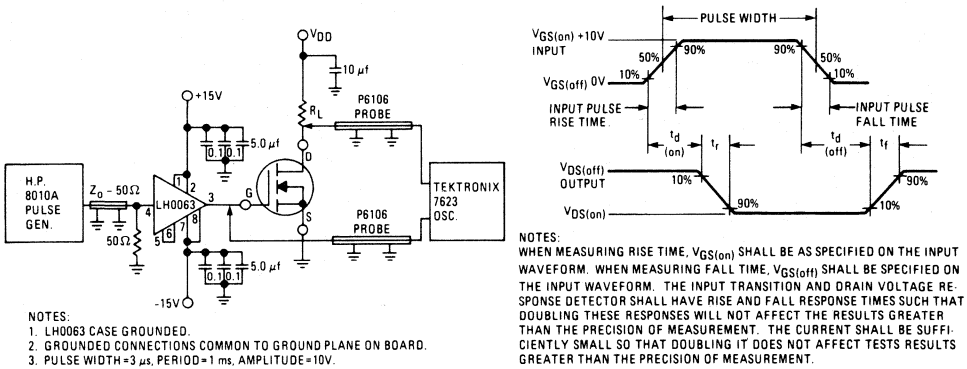


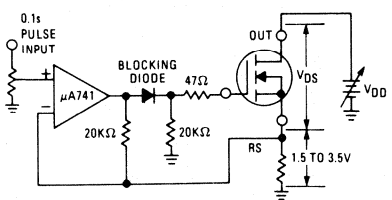
Fig. 14 - Power versus temperature derating curve.



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.

NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

File Number **1904**

2N6800

Power MOS Field-Effect Transistors

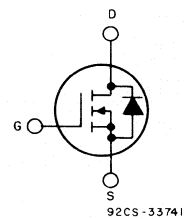
N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

3A, 400V
$r_{DS(on)}$ = 1Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

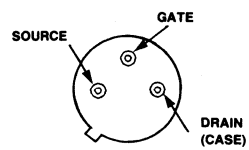
N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

The 2N6800 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6800 is supplied in the JEDEC TO-205AF metal package.



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

*DRAIN-SOURCE VOLTAGE, V_{DS}	400V
*DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ), V_{DGR}	400V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
*DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	3A
At T_C = 100°C	2A
Pulsed, I_{DM}	14A
*SOURCE CURRENT:	
Continuous, I_S	3A
Pulsed, I_{SM}	14A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	25W
Above T_C = 25°C	Derate linearly 0.20 W/°C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	14A
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

2N6800

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	3.0*	V	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 25°C
		–	–	2.4*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	–	1.4*	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	2.0*	3.5	6.0*	S(℧)	V_{DS} = 5V, I_D = 2.0A
C_{iss}	Input Capacitance	350*	700	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	50*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 176V, I_D = 2.0A, Z_o = 50Ω
t_r	Rise Time	–	–	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	55*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	35*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 8.3V, I_D = 3.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	600	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	4.0	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

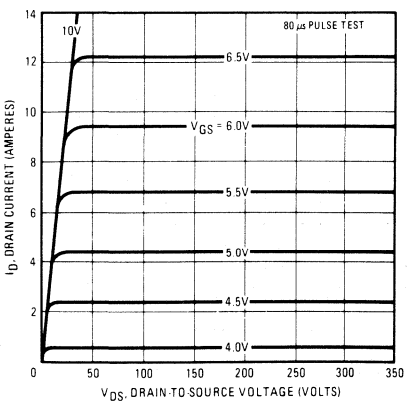


Fig. 1 - Typical output characteristics.

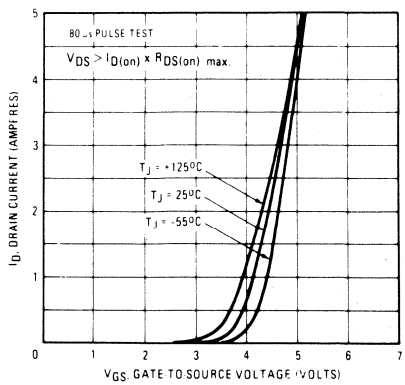


Fig. 2 - Typical transfer characteristics.

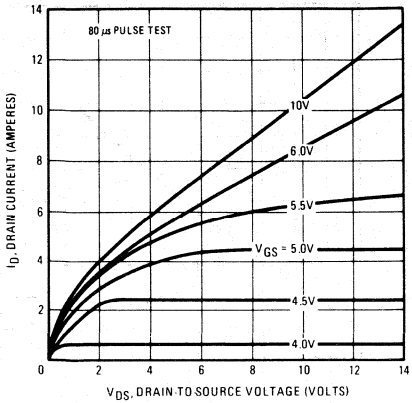


Fig. 3 - Typical saturation characteristics.

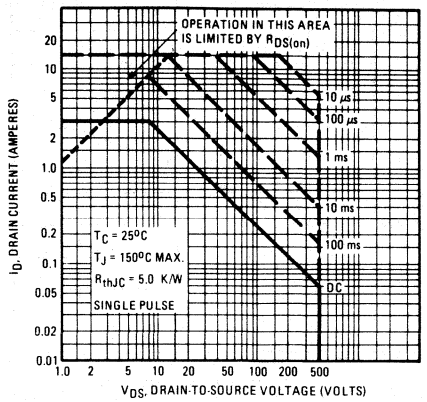


Fig. 4 - Maximum safe operating area.

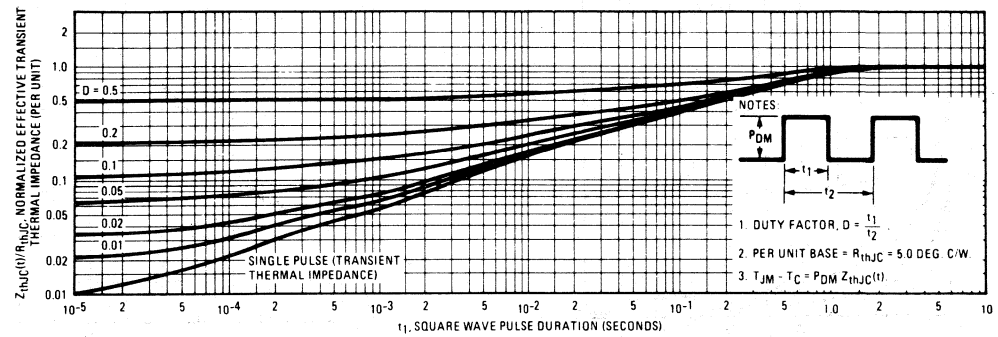


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

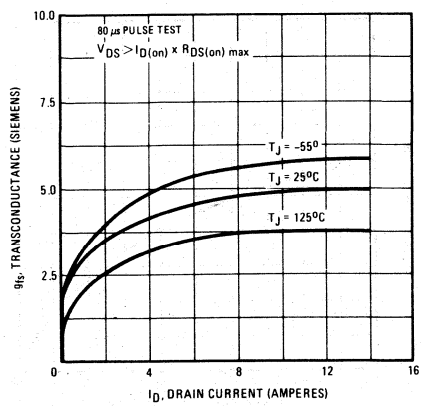


Fig. 6 - Typical transconductance versus drain current.

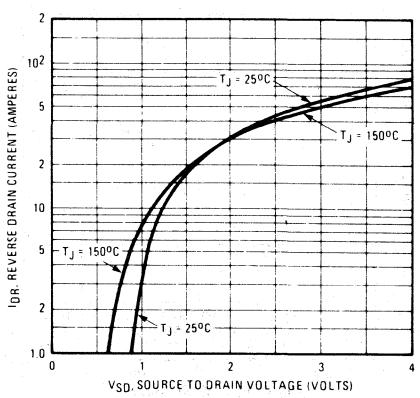


Fig. 7 - Typical source-drain diode forward voltage.

2N6800

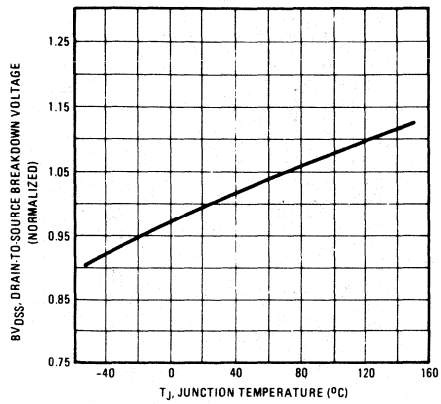


Fig. 8 - Breakdown voltage versus temperature.

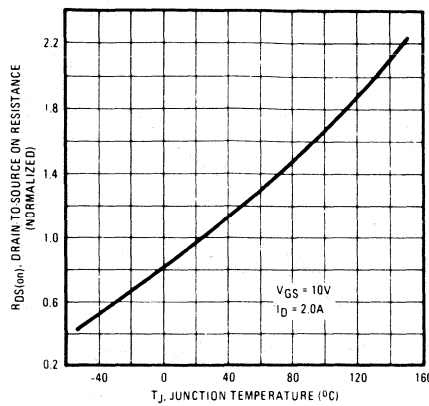


Fig. 9 - Typical normalized on-resistance versus temperature.

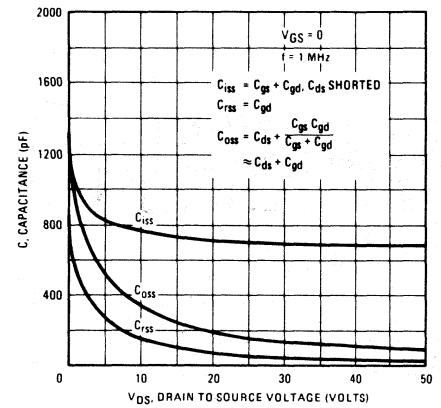


Fig. 10 - Typical capacitance versus drain-to-source voltage.

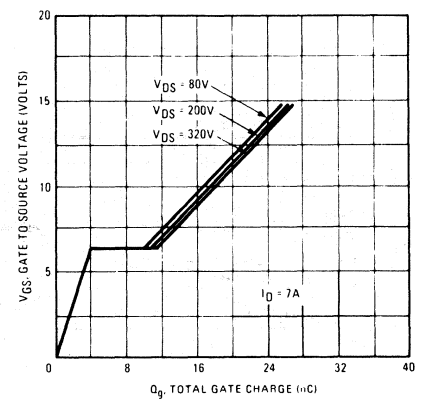


Fig. 11 - Typical gate charge versus gate-to-source voltage.

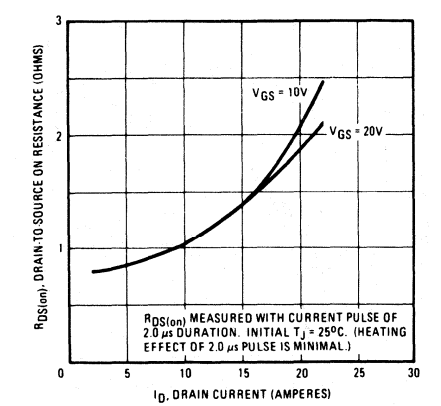


Fig. 12 - Typical on-resistance versus drain current.

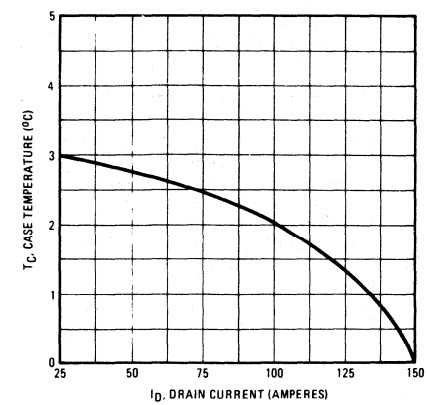


Fig. 13 - Maximum drain current versus case temperature.

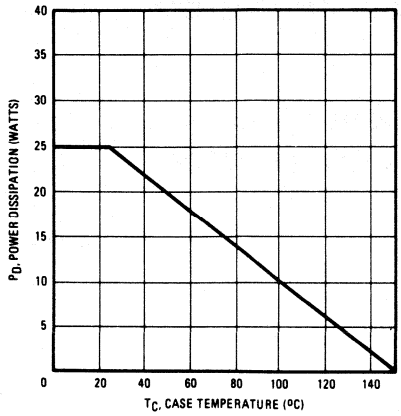
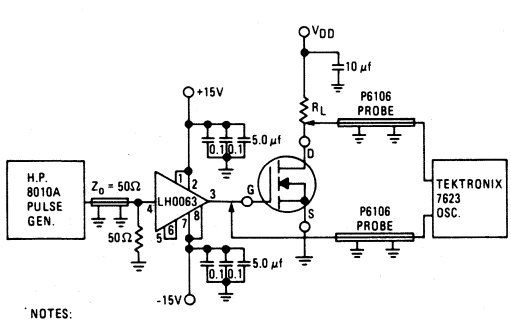
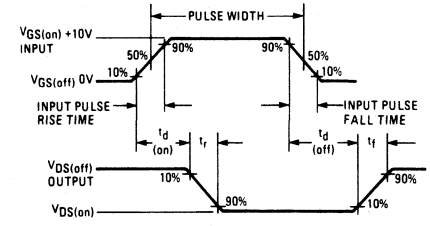


Fig. 14 - Power versus temperature derating curve.

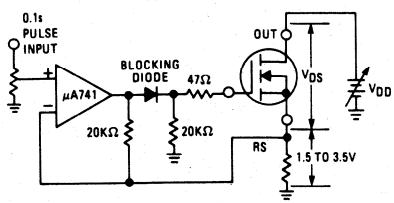


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S$ = 2.5 ± 1.0 Vdc.

Fig. 16 - Safe operating test circuit.

2N6802

File Number **1905**

Power MOS Field-Effect Transistors

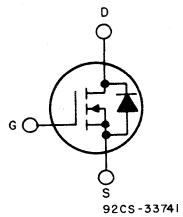
N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

3.5A, 500V
$r_{DS(on)}$ = 1.5Ω

Features:

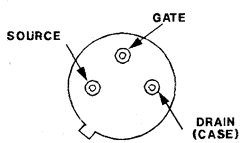
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The 2N6802 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6802 is supplied in the JEDEC TO-205AF metal package.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

*DRAIN-SOURCE VOLTAGE, V_{DS}	500V
*DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ), V_{DGR}	500V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
*DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	3.5A
At T_C = 100°C	1.5A
Pulsed, I_{DM}	11A
*SOURCE CURRENT:	
Continuous, I_S	2.5A
Pulsed, I_{SM}	11A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	25W
Above T_C = 25°C	Derate linearly 0.20 W/°C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	11A
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	500*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 500V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	—	—	3.75*	V	V_{GS} = 10V, I_D = 2.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	—	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 25°C
		—	—	3.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	—	1.4*	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.5*	2.5	4.5*	S(℧)	V_{DS} = 5V, I_D = 1.5A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	25*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	15*	30	60*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30*	ns	V_{DD} ≅ 225V, I_D = 1.5A, Z_o = 50Ω
t_r	Rise Time	—	—	30*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	55*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	30*	ns	of operating temperature.)
SOA	Safe Operating Area	25	—	—	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
		25	—	—	W	V_{DS} = 10V, I_D = 2.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	800	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	4.6	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a]Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

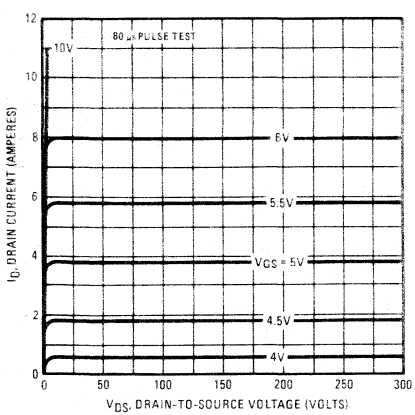


Fig. 1 - Typical output characteristics.

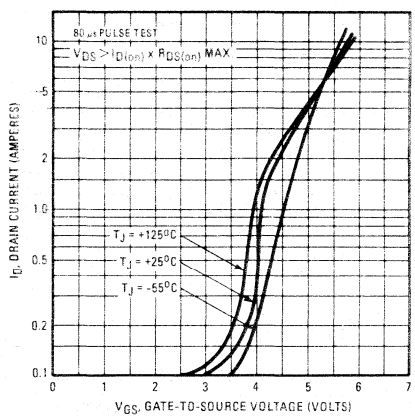


Fig. 2 - Typical transfer characteristics.

2N6802

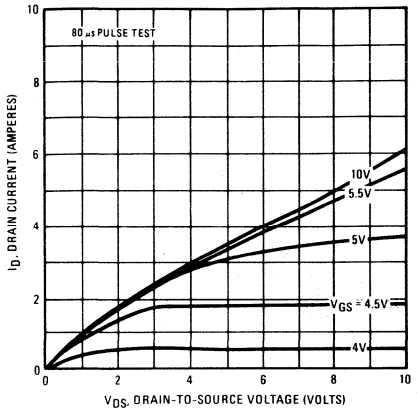


Fig. 3 - Typical saturation characteristics.

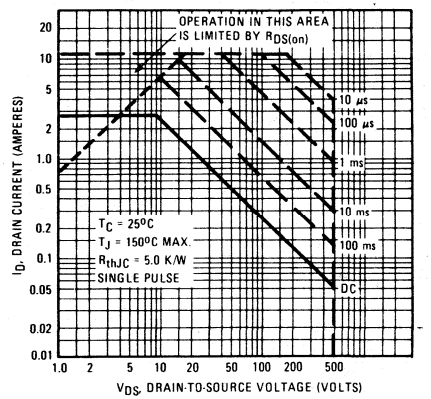


Fig. 4 - Maximum safe operating area.

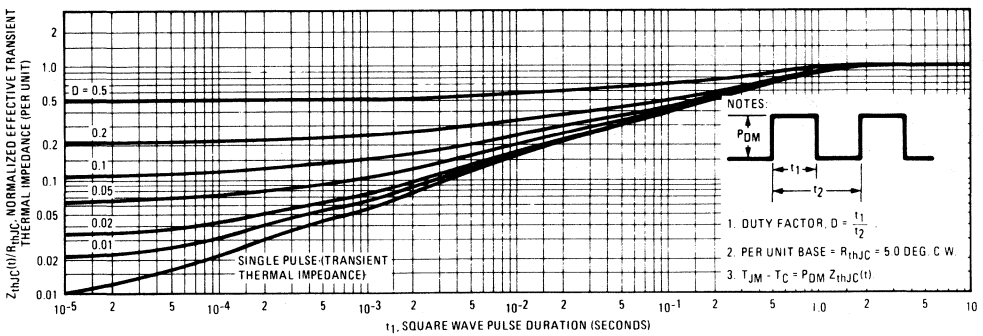


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

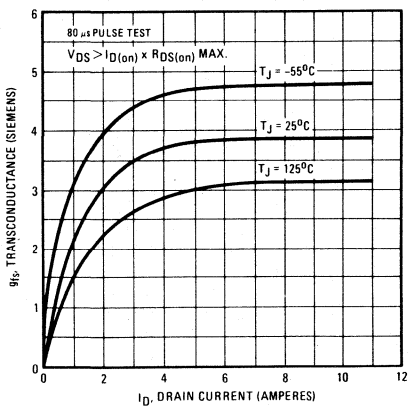


Fig. 6 - Typical transconductance versus drain current.

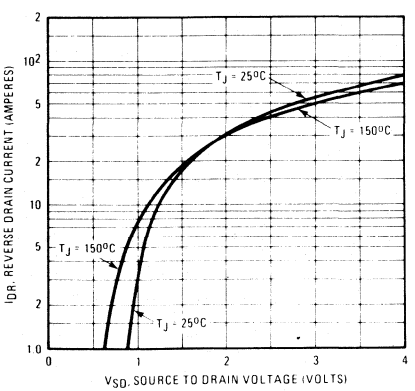


Fig. 7 - Typical source-drain diode forward voltage.

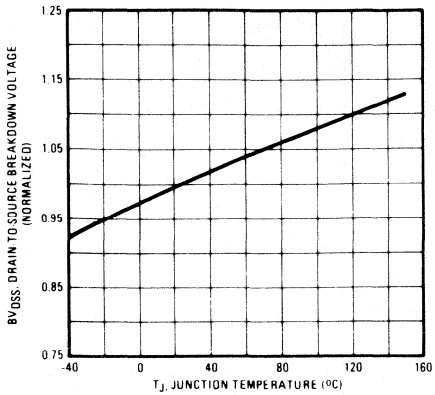


Fig. 8 - Breakdown voltage versus temperature.

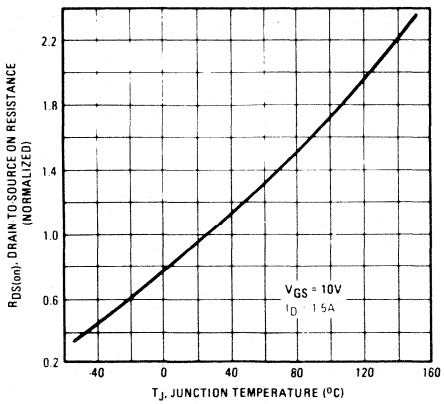


Fig. 9 - Typical normalized on-resistance versus temperature.

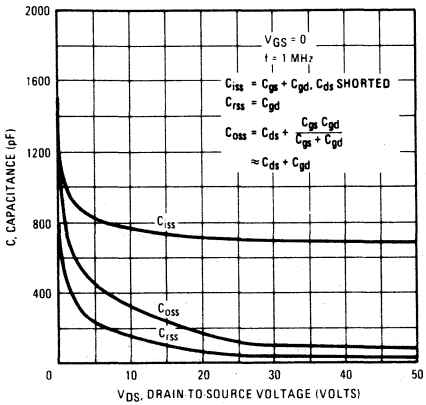


Fig. 10 - Typical capacitance versus drain-to-source voltage.

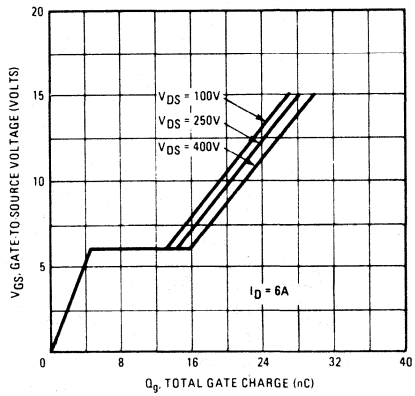


Fig. 11 - Typical gate charge versus gate-to-source voltage.

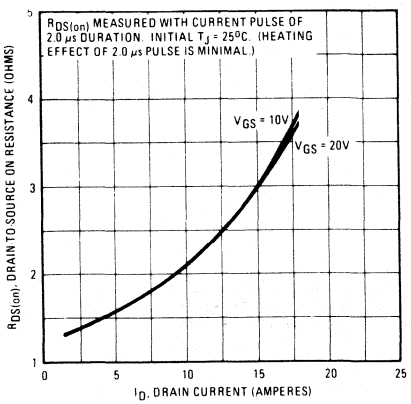


Fig. 12 - Typical on-resistance versus drain current.

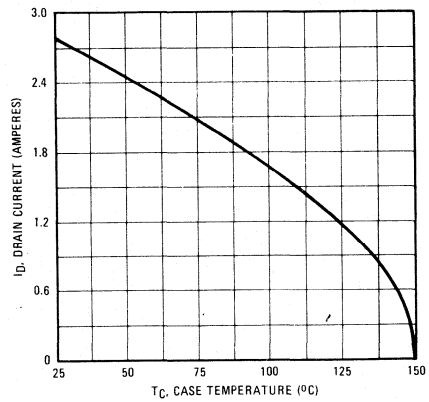


Fig. 13 - Maximum drain current versus case temperature.

2N6802

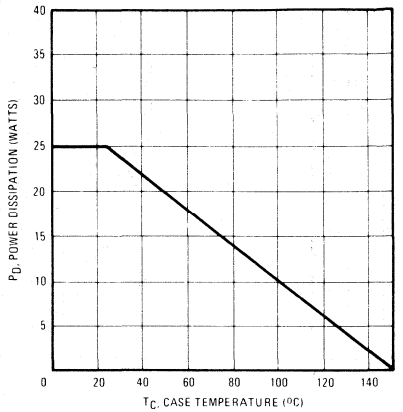
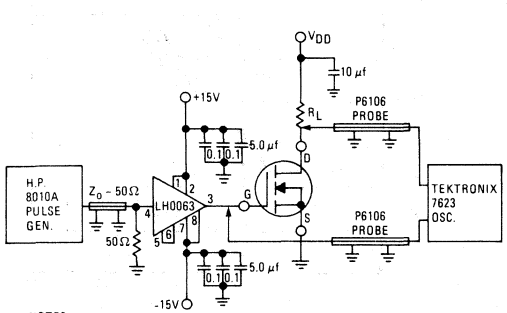
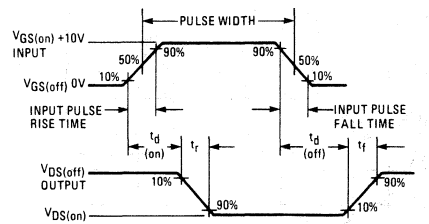


Fig. 14 - Power versus temperature derating curve.

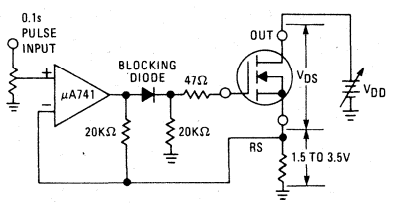


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

File Number **1873**

2N6895

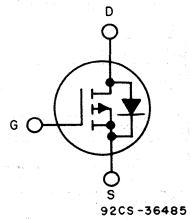
Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

1.16 A, 100 V
$r_{DS}(on)$: 3.65 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM

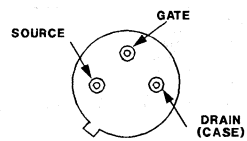


P-CHANNEL ENHANCEMENT MODE

The 2N6895 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6895 is supplied in the JEDEC TO-205AF metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

*DRAIN-SOURCE VOLTAGE, V_{DSS}	-100 V
*DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	-100 V
*GATE-SOURCE VOLTAGE, V_{GS}	±20 V
*DRAIN CURRENT:	
RMS Continuous, I_D	1.16 A
Pulsed, I_{DM}	5 A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	8.33 W
Above T_C = 25°C	Derate linearly 0.0667 W/°C
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances ≥ ⅛ in. (3.17 mm) from seating plane for 10 s max.	260°C

*In accordance with JEDEC registration data.

2N6895

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 0.74 A, V_{GS} = -10 V	—	2.7	V
			I_D = 1.16 A, V_{GS} = -10 V	—	6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 0.74 A, V_{GS} = -10 V	—	3.65	Ω
			T_C = 125°C, I_D = 0.74 A, V_{GS} = 10 V	—	5.66	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 0.74 A	200	800	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	40	150	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	20	80	
*	Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	7.5	30	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	25	ns
*	Rise Time	t_r	I_D = 0.74 A	—	45	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	45	
*	Fall Time	t_f	V_{GS} = -10 V	—	50	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1.16 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 50 A/μs	—	340	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

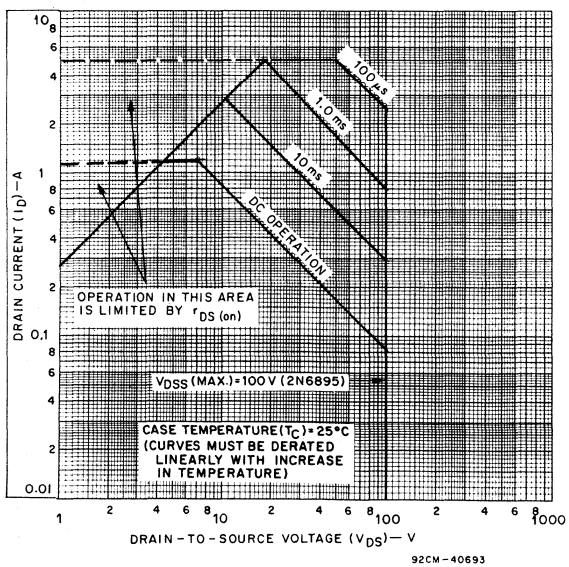


Fig. 1 - Maximum operating areas.

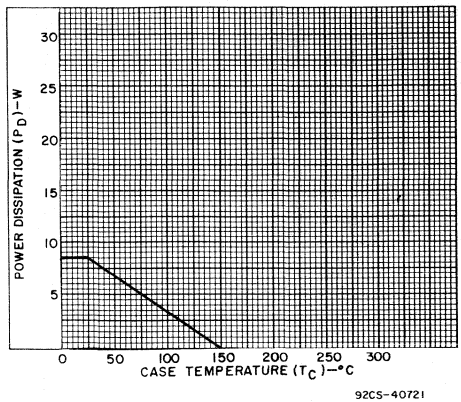


Fig. 2 - Power dissipation vs. temperature derating curve.

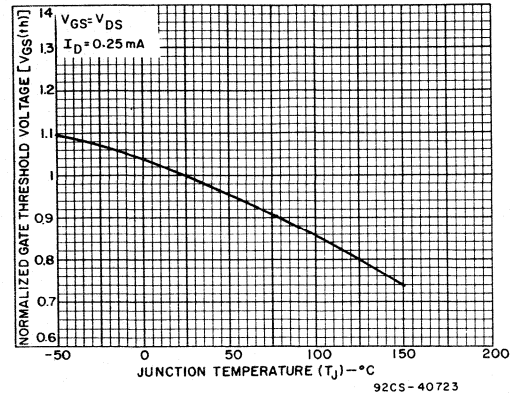


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

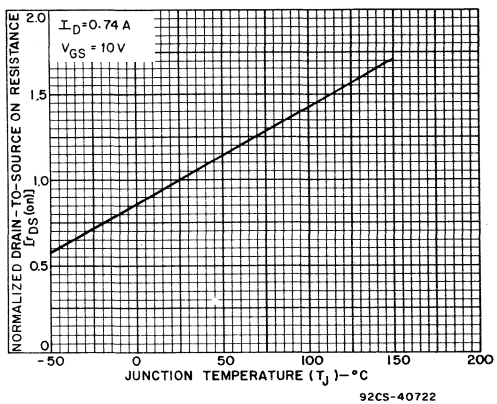


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

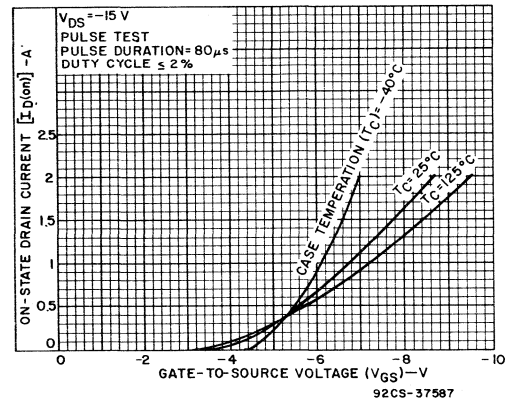


Fig. 5 - Typical transfer characteristics.

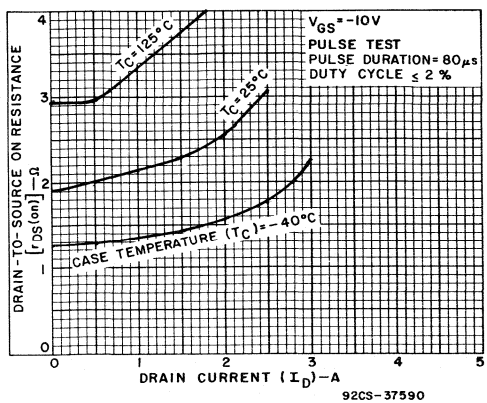


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

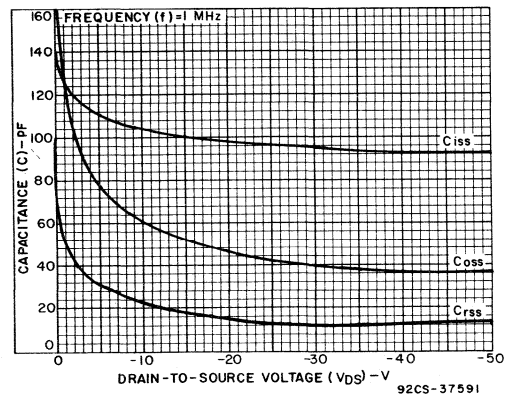


Fig. 7 - Capacitance as a function of drain-to-source voltage.

2N6895

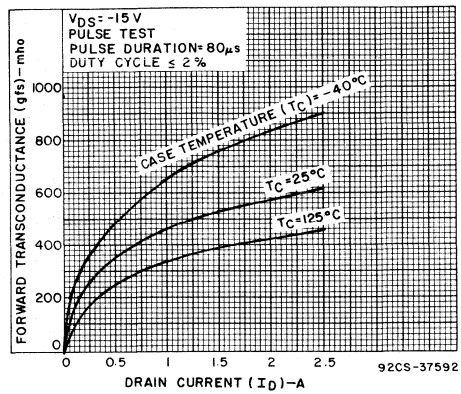


Fig. 8 - Typical forward transconductance as a function of drain current.

File Number **1874**

2N6896

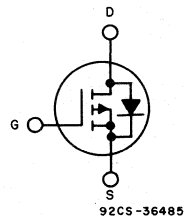
Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

6 A, 100 V
$r_{DS}(on)$: 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM

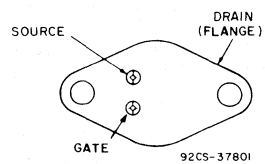


P-CHANNEL ENHANCEMENT MODE

The 2N6896 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The 2N6896 is supplied in the JEDEC TO-204AA metal package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$)

*DRAIN-SOURCE VOLTAGE, V_{DSS}	100 V
*DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	100 V
*GATE-SOURCE VOLTAGE, V_{GS}	±20 V
*DRAIN CURRENT:	
RMS Continuous, I_D	6 A
Pulsed, I_{DM}	20 A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	60 W
Above T_C = 25°C	Derate linearly 0.48 W/°C
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances ≥ ⅛ in. (3.17 mm) from seating plane for 10 s max.	260°C

*In accordance with JEDEC registration data.

2N6896

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	2.28	V
			I_D = 6 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	0.6	Ω
			T_C = 125°C, I_D = 3.8 A, V_{GS} = 10 V	—	0.96	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 3.8 A	1	4	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	200	800	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	100	350	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	40	150	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	60	ns
*	Rise Time	t_r	I_D = 3.8 A	—	100	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	150	
*	Fall Time	t_f	V_{GS} = -10 V	—	100	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 50 A/μs	—	375	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

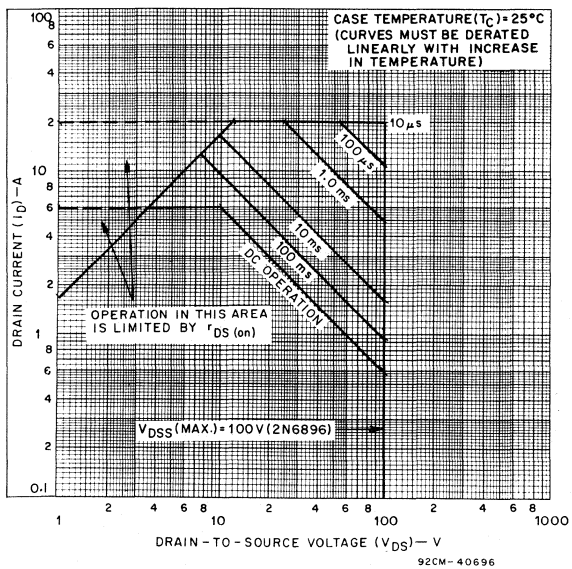


Fig. 1 - Maximum safe operating areas.

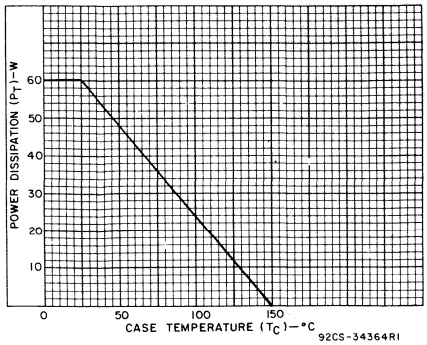


Fig. 2 - Power dissipation vs. temperature derating curve.

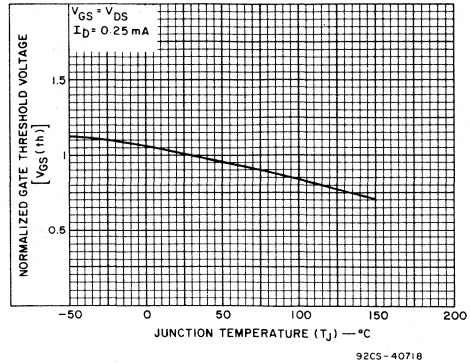


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

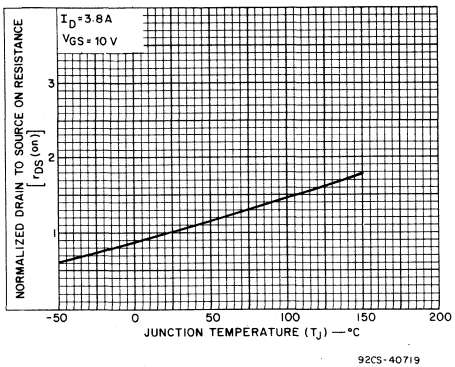


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

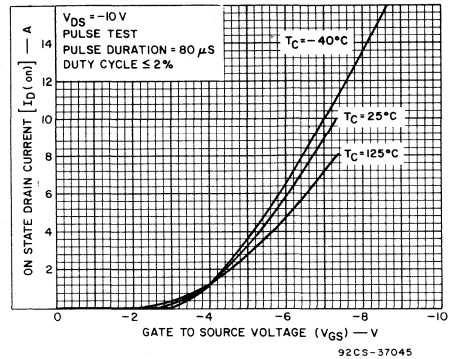


Fig. 5 - Typical transfer characteristics.

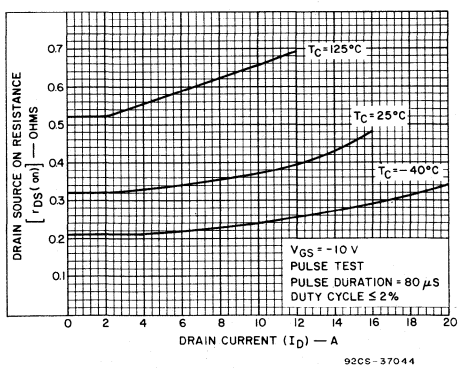


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

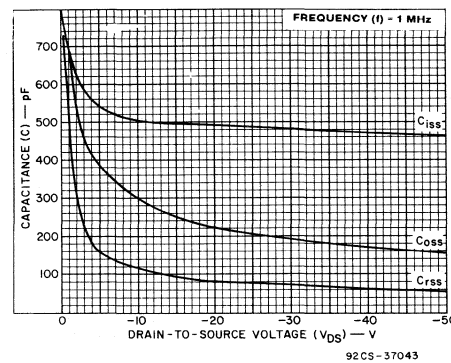


Fig. 7 - Capacitance as a function of drain-to-source voltage.

2N6896

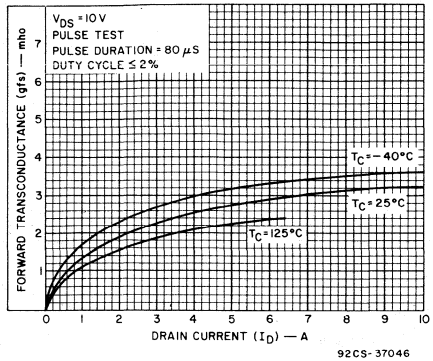


Fig. 8 - Typical forward transconductance as a function of drain current.

File Number **1875**

2N6897

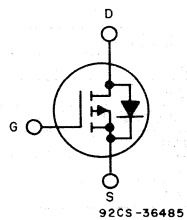
Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

12 A, 100 V
$r_{DS}(on)$: 0.3 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM

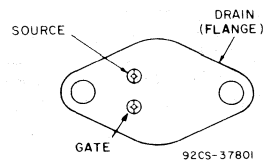


P-CHANNEL ENHANCEMENT MODE

The 2N6897 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6897 is supplied in the JEDEC TO-204AA metal package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$)

*DRAIN-SOURCE VOLTAGE, V_{DSS}	-100 V
*DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	-100 V
*GATE-SOURCE VOLTAGE, V_{GS}	±20 V
*DRAIN CURRENT:	
RMS Continuous, I_D	12 A
Pulsed, I_{DM}	30 A
*POWER DISSIPATION, P_T:	
At T_C = 25° C	100 W
Above T_C = 25° C	Derate linearly 0.8 W/° C
*OPERATING AND STORAGE TEMPERATURE, T_J, T_{stg}	-55 to +150° C
*LEAD TEMPERATURE, T_L:	
At distances ≥ ⅛ in. (3.17 mm) from seating plane for 10 s max.	260° C

*In accordance with JEDEC registration data.

2N6897

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = -10 V	—	2.28	V
			I_D = 12 A, V_{GS} = -10 V	—	-4.8	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = -10 V	—	0.3	Ω
			T_C = 125°C, I_D = 7.6 A, V_{GS} = 10 V	—	0.465	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 7.6 A	2	8	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	400	1500	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	200	700	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	60	240	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	60	ns
*	Rise Time	t_r	I_D = 7.6 A	—	175	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	275	
*	Fall Time	t_f	V_{GS} = -10 V	—	175	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	1.25	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 100 A/μs	—	500	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

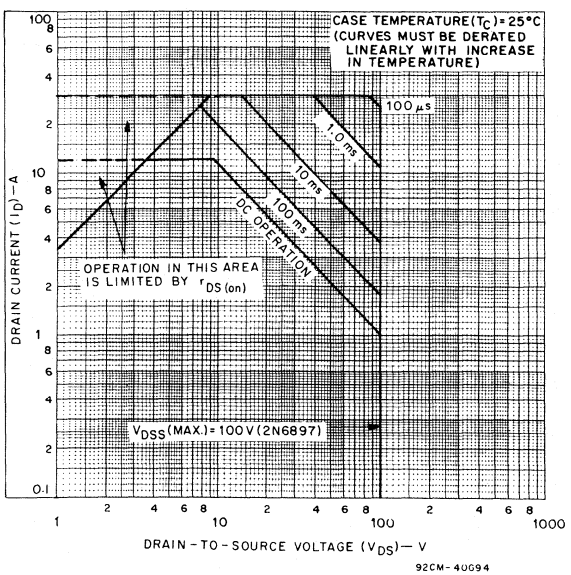


Fig. 1 - Maximum safe operating areas.

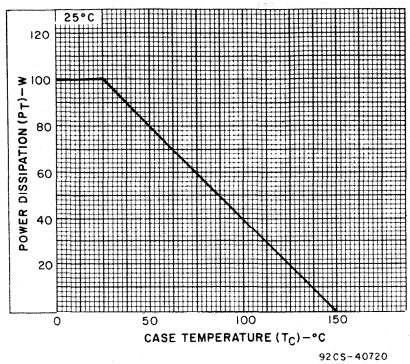


Fig. 2 - Power dissipation vs. temperature derating curve.

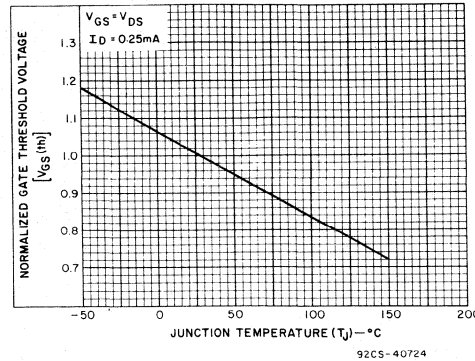


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

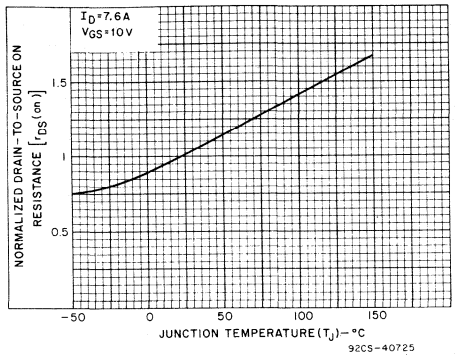


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

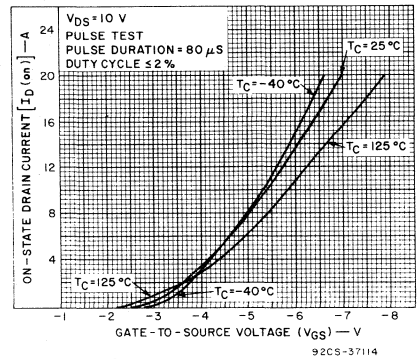


Fig. 5 - Typical transfer characteristics.

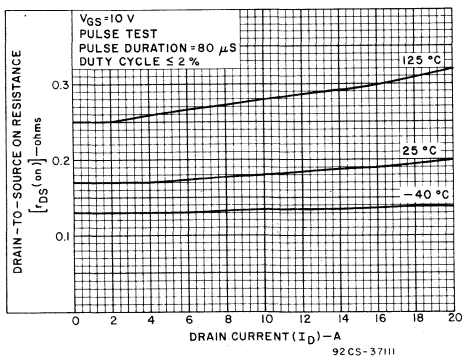


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

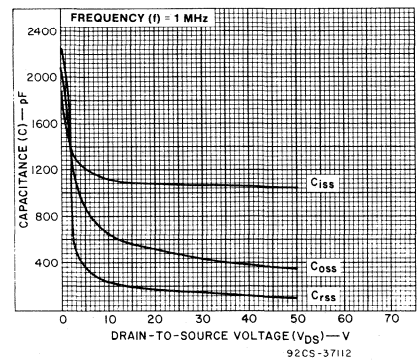


Fig. 7 - Capacitance as a function of drain-to-source voltage.

2N6897

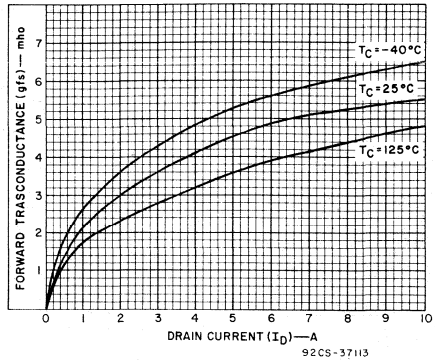


Fig. 8 - Typical forward transconductance as a function of drain current.

File Number **1876**

2N6898

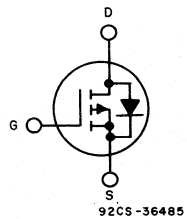
Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

25 A, -100 V
$r_{DS}(on)$: 0.20 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM

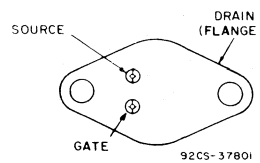


P-CHANNEL ENHANCEMENT MODE

The 2N6898 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6898 is supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATION



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$)

*DRAIN-SOURCE VOLTAGE, V_{DSS}	-100 V
*DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	-100 V
*GATE-SOURCE VOLTAGE, V_{GS}	±20 V
*DRAIN CURRENT:	
RMS Continuous, I_D	25 A
Pulsed, I_{DM}	60 A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	150 W
Above T_C = 25°C	Derate linearly 1.2 W/°C
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances ≥ ⅛ in. (3.17 mm) from seating plane for 10 s max.	260°C

*In accordance with JEDEC registration data.

2N6898

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	3.16	V
			I_D = 25 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	0.2	Ω
			T_C = 125°C, I_D = 15.8 A, V_{GS} = 10 V	—	0.24	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 15.8 A	4	16	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	—	3000	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	500	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	50	ns
*	Rise Time	t_r	I_D = 12.5 A	—	250	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	—	400	
*	Fall Time	t_f	V_{GS} = -10 V	—	250	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 25 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 100 A/μs	—	750	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

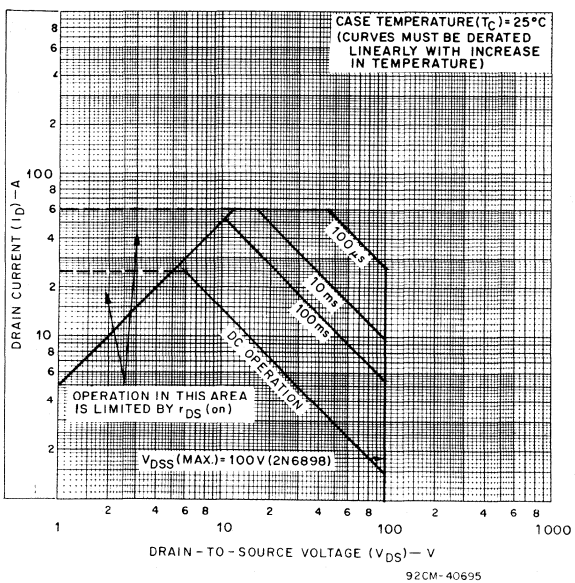


Fig. 1 - Maximum safe operating areas.

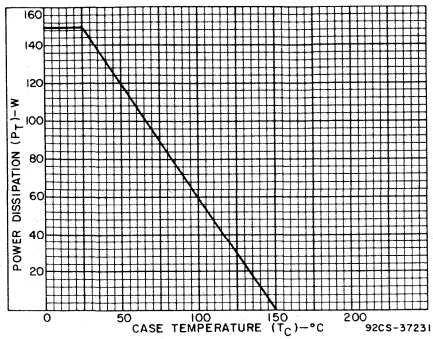


Fig. 2 - Power dissipation vs. temperature derating curve.

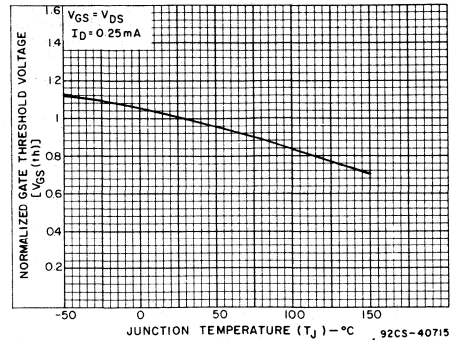


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

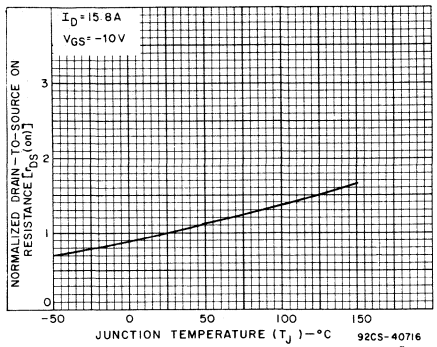


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

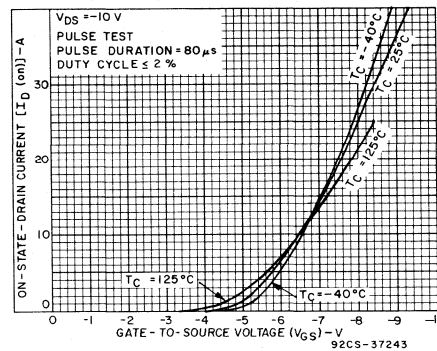


Fig. 5 - Typical transfer characteristics.

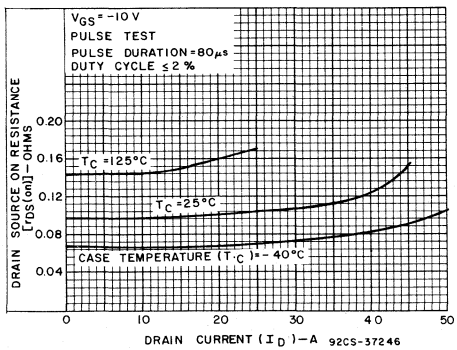


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

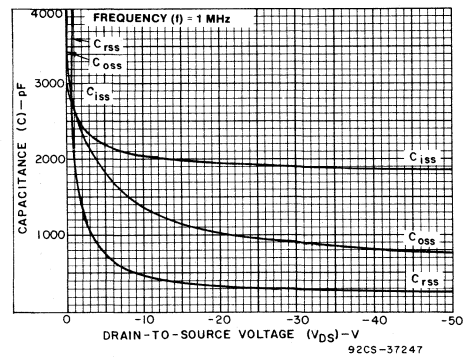


Fig. 7 - Capacitance as a function of drain-to-source voltage.

2N6898

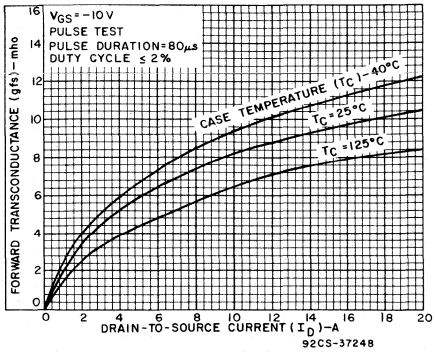


Fig. 8 - Typical forward transconductance as a function of drain current.

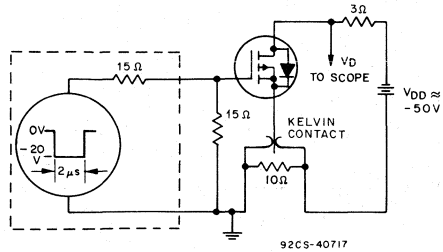


Fig. 9 - Switching time test circuit.

Power MegaFETs

RFD10N05, RFD10N05SM

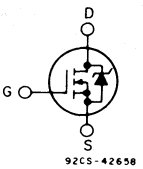
File Number **2107**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

10 A, 50 V
$r_{DS}(on)$ = 0.1 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



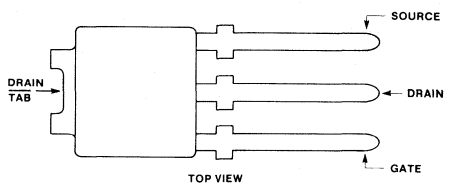
TERMINAL DIAGRAM

The RFD10N05 and RFD10N05SM n-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. These devices were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

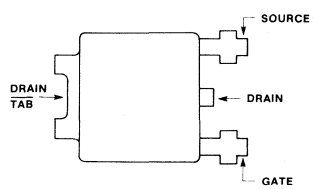
Because of space limitations branding (marking) on type RFD10N05 and on type RFD10N05SM is D10N05.

The RFD10N05 is supplied in the JEDEC TO-251 plastic package and the RFD10N05SM is supplied in the JEDEC TO-252 surface-mount plastic package.

TERMINAL DESIGNATION



TO-251AA



TO-252AA

92CS-43478

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

DRAIN-SOURCE VOLTAGE, V_{DSS} ..... 50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{gs} = 1 MΩ) ..... 50 V
GATE-SOURCE VOLTAGE, V_{GS} ..... ±20 V
DRAIN CURRENT:
- I_D, RMS Continuous ..... 10 A
- I_{DM}, Pulsed ..... 24 A

SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}• ..... 100 mj
AVALANCHE CURRENT, I_{AS} ..... 10 A
POWER DISSIPATION, P_T:
- At T_C = 25°C ..... 20 W
- Derated above T_C = 25°C ..... 0.16 W/°C

OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg} ..... -55 to +150°C

•V_{DD}=10 V, starting T_j=25°C, L=2 mH, R_{gs}=50 Ω, I_{peak}=10 A. See Figs. 12 and 13.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS RFD10N05 RFD10N05SM		UNITS
			MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=0.25 mA, V_{GS}=0 V	50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=0.25 mA	2	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V	—	1	μA
		T_C=150° C	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D=10 A, V_{GS}=10 V	—	0.1	Ω
Turn-On Time	t(on)	V_{DD}=25 V, I_D=5 A I_{g1}=I_{g2}=0.2 A V_{GS} (clamp) + 10 V, -0.6 V R1=5 Ω (See Figs. 10 and 11)	—	50	ns
Turn-On Delay Time	$t_d(on)$		—	13(typ.)	
Rise Time	t_r		—	24(typ.)	
Turn-Off Delay Time	$t_d(off)$		—	42(typ.)	
Fall Time	t_f		—	16(typ.)	
Turn-Off Time	t(off)		—	100	
Total Gate Charge	Q_g(total)	I_D=10 A, V_{DD}=40 V, R1=4 Ω, V_{GS}=15 V	—	30	nC
Gate Charge at 10 V	$Q_g(10)$	V_{GS}=10 V	—	20	
Threshold Gate Charge	$Q_g(th)$	V_{GS}=2 V	—	1.5	
Plateau Voltage	V(plateau)	I_D=10 A, V_{DS}=15 V	—	7.5	V
Turn-Off Energy Loss Per Cycle	E_{off}	I_D=5 A, R1=5 Ω, L=0.2 μH I_{g1}=I_{g2}=0.2 A V_{GS}(clamp) +10 V, -0.6 V	—	8	μJ
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$		—	6.25	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$		—	100	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS RFD10N05 RFD10N05SM		UNITS
			MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=10 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F=10 A, dI_F/d_t=100 A/μs	—	125	ns

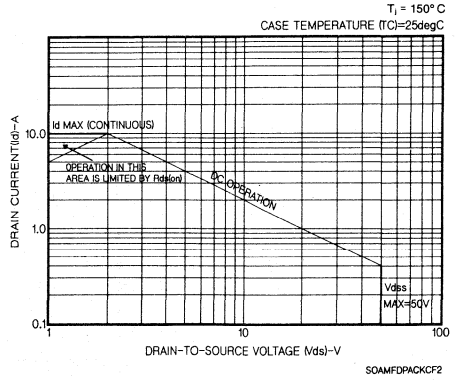


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

RFD10N05, RFD10N05SM

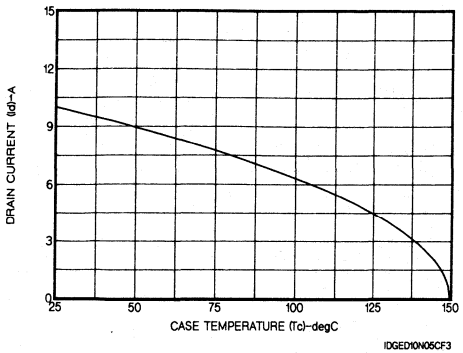


Fig. 2 - Maximum continuous drain current vs temperature.

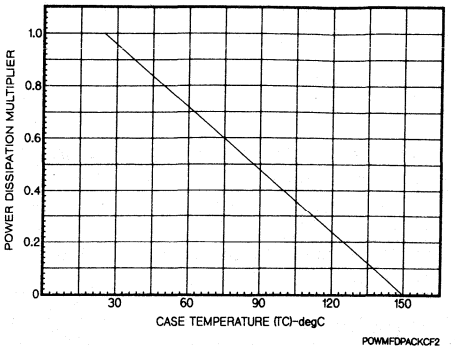


Fig. 3 - Normalized power dissipation vs temperature derating curve.

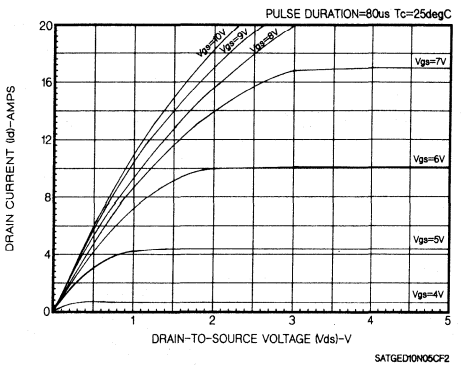


Fig. 4 - Typical saturation characteristics.

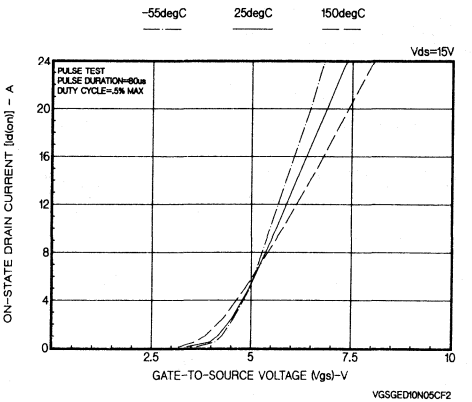


Fig. 5 - Typical transfer characteristics.

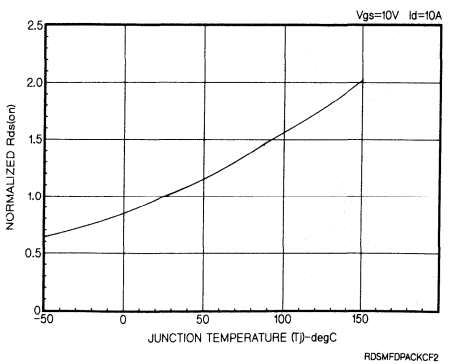


Fig. 6 - Normalized $r_{DS}(on)$ vs junction temperature.

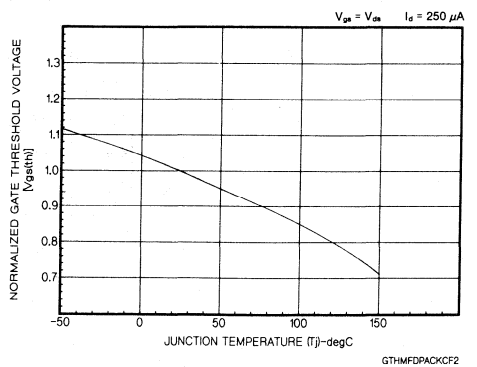


Fig. 7 - Typical normalized gate threshold voltage.

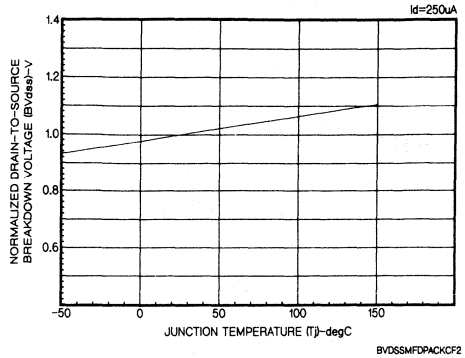


Fig. 8 - Drain source breakdown voltage vs temperature.

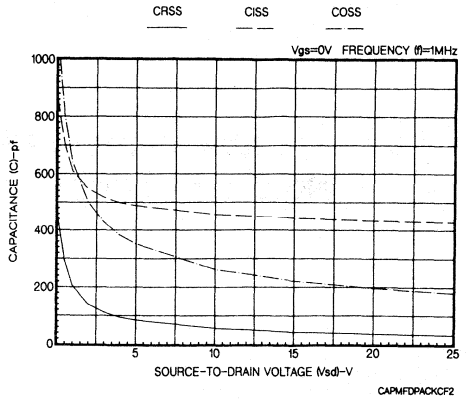


Fig. 9 - Typical capacitance vs voltage.

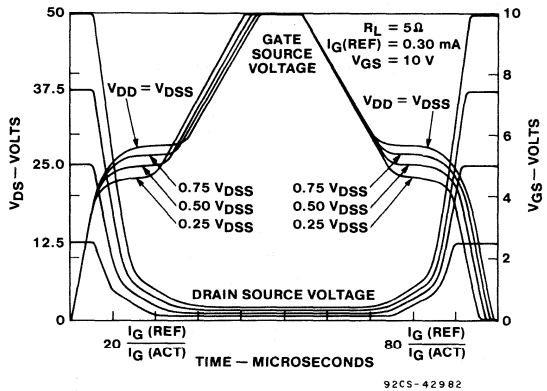


Fig. 10 - Normalized switching waveforms for constant gate-current. (Refer to RCA application notes AN7254 and AN7260.)

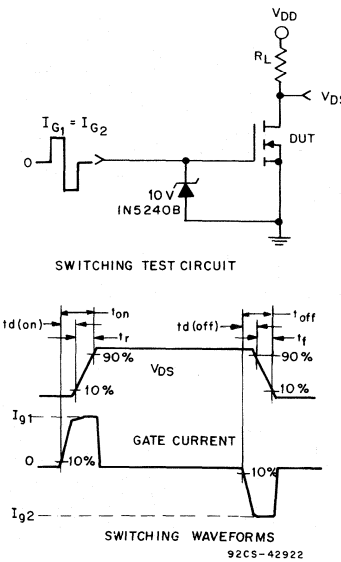


Fig. 11 - Resistive switching.

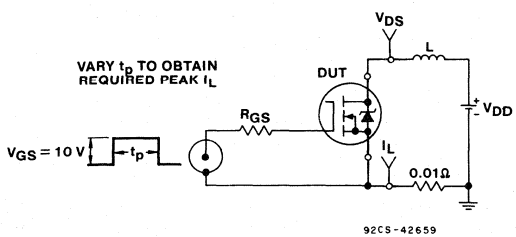


Fig. 12 - Unclamped energy test circuit.

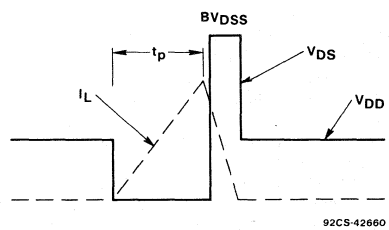


Fig. 13 - Unclamped energy waveforms.

RFD14N05, RFD14N05SM, RFP14N05

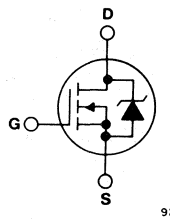
File Number **2268**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

14 A, 50 V
$r_{ds(on)} = 0.1\Omega$

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



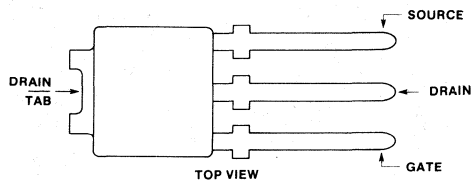
92CS-42658

N-CHANNEL ENHANCEMENT MODE

The RFD14N05, RFD14N05SM, and RFP14N05 n-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

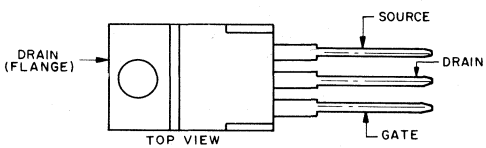
The RFD14N05 is supplied in the JEDEC TO-251 plastic package, the RFD14N05SM in the JEDEC TO-252 plastic package and the RFP14N05 in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



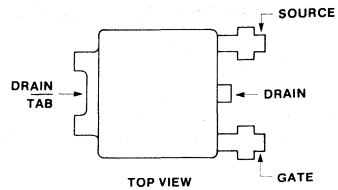
JEDEC TO-251AA

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB



JEDEC TO-252AA

92CS-43478

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ, V_{DGR}	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±20 V
DRAIN CURRENT:	
RMS Continuous, I_D	14 A
Pulsed, I_{DM}	35 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}*	100 mj
AVALANCE CURRENT, I_{AS}	14 A
POWER DISSIPATION, P_T:	
At T_C = 25°C	40 W
Derate above T_C = 25°C	0.32 W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150°C

*V_{DD} = 10 volts, starting T_j = 25°C, L = 820 μHy I_{peak} = 14A, see figures 12 and 13.

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150° C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 10 V		—	0.1	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A I_{g1} = I_{g2} = 0.2 A V_{GS} (clamp) + 10 V, - 0.6 V R_L = 3.57 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	14 (typ.)	
Rise Time	t_r			—	26 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	45 (typ.)	
Fall Time	t_f			—	17 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	$Q_g(total)$	V_{DD} = 40 V	V_{GS} = 0-20 V	—	40	nC
Gate Charge at 10 V	$Q_g(10)$	I_D = 14 A	V_{GS} = 0-10 V	—	25	
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-2 V	—	1.5	
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, R_L = 0.2 μH R_L = 3.57 Ω, I_{g1} = I_{g2} = 0.2 A V_{GS} (clamp) + 10 V, -0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	
		TO-220		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/dt = 100 A/μs	—	125	ns

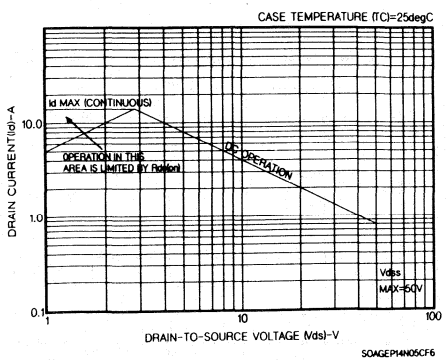


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

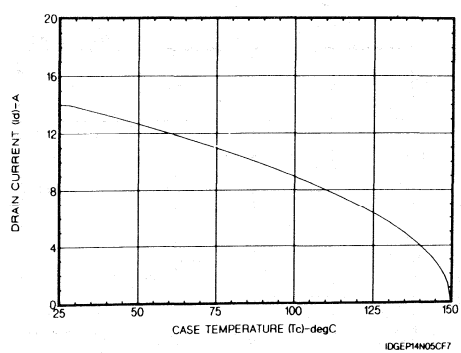


Fig. 2 - Maximum continuous drain current vs. temperature.

RFD14N05, RFD14N05SM, RFP14N05

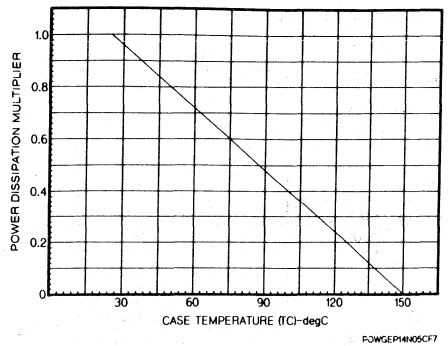


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

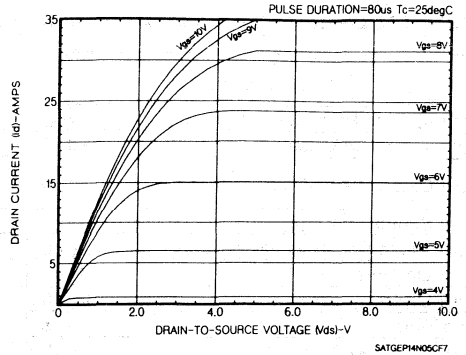


Fig. 4 - Typical saturation characteristics.

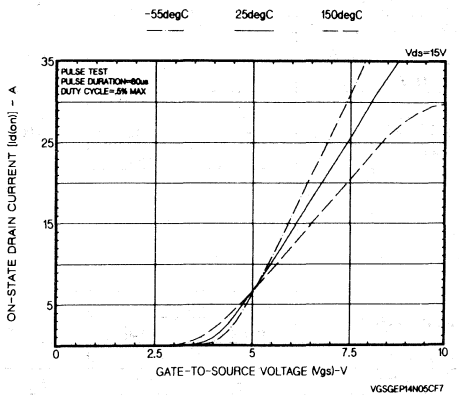


Fig. 5 - Typical transfer characteristics.

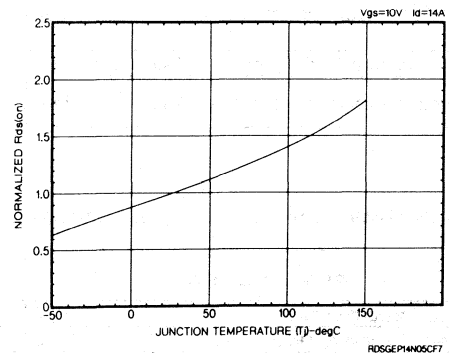


Fig. 6 - Normalized $R_{ds}(on)$ vs. junction temperature.

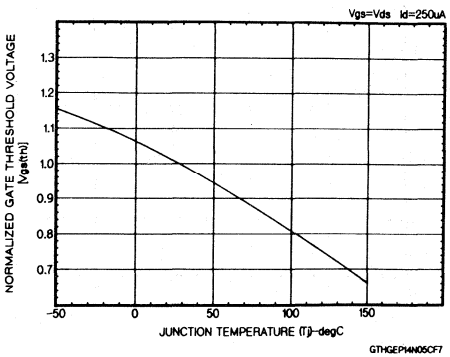


Fig. 7 - Normalized gate threshold voltage.

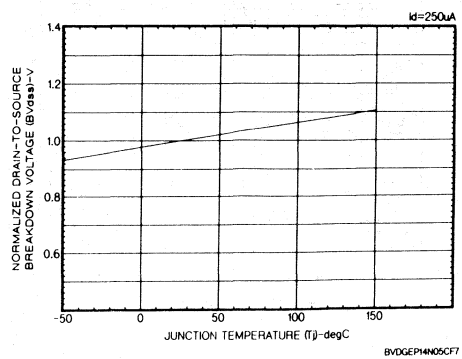


Fig. 8 - Normalized drain source breakdown voltage vs. temperature.

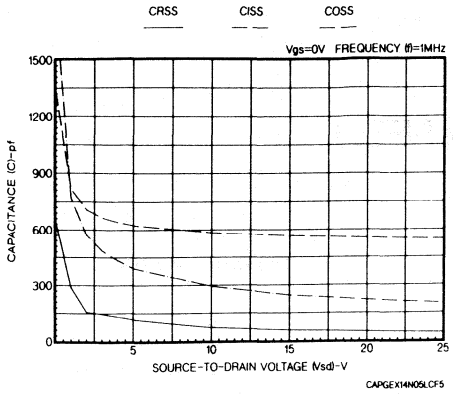


Fig. 9 - Typical capacitance vs. voltage.

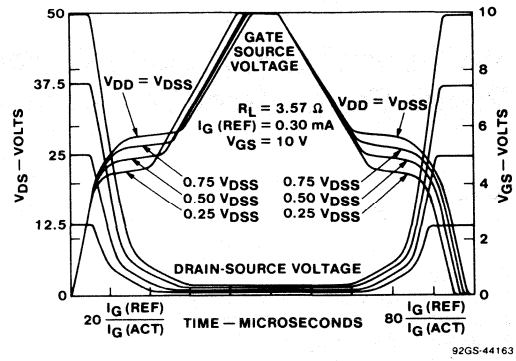


Fig. 10 - Normalized switching waveforms for constant gate-current. (Refer to RCA application notes AN-7254 and AN-7260.)

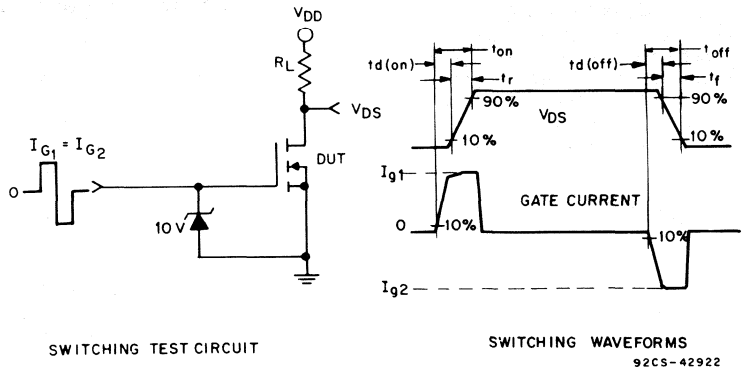


Fig. 11 - Resistive switching.

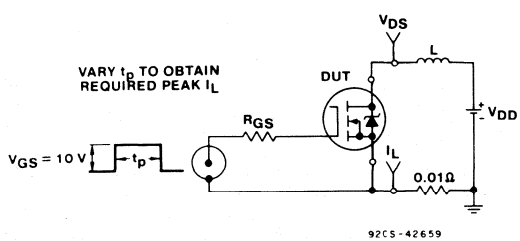


Fig. 12 - Unclamped energy test circuit.

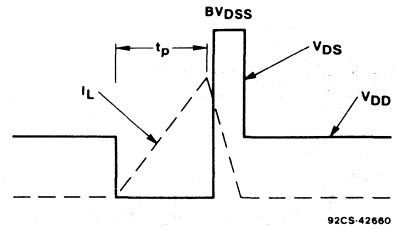


Fig. 13 - Unclamped energy waveforms.

RFD16N05, RFD16N05SM

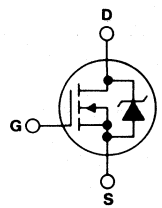
File Number **2267**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

16 A, 50 V
$r_{ds(on)}$ = 0.047 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



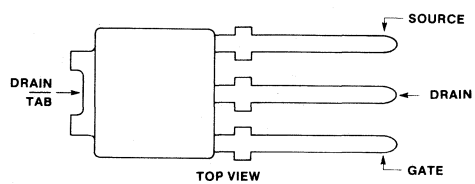
92CS-42658

N-CHANNEL ENHANCEMENT MODE

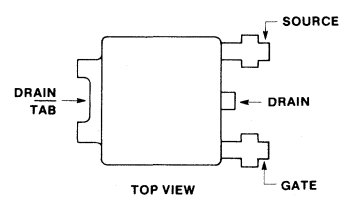
The RFD16N05 and RFD16N05SM n-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFD16N05 is supplied in the JEDEC TO-251 plastic package and the RFD16N05SM in the JEDEC TO-252 plastic package.

TERMINAL DESIGNATION



TO-251AA



TO-252AA

92CS-43478

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c = 25°C):*

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{ge} = 1 MΩ)	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±20 V
DRAIN CURRENT:	
•I_D, RMS Continuous	16 A
I_{DM}, Pulsed	45 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}*	200 mj
AVALANCE CURRENT, I_{AS}	16 A
POWER DISSIPATION P_T:	
At T_C = 25°C	60 W
Derated above T_C = 25°C	0.48 W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150°C

•ID Current Limited by package.
*V_{DD} = 10 volts, starting T_j = 25°C, L = 1.25 mHy I_{peak} = 16A, see figures 12 and 13.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		—	1	μA
		T_C = 150°C			50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 16 A, V_{GS} = 10 V		—	0.047	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 8 A		—	60	ns
Turn-On Delay Time	$t_d(on)$	I_{g1} = I_{g2} = 0.4 A		—	14 (typ.)	
Rise Time	t_r	V_{GS} (clamp) + 10 V, - 0.6 V		—	30 (typ.)	
Turn-Off Delay Time	$t_d(off)$	R_L = 3.125 Ω		—	52 (typ.)	
Fall Time	t_f			—	16 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{GS} = 0-20 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 10 V	$Q_g(10)$	V_{GS} = 0-10 V	I_D = 16 A	—	45	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-2 V	R_L = 2.5 Ω	—	3	
Plateau Voltage	V(plateau)	I_D = 16 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 8 A, R_L = 3.125 Ω L = 0.2 μH, I_{g1} = I_{g2} = 0.4 A V_{GS} (clamp) + 10 V, -0.6 V		—	19	μJ
Thermal Resistance, Junction to Case	$R\theta_{JC}$			—	2.083	°C/W
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$			—	100	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16 A, dI_F/d_t = 100 A/μs	—	125	ns

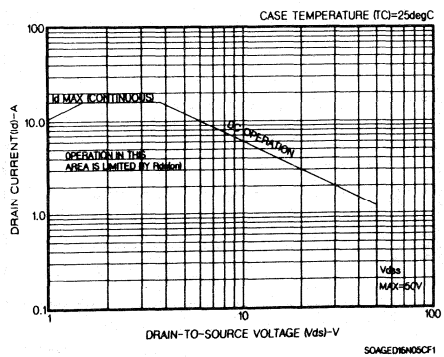


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

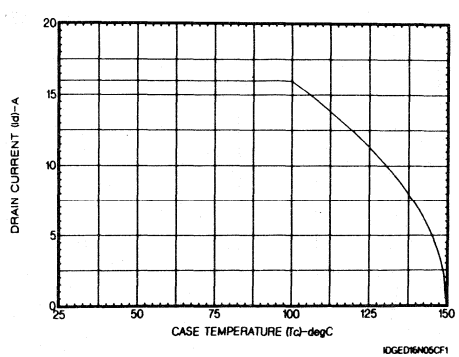


Fig. 2 - Maximum continuous drain current vs. temperature.

RFD16N05, RFD16N05SM

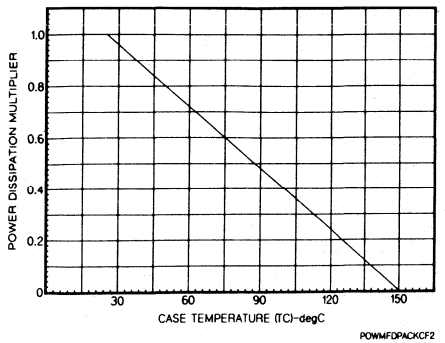


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

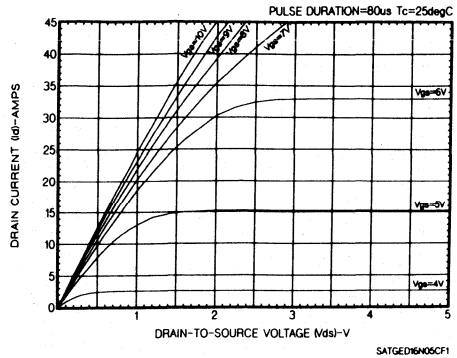


Fig. 4 - Typical saturation characteristics.

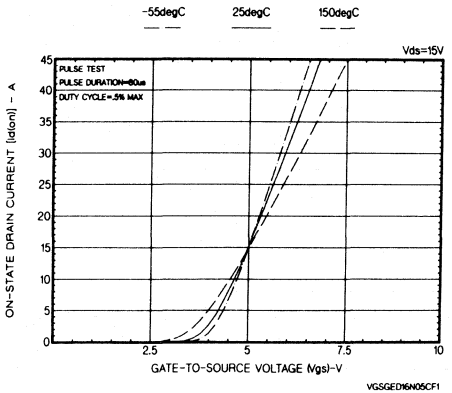


Fig 5 - Typical transfer characteristics.

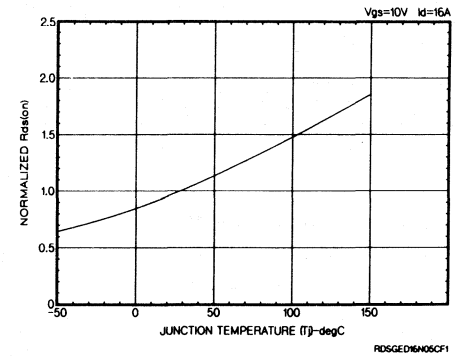


Fig 6 - Normalized $R_{ds(on)}$ vs. junction temperature.

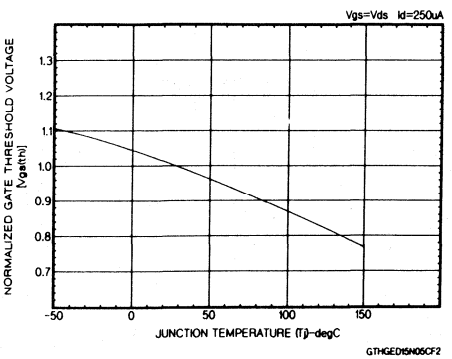


Fig. 7 - Normalized gate threshold voltage.

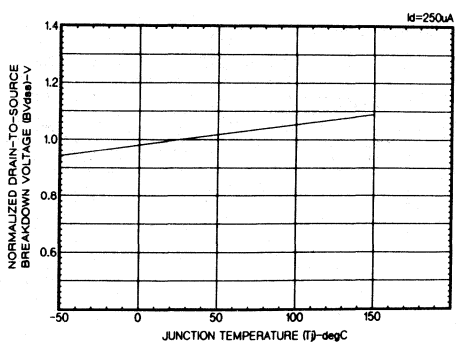


Fig. 8 - Normalized drain source breakdown voltage vs. temperature.

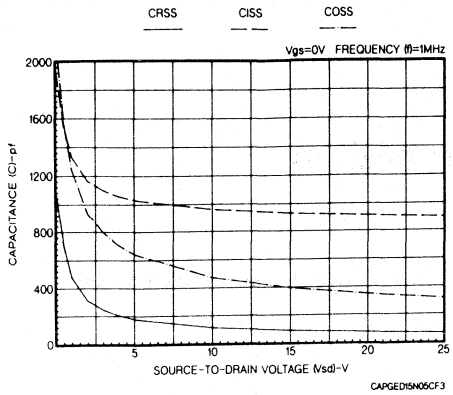


Fig. 9 - Typical capacitance vs. voltage.

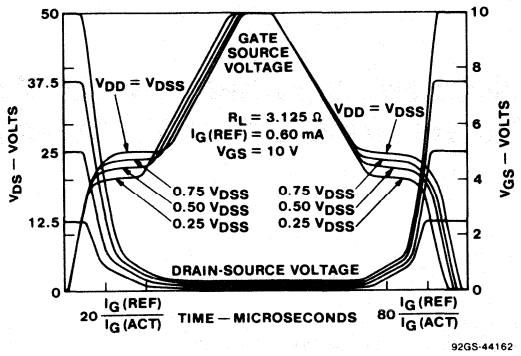


Fig. 10 - Normalized switching waveforms for constant gate current. (Refer to RCA application notes AN-7254 and AN-7260.)

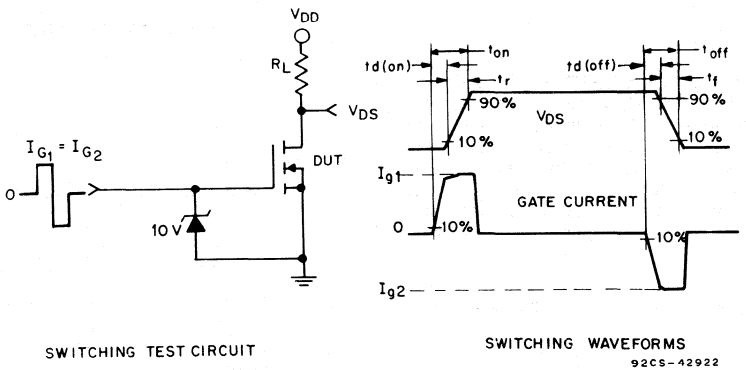


Fig. 11 - Resistive switching.

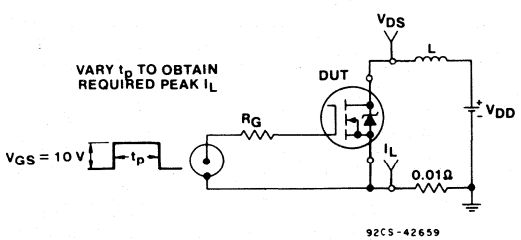


Fig. 12 - Unclamped energy test circuit.

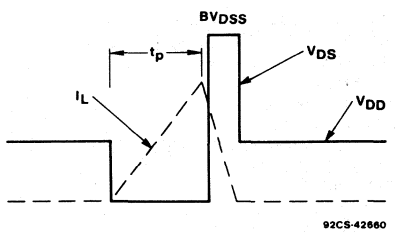


Fig. 13 - Unclamped energy waveforms.

RFG50N05

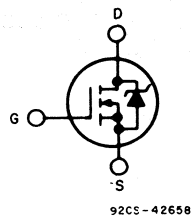
File Number **2197**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

50 A, 50 V
$r_{DS}(on)$ = 0.022 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

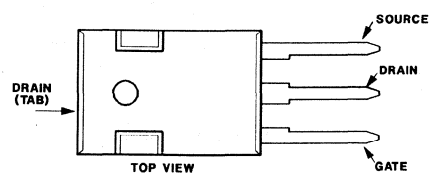


TERMINAL DIAGRAM

The RFG50N05 n-channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFG50N05 was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFG50N05 is supplied in the TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

DRAIN-SOURCE VOLTAGE, V_{DSS} ..... 50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{GS} = 1 MΩ) ..... 50 V
GATE-SOURCE VOLTAGE, V_{GS} ..... ±20 V
DRAIN CURRENT:
- I_D, RMS Continuous ..... 50 A
- I_{DM}, Pulsed * ..... 120 A

SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}• ..... 400 mj
AVALANCHE CURRENT, I_{AS} ..... 50 A
POWER DISSIPATION, P_T:
- At T_C = 25°C ..... 110 W
- Derated above T_C = 25°C ..... 0.88 W/°C

OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg} ..... -55 to +150°C

•V_{DD}=10 V, starting T_j=25°C, L=250 μH, R_{GS}=50 Ω, I_{peak}=50 A. See Figs. 12 and 13.

*I_{DM} will also be changed in the near future.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFG50N05 MIN.	LIMITS RFG50N05 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=0.25 mA, V_{GS}=0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V		—	1	μA
		T_C=150° C		—	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D=50 A, V_{GS}=10 V		—	0.022	Ω
Turn-On Time	t(on)	V_{DD}=25 V, I_D=25 A I_{g1}=I_{g2}=1.5 A V_{GS} (clamp) + 10 V, -0.6 V R_L=1 Ω (See Figs. 10 and 11)		—	100	ns
Turn-On Delay Time	$t_d(on)$			—	15(typ.)	ns
Rise Time	t_r			—	55(typ.)	ns
Turn-Off Delay Time	$t_d(off)$			—	60(typ.)	ns
Fall Time	t_f			—	15(typ.)	ns
Turn-Off Time	t(off)			—	100	ns
Total Gate Charge	Q_g(total)	V_{DD} = 40 V I_D = 50 A R_L = 0.8 Ω	V_{GS} = 0 - 20 V	—	170	nC
Gate Charge at 10 V	$Q_g(10)$		V_{GS} = 0 - 10 V	—	80	nC
Threshold Gate Charge	$Q_g(th)$		V_{GS} = 0 - 2 V	—	6	nC
Plateau Voltage	V(plateau)	I_D=50 A, V_{DS}=15 V		—	7.5	V
Turn-Off Energy Loss Per Cycle	E_{off}	I_D=25 A, R_L=1 Ω, L=0.2 μH I_{g1}=I_{g2}=1.5 A, V_{DD} = 25 V V_{GS}(clamp) +10 V, -0.6 V		—	150	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	1.14	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS RFG50N05 MIN.	LIMITS RFG50N05 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=50 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F=50 A, d_{IF}/d_t=100 A/μs	—	125	ns

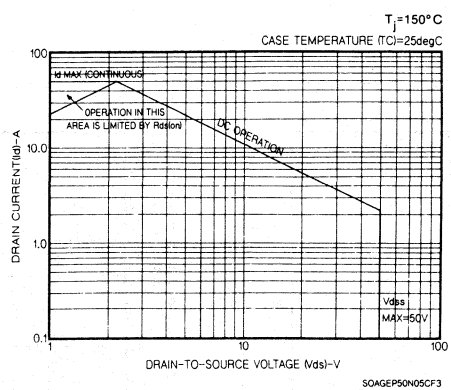


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

RFG50N05

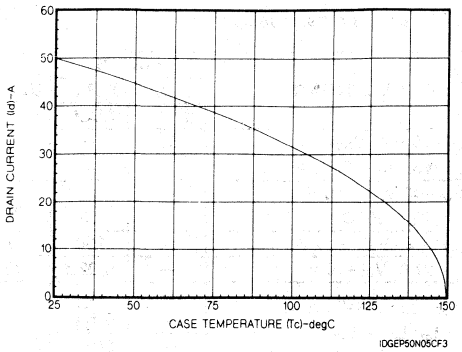


Fig. 2 - Maximum continuous drain current vs temperature.

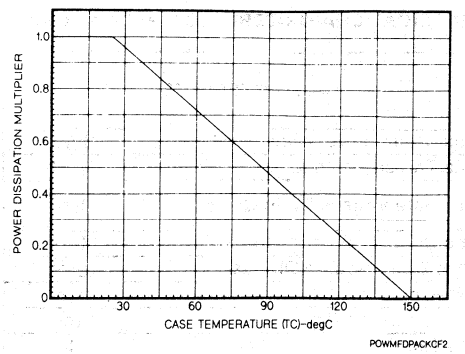


Fig. 3 - Normalized power dissipation vs temperature derating curve.

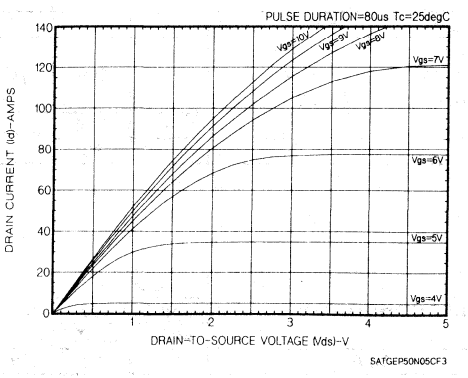


Fig. 4 - Typical saturation characteristics.

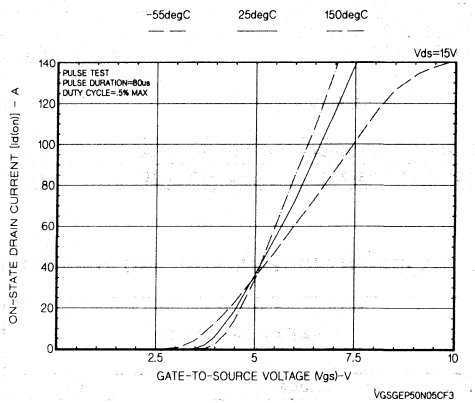


Fig. 5 - Typical transfer characteristics.

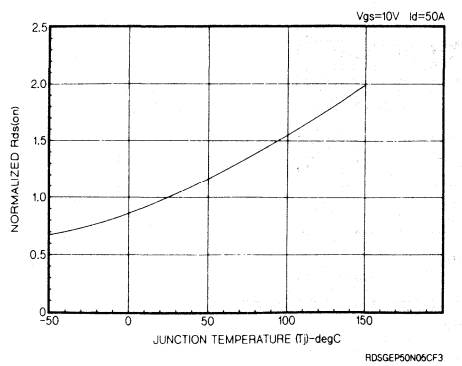


Fig. 6 - Normalized $r_{DS}(on)$ vs junction temperature.

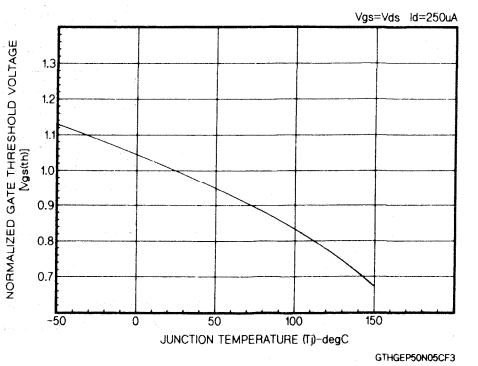


Fig. 7 - Typical normalized gate threshold voltage.

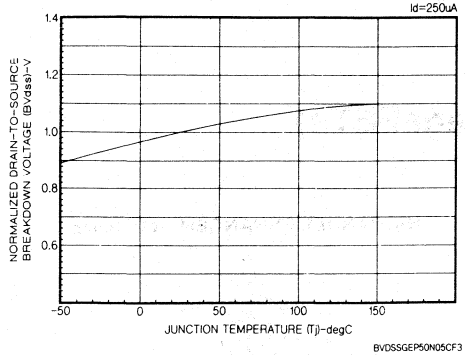


Fig. 8 - Drain source breakdown voltage vs temperature.

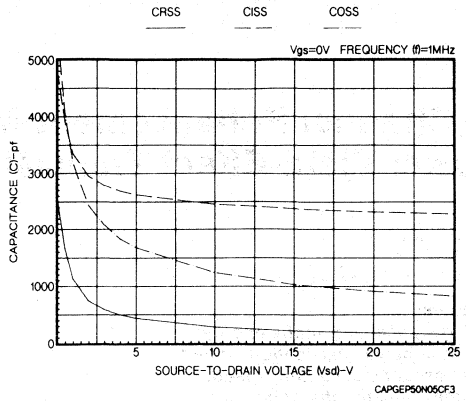


Fig. 9 - Typical capacitance vs voltage.

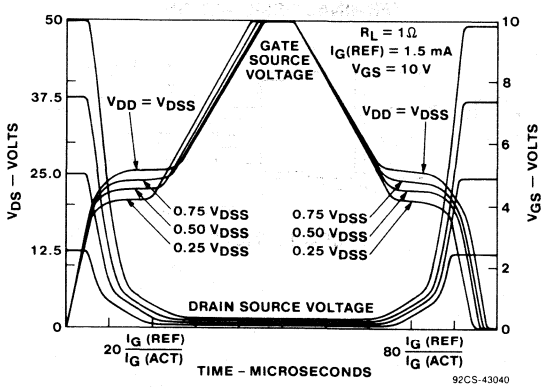


Fig. 10 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN7254 and AN7260.

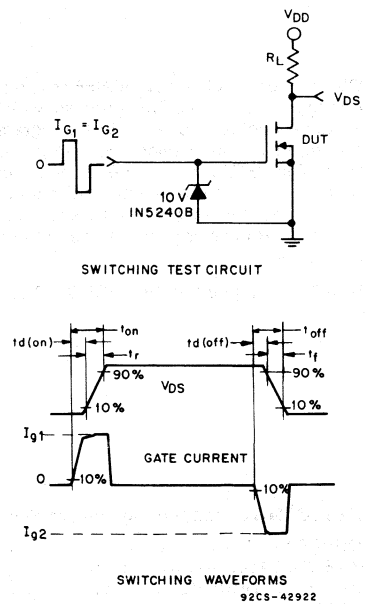


Fig. 11 - Resistive switching.

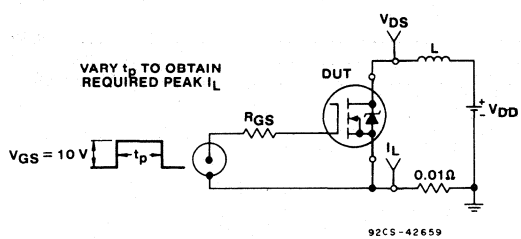


Fig. 12 - Unclamped energy test circuit.

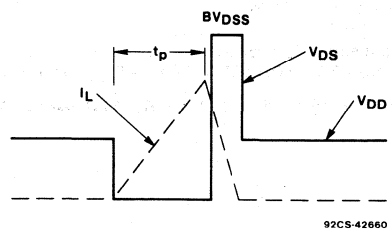


Fig. 13 - Unclamped energy waveforms.

RFP25N05

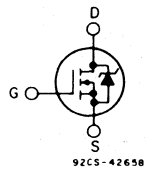
File Number **2112**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

25 A, 50 V
$r_{DS}(on)$ = 0.047 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

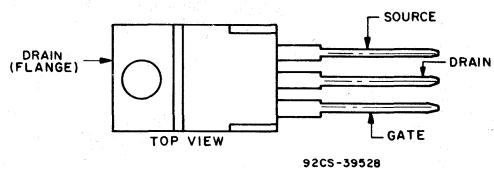


TERMINAL DIAGRAM

The RFP25N05 n-channel power MOSFETs is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05 was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFP25N05 is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{gs} = 1 MΩ)	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±20 V
DRAIN CURRENT:	
I_D, RMS Continuous	25 A
I_{DM}, Pulsed	65 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}•	200 mj
AVALANCHE CURRENT, I_{AS}	25 A
POWER DISSIPATION, P_T:	
At T_C = 25°C	60 W
Derated above T_C = 25°C	0.48 W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C

•V_{DD}=10 V, starting T_j=25°C, L=2 mH, R_{gs}=50 Ω, I_{peak}=25 A. See Figs. 12 and 13.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFP25N05 MIN.	LIMITS RFP25N05 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=0.25 mA, V_{GS}=0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=0.25 mA		2	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V		—	1	μA
		T_C=150°C		—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D=25 A, V_{GS}=10 V		—	0.047	Ω
Turn-On Time	t(on)	V_{DD}=25 V, I_D=12.5 A I_{g1}=I_{g2}=0.5 A V_{GS} (clamp) + 10 V, -0.6 V R1=2 Ω (See Figs. 10 and 11)		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	14 (typ.)	
Rise Time	t_r			—	30 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	45 (typ.)	
Fall Time	t_f			—	14 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	$Q_g(total)$	V_{DD} = 40 V I_D = 25 A R_L = 1.6 Ω	V_{GS} = 0 - 15 V	—	80	nC
Gate Charge at 10 V	$Q_g(10)$		V_{GS} = 0 - 10 V	—	45	
Threshold Gate Charge	$Q_g(th)$		V_{GS} = 0 - 2 V	—	3	
Plateau Voltage	V(plateau)	I_D=25 A, V_{DS}=15 V		—	7.5	V
Turn-Off Energy Loss Per Cycle	E_{off}	I_D = 12.5 A, R_L = 2Ω, L = 0.2 μH V_{DD} = 25 V, I_{g1} = I_{g2} = 0.5 A V_{GS} (clamp) + 10V, -0.6 V		—	30	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS RFP25N05 MIN.	LIMITS RFP25N05 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=25 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F=25 A, dI_F/d_t = 100 A/μs	—	125	ns

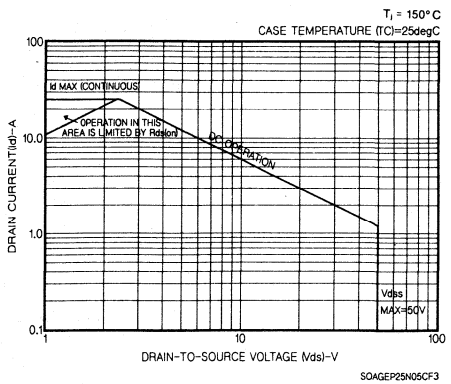


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

RFP25N05

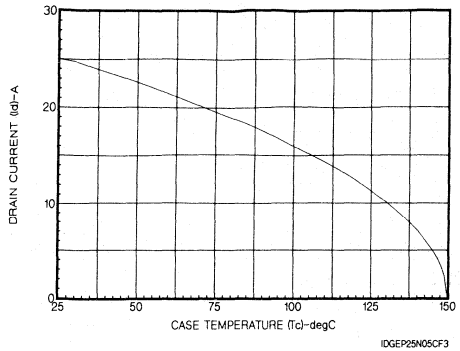


Fig. 2 - Maximum continuous drain current vs temperature.

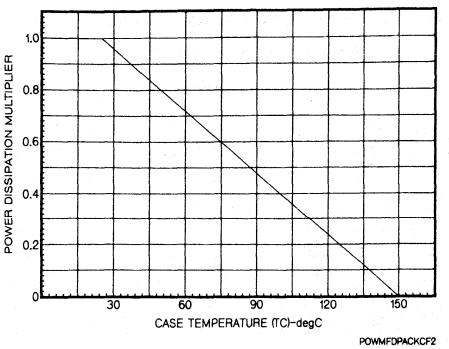


Fig. 3 - Normalized power dissipation vs temperature derating curve.

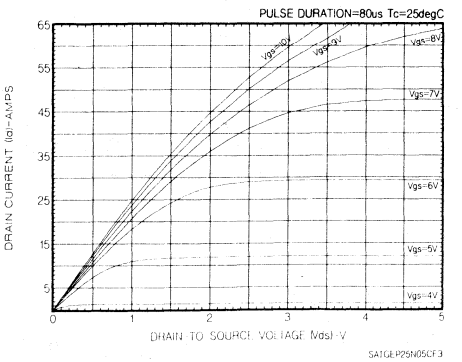


Fig. 4 - Typical saturation characteristics.

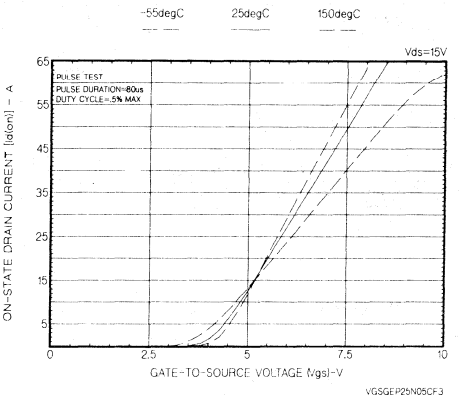


Fig. 5 - Typical transfer characteristics.

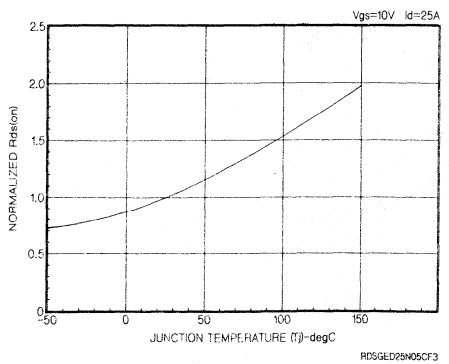


Fig. 6 - Normalized $r_{DS}(on)$ vs junction temperature.

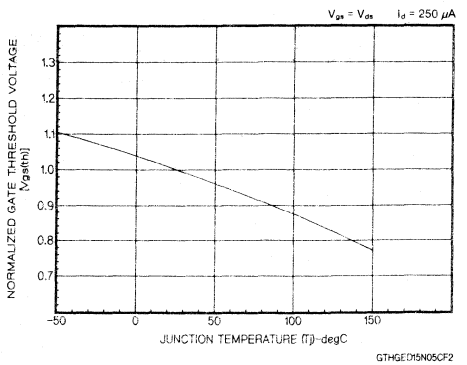


Fig. 7 - Typical normalized gate threshold voltage.

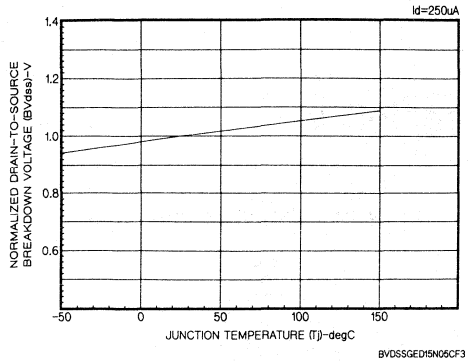


Fig. 8 - Drain source breakdown voltage vs temperature.

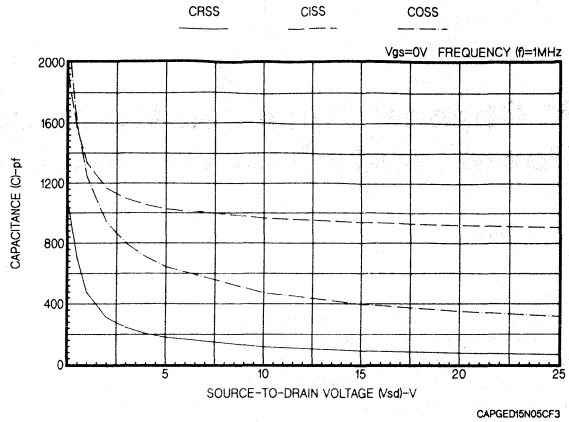


Fig. 9 - Typical capacitance vs voltage.

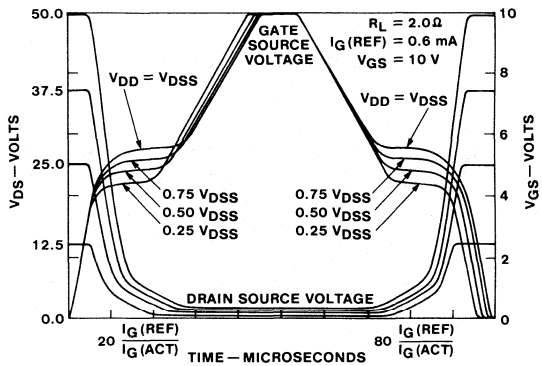


Fig. 10 - Normalized switching waveforms for constant gate-current.
(Refer to RCA application notes AN-7254 and AN-7260.)

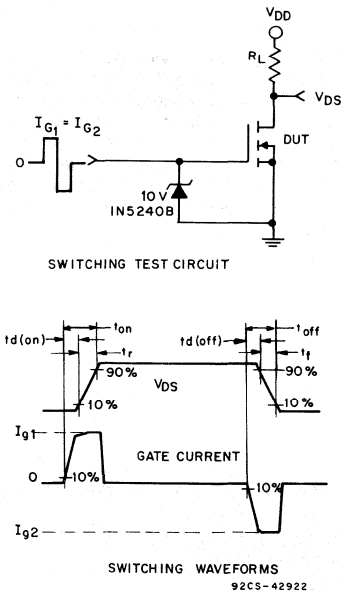


Fig. 11 - Resistive switching.

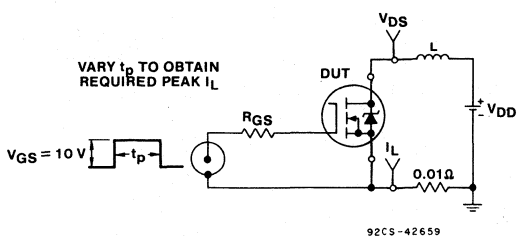


Fig. 12 - Unclamped energy test circuit.

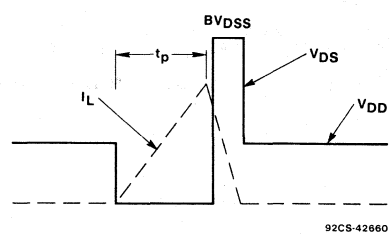


Fig. 13 - Unclamped energy waveforms.

RFP50N05

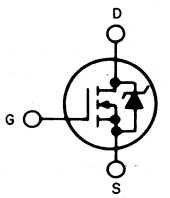
File Number **2119**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

50 A, 50 V
$r_{DS}(on)$ = 0.022 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



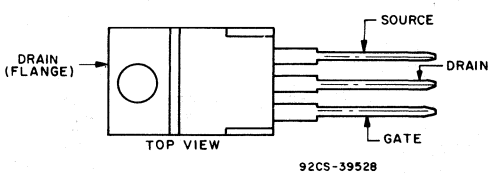
92CS-42658

TERMINAL DIAGRAM

The RFP50N05 n-channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFP50N05 was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFP50N05 is supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

DRAIN-SOURCE VOLTAGE, V_{DSS} ..... 50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{gs} = 1 MΩ) ..... 50 V
GATE-SOURCE VOLTAGE, V_{GS} ..... ±20 V
DRAIN CURRENT:
- I_D, RMS Continuous ..... 50 A
- I_{DM}, Pulsed ..... 120 A

SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}• ..... 400 mj
AVALANCHE CURRENT, I_{AS} ..... 50 A
POWER DISSIPATION, P_T:
- At T_C = 25°C ..... 110 W
- Derated above T_C = 25°C ..... 0.88 W/°C

OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg} ..... -55 to +150°C

•V_{DD}=10 V, starting T_j=25°C, L=250 μH, R_{gs}=50 Ω, I_{peak}=50 A. See Figs. 12 and 13.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFP50N05 MIN.	LIMITS RFP50N05 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=0.25 mA, V_{GS}=0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V		—	1	μA
		T_C=150° C		—	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D=50 A, V_{GS}=10 V		—	0.022	Ω
Turn-On Time	t(on)	V_{DD}=25 V, I_D=25 A		—	100	ns
Turn-On Delay Time	$t_d(on)$	I_{g1}=I_{g2}=1.5 A		—	15(typ.)	ns
Rise Time	t_r	V_{GS} (clamp) + 10 V, -0.6 V		—	55(typ.)	ns
Turn-Off Delay Time	$t_d(off)$	R1=1 Ω		—	60(typ.)	ns
Fall Time	t_f	(See Figs. 10 and 11)		—	15(typ.)	ns
Turn-Off Time	t(off)			—	100	ns
Total Gate Charge	$Q_g(total)$	V_{DD} = 40 V, I_D = 50 A, R_L = 0.8 Ω	V_{GS} = 0 - 15 V	—	140	nC
Gate Charge at 10 V	$Q_g(10)$		V_{GS} = 0 - 10 V	—	80	nC
Threshold Gate Charge	$Q_g(th)$		V_{GS} = 0 - 2 V	—	6	nC
Plateau Voltage	V(plateau)	I_D=50 A, V_{DS}=15 V		—	7.5	V
Turn-Off Energy Loss Per Cycle	E_{off}	I_D=25 A, R1=1 Ω, L=0.2 μH I_{g1}=I_{g2}=1.5 A, V_{DD} = 25 V V_{GS}(clamp) +10 V, -0.6 V		—	150	μJ
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$			—	1.14	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$			—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS RFP50N05 MIN.	LIMITS RFP50N05 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=50 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F=50 A, dI_F/d_t = 100 A/μs	—	125	ns

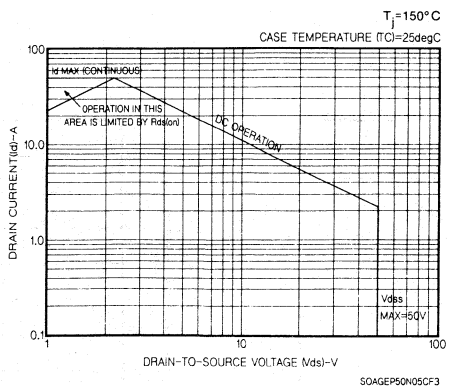


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

RFP50N05

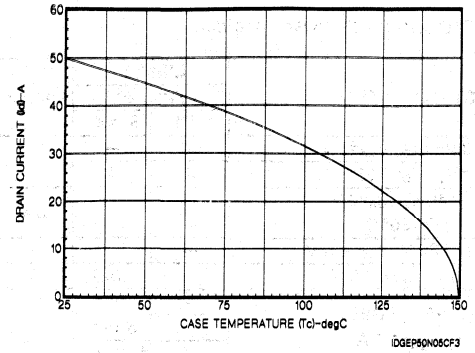


Fig. 2 - Maximum continuous drain current vs temperature.

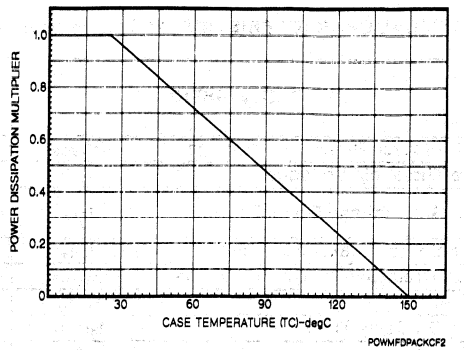


Fig. 3 - Normalized power dissipation vs temperature derating curve.

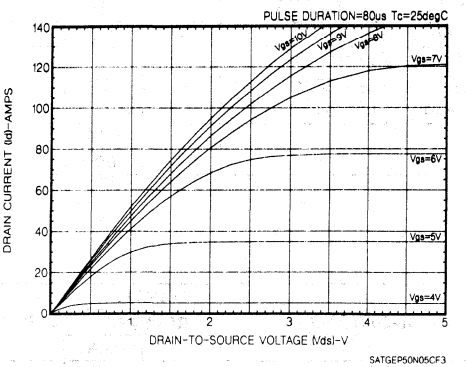


Fig. 4 - Typical saturation characteristics.

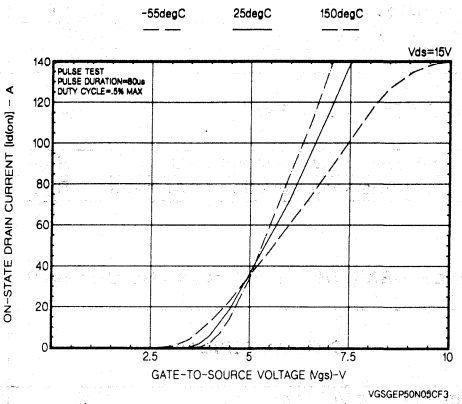


Fig. 5 - Typical transfer characteristics.

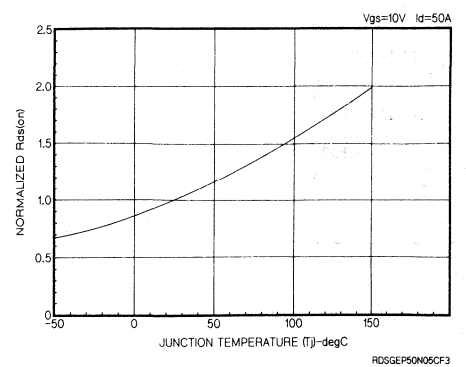


Fig. 6 - Normalized $r_{DS}(on)$ vs junction temperature.

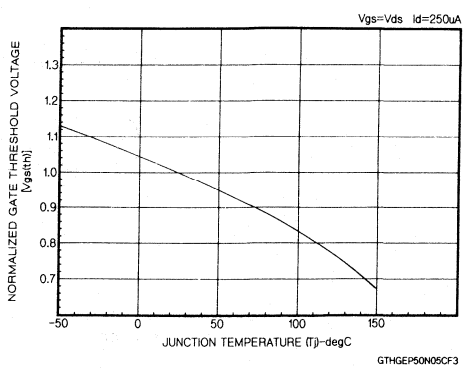


Fig. 7 - Typical normalized gate threshold voltage.

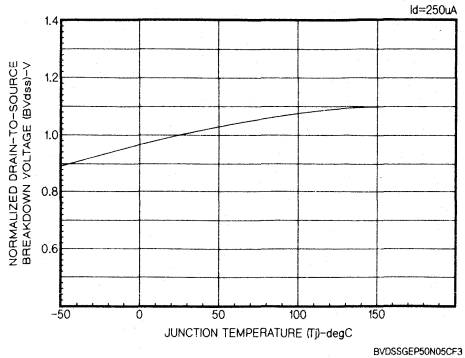


Fig. 8 - Drain source breakdown voltage vs temperature.

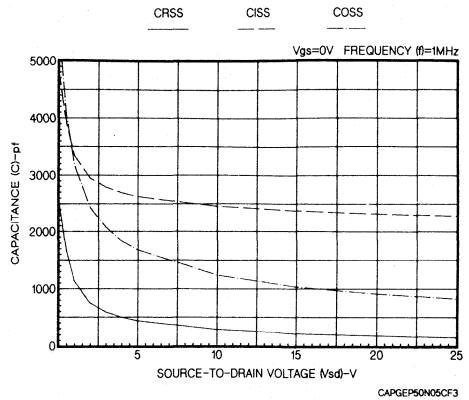


Fig. 9 - Typical capacitance vs voltage.

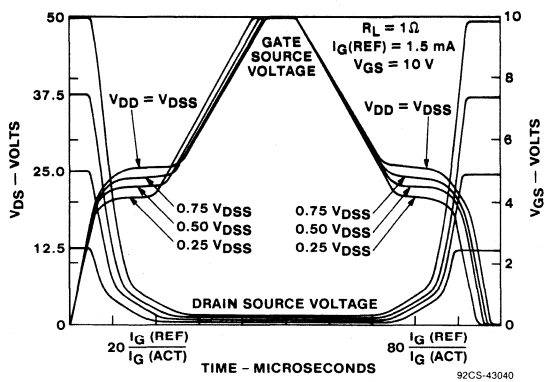


Fig. 10 - Normalized switching waveforms for constant gate-current. (Refer to RCA application notes AN7254 and AN7260.)

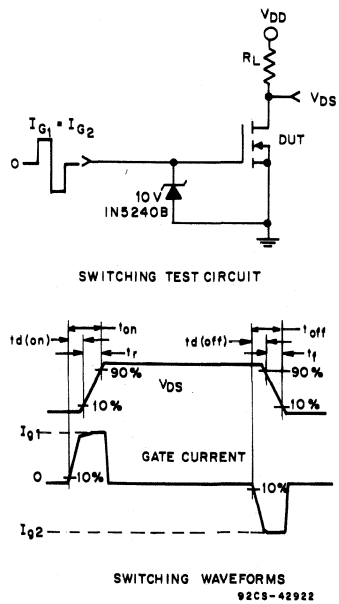


Fig. 11 - Resistive switching.

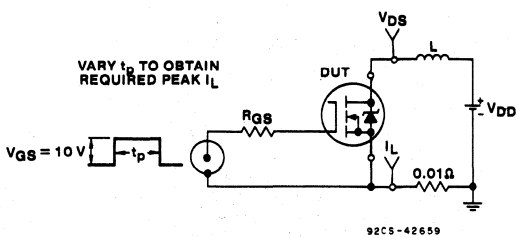


Fig. 12 - Unclamped energy test circuit.

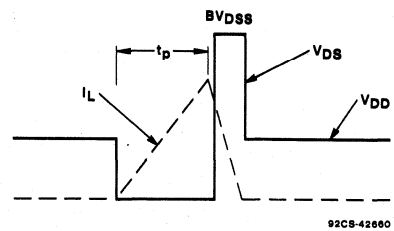


Fig. 13 - Unclamped energy waveforms.

Logic Level Power MOSFETs (L^2FETs)

L^2MegaFETs 5-2
Standard Power L^2FETs 5-16
Current Limited-ESD Protected L^2FETs 5-57
JEDEC (L^2FETs) 5-63

RFD14N05L, RFD14N05LSM, RFP14N05L

File Number **2246**

N-Channel Logic-Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

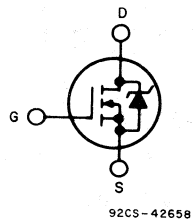
14 A, 50 V
$r_{DS}(on)$: 0.1 Ω

Features
- *Design optimized for 5-volt gate drive*
- *Can be driven directly from QMOS, NMOS, TTL circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFD14N05L, RFD14N05LSM, and RFP14N05L n-channel logic-level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5 volt) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor-relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate-oxide design which provides fully rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFD14N05L is supplied in the JEDEC TO-251 plastic package and the RFD14N05LSM is supplied in the JEDEC TO-252 surface-mount plastic package. The RFP14N05L is supplied in the JEDEC TO-220AB plastic package.

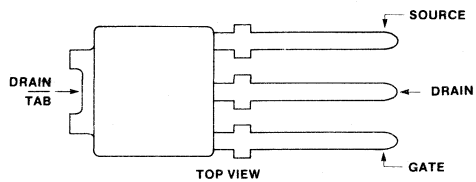
N-CHANNEL ENHANCEMENT MODE



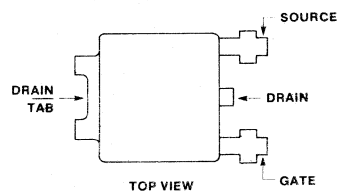
92CS-42658

TERMINAL DIAGRAM

TERMINAL DESIGNATION



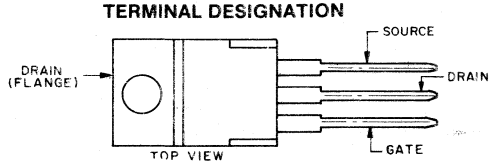
JEDEC TO-251AA



JEDEC TO-252AA

92CS-43478

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25° C):

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ, V_{DGR}	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±10 V
DRAIN CURRENT:	
RMS Continuous, I_D	14 A
Pulsed, I_{DM}	35 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}	100 mj
AVALANCHE CURRENT, I_{AS}	14 A
POWER DISSIPATION, P_T:	
At T_C=25° C	40 W
Derate above T_C=25° C	0.32 W/° C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150° C

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25° C Unless Otherwise Specified.

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		—	1	μA
		T_C = 150° C		—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 5 V		—	0.1	Ω
		I_D = 14 A, V_{GS} = 4 V		—	0.12	
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A		—	60	ns
Turn-On Delay Time	$t_d(on)$	I_{g1} = I_{g2} = 0.4 A		—	13 (typ.)	
Rise Time	t_r	V_{GS}(clamp) +5 V, -0.6 V		—	24 (typ.)	
Turn-Off Delay Time	$t_d(off)$	R_L = 3.57 Ω		—	42 (typ.)	
Fall Time	t_f	(See Figs. 10 & 11)		—	16 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{DD} = 40 V	V_{GS} = 0-10 V	—	40	nC
Gate Charge at 5 V	$Q_g(5)$	I_D = 14 A	V_{GS} = 0-5 V	—	25	
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-1 V	—	1.5	
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss Per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, L = 0.2 μH, R_L = 3.57 Ω, i_{g1} = I_{g2} = 0.2 A, V_{GS}(clamp) +5 V, -0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	
		TO-220		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/d_t = 100 A/μs	—	125	ns

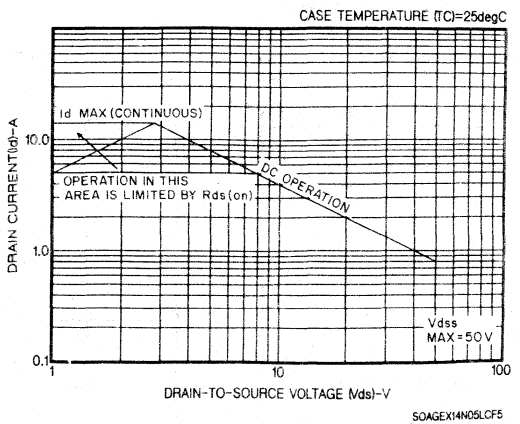


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

RFD14N05L, RFD14N05LSM, RFP14N05L

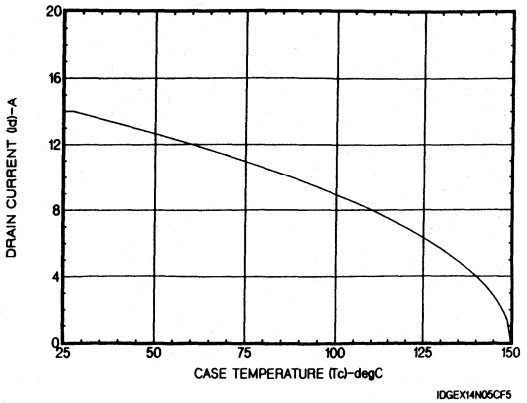


Fig. 2 - Maximum continuous drain current vs. temperature.

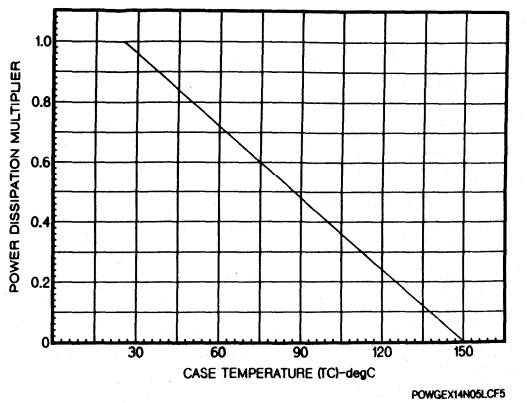


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

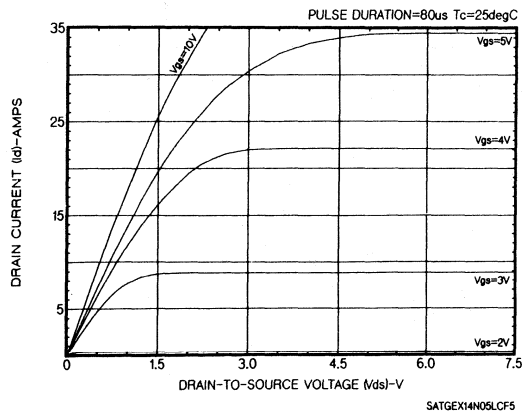


Fig. 4 - Typical saturation characteristics.

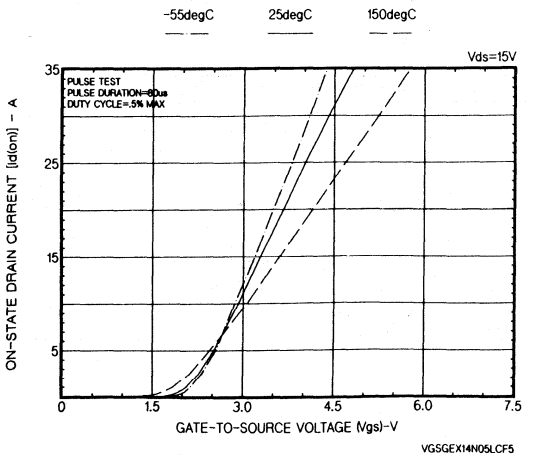


Fig. 5 - Typical transfer characteristics.

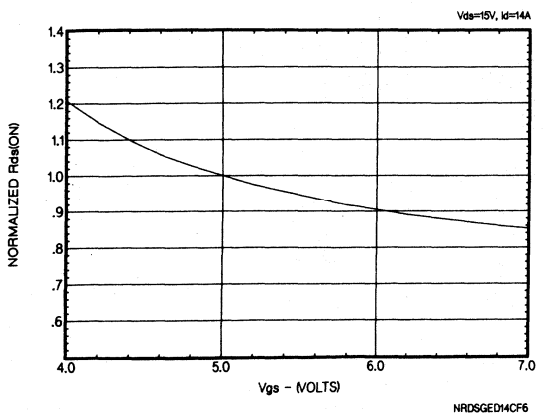


Fig. 6 - Normalized $r_{DS}(on)$ vs. V_{gs}.

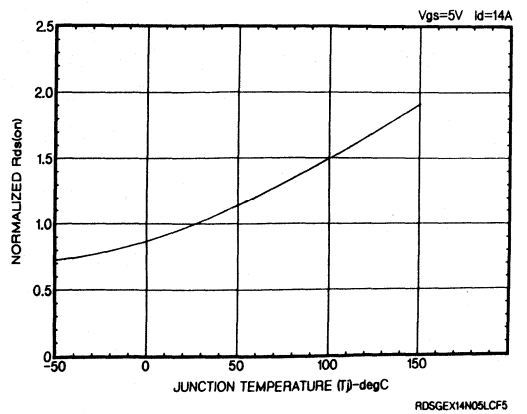


Fig. 7 - Normalized $r_{DS}(on)$ vs. junction temperature.

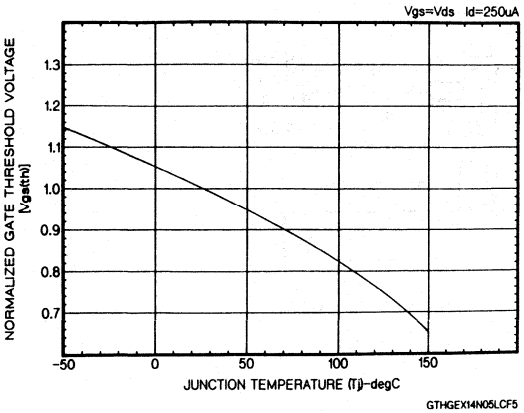


Fig. 8 - Gate threshold voltage vs. temperature.

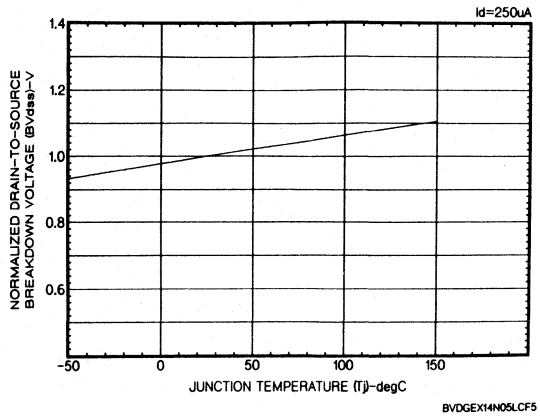


Fig. 9 - Drain source breakdown voltage vs. temperature.

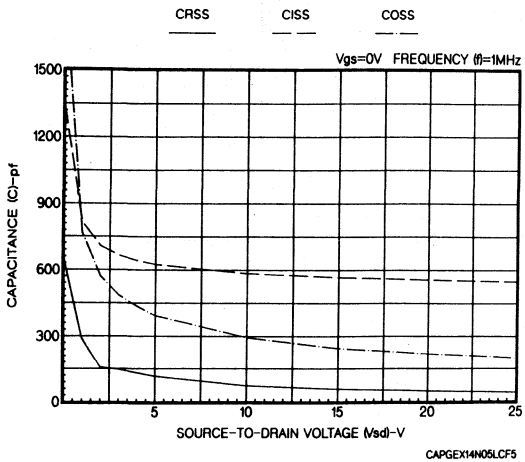


Fig. 10 - Typical capacitance vs. voltage.

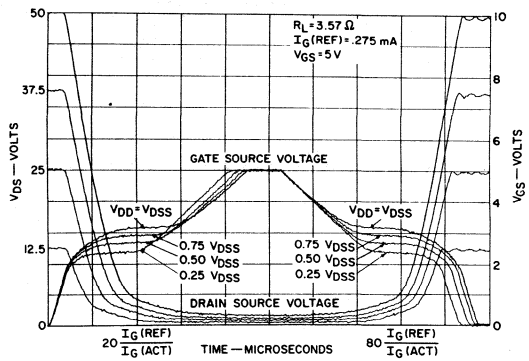


Fig. 11 - Normalized switching waveforms for constant gate current. (Refer to RCA application notes AN-7254 and AN7260.)

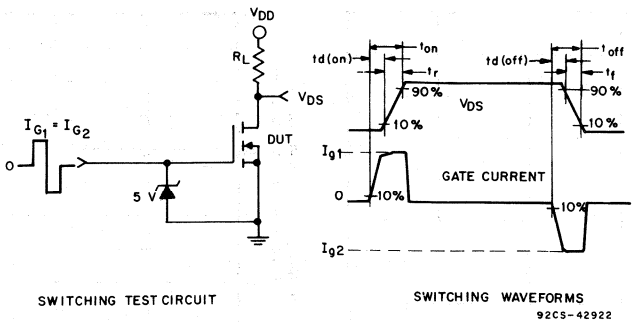


Fig. 12 - Resistive switching.

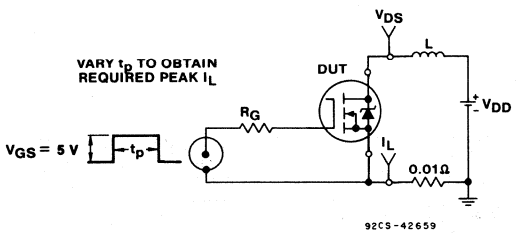


Fig. 13 - Unclamped energy test circuit.

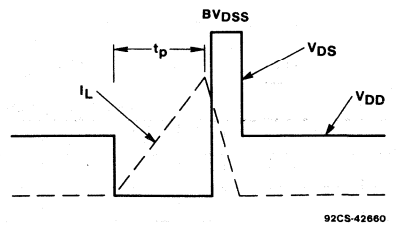


Fig. 14 - Unclamped energy waveforms.

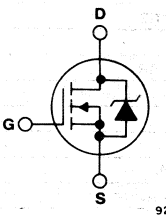
File Number **2269**

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

16 A, 50 V
$r_{ds(on)}$ = 0.047 Ω

Features:
- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



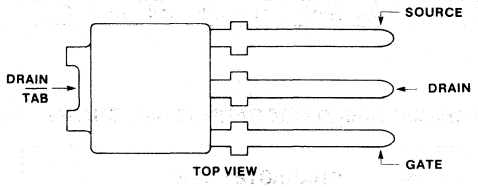
92CS-42658

N-CHANNEL ENHANCEMENT MODE

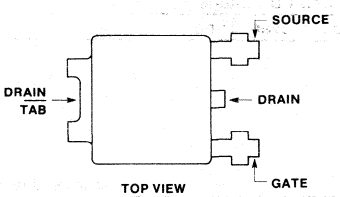
The RFD16N05L and RFD16N05LSM n-channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor-relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFD16N05L is supplied in the JEDEC TO-251 plastic package and the RFD16N05LSM in the JEDEC TO-252 plastic package.

TERMINAL DESIGNATION



TO-251AA



TO-252AA

92CS-43478

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c = 25° C):*

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{GE} = 1MΩ)	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±10 V
DRAIN CURRENT:	
•I_D, RMS Continuous	16 A
I_{DM}, Pulsed	45 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}†	200 mj
AVALANCHE CURRENT, I_{AS}	16 A
POWER DISSIPATION P_T:	
At T_C = 25°C	60 W
Derated above T_C = 25°C	0.48 W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C

•ID Current Limited by package.
†V_{DD} = 10 V, starting T_j = 25°C, L = 1.25 mHy, I_{peak} = 16 A. See Figs. 13 and 14.

RFD16N05L, RFD16N05LSM

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25 mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150° C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS(on)}$	I_D = 16 A, V_{GS} = 5 V I_D = 16 A, V_{GS} = 4 V		—	0.047 0.056	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 8 A $I_{g1} = I_{g2}$ = 0.8 A V_{GS} (clamp) + 5 V, − 0.6 V R_L = 3.125 Ω		—	60	ns
Turn-On Delay Time	$t_{d(on)}$			—	15 (typ.)	
Rise Time	t_r			—	30 (typ.)	
Turn-Off Delay Time	$t_{d(off)}$			—	42 (typ.)	
Fall Time	t_f			—	14 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{GS} = 0-10 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 5 V	Q_g(5)	V_{GS} = 0-5 V	I_D = 16 A	—	45	
Threshold Gate Charge	Q_g(th)	V_{GS} = 0-1 V	R_L = 2.5 Ω	—	3	
Plateau Voltage	V(plateau)	I_D = 16 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 8 A, R_L = 3.125 Ω L = 0.2 μH, $I_{g1} = I_{g2}$ = 0.8 A V_{GS} (clamp) + 5 V, −0.6 V		—	19	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			—	100	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16 A, dI_F/d_t = 100 A/μs	—	125	ns

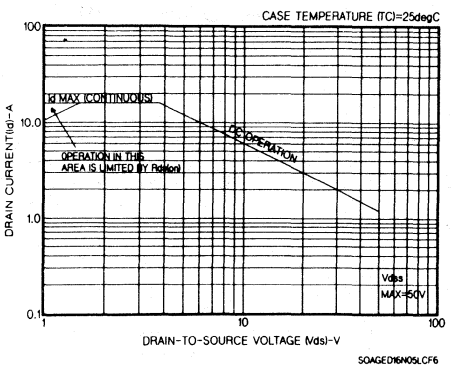


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

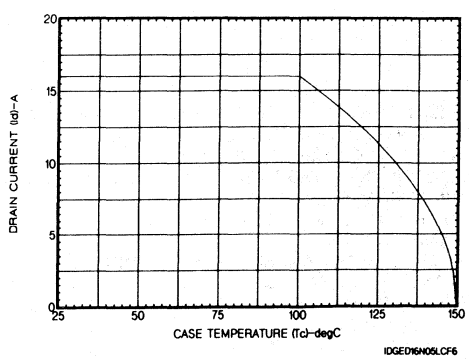


Fig. 2 - Maximum continuous drain current vs. temperature.

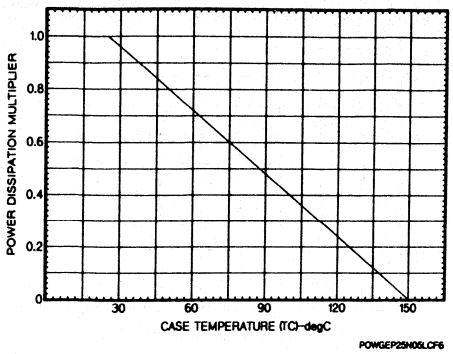


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

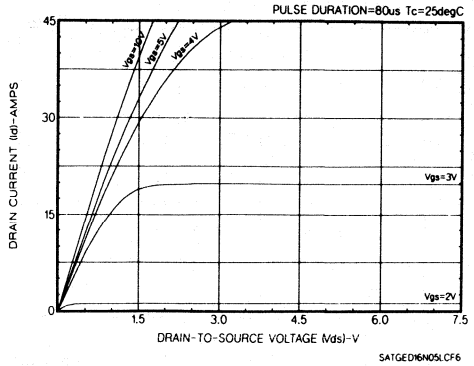


Fig. 4 - Typical saturation characteristics.

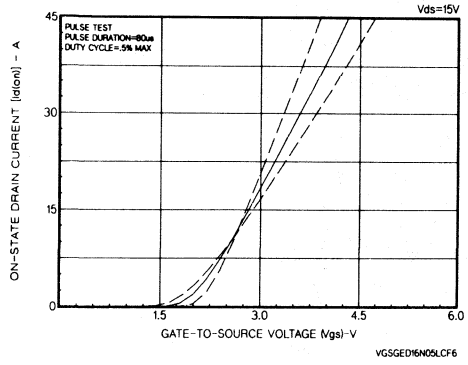


Fig. 5 - Typical transfer characteristics.

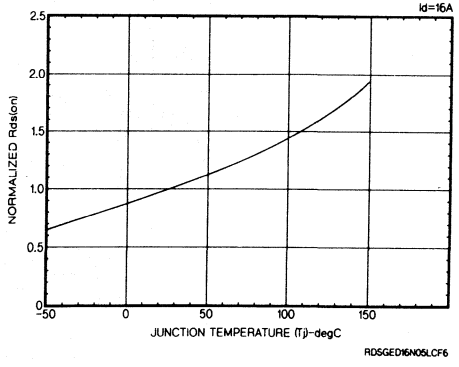


Fig. 6 - Normalized $r_{ds}(on)$ vs. junction temperature.

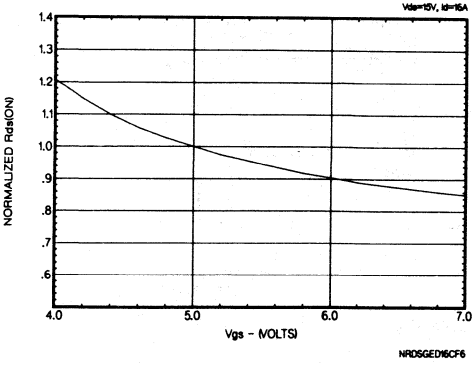


Fig. 7 - Normalized $r_{ds}(on)$ vs. V_{gs}.

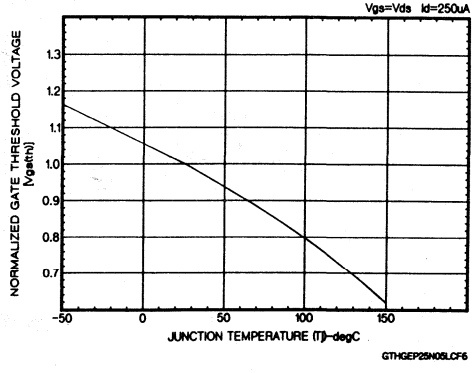


Fig. 8 - Typical normalized gate threshold voltage.

RFD16N05L, RFD16N05LSM

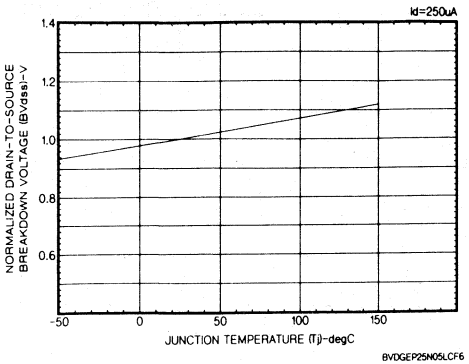


Fig. 9 - Drain source breakdown voltage vs. temperature.

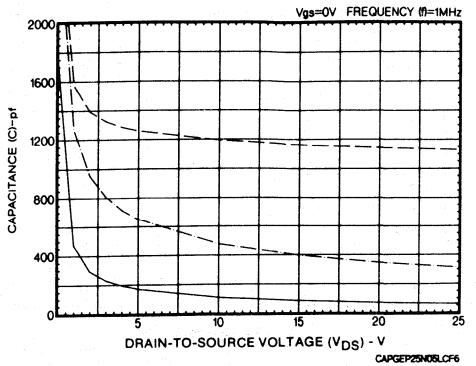


Fig. 10 - Typical capacitance vs. voltage.

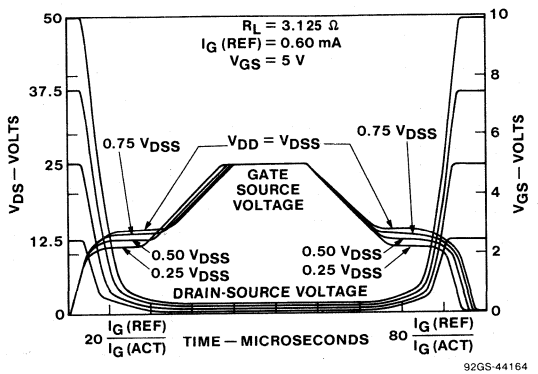


Fig. 11 - Normalized switching waveforms for constant gate-current.
(Refer to RCA application notes AN-7254 and AN-7260.)

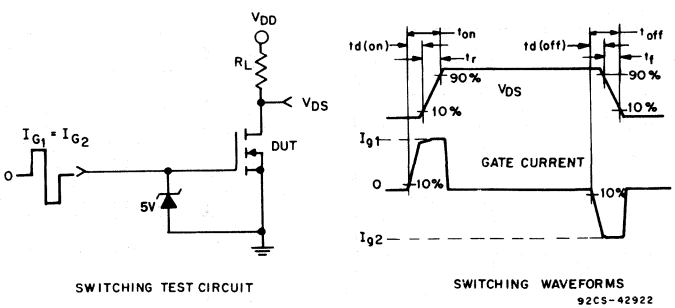


Fig. 12 - Resistive switching.

File Number **2270**

RFP25N05L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

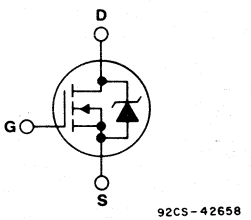
25 A, 50 V
$r_{ds(on)}$ = 0.047 Ω

Features:
- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFP25N05L n-channel logic level power MOSFET is manufactured using the MegaFET process. This process, which uses feature size approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05L was designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor-relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP25N05L is supplied in the JEDEC TO-220AB plastic package.

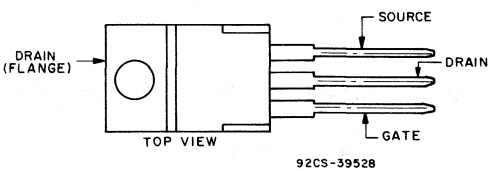
N-CHANNEL ENHANCEMENT MODE



92CS-42658

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{GE} = 1MΩ)	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±10 V
DRAIN CURRENT:	
I_D, RMS Continuous	25 A
I_{DM}, Pulsed	65 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}•	200 mj
AVALANCHE CURRENT, I_{AS}	25 A
POWER DISSIPATION P_T:	
At T_C = 25°C	60 W
Derate above T_C = 25°C	0.48 W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C

•V_{DD} = 10 V, starting T_j = 25°C, L = 510 μHy, I_{peak} = 25 A. See Figs. 13 and 14.

RFP25N05L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150°C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 25 A, V_{GS} = 5 V I_D = 25 A, V_{GS} = 4 V		—	0.047 0.056	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 12.5 A I_{g1} = I_{g2} = 1 A V_{GS} (clamp) + 5 V, − 0.6 V R_L = 2 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	15 (typ.)	
Rise Time	t_r			—	35 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	40 (typ.)	
Fall Time	t_f			—	14 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{GS} = 0-10 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 5 V	$Q_g(5)$	V_{GS} = 0-5 V	I_D = 25 A	—	45	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-1 V	R_L = 1.6 Ω	—	3	
Plateau Voltage	V(plateau)	I_D = 25 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 12.5 A, R_L = 2 Ω L = 0.2 μH, I_{g1} = I_{g2} = 1 A V_{GS} (clamp) + 5 V, −0.6 V		—	30	μJ
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$			—	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$			—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 25 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 25 A, dI_F/dt = 100 A/μs	—	125	ns

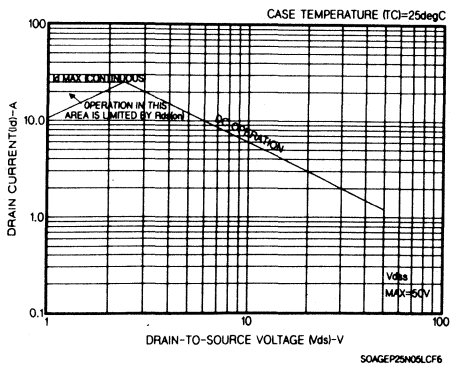


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

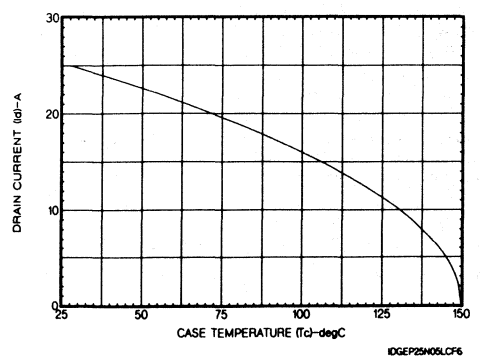


Fig. 2 - Maximum continuous drain current vs. temperature.

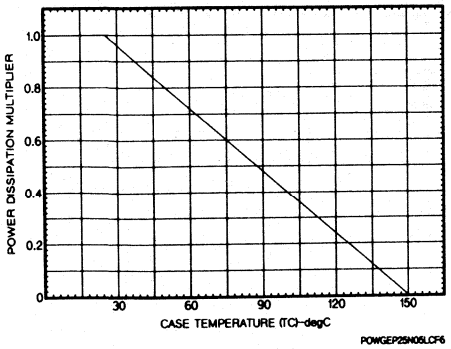


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

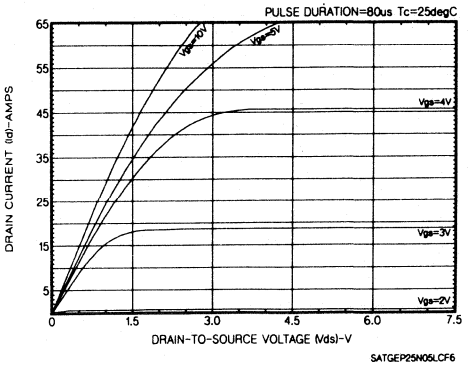


Fig. 4 - Typical saturation characteristics.

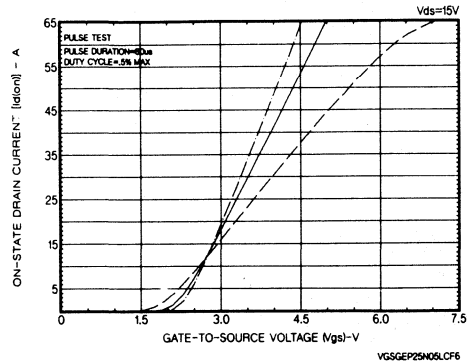


Fig. 5 - Typical transfer characteristics.

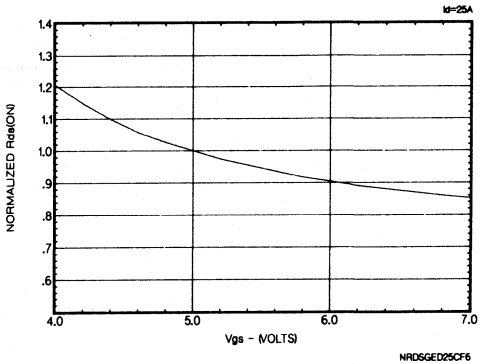


Fig. 6 - Normalized $r_{ds}(on)$ vs. V_{gs}.

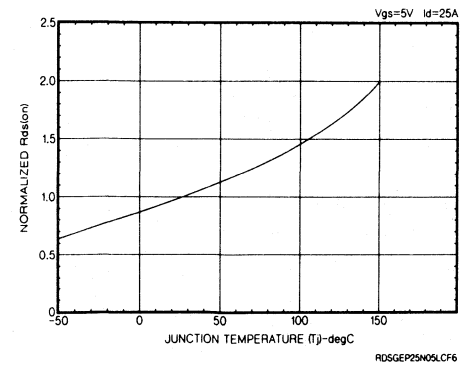


Fig. 7 - Normalized $r_{ds}(on)$ vs. junction temperature.

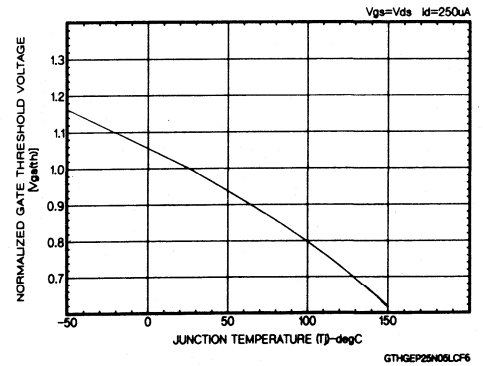


Fig. 8 - Typical normalized gate threshold voltage.

RFP25N05L

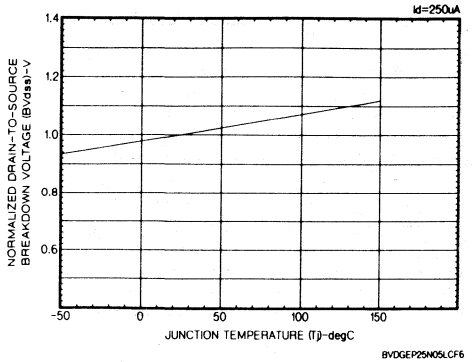


Fig. 9 - Drain source breakdown voltage vs. temperature.

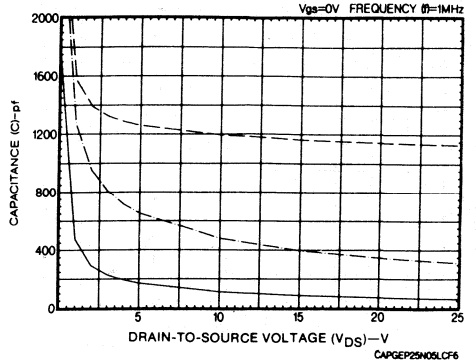


Fig. 10 - Normalized switching waveforms for constant gate-current. (Refer to RCA application notes AN-7254 and AN-7260.)

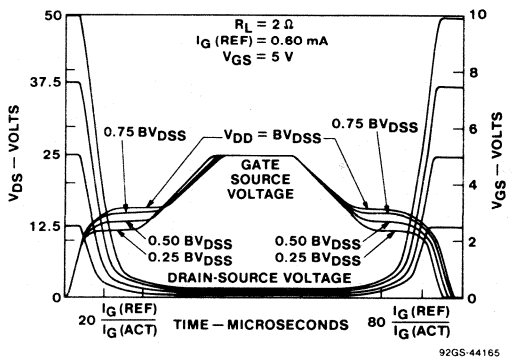


Fig. 11 - Normalized switching waveforms for constant gate-current.
(Refer to RCA application notes AN-7254 and AN-7260.)

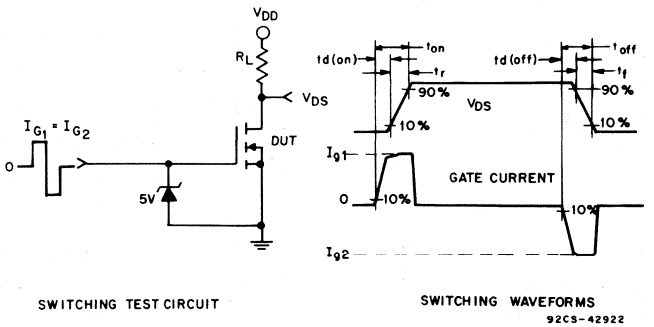


Fig. 12 - Resistive switching.

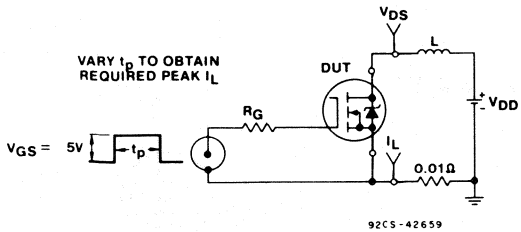


Fig. 13 - Unclamped energy test circuit.

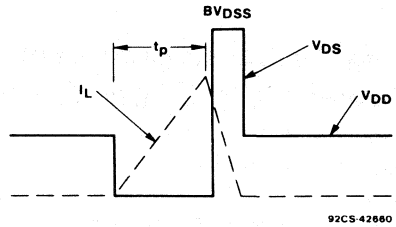


Fig. 14 - Unclamped energy waveforms.

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

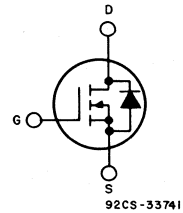
File Number **1510**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 80 V and 100 V
$r_{DS}(on)$: 1.05Ω and 1.2Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

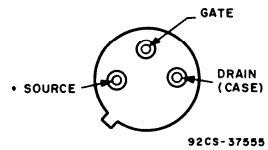
The RFL1N08L and RFL1N10L and the RFP2N08L and RFP2N10L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9524 and TA9525.

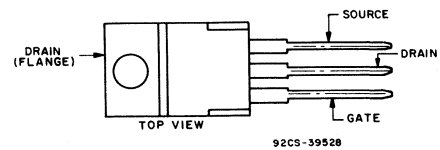
TERMINAL DESIGNATIONS

RFL1N08L
RFL1N10L



JEDEC TO-205AF

RFP2N08L
RFP2N10L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N08L	RFL1N10L		RFP2N08L	RFP2N10L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D	1	1		2	2	A
Pulsed ..... I_{DM}			5			A
POWER DISSIPATION @ T_C=25°C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25°C	0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
				RFL1N08L RFP2N08L		RFL1N10L RFP2N10L		
				MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0		80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V		— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V		— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A	RFP	—	1.05	—	1.05	V
		V_{GS}=5 V	RFL	—	1.2	—	1.2	V
		I_D=2 A	RFP	—	2.5	—	2.5	V
		V_{GS}=5 V	RFL	—	2.9	—	2.9	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A	RFP	—	1.05	—	1.05	Ω
		V_{GS}=5 V	RFL	—	1.2	—	1.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=1 A		800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz		—	200	—	200	pF
Output Capacitance	C_{oss}			—	80	—	80	pF
Reverse-Transfer Capacitance	C_{rss}			—	35	—	35	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=1 A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r			15(typ)	45	15(typ)	45	ns
Turn-Off Delay Time	$t_d(off)$			25(typ)	45	25(typ)	45	ns
Fall Time	t_f		RFP	20(typ)	25	20(typ)	25	ns
			RFL	30(typ)	50	30(typ)	50	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N08L, RFL1N10L		—	15	—	15	°C/W
		RFP2N08L, RFP2N10L		—	5	—	5	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08L RFP2N08L		RFL1N10L RFP2N10L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A d_{IF}/d_t=50 A/μs	100(typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

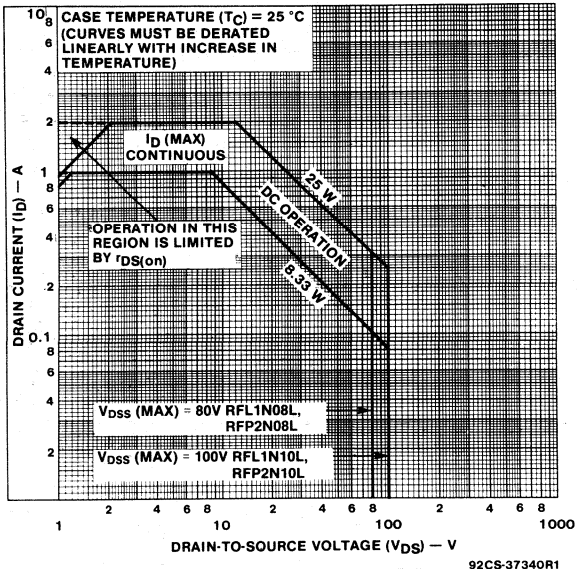


Fig. 1 — Maximum operating areas for all types.

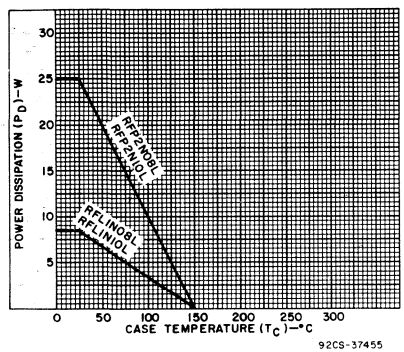


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

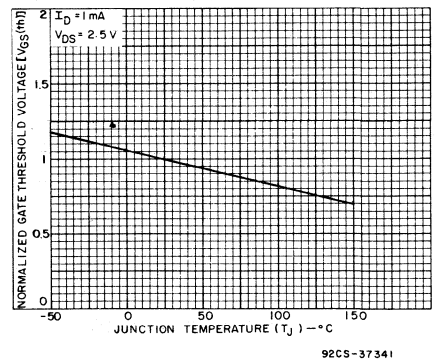


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

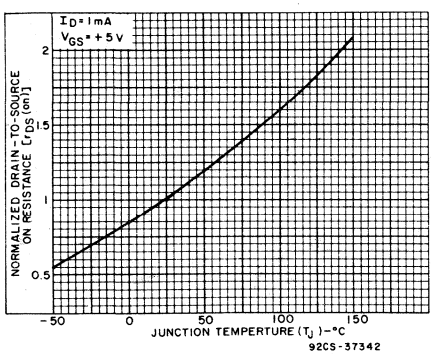


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

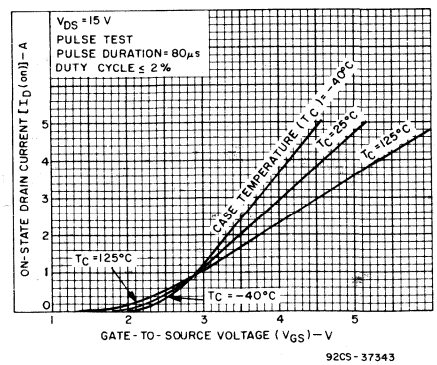


Fig. 5 — Typical transfer characteristics for all types.

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

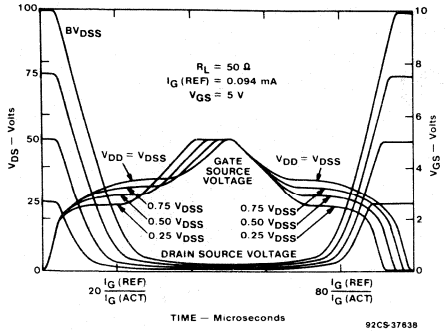


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

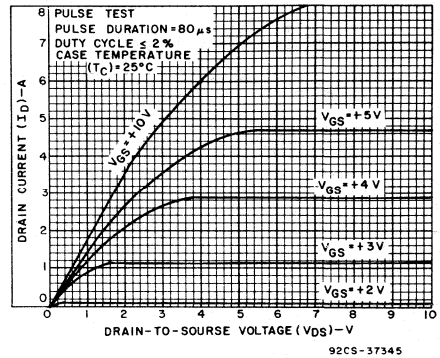


Fig. 7 — Typical saturation characteristics for all types.

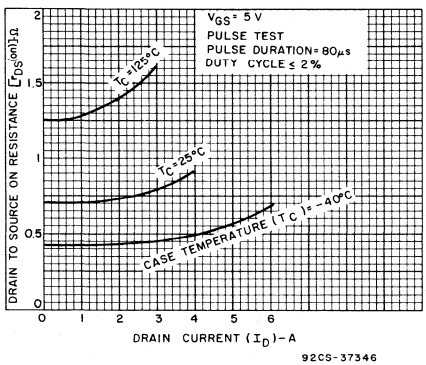


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

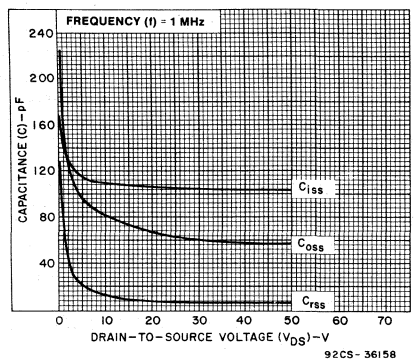


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

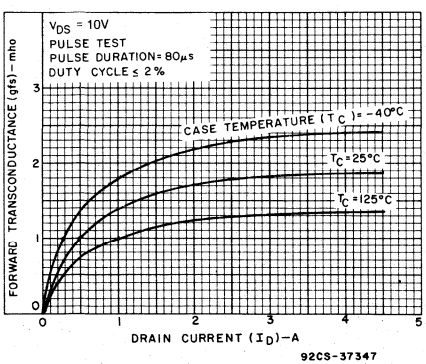


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

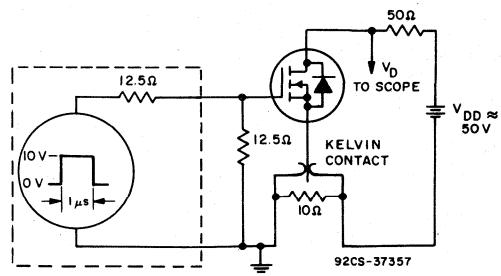


Fig. 11 — Switching Time Test Circuit.

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

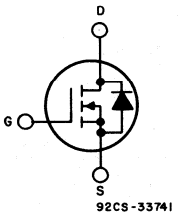
File Number **1513**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 120 V and 150 V
$r_{DS}(on)$: 1.75Ω and 1.9Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

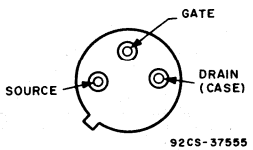
The RFL1N12L and RFL1N15L and the RFP2N12L and RFP2N15L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9528 and TA9529.

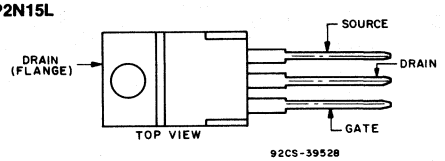
TERMINAL DESIGNATIONS

RFL1N12L
RFL1N15L



JEDEC TO-205AF

RFP2N12L
RFP2N15L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N12L	RFL1N15L		RFP1N12L	RFP2N15L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D	1	1		2	2	A
Pulsed ..... I_{DM}			5			A
POWER DISSIPATION @ T_C=25° C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25° C	0.0667	0.0667		0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N12L RFP2N12L MIN.	LIMITS RFL1N12L RFP2N12L MAX.	LIMITS RFL1N15L RFP2N15L MIN.	LIMITS RFL1N15L RFP2N15L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0		120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=2 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V V_{DS}=120 V		— —	1 —	— —	— 1	μA
		T_C=125°C V_{DS}=100 V V_{DS}=120 V		— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A V_{GS}=5 V	RFP RFL	— —	1.75 1.9	— —	1.75 1.9	V
		I_D=2 A V_{GS}=5 V	RFP RFL	— —	4.2 4.6	— —	4.2 4.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A V_{GS}=5 V	RFP RFL	— —	1.75 1.9	— —	1.75 1.9	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=1 A		800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz		—	200	—	200	pF
Output Capacitance	C_{oss}			—	80	—	80	pF
Reverse-Transfer Capacitance	C_{rss}			—	35	—	35	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V I_D=1 A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r			10(typ)	45	10(typ)	45	ns
Turn-Off Delay Time	$t_d(off)$			24(typ)	45	24(typ)	45	ns
Fall Time	t_f		RFP RFL	20(typ) 30(typ)	25 50	20(typ) 30(typ)	25 50	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N12L, RFL1N15L		—	15	—	15	°C/W
		RFP2N12L, RFP2N15L		—	5	—	5	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N12L RFP2N12L MIN.	LIMITS RFL1N12L RFP2N12L MAX.	LIMITS RFL1N15L RFP2N15L MIN.	LIMITS RFL1N15L RFP2N15L MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A d_{IF}/d_t=50 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

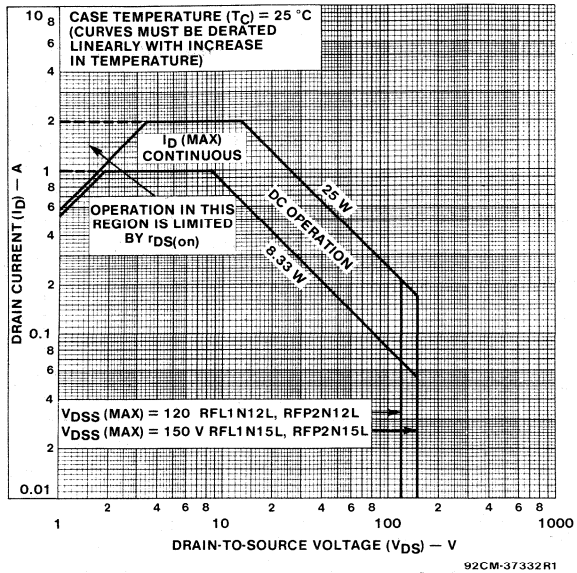


Fig. 1 — Maximum operating areas for all types.

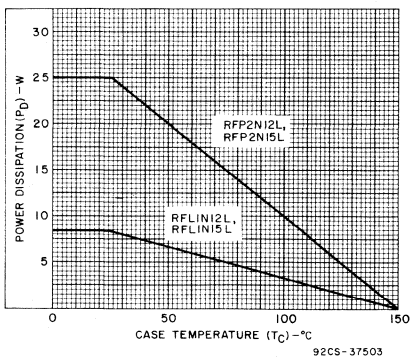


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

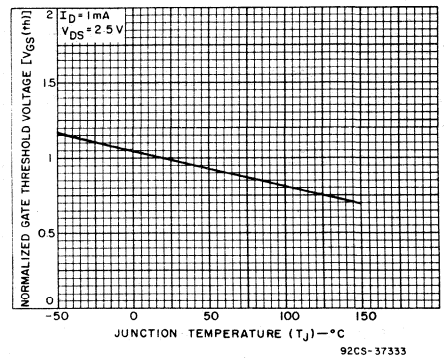


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

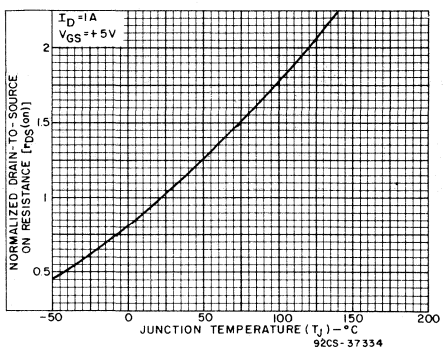


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

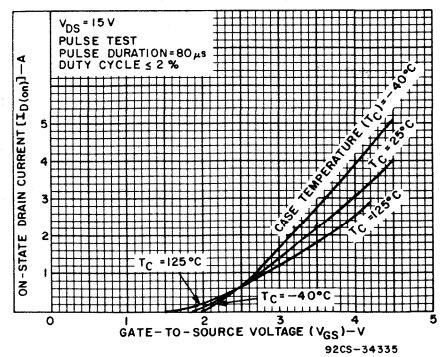


Fig. 5 — Typical transfer characteristics for all types.

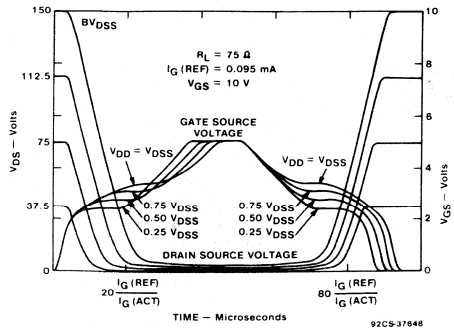


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

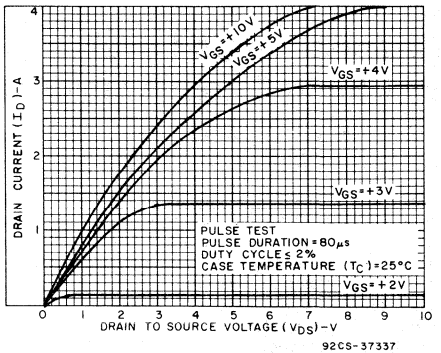


Fig. 7 — Typical saturation characteristics for all types.

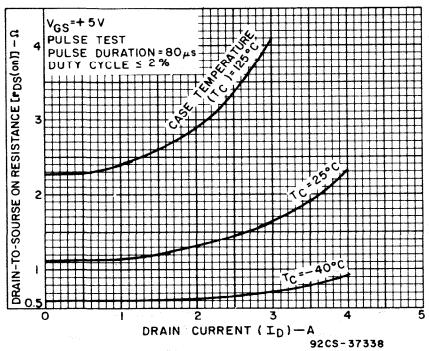


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

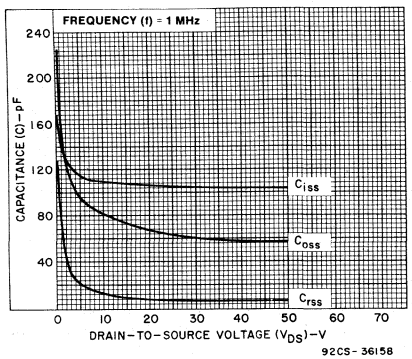


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

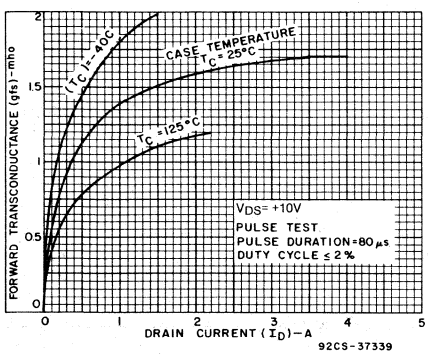


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

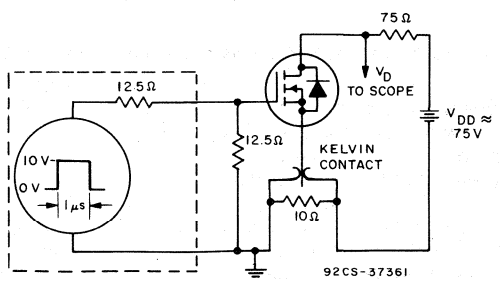


Fig. 11 — Switching Time Test Circuit.

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

File Number **1511**

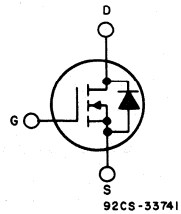
N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 180 V and 200 V

$r_{DS(on)}$: 3.5 Ω and 3.65 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

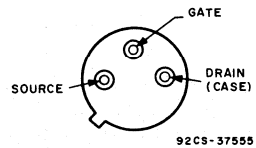
The RFL1N18L and RFL1N20L and the RFP2N18L and RFP2N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9532 and TA9533.

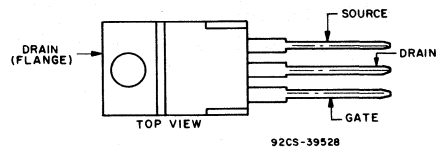
TERMINAL DESIGNATIONS

RFL1N18L
RFL1N20L



JEDEC TO-205AF

RFP2N18L
RFP2N20L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N18L	RFL1N20L		RFP2N18L	RFP2N20L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D	1	1		2	2	A
Pulsed ..... I_{DM}			4			A
POWER DISSIPATION @ T_C=25°C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25°C	0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N18L RFP2N18L MIN.	LIMITS RFL1N18L RFP2N18L MAX.	LIMITS RFL1N20L RFP2N20L MIN.	LIMITS RFL1N20L RFP2N20L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA, V_{GS}=0		180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V		—	1	—	—	μA
		V_{DS}=160 V		—	—	—	1	
		T_C=125° C, V_{DS}=145 V		—	50	—	—	
		V_{DS}=160 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V, V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A	RFP	—	3.5	—	3.5	V
		V_{GS}=5 V	RFL	—	3.65	—	3.65	
		I_D=2 A	RFP	—	9	—	9	
		V_{GS}=5 V	RFL	—	9.3	—	9.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A	RFP	—	3.5	—	3.5	Ω
		V_{GS}=5 V	RFL	—	3.65	—	3.65	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A		800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	60	—	60	
Reverse-Transfer Capacitance	C_{rss}	f=1MHz		—	35	—	35	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r	I_D=1 A		10(typ)	30	10(typ)	30	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=∞		25(typ)	40	25(typ)	40	
Fall Time	t_f	R_{gs}=6.25 Ω, V_{GS}=5 V	RFP	20(typ)	25	20(typ)	25	
			RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N18L, RFL1N20L		—	15	—	15	°C/W
		RFP2N18L, RFP2N20L		—	5	—	5	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N18L RFP2N18L MIN.	LIMITS RFL1N18L RFP2N18L MAX.	LIMITS RFL1N20L RFP2N20L MIN.	LIMITS RFL1N20L RFP2N20L MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A, d_{IF}/d_t=50 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

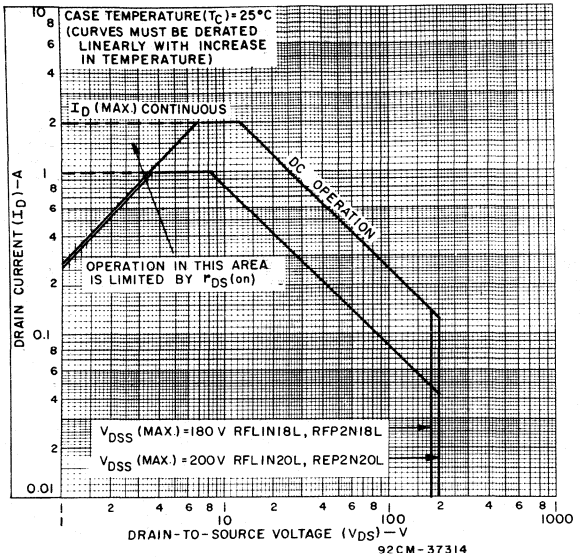


Fig. 1 — Maximum operating areas for all types.

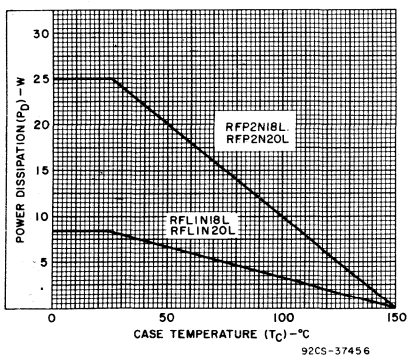


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

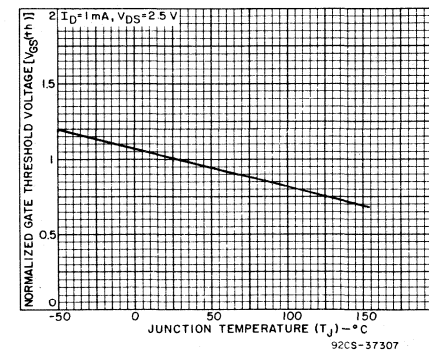


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

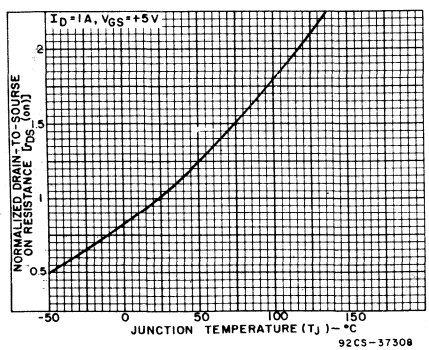


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

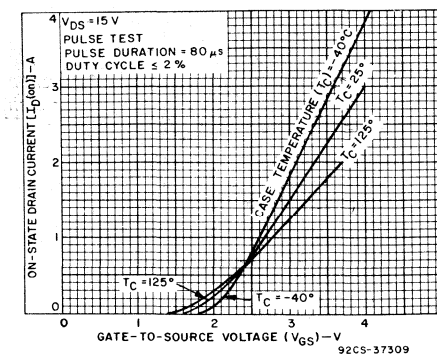


Fig. 5 — Typical transfer characteristics for all types.

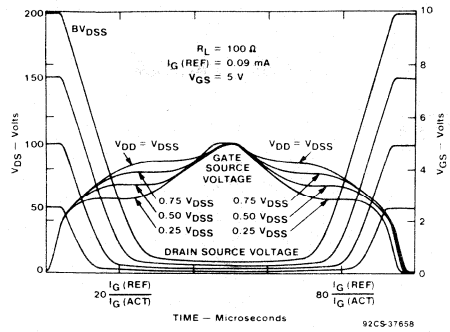


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

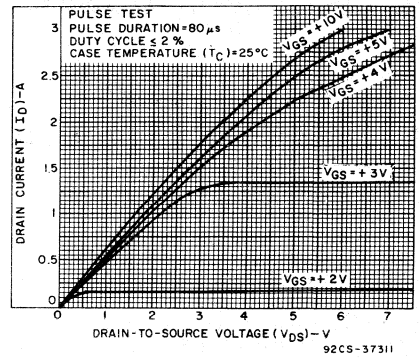


Fig. 7 — Typical saturation characteristics for all types.

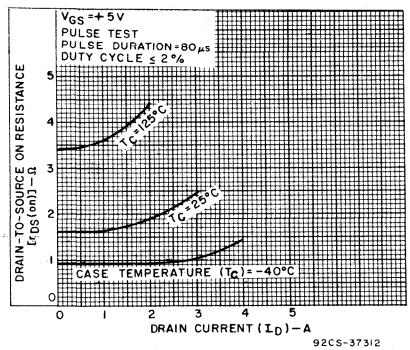


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

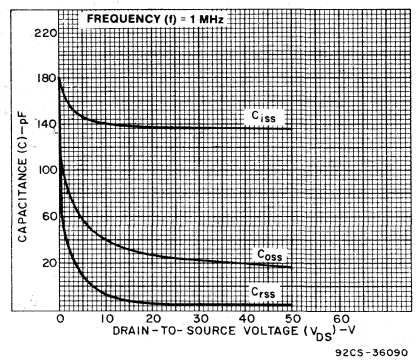


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

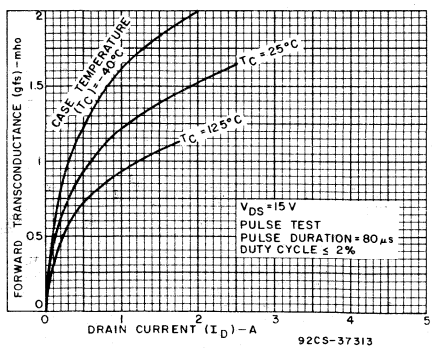


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

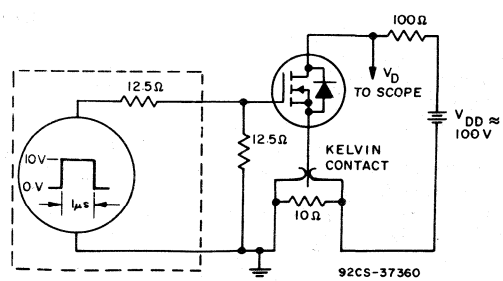


Fig. 11 — Switching Time Test Circuit.

RFL2N05L, RFL2N06L, RFP4N05L, RFP4N06L

File Number **1560**

Power Logic Level MOSFETs

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

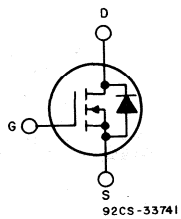
2 and 4 A, 50 V — 60 V

r_{DS}(on): 0.6Ω and 0.75Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

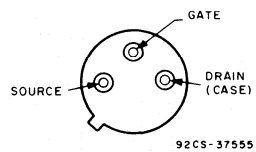
TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

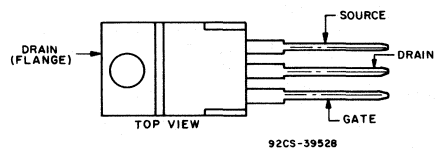
TERMINAL DESIGNATIONS

RFL2N05L
RFL2N06L



JEDEC TO-205AF

RFP4N05L
RFP4N06L



JEDEC TO-220AB

The RFL2N05L and RFL2N06L and the RFP4N05L and RFP4N06L* are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9520 and TA9521, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFL2N05L	RFL2N06L	RFP4N05L	RFP4N06L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50	60	50	60	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ)	V_{DGR}	50	60	50	60	V
GATE-SOURCE VOLTAGE	V_{GS}	±10				V
DRAIN CURRENT, RMS Continuous	I_D	2	2	4	4	A
Pulsed	I_{DM}	10				A
POWER DISSIPATION @ T_C = 25°C	P_T	8.33	8.33	25	25	W
Derate above T_C = 25°C		0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFL2N05L, RFL2N06L, RFP4N05L, RFP4N06L

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05L RFP4N05L		RFL2N06L RFP4N06L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 2 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V V_{DS} = 50 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 40 V V_{DS} = 50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 1 A V_{GS} = 5 V	—	.8	—	.8	V
		I_D = 2 A V_{GS} = 5 V	—	2.0	—	2.0	V
		I_D = 4 A V_{GS} = 7.5 V	—	4.8	—	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 1 A, V_{GS} = 5 V — RFP	—	0.6	—	0.6	Ω
		I_D = 1 A, V_{GS} = 5 V — RFL	—	0.75	—	0.75	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 1 A	800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	225	—	225	pF
Output Capacitance	C_{oss}		—	100	—	100	pF
Reverse-Transfer Capacitance	C_{rss}		—	40	—	40	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V I_D = 1 A R_{gen} = ∞ R_{gs} = 6.25 Ω V_{GS} = 5 V	10(typ)	20	10(typ)	20	ns
Rise Time	t_r		65(typ)	130	65(typ)	130	ns
Turn-Off Delay Time	$t_{d(off)}$		20(typ)	40	20(typ)	40	ns
Fall Time	t_f		30(typ)	60	30(typ)	60	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL2N05L, RFL2N06L	—	15	—	15	°C/W
		RFP4N05L, RFP4N06L	—	5	—	5	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05L RFP4N05L		RFL2N06L RFP4N06L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2 A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFL2N05L, RFL2N06L, RFP4N05L, RFP4N06L

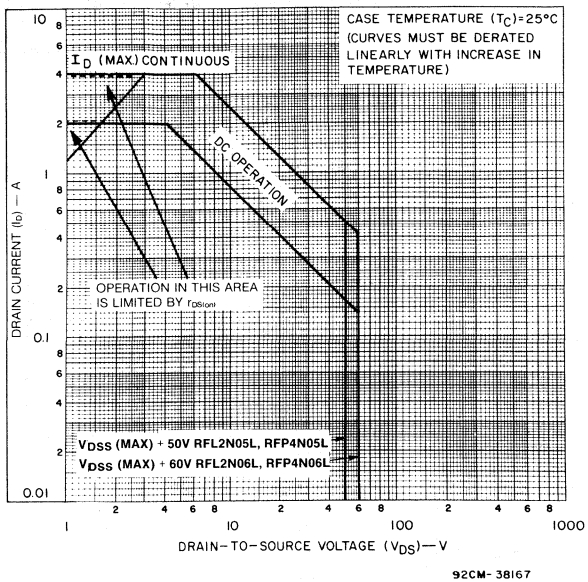


Fig. 1 - Maximum operating areas for all types.

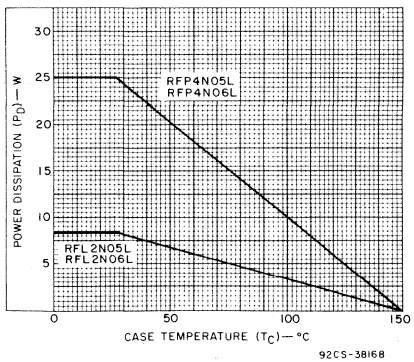


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

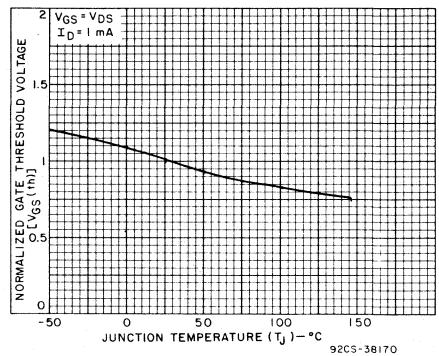


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

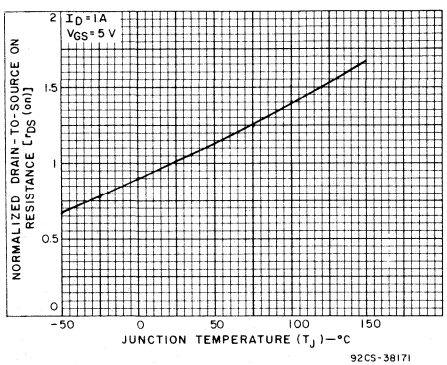


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

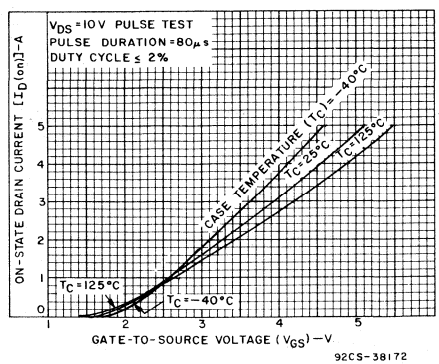


Fig. 5 - Typical transfer characteristics for all types.

RFL2N05L, RFL2N06L, RFP4N05L, RFP4N06L

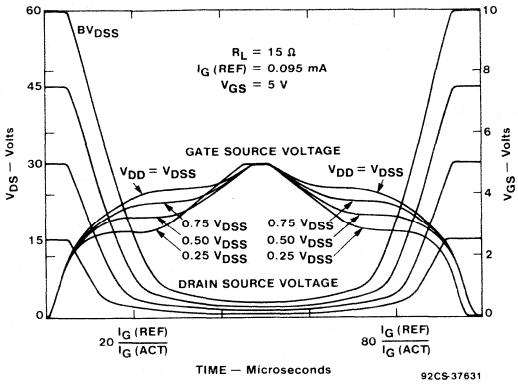


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

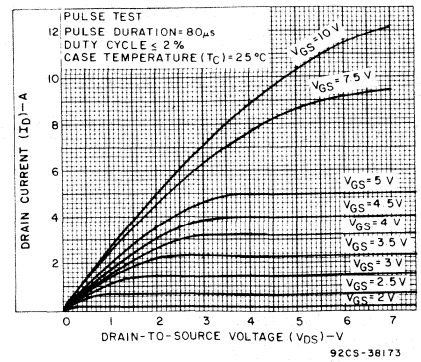


Fig. 7 - Typical saturation characteristics for all types.

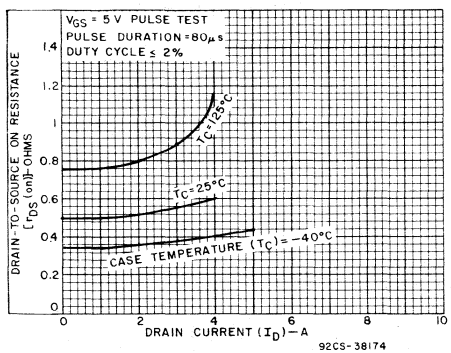


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

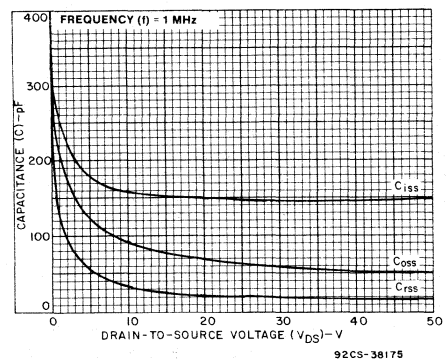


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

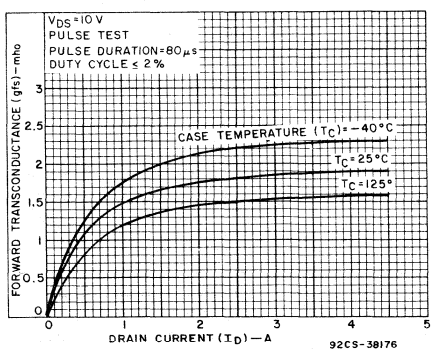


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

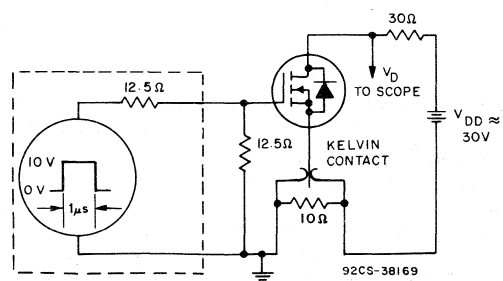


Fig. 11 - Switching Time Test Circuit.

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

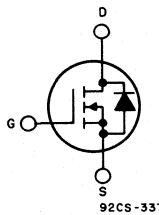
File Number **1514**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

8 A, 180 V and 200 V
$r_{DS}(on)$: 0.5Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

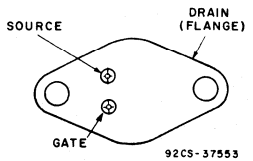
The RFM8N18L and RFM8N20L and the RFP8N18L and RFP8N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9534 and TA9535.

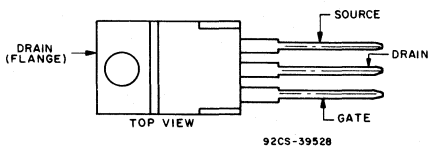
TERMINAL DESIGNATIONS

RFM8N18L
RFM8N20L



JEDEC TO-204AA

RFP8N18L
RFP8N20L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFM8N18L	RFM8N20L		RFP8N18L	RFP8N20L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE	V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous	I_D			8			A
Pulsed	I_{DM}			20			A
POWER DISSIPATION @ T_C=25° C	P_T	75	75		60	60	W
Derate above T_C=25° C		0.6	0.6		0.48	0.48	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	2.0	—	2.0	V
		I_D=8 A V_{GS}=5 V	—	4.6	—	4.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=4 A	3.0	—	3.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	250	—	250	pF
Reverse-Transfer Capacitance	C_{rss}		—	120	—	120	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=4A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r		45(typ)	150	45(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	135	100(typ)	135	ns
Fall Time	t_f		60(typ)	105	60(typ)	105	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8N18L, RFM8N20L	—	1.67	—	1.67	°C/W
		RFP8N18L, RFP8N20L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=4 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	250(typ)		250(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

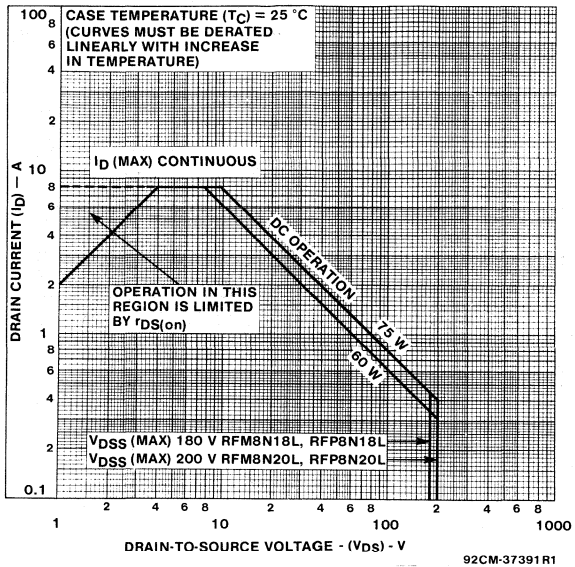


Fig. 1 — Maximum safe operating areas for all types.

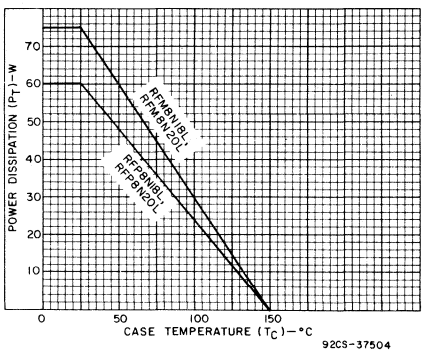


Fig. 2 — Power vs. temperature derating curve for all types.

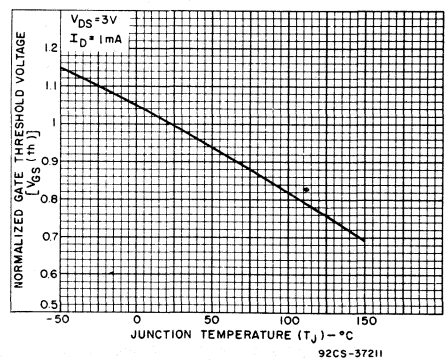


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

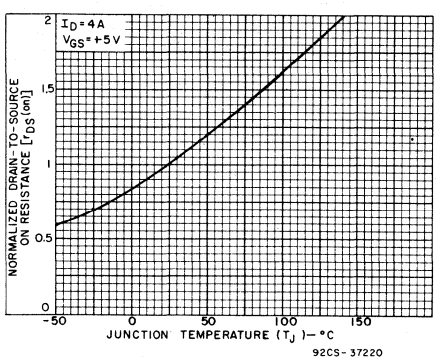


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

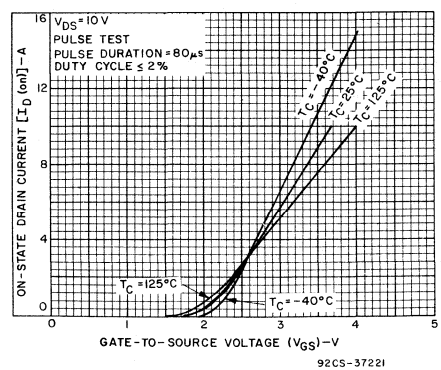


Fig. 5 — Typical transfer characteristics for all types.

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

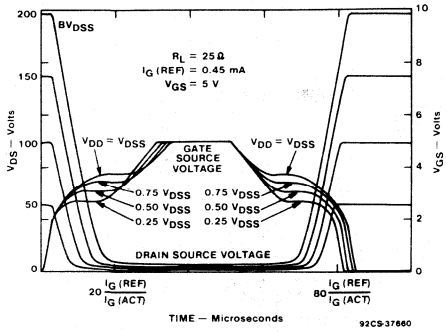


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

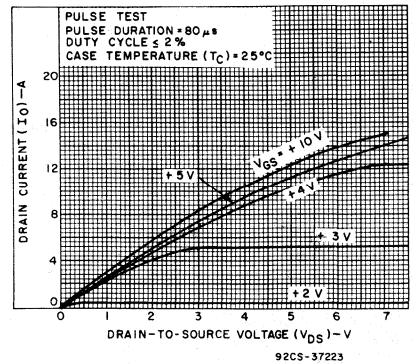


Fig. 7 — Typical saturation characteristics for all types.

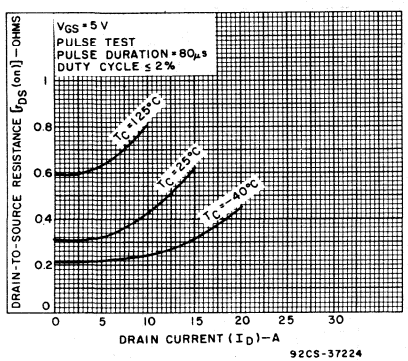


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

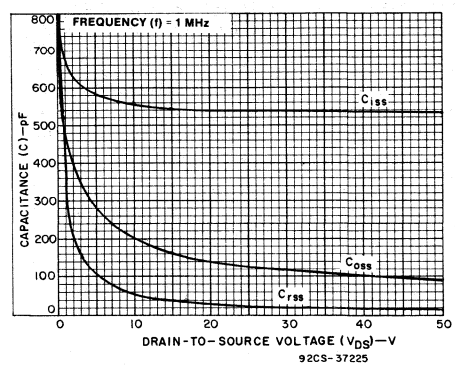


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

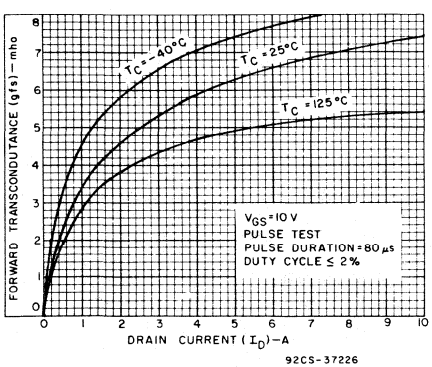


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

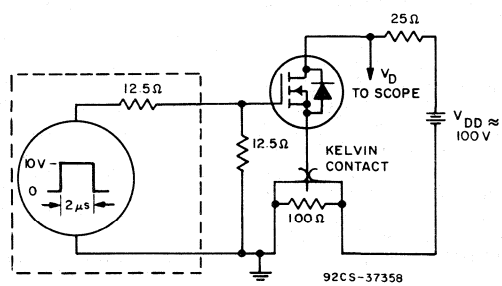


Fig. 11 — Switching Time Test Circuit.

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

File Number **1559**

Power Logic Level MOSFETs

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

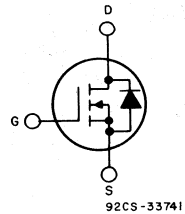
10 A, 120 V — 150 V

$r_{DS(on)}$: 0.3 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

The RFM10N12L and RFM10N15L and the RFP10N12L and RFP10N15L* are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

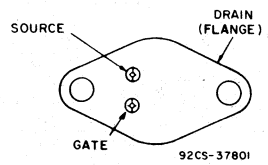
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP10N12L is F10N12L and on type RFP10N15L is F10N15L.

*The RFM and RFP series were formerly RCA developmental numbers TA9530 and TA9531, respectively.

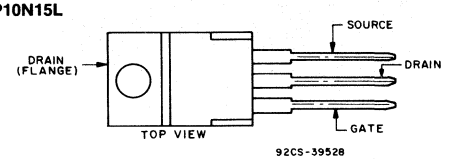
TERMINAL DESIGNATIONS

RFM10N12L
RFM10N15L



JEDEC TO-204AA

RFP10N12L
RFP10N15L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

	RFM10N12L	RFM10N15L	RFP10N12L	RFP10N15L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	120	150	120	150	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ) ..... V_{DGR}	120	150	120	150	V
GATE-SOURCE VOLTAGE ..... V_{GS}	±10				V
DRAIN CURRENT, RMS Continuous ..... I_D	10				A
Pulsed ..... I_{DM}	25				A
POWER DISSIPATION @ T_C = 25° C ..... P_T	75	75	60	60	W
Derate above T_C = 25° C	0.6	0.6	0.48	0.48	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}	-55 to +150				°C

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 2 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	1.5	—	1.5	V
		I_D = 10 A V_{GS} = 5 V	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	1200	—	1200	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	250	—	250	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	120	—	120	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 75 V	15(typ)	60	15(typ)	60	ns
Rise Time	t_r	I_D = 5 A R_{gen} = ∞	50(typ)	135	50(typ)	135	
Turn-Off Delay Time	$t_{d(off)}$	R_{gs} = 6.25 Ω	90(typ)	135	90(typ)	135	
Fall Time	t_f	V_{GS} = 5 V	90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N12L, RFM10N15L	—	1.67	—	1.67	°C/W
		RFP10N12L, RFP10N15L	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

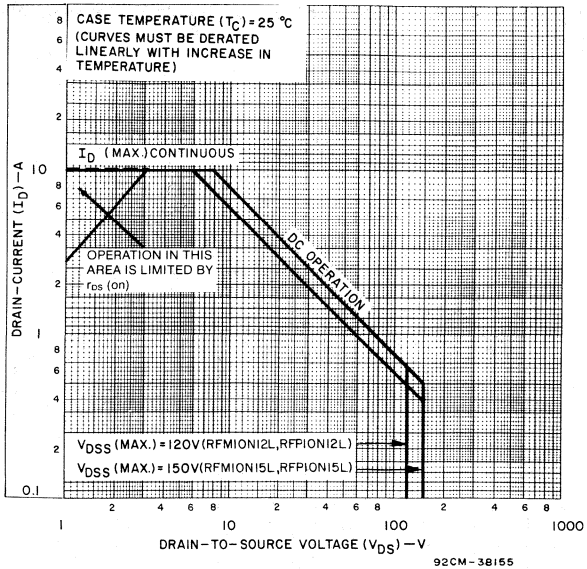


Fig. 1 - Maximum safe operating areas for all types.

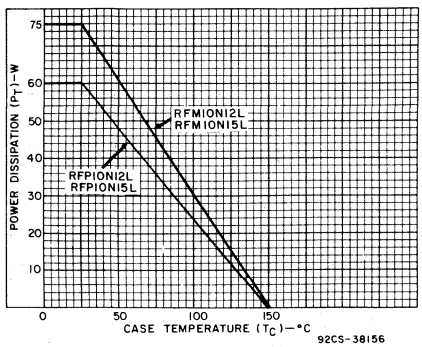


Fig. 2 - Power vs. temperature derating curve for all types.

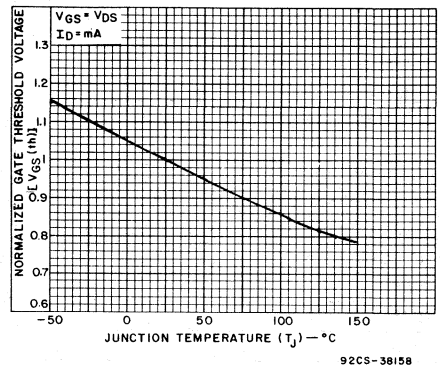


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

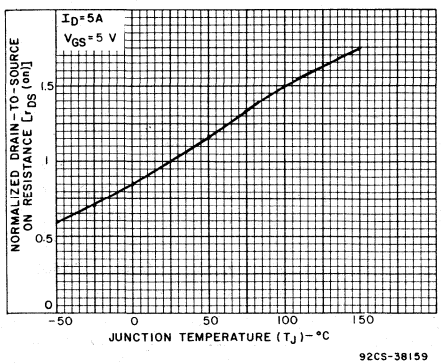


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

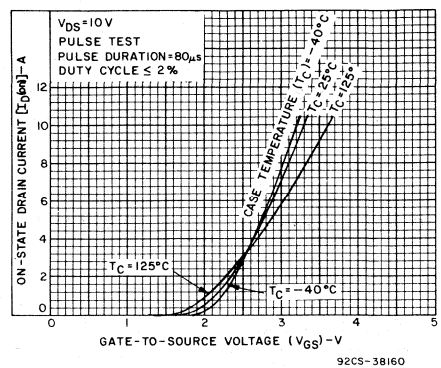


Fig. 5 - Typical transfer characteristics for all types.

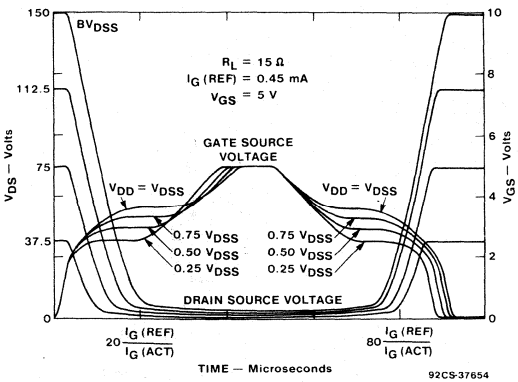


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

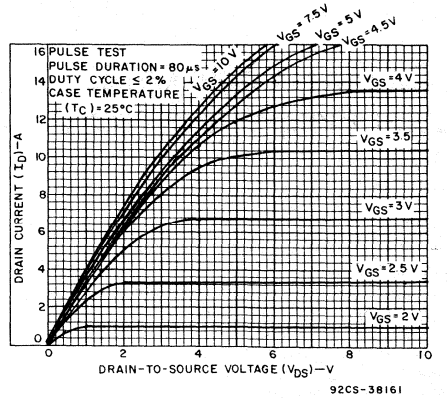


Fig. 7 - Typical saturation characteristics for all types.

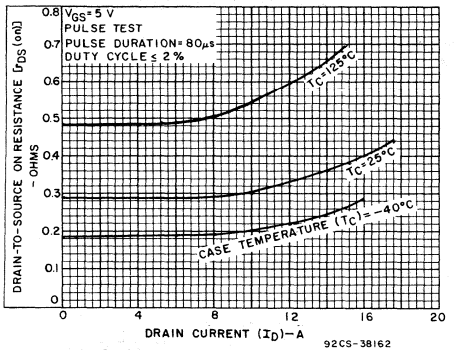


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

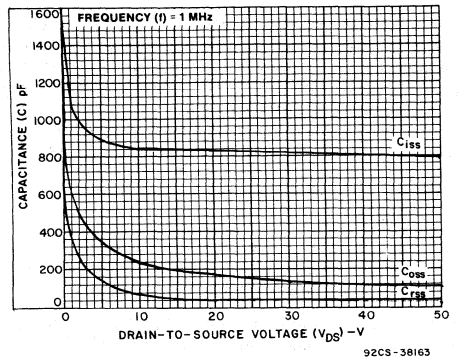


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

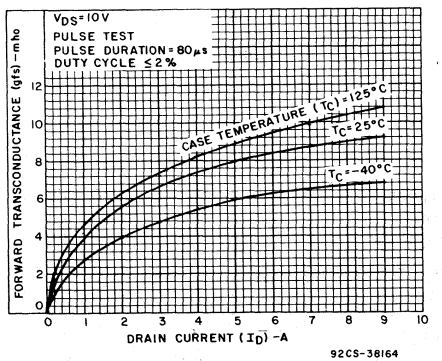


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

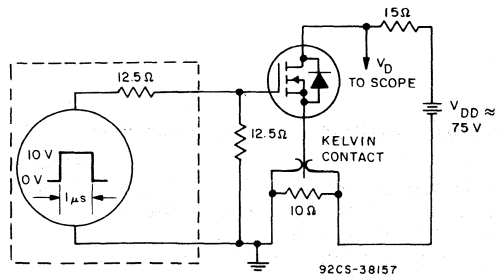


Fig. 11 - Switching Time Test Circuit.

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

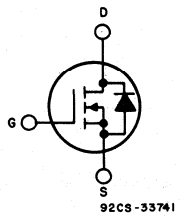
File Number **1512**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

12 A, 80 V and 100 V
$r_{DS}(on)$: 0.2 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

The RFM12N08L and RFM12N10L and the RFP12N08L and RFP12N10L* are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

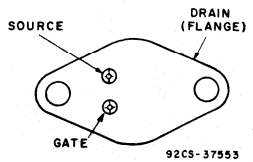
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP12N08L is F12N08L and on type RFP12N10L is F12N10L.

*The RFM and RFP series were formerly RCA developmental number TA9526 and TA9527.

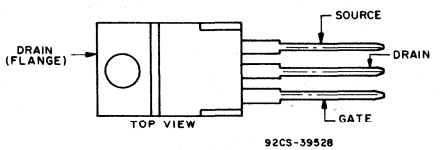
TERMINAL DESIGNATIONS

RFM12N08L
RFM12N10L



JEDEC TO-204AA

RFP12N08L
RFP12N10L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12N08L	RFM12N10L		RFP12N08L	RFP12N10L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=5 V	—	3.3	—	3.3	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	325	—	325	pF
Reverse-Transfer Capacitance	C_{rss}		—	170	—	170	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=6 A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	50	15(typ)	50	ns
Rise Time	t_r		70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	130	100(typ)	130	ns
Fall Time	t_f		80(typ)	150	80(typ)	150	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12N08L, RFM12N10L	—	1.67	—	1.67	°C/W
		RFP12N08L, RFP12N10L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

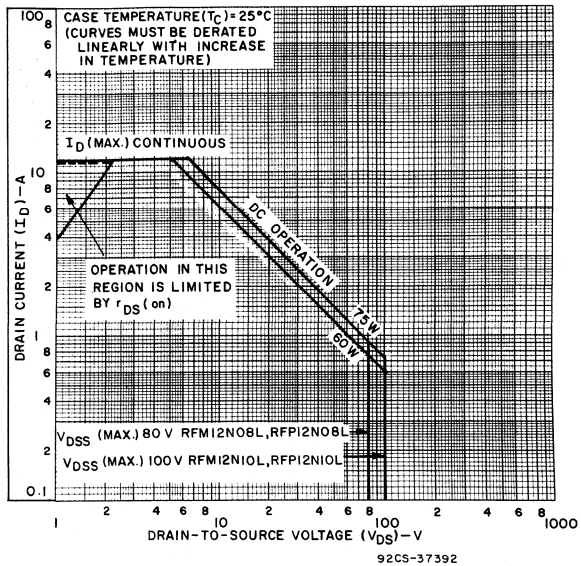


Fig. 1 — Maximum operating areas for all types.

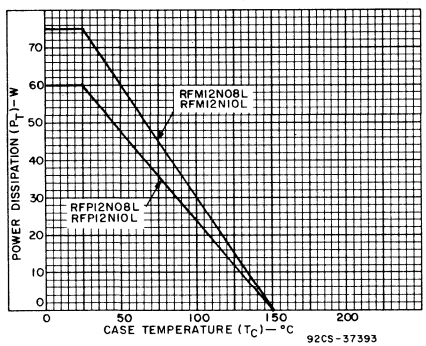


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

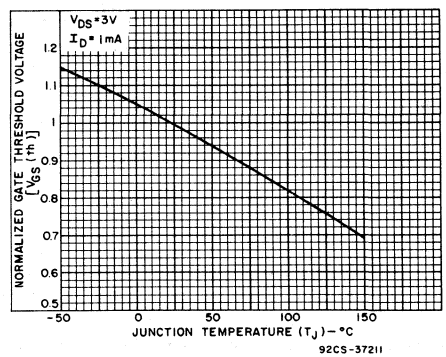


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

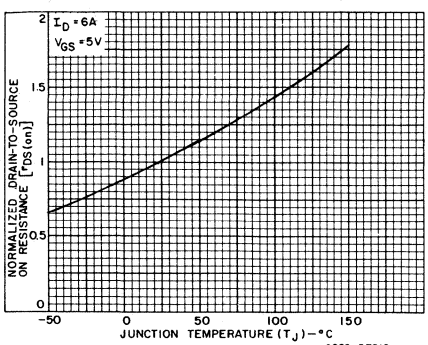


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

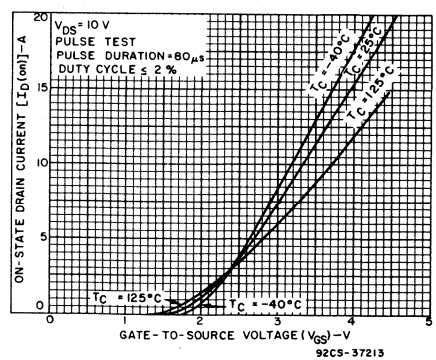


Fig. 5 — Typical transfer characteristics for all types.

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

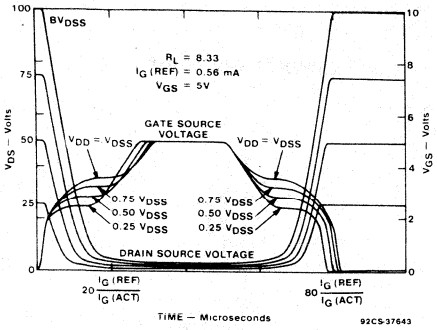


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

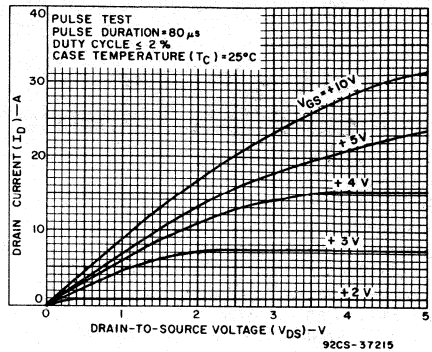


Fig. 7 — Typical saturation characteristics for all types.

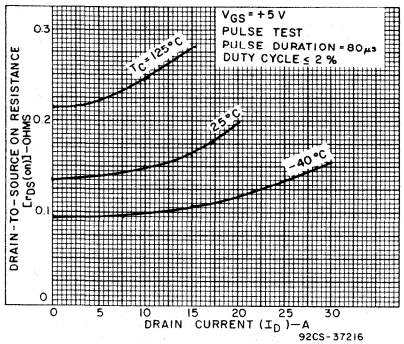


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

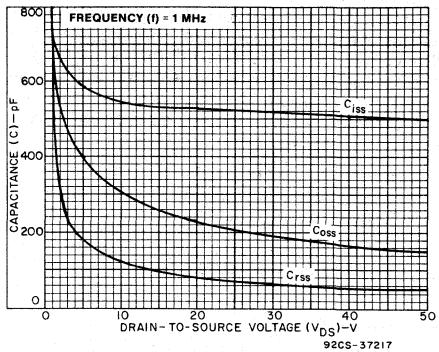


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

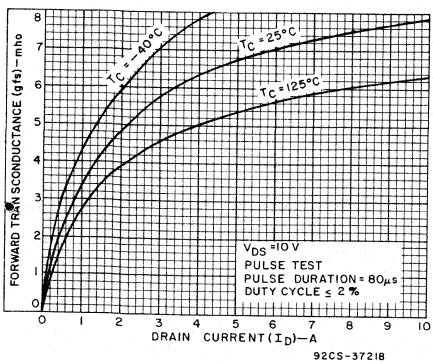


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

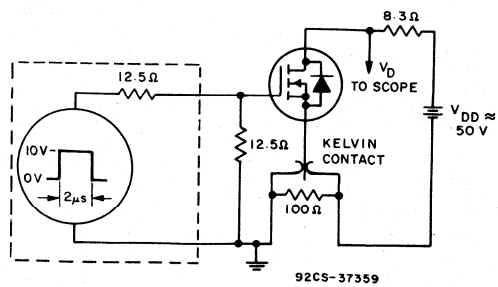


Fig. 11 — Switching Time Test Circuit.

RFM15N05L, RFM15N06L, RFP15N05L, RFP15N06L

File Number **1558**

Power Logic Level MOSFETs

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

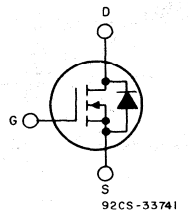
15 A, 50 and 60 V

$r_{DS}(on)$: 0.14 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

The RFM15N05L and RFM15N06L and the RFP15N05L and RFP15N06L* are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

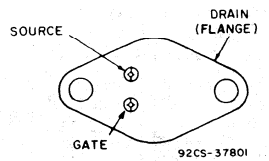
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP15N05L is F15NO5L and on type RFP15N06L is F15N06L.

*The RFM and RFP series were formerly RCA developmental numbers TA9522 and TA9523, respectively.

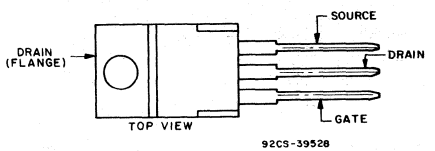
TERMINAL DESIGNATIONS

RFM15N05L
RFM15N06L



JEDEC TO-204AA

RFP15N05L
RFP15N06L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

	RFM15N05L	RFM15N06L	RFP15N05L	RFP15N06L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60	50	60	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ) ..... V_{DGR}	50	60	50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}	±10				V
DRAIN CURRENT, RMS Continuous ..... I_D	15				A
Pulsed ..... I_{DM}	40				A
POWER DISSIPATION @ T_C = 25° C ..... P_T	75	75	60	60	W
Derate above T_C = 25° C	0.6	0.6	0.48	0.48	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}	-55 to +150				°C

RFM15N05L, RFM15N06L, RFP15N05L, RFP15N06L

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V V_{DS} = 50 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 40 V V_{DS} = 50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	1.05	—	1.05	V
		I_D = 15 A V_{GS} = 5 V	—	3.0	—	3.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 7.5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	450	—	450	pF
Reverse-Transfer Capacitance	C_{rss}		—	200	—	200	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V I_D = 7.5 A R_{gen} = ∞ R_{gs} = 6.25 Ω V_{GS} = 5 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r		250(typ)	325	250(typ)	325	ns
Turn-Off Delay Time	$t_{d(off)}$		200(typ)	325	200(typ)	325	ns
Fall Time	t_f		225(typ)	325	225(typ)	325	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM15N05L, RFM15N06L	—	1.67	—	1.67	°C/W
		RFP15N05L, RFP15N06L	—	2.083	—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 7.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	225 (typ.)		225 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs, duty cycle = 2%.

RFM15N05L, RFM15N06L, RFP15N05L, RFP15N06L

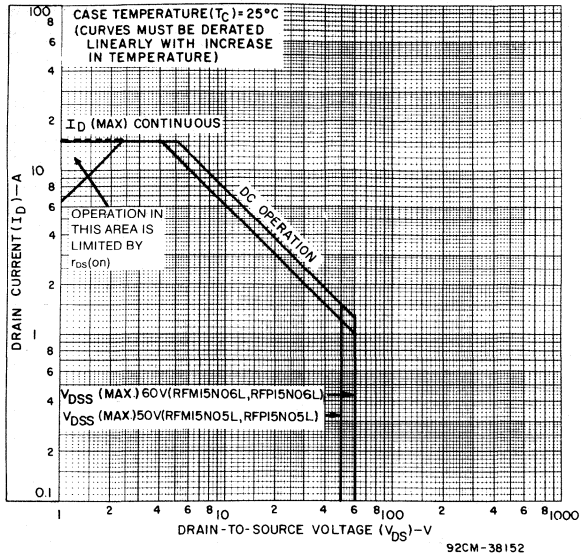


Fig. 1 - Maximum safe operating areas for all types.

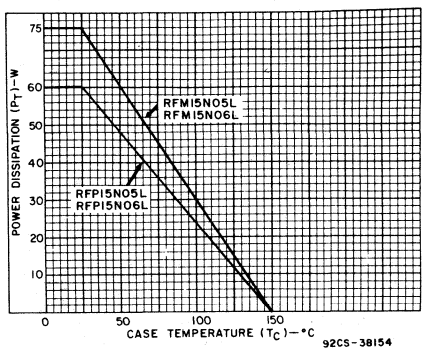


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

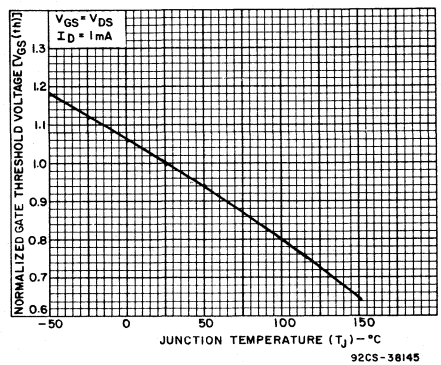


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

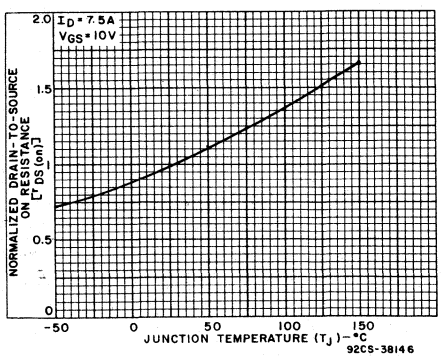


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

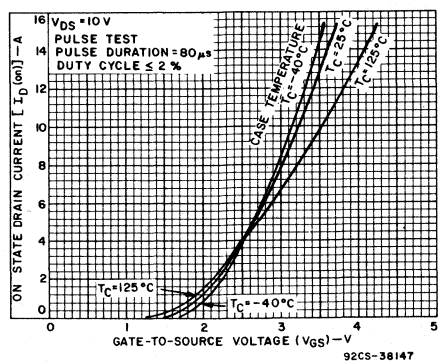


Fig. 5 - Typical transfer characteristics for all types.

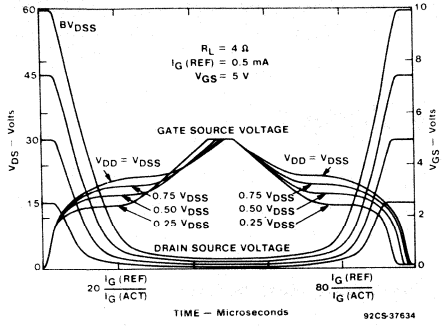


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to RCA application notes AN-7254 and AN-7260.

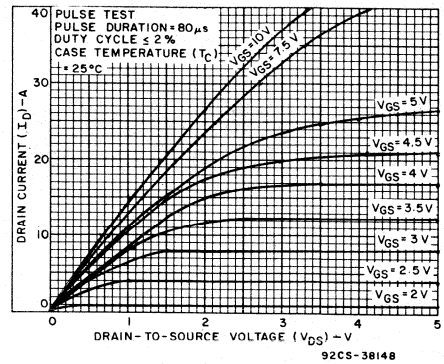


Fig. 7 - Typical saturation characteristics for all types.

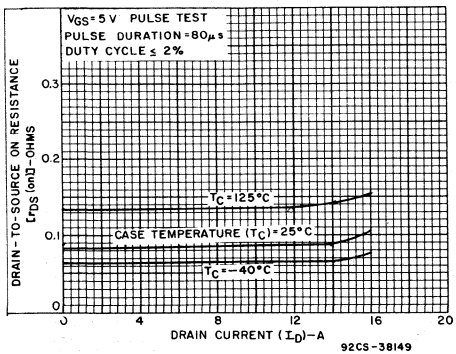


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

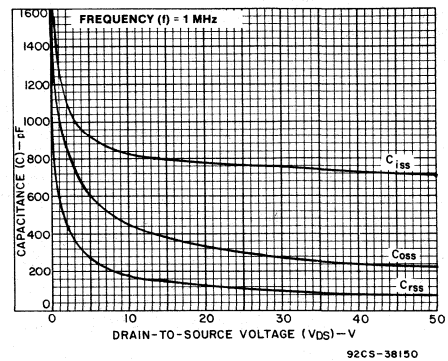


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

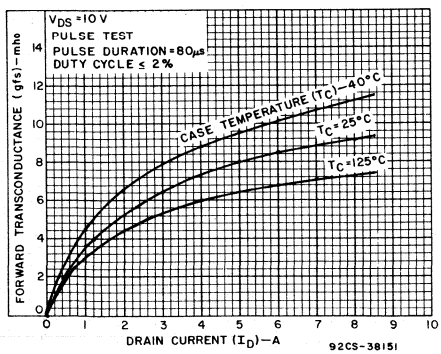


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

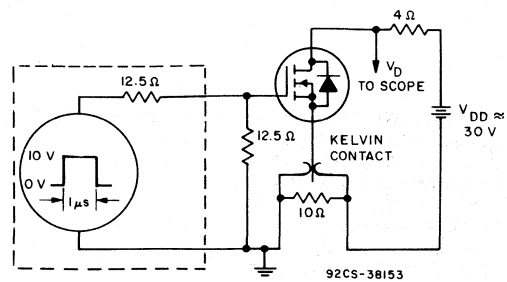


Fig. 11 - Switching Time Test Circuit.

RFP17N06L File Number **2272**

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors

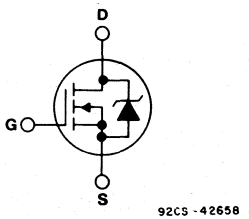
17 A, 60 V
$r_{ds(on)}$ = 0.100 Ω

Features:
- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFP17N06L is an n-channel enhancement mode silicon-gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3 - 5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

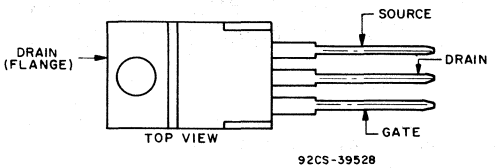
The RFP17N06L is supplied in the JEDEC TO-220AB plastic package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

DRAIN-SOURCE VOLTAGE, V_{DSS}	60 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{GE}=1MΩ)	60 V
GATE-SOURCE VOLTAGE, V_{GS}	±10 V
DRAIN CURRENT:	
I_D, RMS Continuous	17 A
I_{DM}, Pulsed	50 A
POWER DISSIPATION P_T @ T_C = 25°C	60 W
Derate above T_C = 25°C	0.48 W/°C
OPERATING AND STORAGE TEMPERATURE, T_J, T_{STG}	−55 to +150°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1.0 mA, V_{GS} = 0 V	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1.0 mA	1	2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0 V	—	1	μA
		T_C = 150° C		50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V	—	100	nA
On Resistance	$R_{DS}(on)$	I_D = 8.5 A, V_{GS} = 4.0 V	—	0.150	Ω
		I_D = 8.5 A, V_{GS} = 5.0 V	—	0.100	
		I_D = 17.0 A, V_{GS} = 5.0 V	—	0.130	
Forward Transconductance	g_{FS}	I_D = 8.5 A, V_{DS} = 5.0 V	6.0	—	S
Turn-On Delay Time	$T_d(on)$	V_{DD} = 30 V, I_D = 8.5 A	—	40	ns
Rise Time	T_R	R_{GEN} = 12.5 ohms	—	150	
Turn-Off Delay Time	$T_d(off)$	R_{GS} = 12.5 ohms	—	240	
Fall Time	T_F	V_{GS} = +5 V	—	110	
Total Gate Charge	$Q_g(total)$	I_D = 8.5 A, V_{DD} = 30 V	—	45	nC
		V_{GS} = 10 V, R_L = 3.5 ohms			
Gate Charge at 5 volts	$Q_g(5)$	V_{GS} = 5 V	—	25	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 1 V	—	2.0	
Thermal Resistance Junction to Case	$R_{\theta JC}$		—	2.083	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 17 A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 17 A, dI_F/d_t = 100 A/μs	115 (typ)		ns

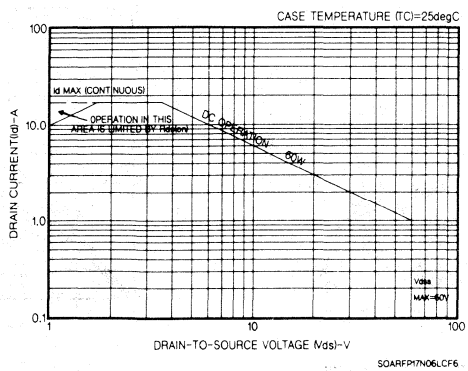


Fig. 1 - Maximum safe operating areas for all types.

RFP17N06L

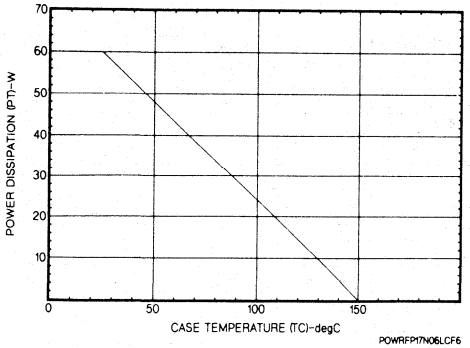


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

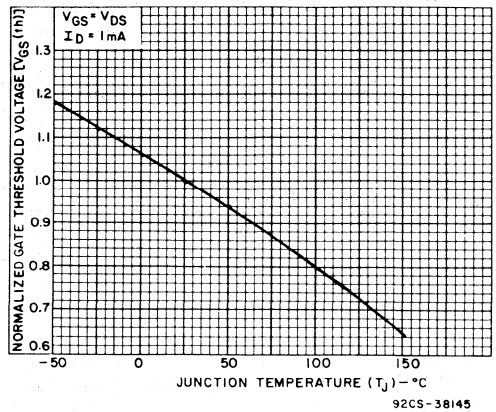


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

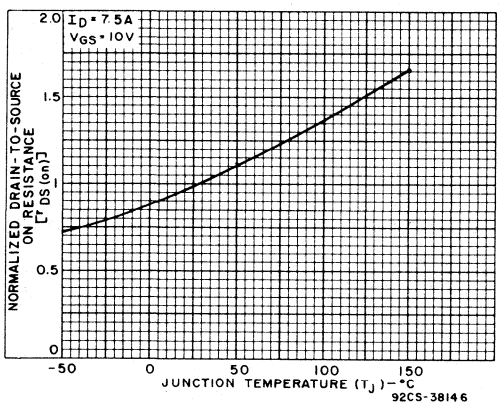


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

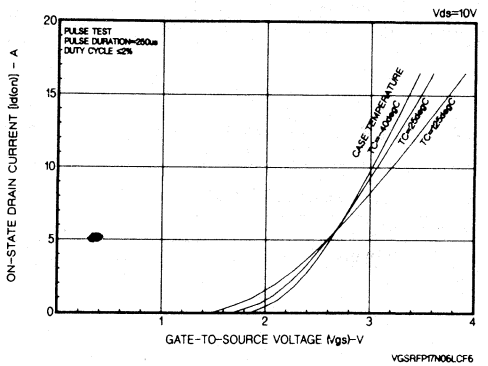


Fig. 5 - Typical transfer characteristics for all types.

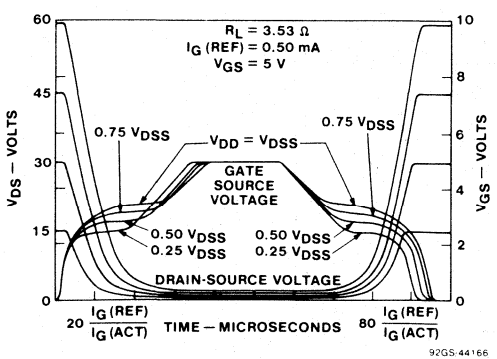


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA application notes AN-7254 and AN-7260.

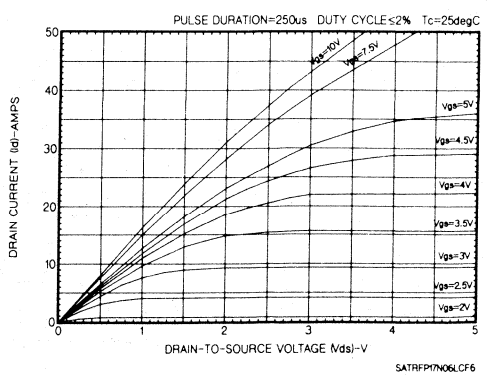


Fig. 7 - Typical saturation characteristics for all types.

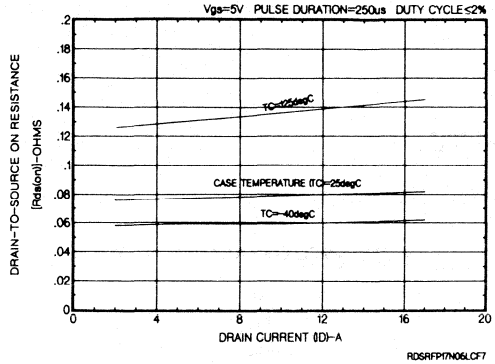


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

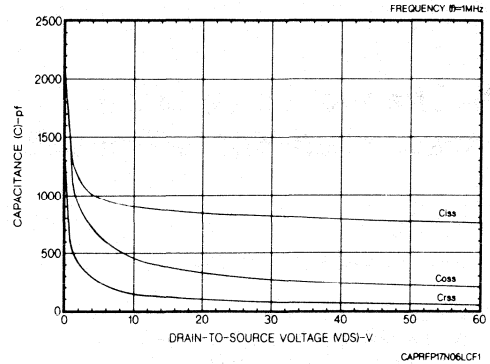


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

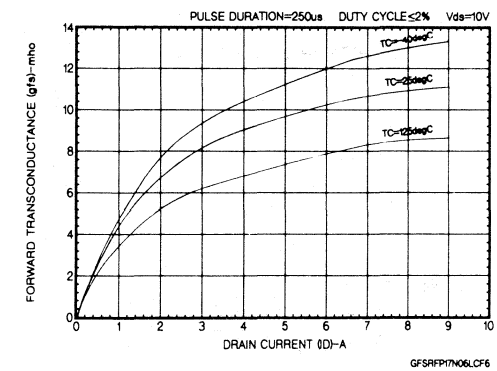


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

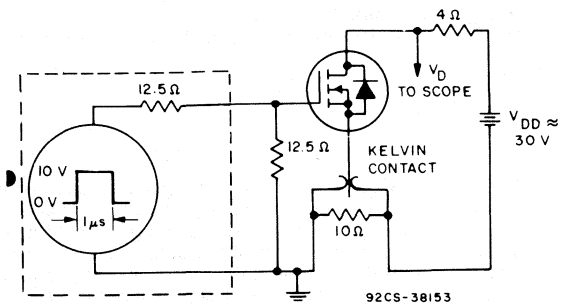


Fig. 11 - Switching Time Test Circuit.

RFP25N06L

File Number **2044**

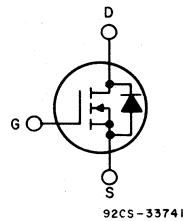
N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

25 A, 50 V - 60 V
$r_{DS}(on)$ = 0.085 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



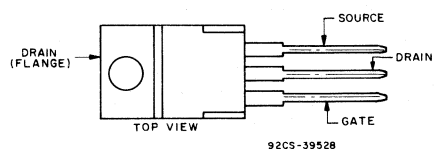
TERMINAL DIAGRAM

The RFP25N06L* is an n-channel enhancement-mode silicon-gate power field-effect transistor specifically designed for use with logic level (5-volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3 - 5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP-series types are supplied in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP2506L is F25N06L.

TERMINAL DESIGNATION



JEDEC TO-220AB

*The RFP series was formerly RCA developmental number TA9638.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	60	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ)	V_{DGR}	60	V
GATE-SOURCE VOLTAGE	V_{GS}	±10	V
DRAIN CURRENT, RMS Continuous	I_D	25	A
RMS Continuous @ T_C = 85 °C		18	A
Pulsed	I_{DM}	60	W
POWER DISSIPATION @ T_C = 25 °C	P_T	75	W
Derate Above T_c = 25 °C		0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTICS		TEST CONDITIONS	LIMITS RFP25N06L MIN.	LIMITS RFP25N06L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 1$ mA	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40$ V	—	—	μA
		$V_{DS} = 50$ V	—	1	
		$T_c = 125$ °C, $V_{DS} = 40$ V	—	—	
		$T_c = 125$ °C, $V_{DS} = 50$ V	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 10$ V, $V_{DS} = 0$	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 5$ V	—	1.06	V
		$I_D = 25$ A, $V_{GS} = 5$ V	—	2.5	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 5$ V	—	0.085	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 5$ V, $I_D = 12.5$ A	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1 MHz	—	2000	pF
Output Capacitance	C_{oss}		—	900	
Reverse Transfer Capacitance	C_{rss}		—	400	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 30$ V, $I_D = 12.5$ A, $R_{gen} = \infty$, $R_{gs} = 6.25\ \Omega$, $V_{GS} = 5$ V	18 (typ.)	60	ns
Rise Time	t_r		120 (typ.)	225	
Turn-Off Delay Time	$t_{d(off)}$		123 (typ.)	225	
Fall Time	t_f		123 (typ.)	200	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFP25N06L	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFP25N06L

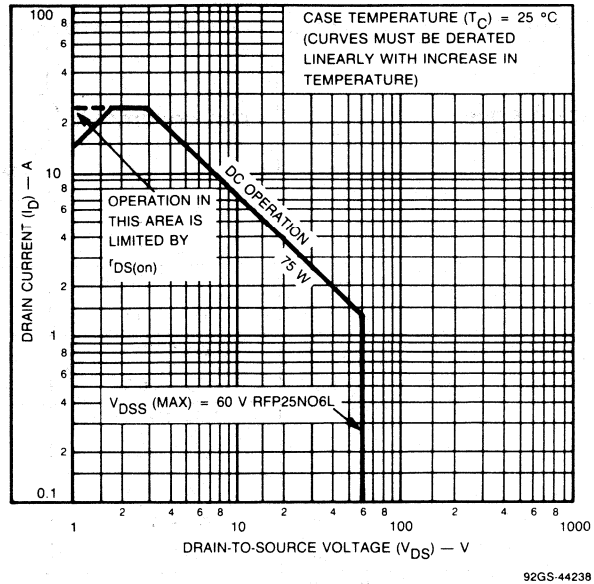


Fig. 1 - Maximum operating areas for all types.

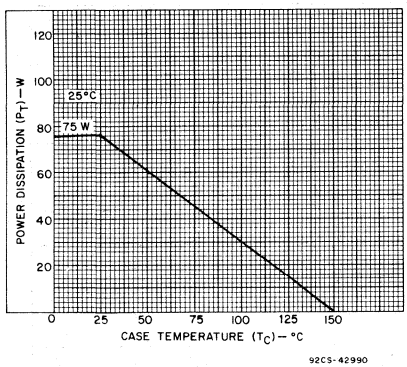


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

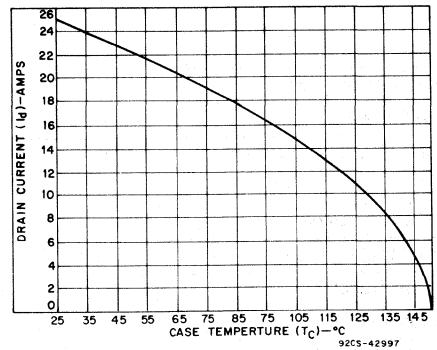


Fig. 3 - Maximum continuous drain current vs. case temperature.

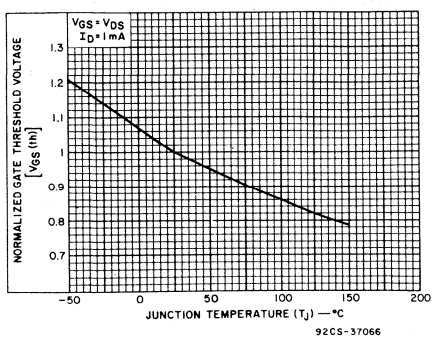


Fig. 4 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

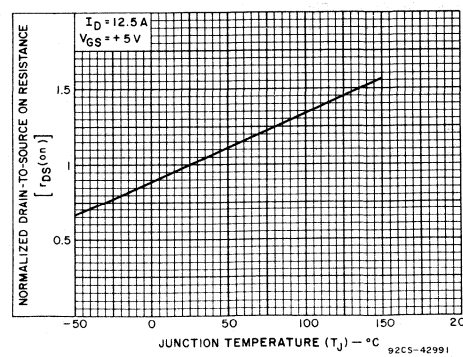


Fig. 5 - Normalized drain-to-source on resistance to junction temperature for all types.

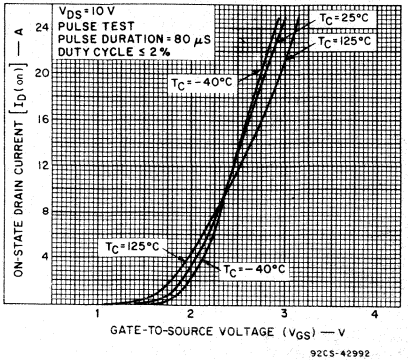


Fig. 6 - Typical transfer characteristics for all types.

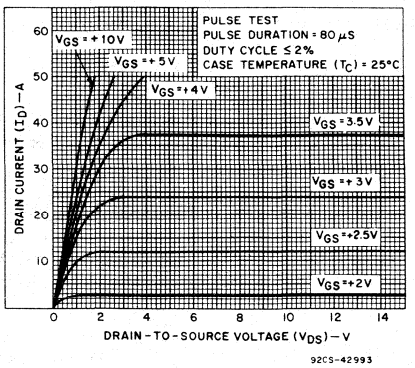


Fig. 7 - Typical output characteristics for all types.

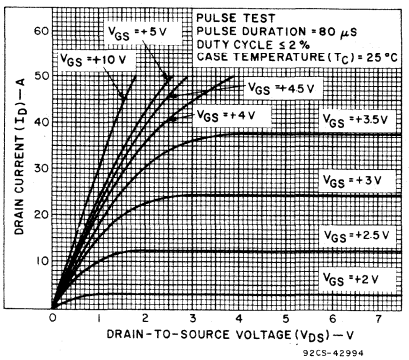


Fig. 8 - Typical saturation characteristics for all types.

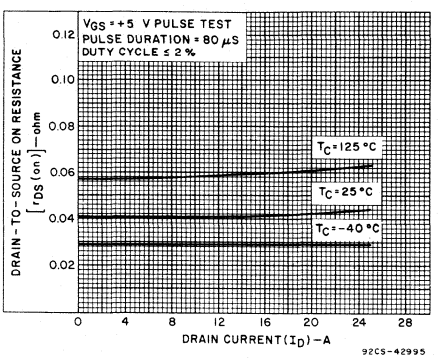


Fig. 9 - Typical drain-to-source on resistance as a function of drain current for all types.

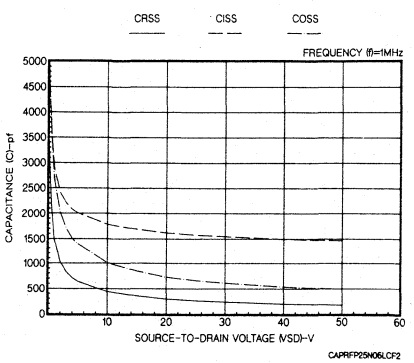


Fig. 10 - Typical capacitance vs. voltage.

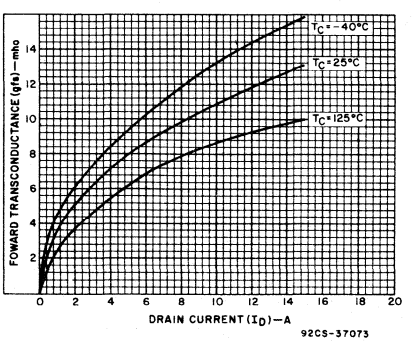


Fig. 11 - Typical forward transconductance as a function of drain current for all types.

RFP25N06L

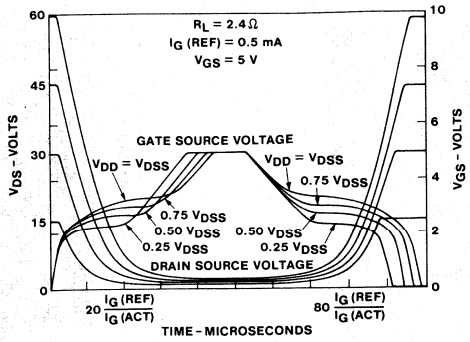


Fig. 12 - Normalized switching waveforms for constant gate-current. (Refer to RCA application notes AN7254 and AN7260.)

File Number **2252**

RLP1N08L

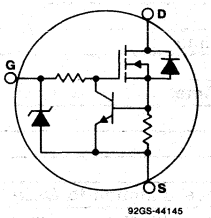
Current Limited - ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

1 A, 80 V
$r_{DS}(on)$: 0.75 Ω
I_{limit} = 1.5 A Maximum at 150° C

Features:

- *Built-in current limiting*
- *ESD protected*
- *Controlled switching limits EMI and RFI*
- *Specified for 150° C operation*

N-CHANNEL ENHANCEMENT MODE



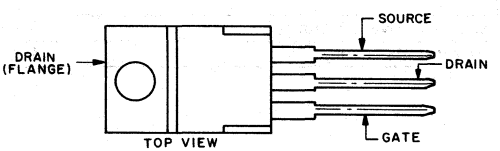
92GS-44145

TERMINAL DIAGRAM

The RLP1N08L is a semi-smart monolithic power circuit which incorporates a lateral bipolar transistor, two resistors, a zener diode, and a PowerMOS transistor. Good control of the current-limiting levels allows use of these devices where a shorted load condition may be encountered. "Logic level" gates allow this device to be fully biased on with only 5 volts from gate to source. The zener diode provides ESD protection up to 2 kV. These devices can be produced on the standard PowerMOS production line.

The RLP-series types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

DRAIN-SOURCE VOLTAGE	V_{DSS}	80	V
DRAIN-GATE VOLTAGE	V_{DGR}	80	V
• GATE-SOURCE VOLTAGE	V_{GS}	5.5	V
Reverse voltage gate bias not allowed			
ELECTROSTATIC VOLTAGE at 100 pF, 1500 Ω	ESD	2	kV
DRAIN CURRENT, RMS Continuous	I_D	Self Limited	
POWER DISSIPATION at T_C = 25° C	P_T	75	W
Derate above 25° C		0.24	W/° C
OPERATING AND STORAGE TEMPERATURE	T_S, T_J	-55 to +150	°C

•May be exceeded if current is limited to 10 mA.

RLP1N08L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V	80	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	1	2	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V, V_{GS} = 0 V	—	1	μA
		T_C = 150° C	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 5 V, T_C = 150° C	—	50	
On Resistance	$r_{DS}(on)$	I_D = 1 A, V_{GS} = 5 V	—	0.75	Ω
		T_C = 150° C	—	1.5	
Limiting Current	$I_{DS}(Lim)$	V_{DS} = 15 V, V_{GS} = 5 V	1.8	3	A
		T_C = 150° C	1.1	1.5	
Turn-On Time	t(on)	V_{DD} = 30 V, I_D = 1 A	—	6.5	μs
Turn-On Delay Time	$t_d(on)$	V_{GS} = 5 V, R_{GS} = 25 Ω	—	1.5	
Rise Time	t_r	R1 = 30 Ω	1	5	
Turn-Off Delay Time	$t_d(off)$		—	7.5	
Fall Time	t_f		1	5	
Turn-Off Time	t(off)		—	12.5	
Plateau Voltage	V(plateau)	I_D = 1 A, V_{DS} = 15 V	—	5	V
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$		—	4.17	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$		—	80	
Electrostatic Voltage	ESD	Human Model (100 pF, 1.5 kΩ)	2000	—	V

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 1 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 1 A	—	1	ms

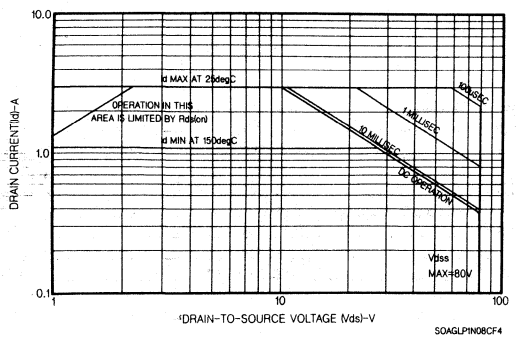


Fig. 1 - Safe-operating-area curve.

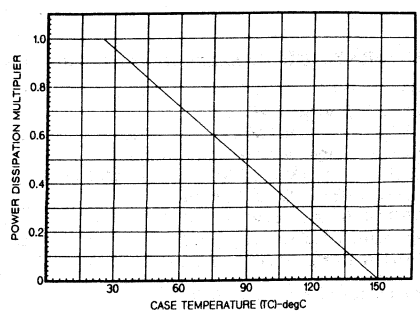


Fig. 2 - Normalized power dissipation vs. temperature derating curve.

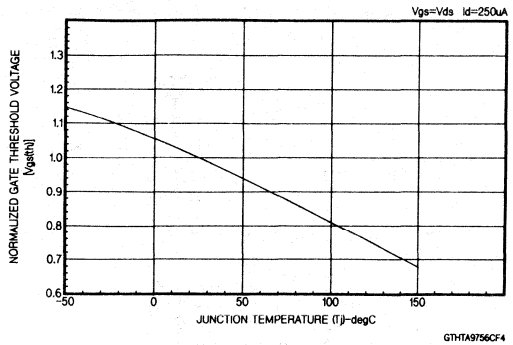


Fig. 3 - Typical normalized gate-threshold voltage.

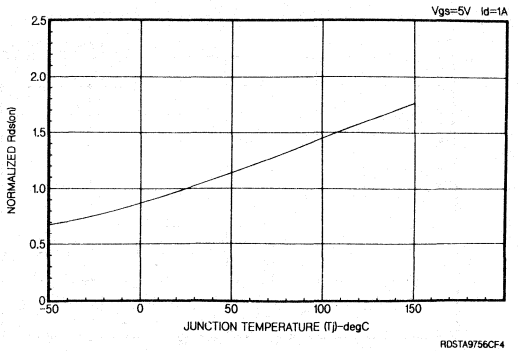


Fig. 4 - Normalized $r_{DS}(on)$ vs. junction temperature.

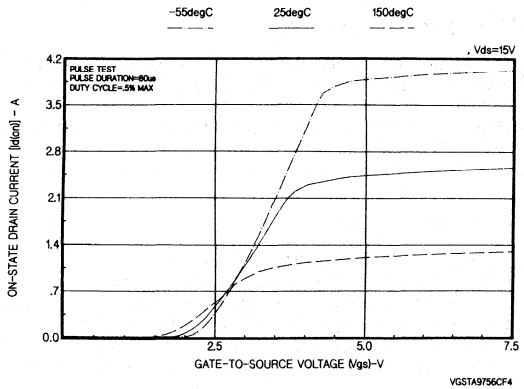


Fig. 5 - Typical transfer characteristics.

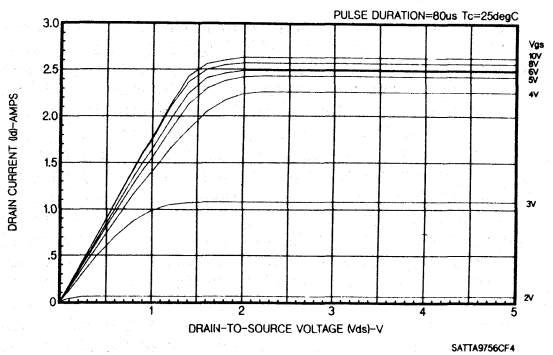


Fig. 6 - Typical saturation characteristics.

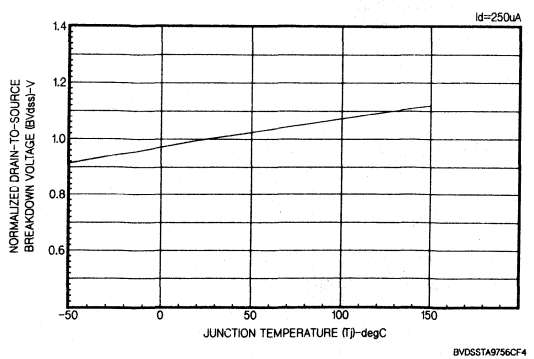


Fig. 7 - Drain-source breakdown voltage vs. temperature.

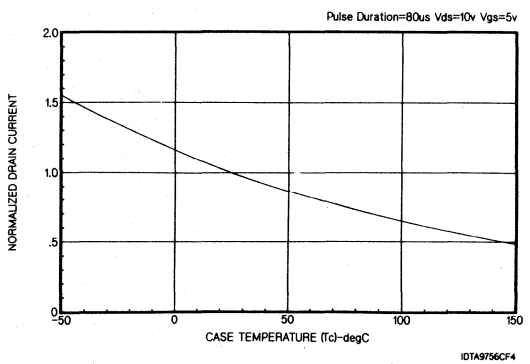


Fig. 8 - Normalized current limit vs. temperature.

RLP1N08L

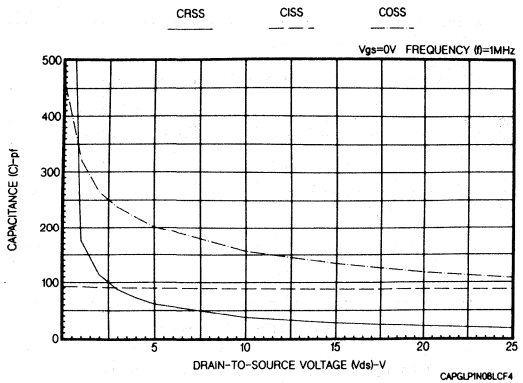


Fig. 9 - Typical capacitance vs. voltage.

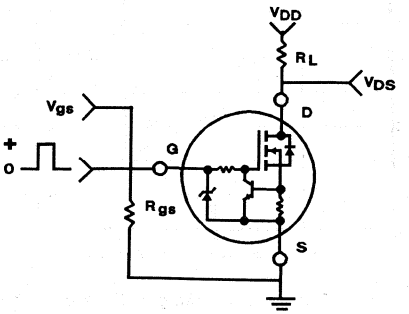


Fig. 10 - Switching test circuit.

Temperature Dependence of Current Limiting and Switching Speed

The RLP1N08L is a monolithic power device which incorporates a Logic Level PowerMOS transistor with a resistor in series with the source. The base and emitter of a lateral bipolar transistor is connected across this resistor, and the collector of the bipolar transistor is connected to the gate of the PowerMOS transistor. When the voltage across the resistor reaches the value required to forward bias the emitter base junction of the bipolar transistor, the bipolar transistor "turns on". A series resistor is incorporated in series with the gate of the PowerMOS transistor allowing the bipolar transistor to drive the gate of the PowerMOS transistor to a voltage which just maintains a constant current in the PowerMOS transistor. Since both the resistance of the resistor in series with the PowerMOS transistor source and the voltage required to forward bias the base emitter junction of the bipolar transistor vary with the temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 8.

The resistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP1N08L

The limit on drain-to-source voltage for operation in current limiting on a steady state (dc) basis is shown as Figure A. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOS devices today, is limited to 150°C. The maximum voltage allowable can, therefore, be expressed as:

$$V_s = \frac{(150 - \text{Tambient})}{I_{lim}\,(R_{\theta JC} + R_{\theta})}$$

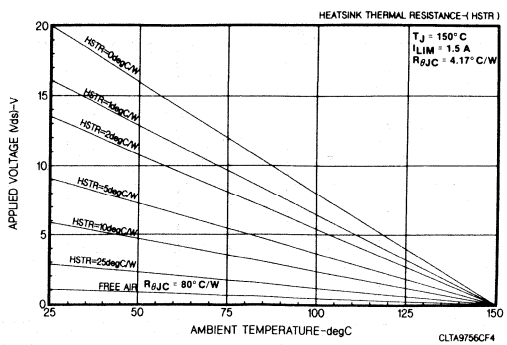


Fig. A - DC operation in current limiting.

Duty Cycle Operation of the RLP1N08L

In many applications either the drain-to-source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N08L is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_c = (V_{SD} * I_D * D * R_{\theta CA}) + \text{Tambient}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 150°C and using the T_C calculated above, the expression for maximum V_{SD} under duty cycle operation is:

$$V_{SD} = \frac{150 - T_c}{I_{lim} * D * R_{\theta JC}}$$

These values are plotted as Figures B1 - B5 for various heat sink thermal resistances.

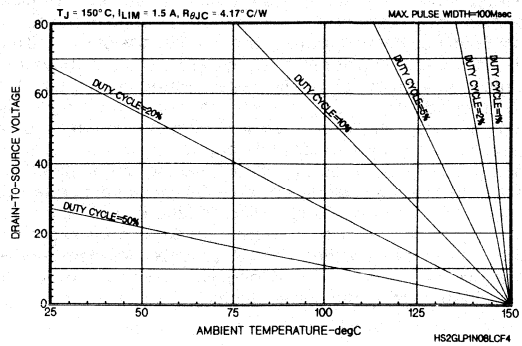


Fig. B1 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 2° C/W)

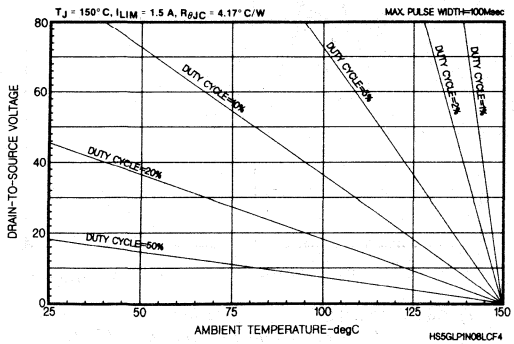


Fig. B2 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 5° C/W)

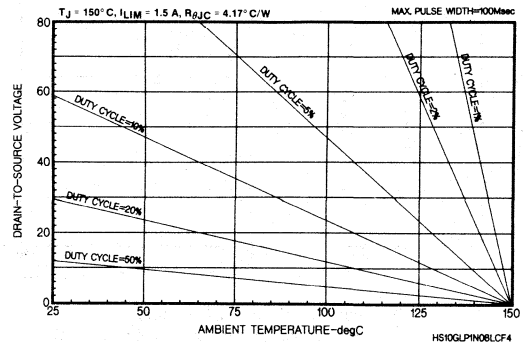


Fig. B3 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 10° C/W)

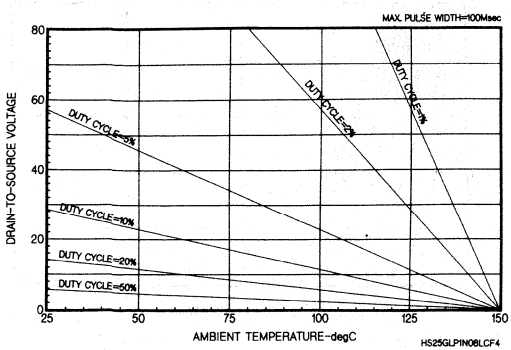


Fig. B4 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 25° C/W)

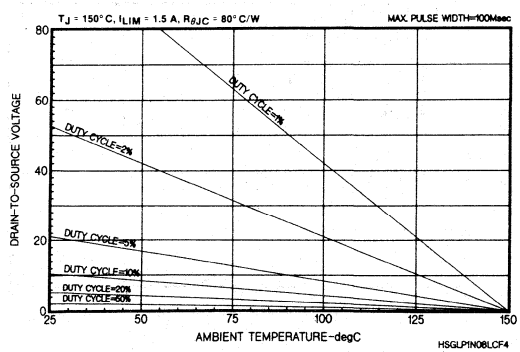


Fig. B5 - Maximum V_{DS} vs. ambient temperature in current limiting. (No external heatsink)

RLP1N08L

Limited Time Operations of the RLP1N08L

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1 - C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 150°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

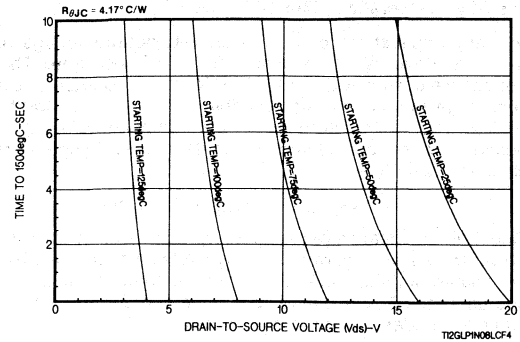


Fig. C1 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 2° C/W
Heatsink thermal capacitance = 4 j/° C)

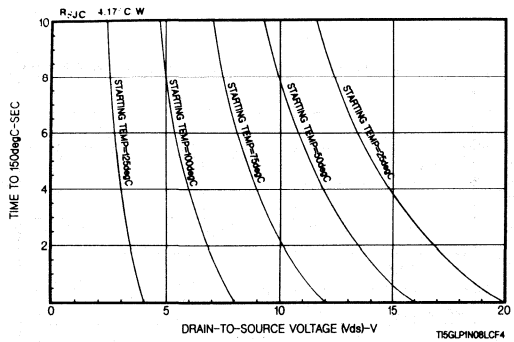


Fig. C2 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 5° C/W
Heatsink thermal capacitance = 2 j/° C)

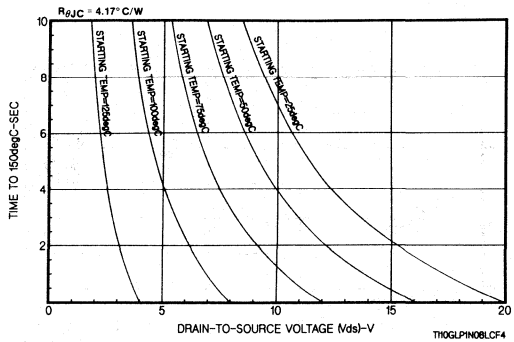


Fig. C3 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 10° C/W
Heatsink thermal capacitance = 1 j/° C)

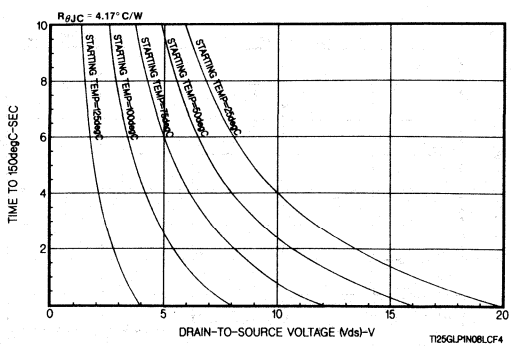


Fig. C4 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 25° C/W
Heatsink thermal capacitance = 5 j/° C)

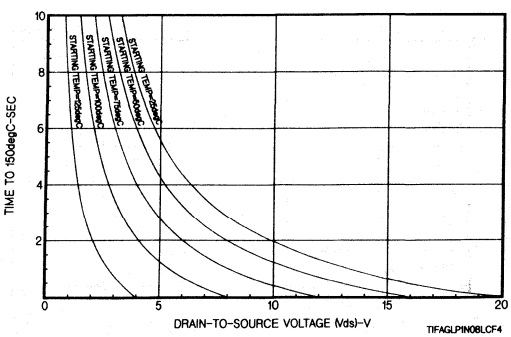


Fig. C5 - Time to 150° C in current limiting.
(No external heatsink)

File Number **1877**

2N6901

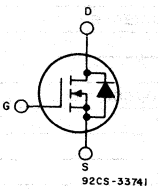
N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

$r_{DS}(on)$: 1.4 Ω

Features:

- *Design optimized for 5-volt gate drive*
- *Can be driven directly from QMOS, NMOS, TTL circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

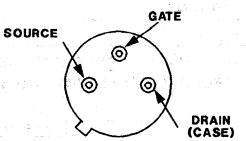


TERMINAL DIAGRAM

The 2N6901 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6901 is supplied in the JEDEC TO-205AF metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

*DRAIN-SOURCE VOLTAGE, V_{DSS}	100 V
*DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	100 V
*GATE-SOURCE VOLTAGE, V_{GS}	±10 V
*DRAIN CURRENT:	
RMS Continuous, I_D	1.69 A
Pulsed, I_{DM}	5 A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	8.33 W
Above T_C = 25°C	Derate linearly 0.0667 W/°C
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances ≥ ⅛ in. (3.17 mm) from seating plane for 10 s max.	260°C

*In accordance with JEDEC registration data.

2N6901

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V	—	1	μA
			T_C = 125°C, V_{DS} = 80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 1.07 A, V_{GS} = 5 V	—	1.5	V
			I_D = 1.69 A, V_{GS} = 5 V	—	2.4	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 1.07 A, V_{GS} = 5 V	—	1.4	Ω
			T_C = 125°C, I_D = 1.07 A, V_{GS} = 5 V	—	2.6	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 1.07 A	500	2000	mmho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	50	200	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	20	80	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	5	20	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	—	25	ns
*	Rise Time	t_r	I_D = 1.07 A	—	45	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	45	
*	Fall Time	t_f	V_{GS} = 5 V	—	80	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1.69 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 1 A, d_{IF}/dt = 50 A/μs	—	250	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

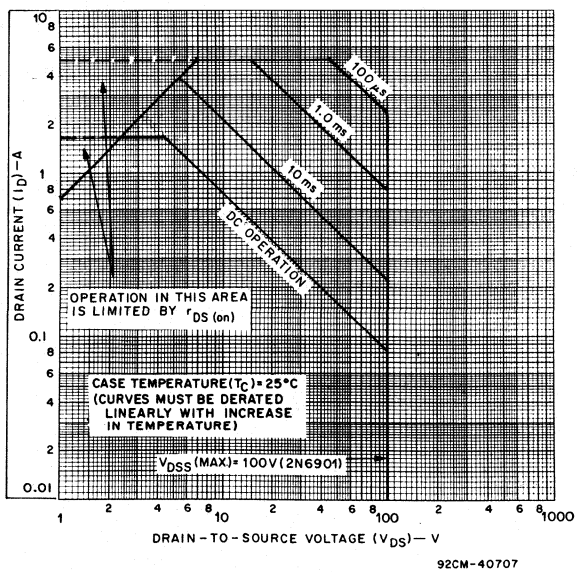


Fig. 1 - Maximum operating areas.

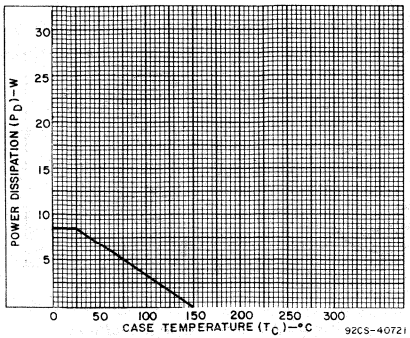


Fig. 2 - Power dissipation vs. temperature derating curve.

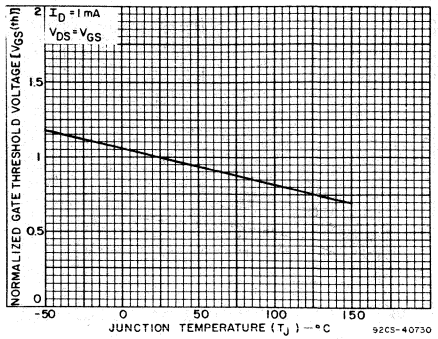


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

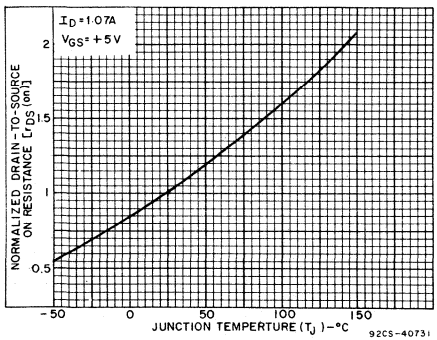


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

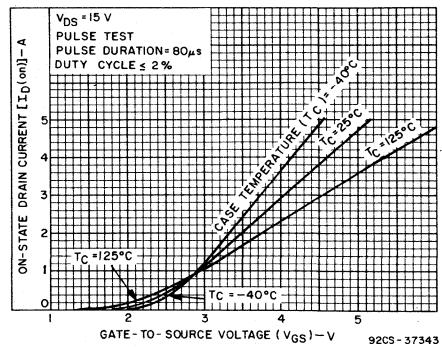


Fig. 5 - Typical transfer characteristics.

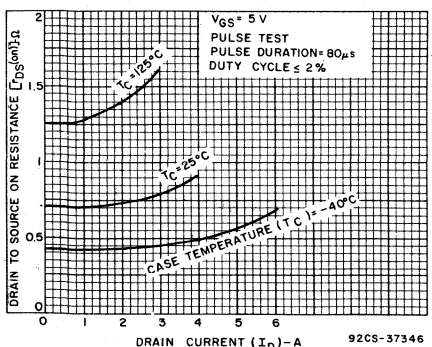


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

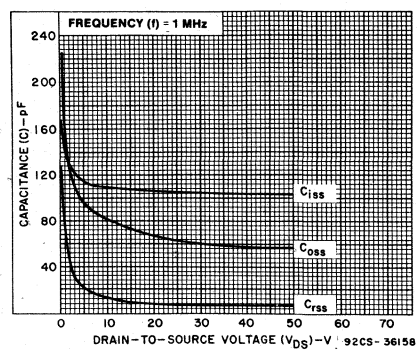


Fig. 7 - Capacitance as a function of drain-to-source voltage.

2N6901

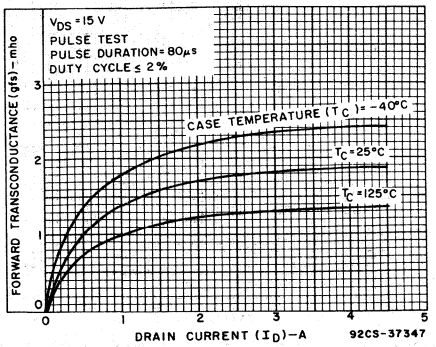


Fig. 8 - Typical forward transconductance as a function of drain current.

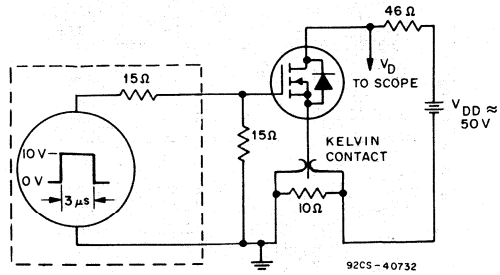


Fig. 9 - Switching time test circuit.

File Number **1878**

2N6902

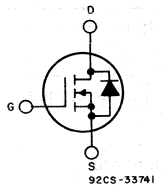
N-Channel Logic Level Power MOS Field-Effect Transistors (L^2 FET)

12 A, 100 V
$r_{DS}(on)$: 0.2 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

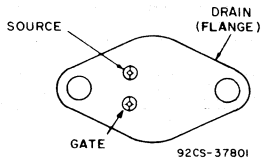


TERMINAL DIAGRAM

The 2N6902 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6902 is supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute Maximum Values* (T_C = 25° C):

* DRAIN-SOURCE VOLTAGE, V_{DSS}	100 V
* DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ), V_{DGR}	100 V
* GATE-SOURCE VOLTAGE, V_{GS}	±10 V
* DRAIN CURRENT, RMS Continuous, I_D	12 A
Pulsed, I_{DM}	30 A
* POWER DISSIPATION, P_T	
At T_C = 25° C	75 W
Above T_C = 25° C, Derate Linearly	0.6 W/° C
* OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150° C
* LEAD TEMPERATURE, T_L	
At distance ≥ 1/8 in. (3.17 mm) from seating plane for 10 s max.	260° C

* In accordance with JEDEC registration data

2N6902

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C = 25° C) unless otherwise specified

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V	—	1	μA
			T_C = 125° C, V_{DS} = 80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = 5 V	—	1.52	V
			I_D = 12 A, V_{GS} = 5 V	—	3.3	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.6 A	—	0.2	Ω
			T_C=125° C, I_D=7.6 A, V_{GS}=5 V	—	0.32	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 7.6 A	3	12	mho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	350	900	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	100	325	
*	Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	25	100	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	—	50	ns
*	Rise Time	t_r	I_D = 7.6 V	—	150	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	130	
*	Fall Time	t_f	V_{GS} = 5 V	—	150	
*	Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A d_{IF}/d_t = 100 A/μs	—	375	ns

* In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs, max., duty cycle = 2%.

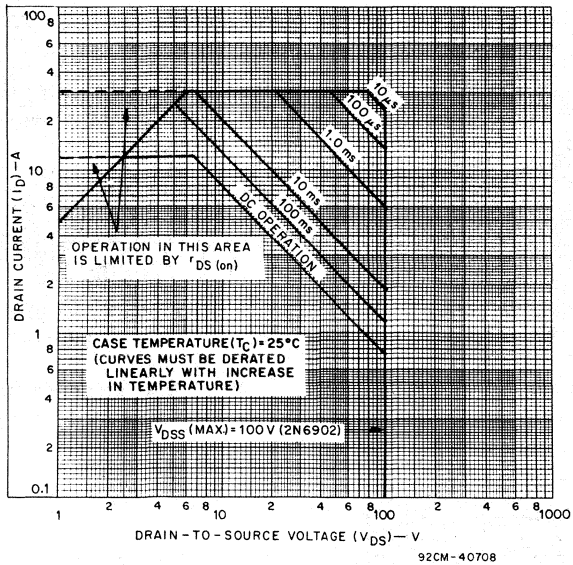


Fig. 1 - Maximum safe operating areas.

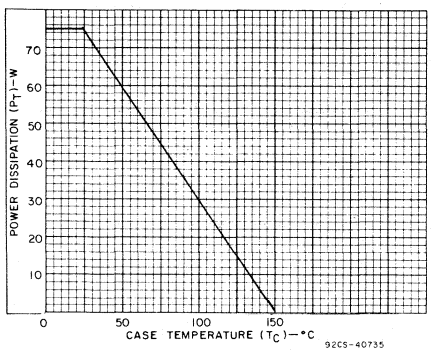


Fig. 2 - Power dissipation vs. temperature derating curve.

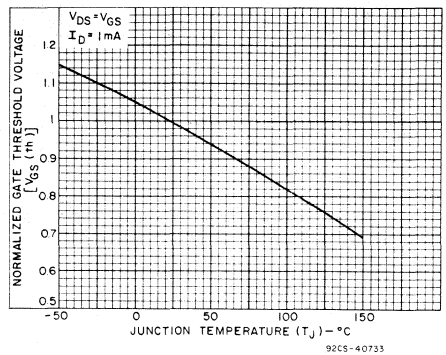


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

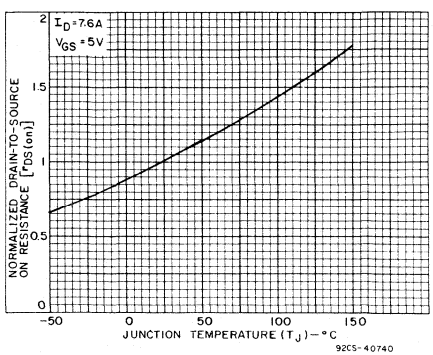


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

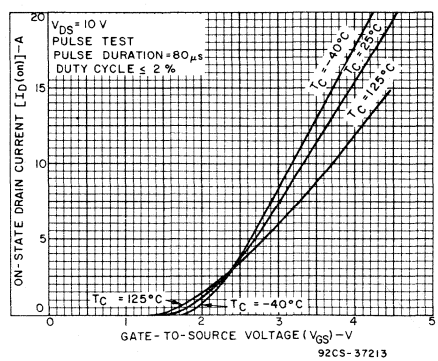


Fig. 5 - Typical transfer characteristics.

2N6902

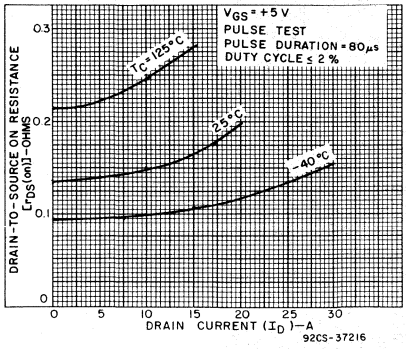


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

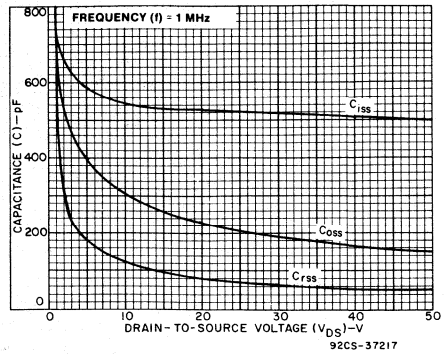


Fig. 7 - Capacitance as a function of drain-to-source voltage.

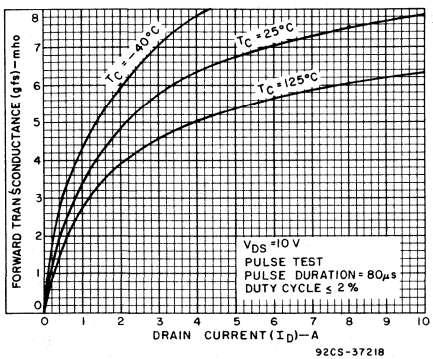


Fig. 8 - Typical forward transconductance as a function of drain current.

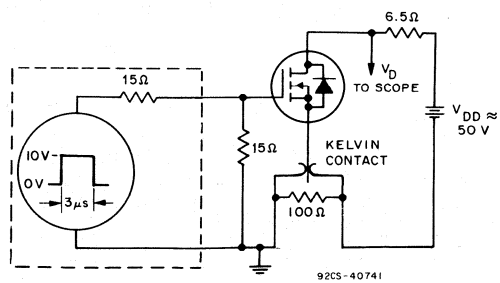


Fig. 9 - Switching time test circuit.

File Number **1879**

2N6903

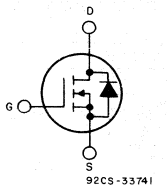
N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

$r_{DS}(on)$: 3.65 Ω

Features:

- *Design optimized for 5-volt gate drive*
- *Can be driven directly from QMOS, NMOS, TTL circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

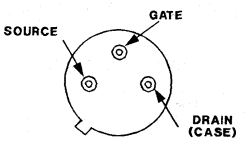


TERMINAL DIAGRAM

The 2N6903 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6903 is supplied in the JEDEC TO-205AF metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

*DRAIN-SOURCE VOLTAGE, V_{DSS}	200 V
*DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	200 V
*GATE-SOURCE VOLTAGE, V_{GS}	±10 V
*DRAIN CURRENT:	
RMS Continuous, I_D	0.98 A
Pulsed, I_{DM}	4 A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	8.33 W
Above T_C = 25°C	Derate linearly 0.0667 W/°C
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances ≥ ⅛ in. (3.17 mm) from seating plane for 10 s max.	260°C

*In accordance with JEDEC registration data.

2N6903

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	200	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V	—	1	μA
			T_C = 125°C, V_{DS} = 160 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 0.62 A, V_{GS} = 5 V	—	2.26	V
			I_D = 0.98 A, V_{GS} = 5 V	—	6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 0.62 A, V_{GS} = 5 V	—	3.65	Ω
			T_C = 125°C, I_D = 0.62 A, V_{GS} = 5 V	—	7.7	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 0.62 A	500	2000	mmho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	50	200	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	15	60	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	2	20	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V	—	25	ns
*	Rise Time	t_r	I_D = 0.62 A	—	30	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	40	
*	Fall Time	t_f	V_{GS} = 5 V	—	80	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 0.98 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 1 A, d_{IF}/dt = 50 A/μs	—	500	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

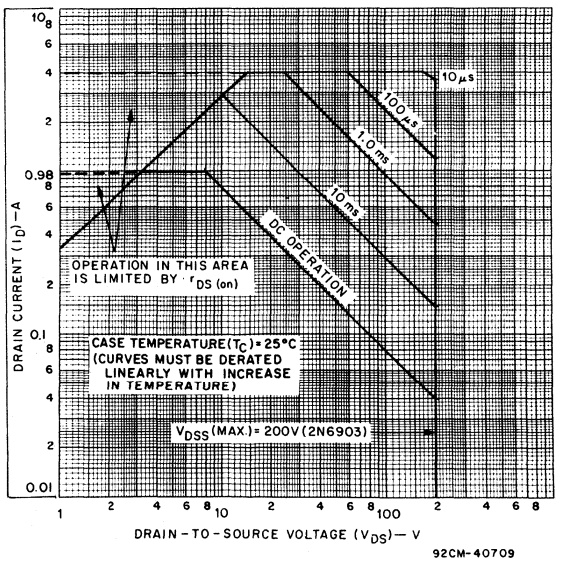


Fig. 1 - Maximum operating areas.

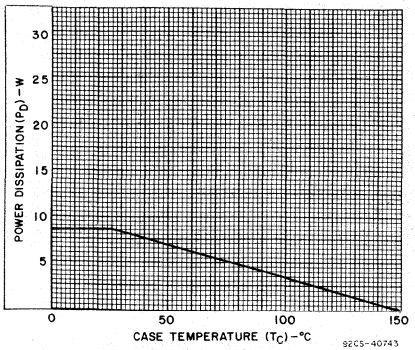


Fig. 2 - Power dissipation vs. temperature derating curve.

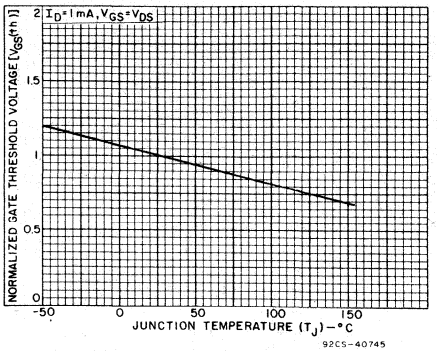


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

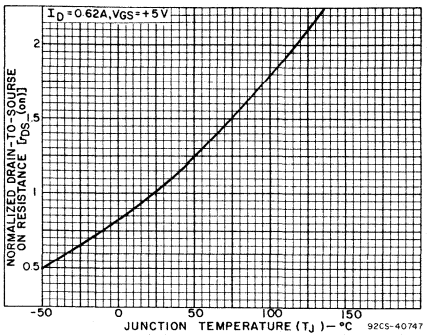


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

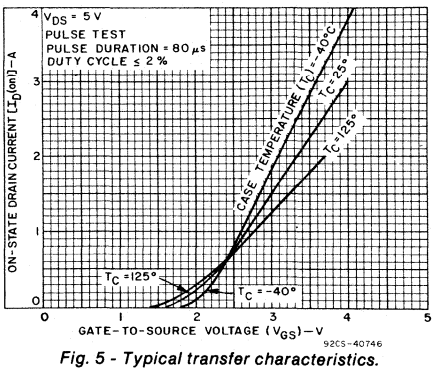


Fig. 5 - Typical transfer characteristics.

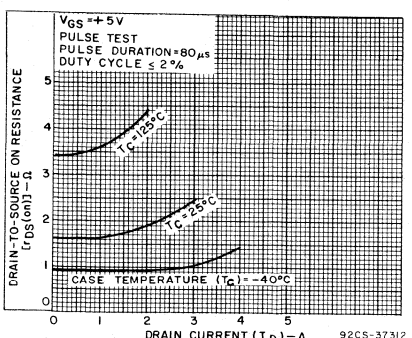


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

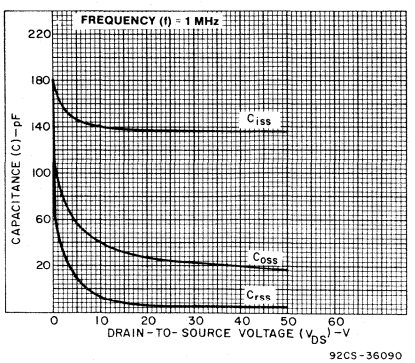


Fig. 7 - Capacitance as a function of drain-to-source voltage.

2N6903

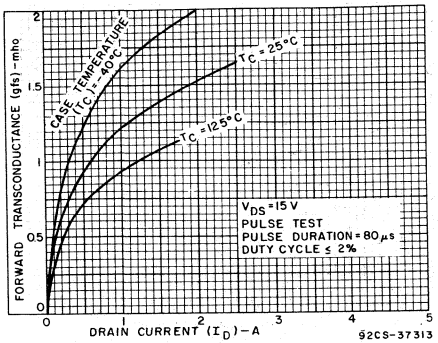


Fig. 8 - Typical forward transconductance as a function of drain current.

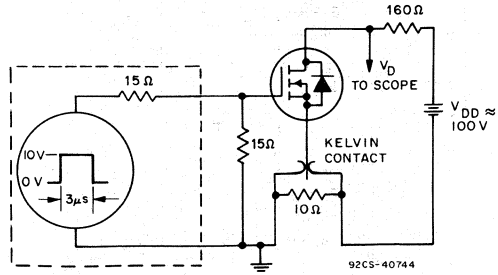


Fig. 9 - Switching time test circuit.

2N6904

File Number **1880**

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2 FET)

8 A, 200 V
$r_{DS}(on)$: 0.6 Ω

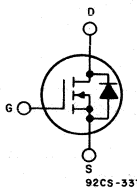
Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6904 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

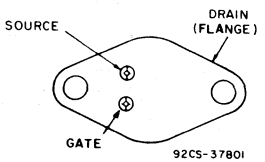
The 2N6904 is supplied in the JEDEC TO-204AA steel package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute Maximum Values* (T_C = 25°C):

* DRAIN-SOURCE VOLTAGE, V_{DSS}	200 V
* DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	200 V
* GATE-SOURCE VOLTAGE, V_{GS}	±10 V
* DAIN CURRENT, RMS Continuous, I_D	8 A
Pulsed, I_{DM}	20 A
* POWER DISSIPATION, P_T	
At T_C = 25°C	75 W
Above T_C = 25°C, Derate Linearly	0.6 W/°C
* OPERATING AND STORAGE TEMPERATURE, T_J, T_{stg}	-55 to +150°C
* LEAD TEMPERATURE, T_L	
At distance ≥ 1/8 in. (3.17 mm) from seating plane for 10 s max.	260°C

* In accordance with JEDEC registration data

2N6904

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C = 25°C) unless otherwise specified

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	200	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V	—	1	μA
			T_C = 125°C, V_{DS} = 160 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5.1 A, V_{GS} = 5 V	—	3.06	V
			I_D = 8 A, V_{GS} = 5 V	—	5.5	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5.1 A	—	0.6	Ω
			T_C=125°C, I_D=5.1 A, V_{GS}=5 V	—	1.11	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 5.1 A	3	12	mho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	350	900	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	75	250	
*	Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	20	100	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V	—	45	ns
*	Rise Time	t_r	I_D = 5.1 A	—	150	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	135	
*	Fall Time	t_f	V_{GS} = 5 V	—	150	
*	Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 8 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A d_{IF}/d_t = 100 A/μs	—	625	ns

* In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs, max., duty cycle = 2%.

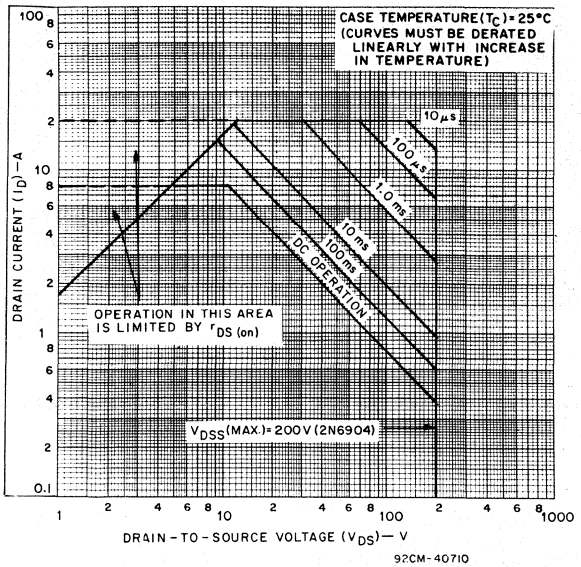


Fig. 1 - Maximum safe operating areas.

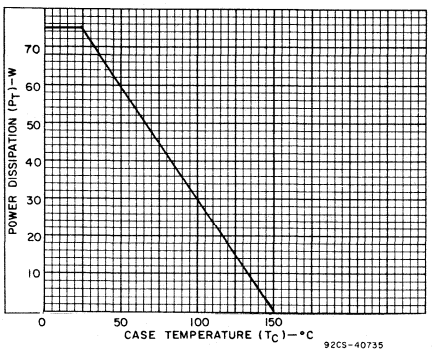


Fig. 2 - Power dissipation vs. temperature derating curve.

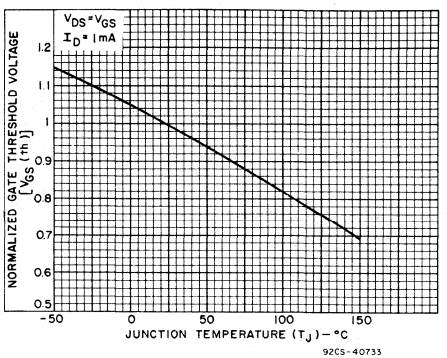


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

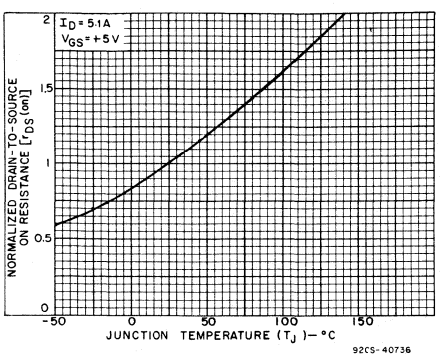


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

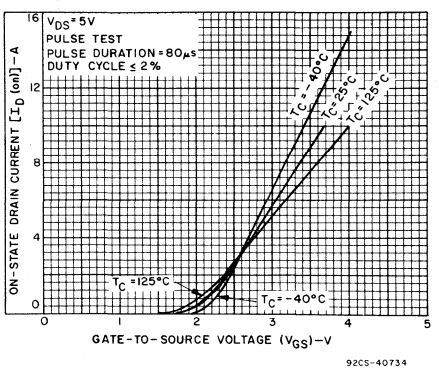


Fig. 5 - Typical transfer characteristics.

2N6904

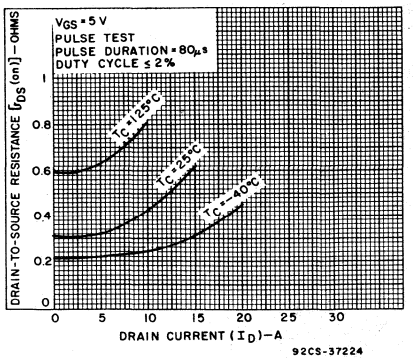


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

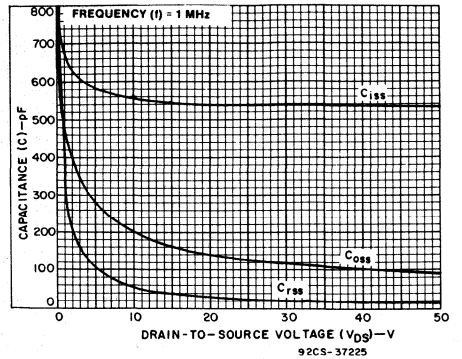


Fig. 7 - Capacitance as a function of drain-to-source voltage.

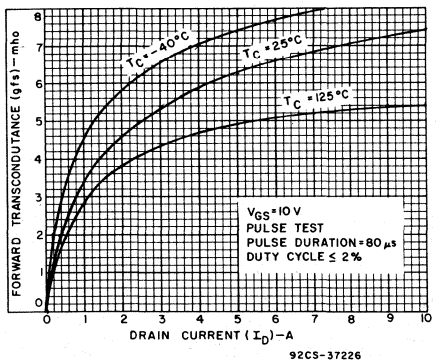


Fig. 8 - Typical forward transconductance as a function of drain current.

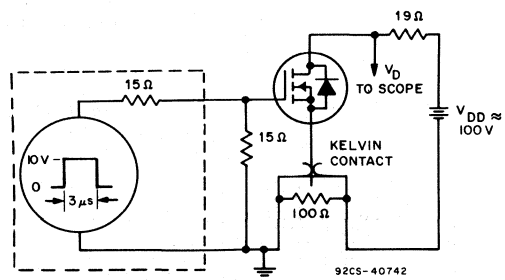


Fig. 9 - Switching time test circuit.

Rugged Power MOSFETs

N-Channel 6-2
P-Channel—JEDEC 6-320
P-Channel 6-335

IRF130R, IRF131R, IRF132R, IRF133R

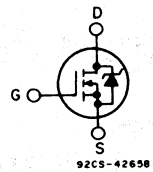
File Number **1986**

Avalanche Energy Rated N-Channel Power MOSFETs

12A and 14A, 60V-100V
$r_{DS}(on) = 0.18\Omega$ and 0.25Ω

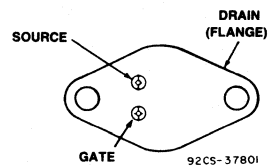
N-CHANNEL ENHANCEMENT MODE

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO - 204AA

The IRF130R, IRF131R, IRF132R and IRF133R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

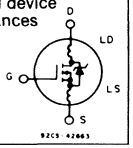
Absolute Maximum Ratings

Parameter		IRF130R	IRF131R	IRF132R	IRF133R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	14	14	12	12	A
I_D @ $T_C = 100°C$	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	69				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF130R IRF132R	100	—	—	V	V_{GS} = 0V
		IRF131R IRF133R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF130R IRF131R	14	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF132R IRF133R	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF130R IRF131R	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF132R IRF133R	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	—	S(Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 8.0A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} = 36V, I_D = 8.0A, Z_o = 15Ω
t_r	Rise Time	ALL	—	—	75	ns	See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	40	ns	
t_f	Fall Time	ALL	—	—	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

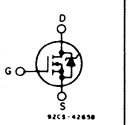


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF130R IRF131R	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF132R IRF133R	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF130R IRF131R	—	—	56	A	
		IRF132R IRF133R	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	IRF130R IRF131R	—	—	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF132R IRF133R	—	—	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_j = 25°C, L = 530μH, R_{gs} = 25Ω, I_{peak} = 14A. See figures 15, 16.

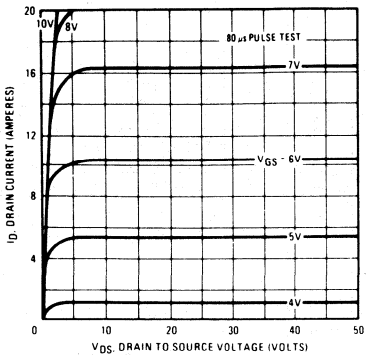


Fig. 1 – Typical Output Characteristics

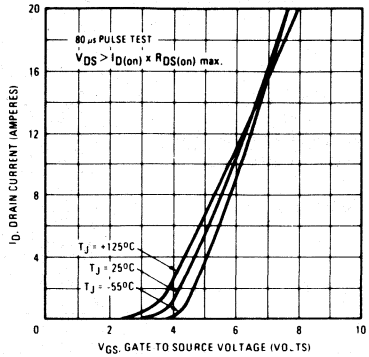


Fig. 2 – Typical Transfer Characteristics

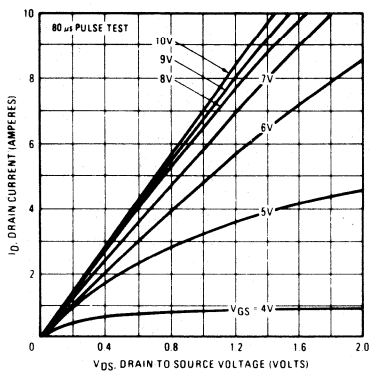


Fig. 3 – Typical Saturation Characteristics

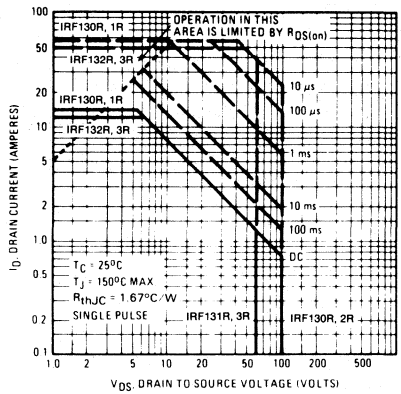


Fig. 4 – Maximum Safe Operating Area

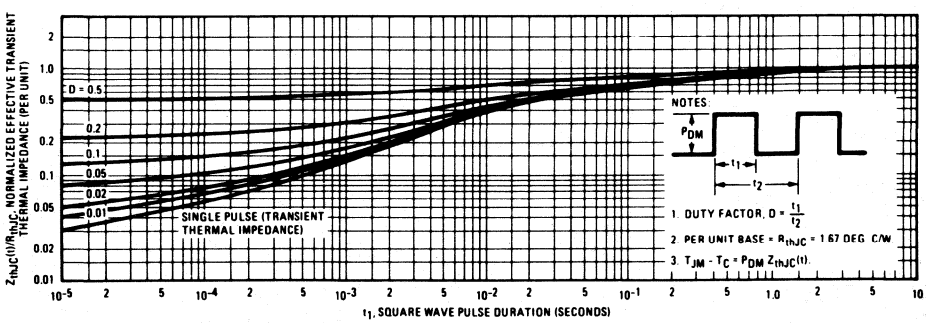


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

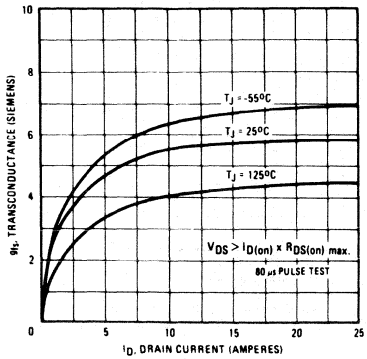


Fig. 6 – Typical Transconductance Vs. Drain Current

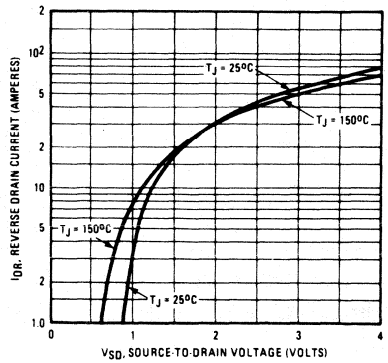


Fig. 7 – Typical Source-Drain Diode Forward Voltage

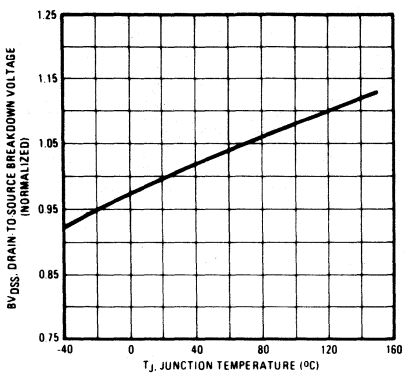


Fig. 8 – Breakdown Voltage Vs. Temperature

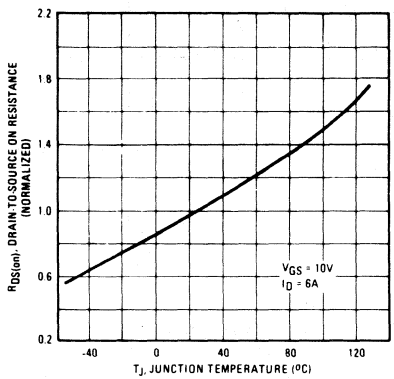


Fig. 9 – Normalized On-Resistance Vs. Temperature

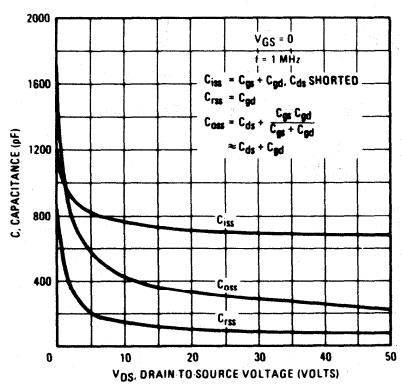


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

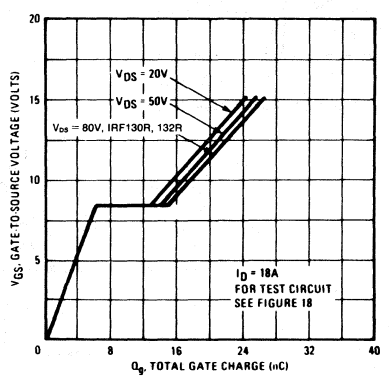


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF130R, IRF131R, IRF132R, IRF133R

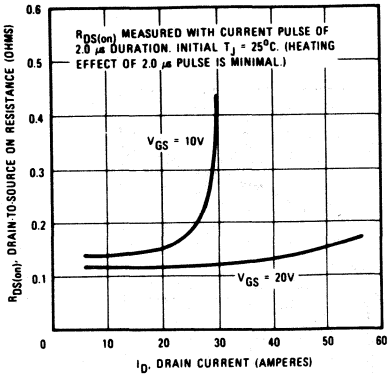


Fig. 12 – Typical On-Resistance Vs. Drain Current

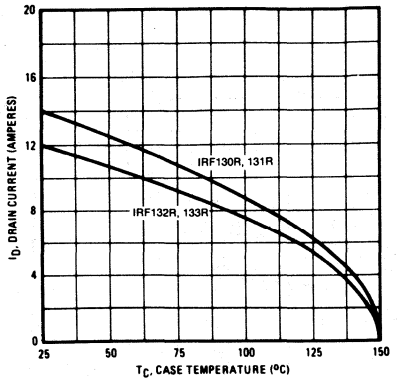


Fig. 13 – Maximum Drain Current Vs. Case Temperature

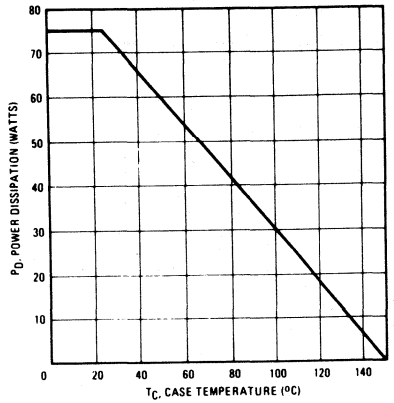


Fig. 14 – Power Vs. Temperature Derating Curve

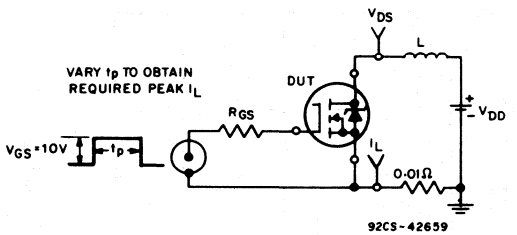


Fig. 15 — Unclamped Energy Test Circuit

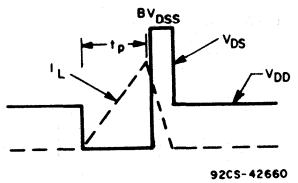


Fig. 16 — Unclamped Energy Waveforms

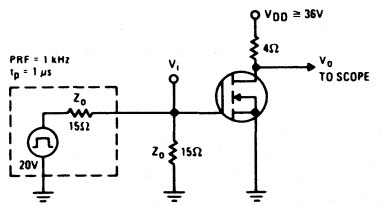


Fig. 17 – Switching Time Test Circuit

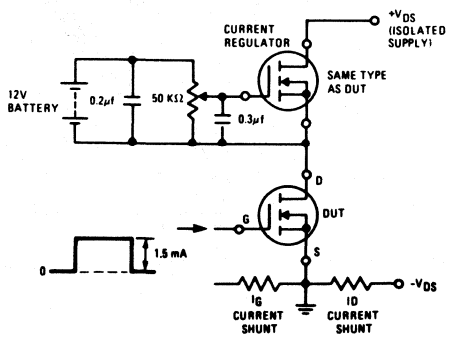


Fig. 18 – Gate Charge Test Circuit

File Number **2001**

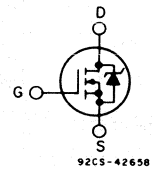
IRF140R, IRF141R
IRF142R, IRF143R

Avalanche Energy Rated N-Channel Power MOSFETs

27A and 24A, 60V-100V
$r_{DS}(on) = 0.085\Omega$ and 0.11Ω

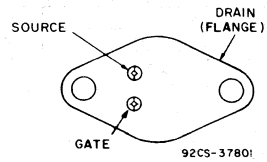
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AE

The IRF140R, IRF141R, IRF142R and IRF143R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE steel package.

Absolute Maximum Ratings

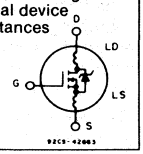
Parameter		IRF140R	IRF141R	IRF142R	IRF143R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	27	27	24	24	A
I_D @ T_C = 100°C	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	100				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF140R, IRF141R
IRF142R, IRF143R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF140R IRF142R	100	—	—	V	V_{GS} = 0V
		IRF141R IRF143R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF140R IRF141R	27	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF142R IRF143R	24	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF140R IRF141R	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		IRF142R IRF143R	—	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 15A
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	550	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} \simeq$ 30V, I_D = 15A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	38	80	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	17	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	21	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

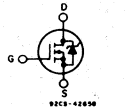


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF140R IRF141R	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF142R IRF143R	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF140R IRF141R	—	—	108	A	
		IRF142R IRF143R	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	IRF140R IRF141R	—	—	2.5	V	T_C = 25°C, I_S = 27A, V_{GS} = 0V
		IRF142R IRF143R	—	—	2.3	V	T_C = 25°C, I_S = 24A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 10V, starting T_J = 25°C, L = 250μH, R_{gs} = 50Ω, I_{peak} = 27A. See figures 15, 16.

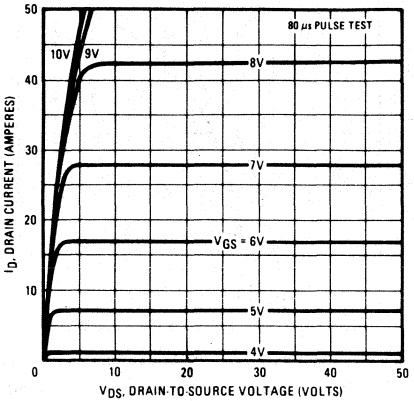


Fig. 1 – Typical Output Characteristics

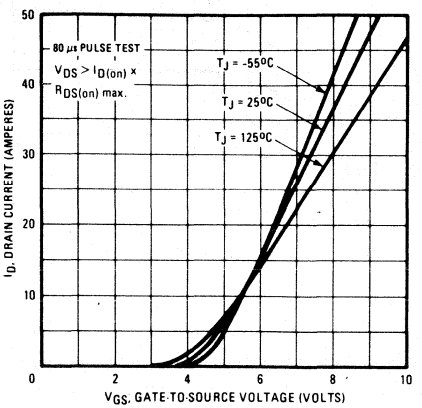


Fig. 2 – Typical Transfer Characteristics

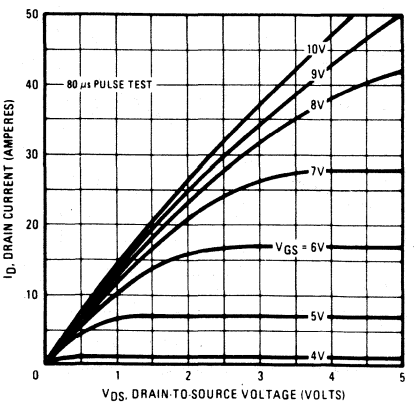


Fig. 3 – Typical Saturation Characteristics

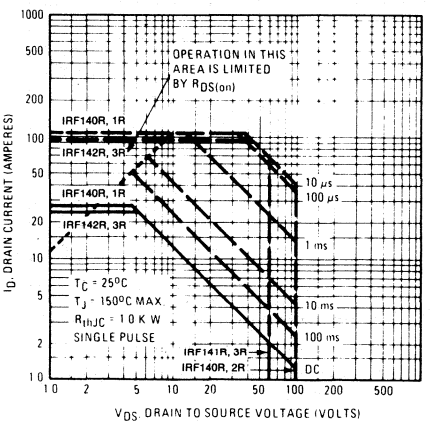


Fig. 4 – Maximum Safe Operating Area

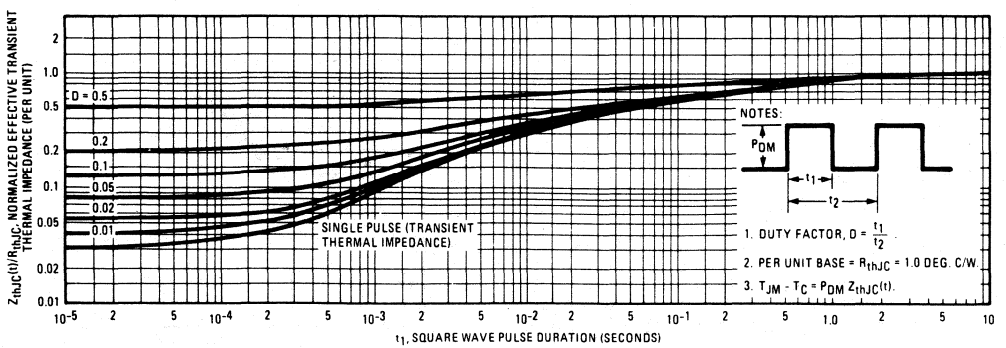


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

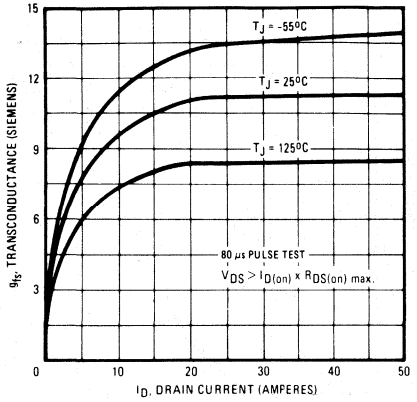


Fig. 6 – Typical Transconductance Vs. Drain Current

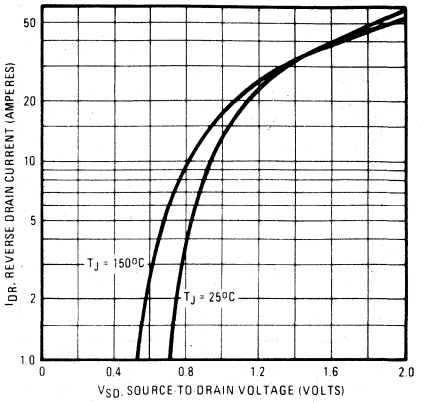


Fig. 7 – Typical Source-Drain Diode Forward Voltage

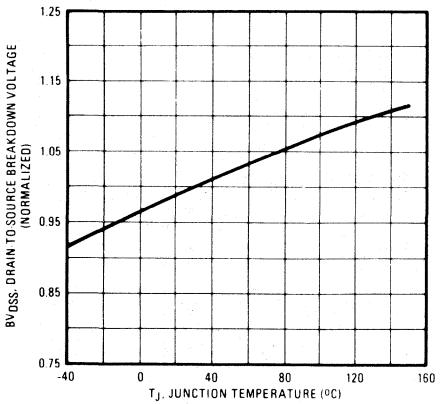


Fig. 8 – Breakdown Voltage Vs. Temperature

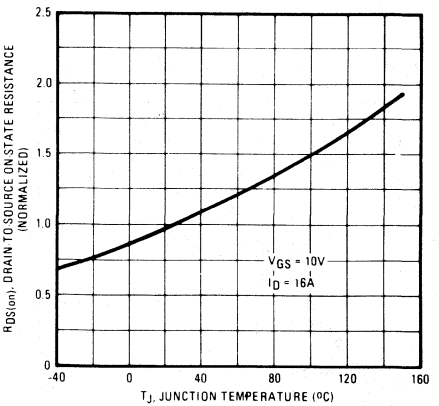


Fig. 9 – Normalized On-Resistance Vs. Temperature

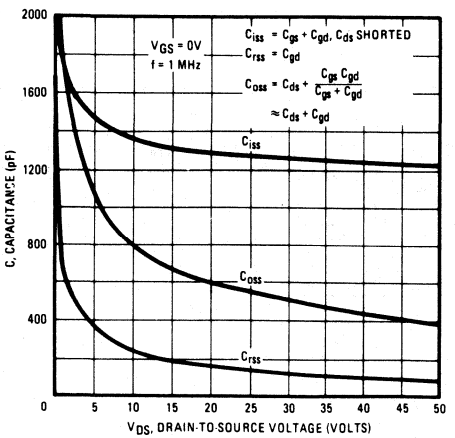


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

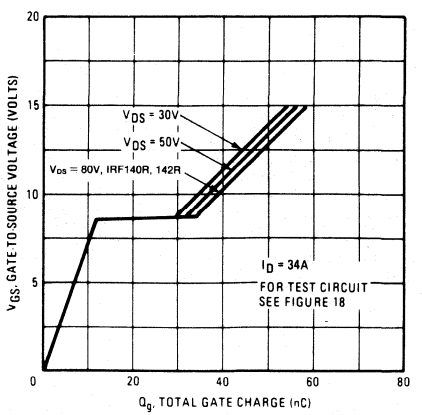


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

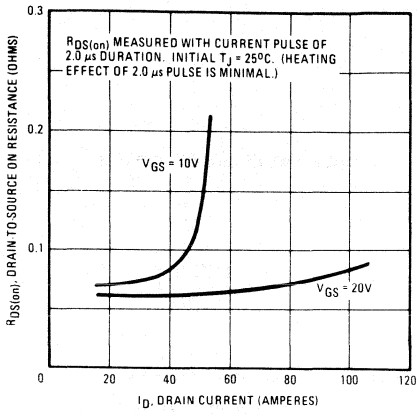


Fig. 12 – Typical On-Resistance Vs. Drain Current

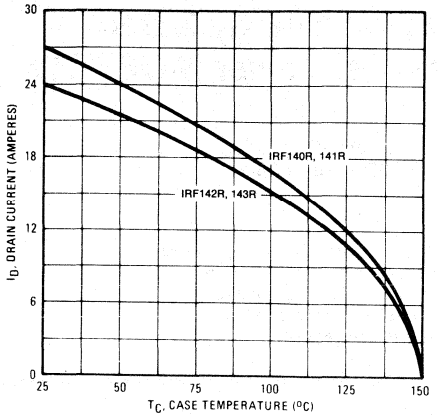


Fig. 13 – Maximum Drain Current Vs. Case Temperature

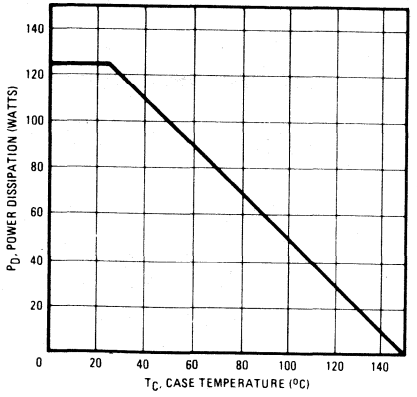


Fig. 14 – Power Vs. Temperature Derating Curve

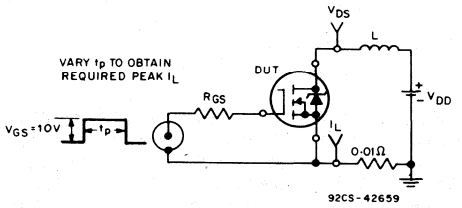


Fig. 15 — Unclamped Energy Test Circuit

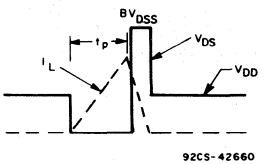


Fig. 16 — Unclamped Energy Waveforms

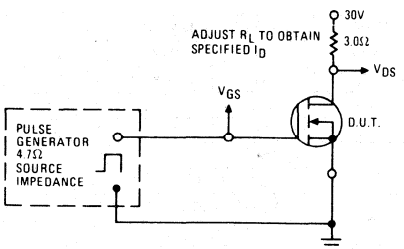


Fig. 17 – Switching Time Test Circuit

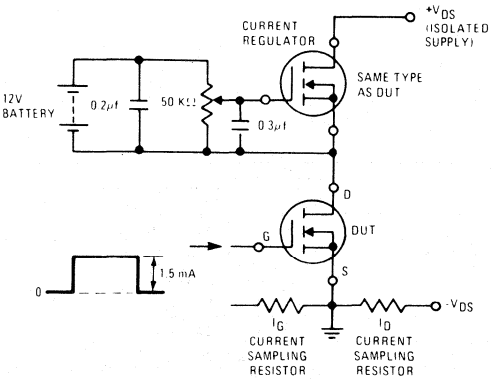


Fig. 18 – Gate Charge Test Circuit

IRF150R, IRF151R, IRF152R, IRF153R

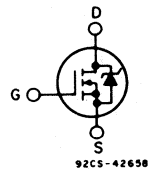
File Number **2002**

Avalanche Energy Rated N-Channel Power MOSFETs

33A and 40A, 60V-100V
$r_{DS}(on) = 0.055\Omega$ and 0.08Ω

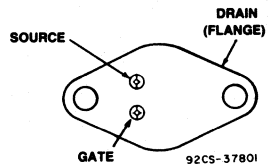
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO - 204 AE

The IRF150R, IRF151R, IRF152R and IRF153R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

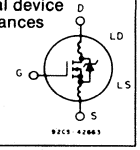
Absolute Maximum Ratings

Parameter		IRF150R	IRF151R	IRF152R	IRF153R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	40	40	33	33	A
I_D @ T_C = 100°C	Continuous Drain Current	25	25	20	20	A
I_{DM}	Pulsed Drain Current ③	160	160	132	132	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	150				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF150R IRF152R	100	—	—	V	V_{GS} = 0V
		IRF151R IRF153R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF150R IRF151R	40	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF152R IRF153R	33	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF150R IRF151R	—	0.045	0.055	Ω	V_{GS} = 10V, I_D = 20A
		IRF152R IRF153R	—	0.06	0.08	Ω	
g_{fs}	Forward Transconductance ②	ALL	9.0	11	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 20A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	1000	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	350	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 24V, I_D = 20A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	125	ns	
t_f	Fall Time	ALL	—	—	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	63	120	nC	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	27	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	36	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

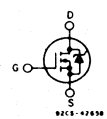


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF150R IRF151R	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF152R IRF153R	—	—	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF150R IRF151R	—	—	160	A	
		IRF152R IRF153R	—	—	132	A	
V_{SD}	Diode Forward Voltage ②	IRF150R IRF151R	—	—	2.5	V	T_C = 25°C, I_S = 40A, V_{GS} = 0V
		IRF152R IRF153R	—	—	2.3	V	T_C = 25°C, I_S = 33A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.3	—	μC	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 10V, starting T_J = 25°C, L = 170μH, R_{gs} = 50Ω, I_{peak} = 40A. See figures 15, 16.

IRF150R, IRF151R, IRF152R, IRF153R

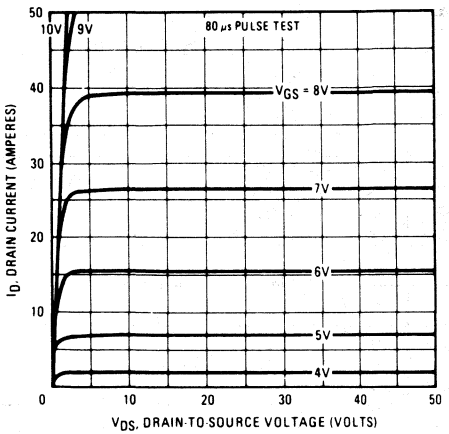


Fig. 1 – Typical Output Characteristics

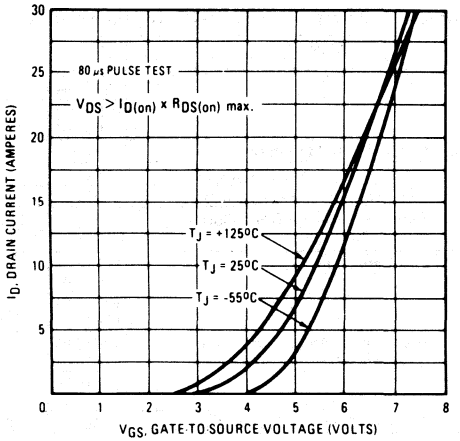


Fig. 2 – Typical Transfer Characteristics

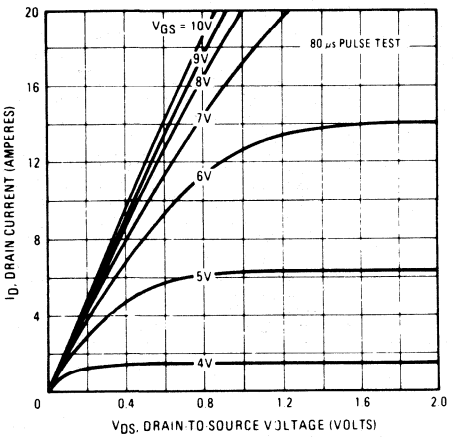


Fig. 3 – Typical Saturation Characteristics

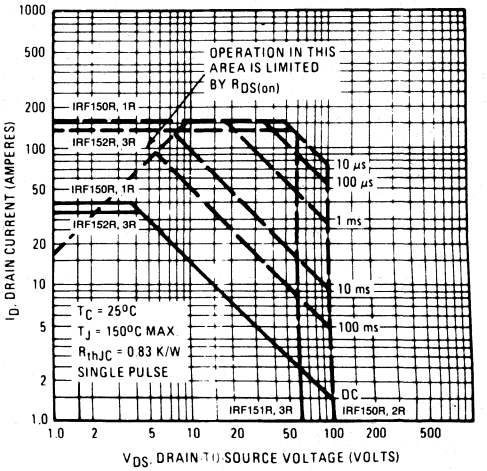


Fig. 4 – Maximum Safe Operating Area

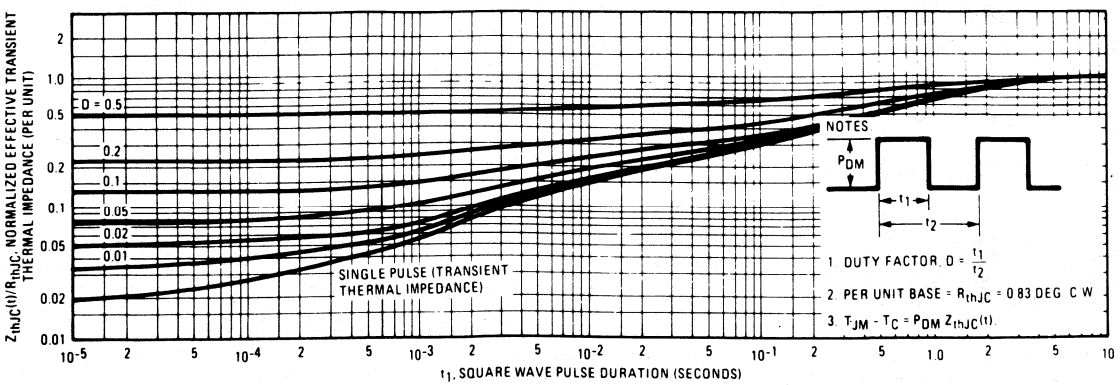


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

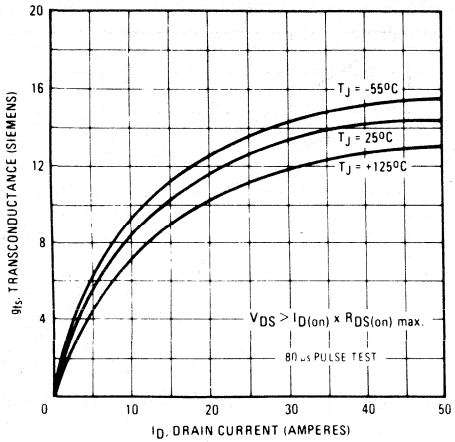


Fig. 6 – Typical Transconductance Vs. Drain Current

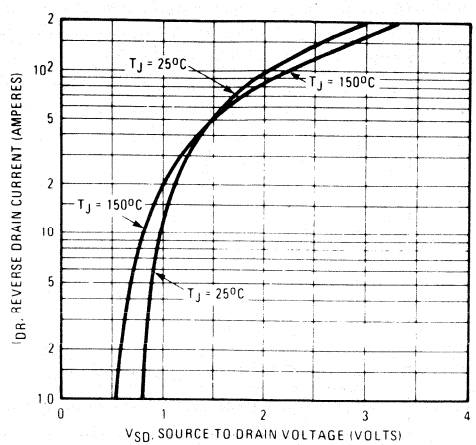


Fig. 7 – Typical Source-Drain Diode Forward Voltage

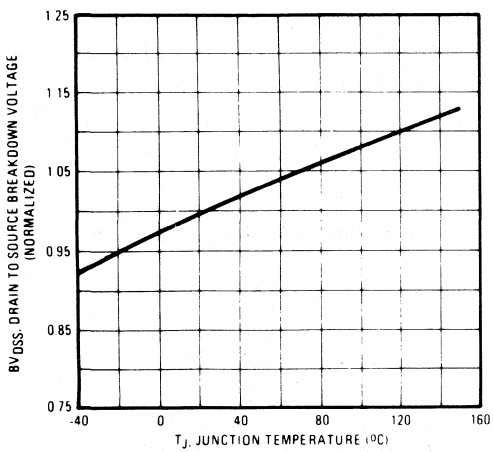


Fig. 8 – Breakdown Voltage Vs. Temperature

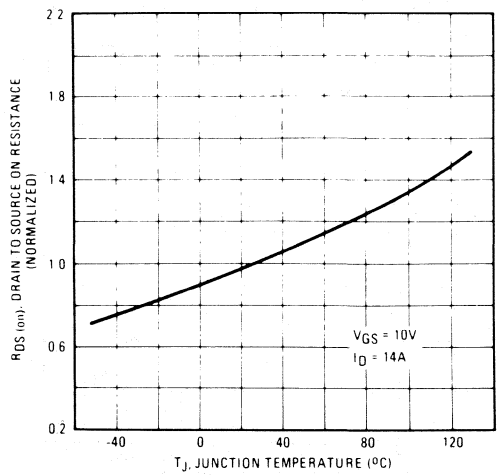


Fig. 9 – Normalized On-Resistance Vs. Temperature

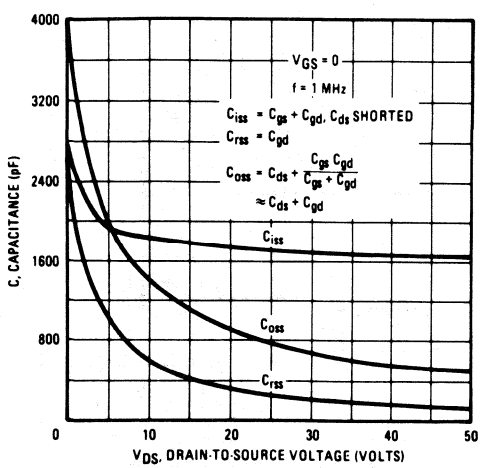


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

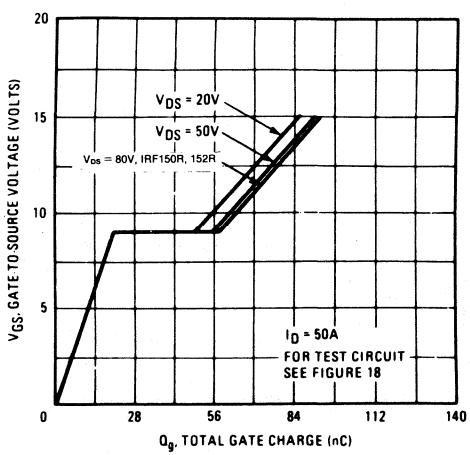


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF150R, IRF151R, IRF152R, IRF153R

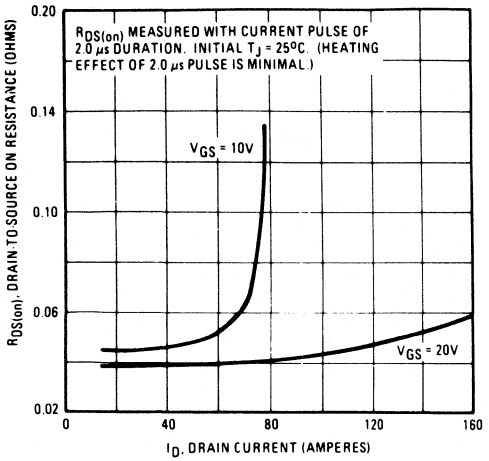


Fig. 12 – Typical On-Resistance Vs. Drain Current

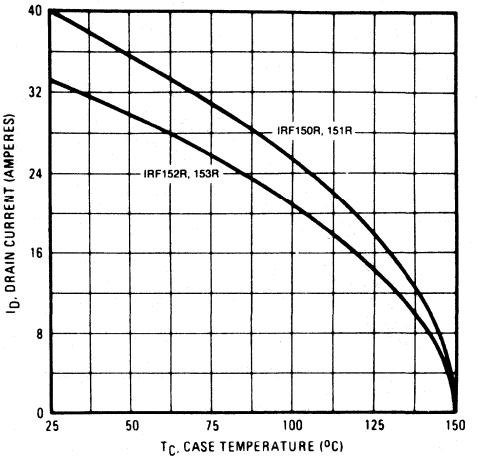


Fig. 13 – Maximum Drain Current Vs. Case Temperature

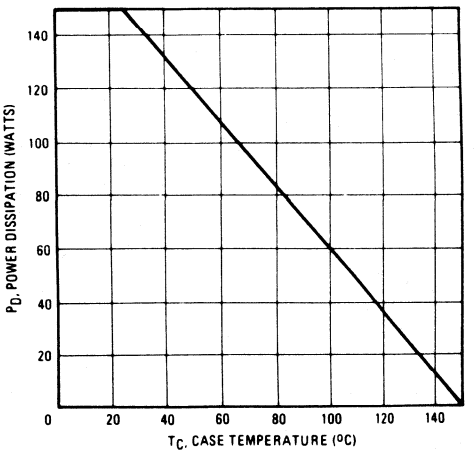


Fig. 14 – Power Vs. Temperature Derating Curve

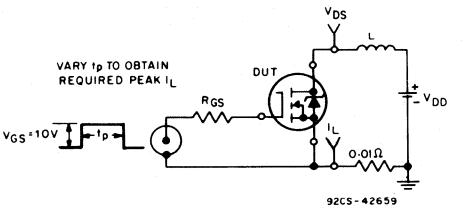


Fig. 15 — Unclamped Energy Test Circuit

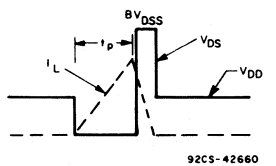


Fig. 16 — Unclamped Energy Waveforms

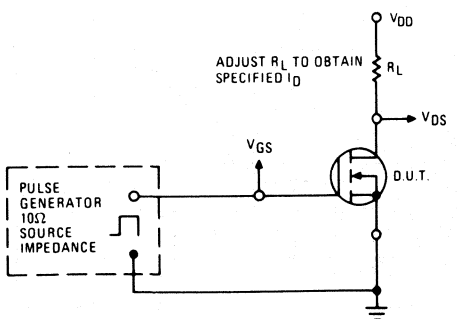


Fig. 17 – Switching Time Test Circuit

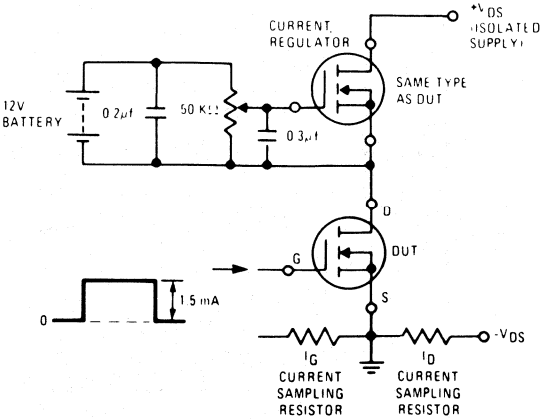


Fig. 18 – Gate Charge Test Circuit

File Number **1999**

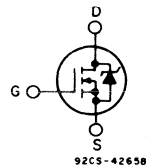
IRF230R, IRF231R, IRF232R, IRF233R

Avalanche Energy Rated N-Channel Power MOSFETs

8.0A and 9.0A, 150V-200V
$r_{DS}(on) = 0.4\Omega$ and 0.6Ω

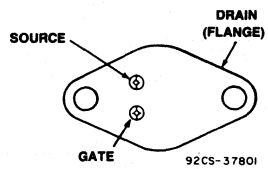
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO - 204AA

The IRF230R, IRF231R, IRF232R and IRF233R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

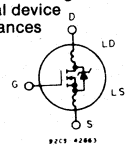
Parameter		IRF230R	IRF231R	IRF232R	IRF233R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	150				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF230R, IRF231R, IRF232R, IRF233R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF230R IRF232R	200	—	—	V	V_{GS} = 0V
		IRF231R IRF233R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF230R IRF231R	9.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF232R IRF233R	8.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF230R IRF231R	—	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF232R IRF233R	—	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 5.0A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	—	250	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 90V, I_D = 5.0A, Z_o = 15Ω
t_r	Rise Time	ALL	—	—	50	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	50	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	—	—	40	ns	independent of operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	10	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

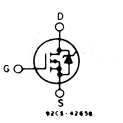


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF230R IRF231R	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF232R IRF233R	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF230R IRF231R	—	—	36	A	
		IRF232R IRF233R	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	IRF230R IRF231R	—	—	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF232R IRF233R	—	—	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 20V, starting T_J = 25°C, L = 3.37mH, R_{gs} = 50Ω, I_{peak} = 9A. See figures 15, 16.

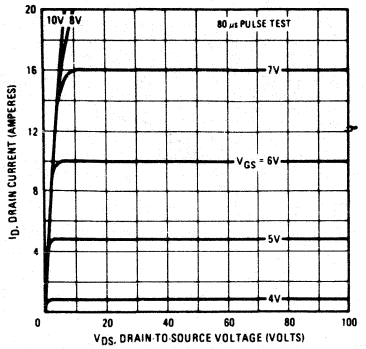


Fig. 1 – Typical Output Characteristics

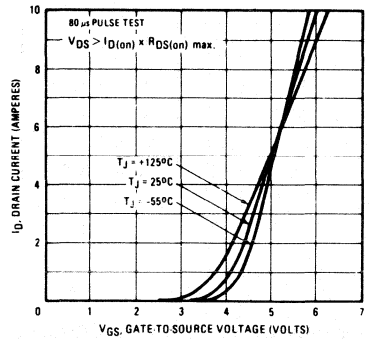


Fig. 2 – Typical Transfer Characteristics

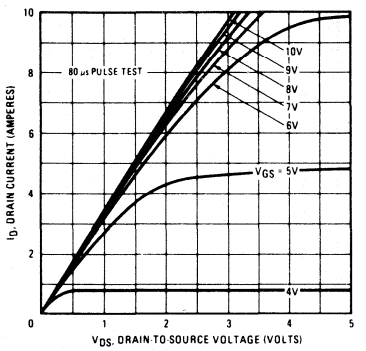


Fig. 3 – Typical Saturation Characteristics

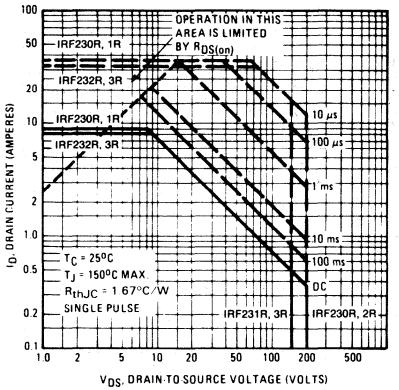


Fig. 4 – Maximum Safe Operating Area

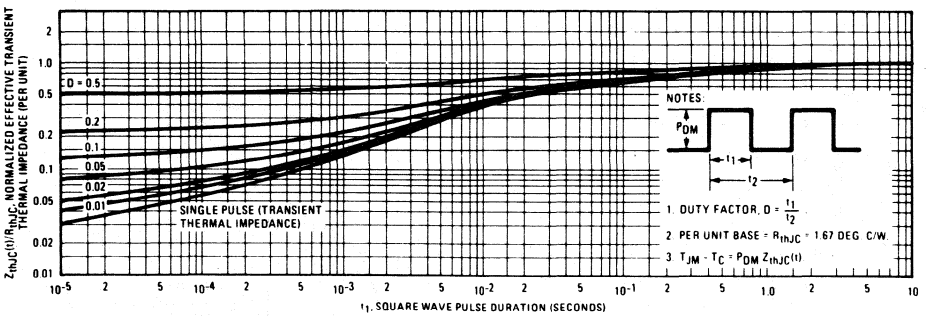


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

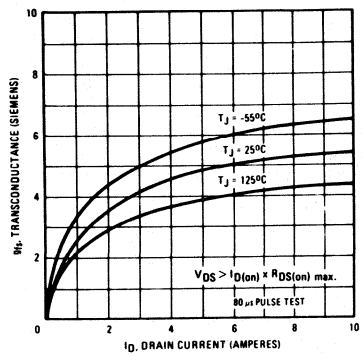


Fig. 6 – Typical Transconductance Vs. Drain Current

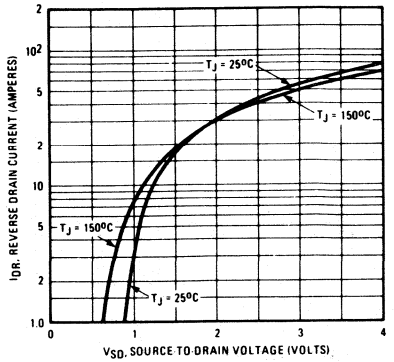


Fig. 7 – Typical Source-Drain Diode Forward Voltage

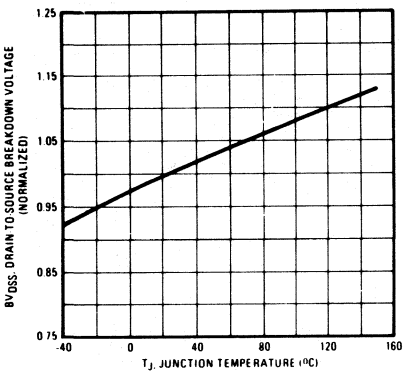


Fig. 8 – Breakdown Voltage Vs. Temperature

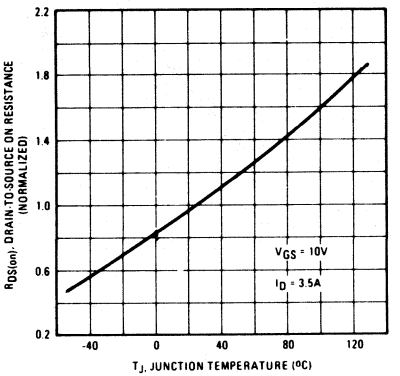


Fig. 9 – Normalized On-Resistance Vs. Temperature

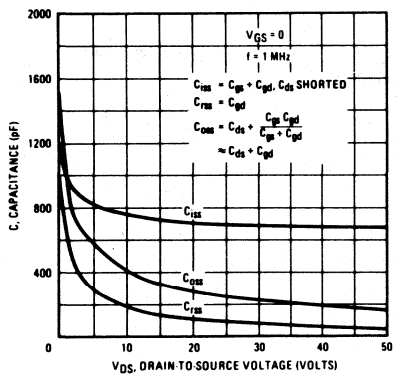


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

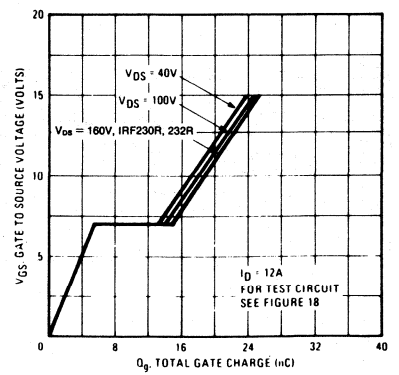


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

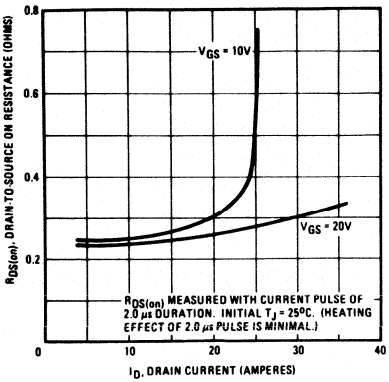


Fig. 12 – Typical On-Resistance Vs. Drain Current

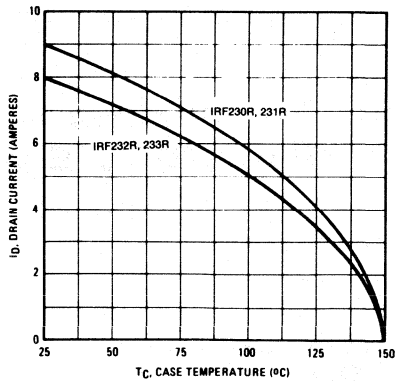


Fig. 13 – Maximum Drain Current Vs. Case Temperature

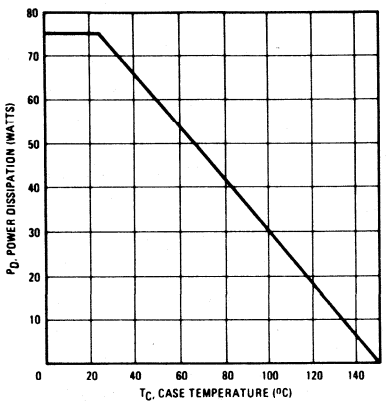


Fig. 14 – Power Vs. Temperature Derating Curve

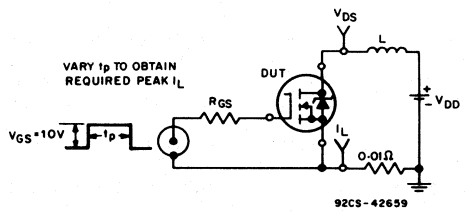


Fig. 15 — Unclamped Energy Test Circuit

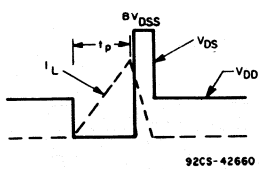


Fig. 16 — Unclamped Energy Waveforms

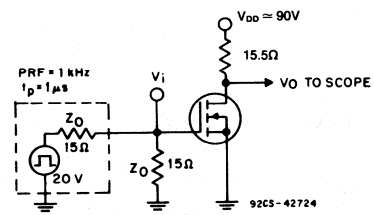


Fig. 17 – Switching Time Test Circuit

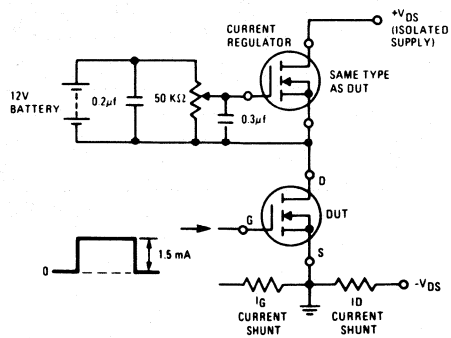


Fig. 18 – Gate Charge Test Circuit

IRF234, IRF235, IRF236, IRF237

File Number **2208**

Avalanche-Energy-Rated N-Channel Power MOSFETs

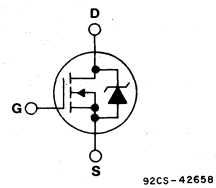
8.1 A and 6.5 A, 275 V and 250 V
$r_{DS}(on)$ = 0.45 Ω and 0.68 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250V rating - 120V ac line system operation*

The IRF234, IRF235, IRF236 and IRF237 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

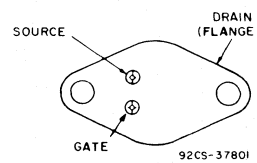
The IRF-types are supplied in the JEDEC TO-204AA steel package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

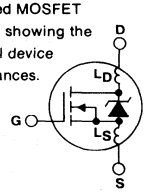
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF234	IRF235	IRF236	IRF237	UNITS
Drain-Source Voltage ①	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	250	250	275	275	V
Continuous Drain Current	I_D @ T_C = 25°C	8.1	6.5	8.1	6.5	A
Continuous Drain Current	I_D @ T_C = 100°C	5.1	4.1	5.1	4.1	A
Pulsed Drain Current ③	I_{DM}	32	26	32	26	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	75				W
Linear Derating Factor		0.6				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	180				mj
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. (1.6 mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS, At T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF236, IRF237	275	—	—	V	V_{GS} = 0 V
		IRF234, IRF235	250	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS}(th)$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_D(on)$	IRF234, IRF236	8.1	—	—	A	V_{DS} > $I_D(on)$ x $r_{DS}(on)$ max., V_{GS} = 10 V
		IRF235, IRF237	6.5	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS}(on)$	IRF234, IRF236	—	0.32	0.45	Ω	V_{GS} = 10 V, I_D = 4.1 A
		IRF235, IRF237	—	0.48	0.68	Ω	
Forward Transconductance ②	g_{fs}	ALL	2.9	4.3	—	S (℧)	V_{DS} > $I_D(on)$ x $r_{DS}(on)$ max., I_D = 4.1 A
Input Capacitance	C_{iss}	ALL	—	600	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	180	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	52	—	pF	
Turn-On Delay Time	$t_d(on)$	ALL	—	9.1	14	ns	V_{DD} = 90 V, I_D = 5 A, Z_O = 15 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	23	35	ns	
Turn-Off Delay Time	$t_d(off)$	ALL	—	31	47	ns	
Fall Time	t_f	ALL	—	19	29	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	24	35	nC	V_{GS} = 10 V, I_D = 12 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	5.1	7.7	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	12	18	nC	
Internal Drain Inductance	L_D	ALL	—	4.5	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

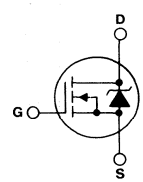


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1.67	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Free air operation.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF234, IRF236	—	—	8.1	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF235, IRF237	—	—	6.5	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF234, IRF236	—	—	32	A	
		IRF235, IRF237	—	—	26	A	
Diode Forward Voltage ②	V_{SD}	ALL	—	—	2.0	V	T_C = 25°C, I_S = 8.1 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	92	180	390	ns	T_J = 150°C, I_F = 8.1 A, di_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	0.63	1.3	2.7	μC	T_J = 150°C, I_F = 8.1 A, di_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs. Duty Cycle ≤ 2%

③ Repetitive Rating: Pulse width limited by max. junction temperature See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50 V, Starting T_J = 25°C, L = 4.5 mH, R_G = 25 Ω, Peak I_L = 8.1 A (See Figs. 14 & 15).

IRF234, IRF235, IRF236, IRF237

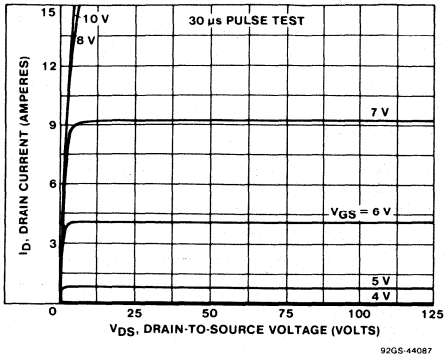


Fig. 1 - Typical output characteristics.

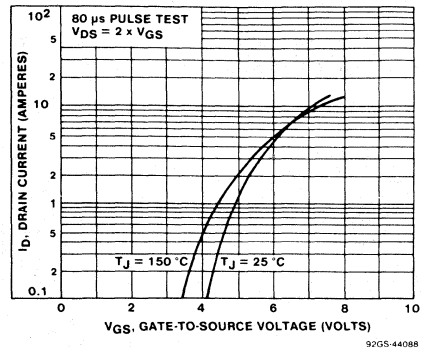


Fig. 2 - Typical transfer characteristics.

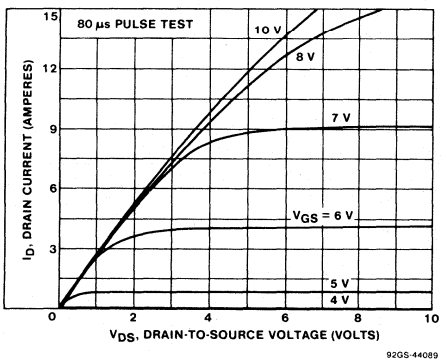


Fig. 3 - Typical saturation characteristics.

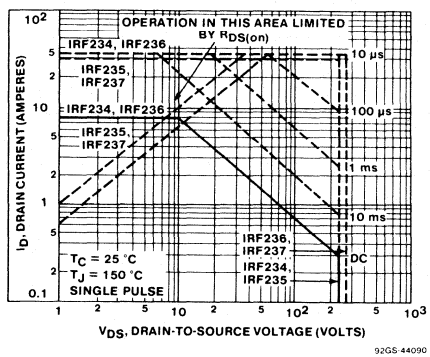


Fig. 4 - Maximum safe operating area.

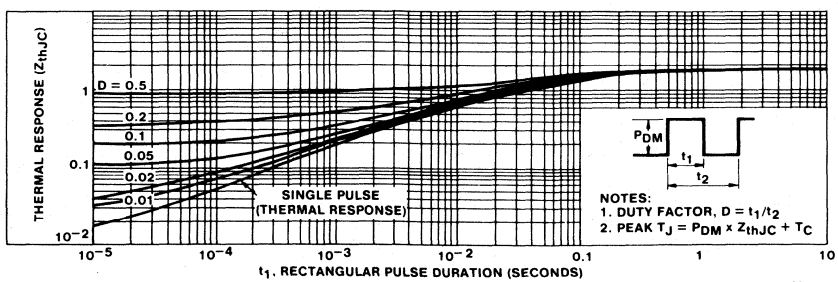


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

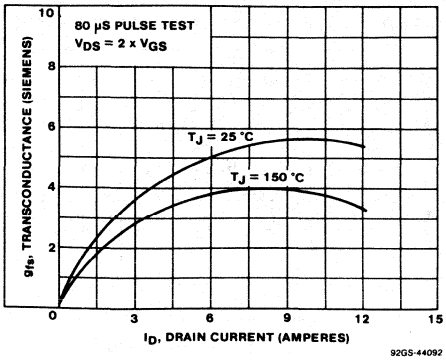


Fig. 6 - Typical transconductance vs. drain current.

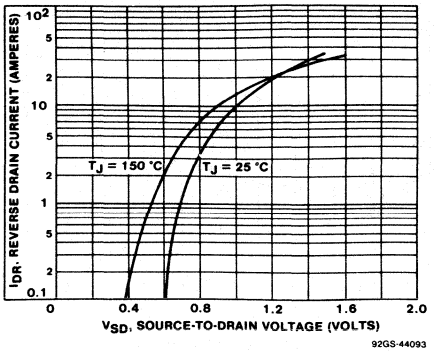


Fig. 7 - Typical source-drain diode forward voltage.

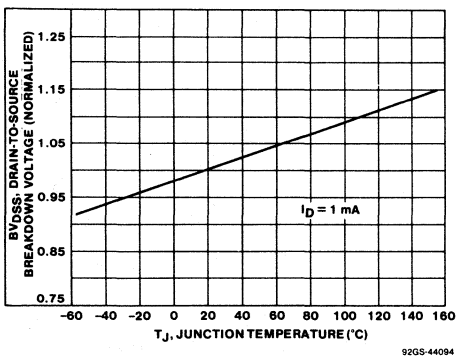


Fig. 8 - Breakdown voltage vs. temperature.

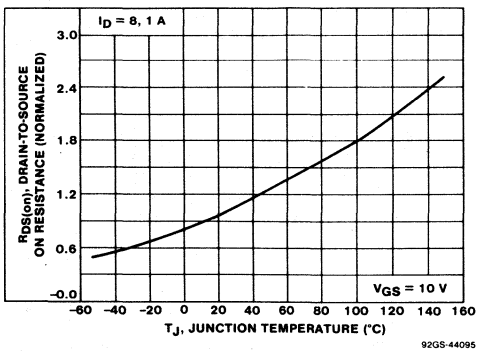


Fig. 9 - Normalized on-resistance vs. temperature.

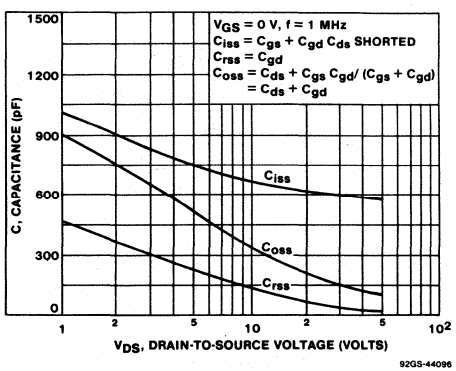


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

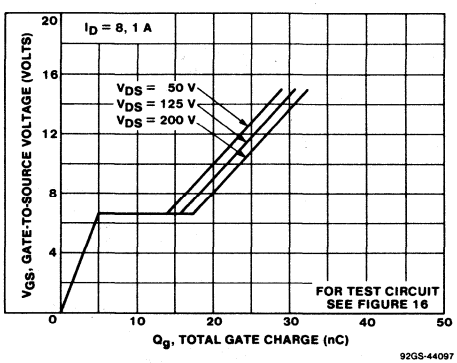


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

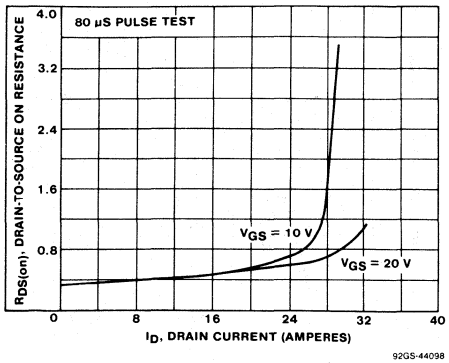


Fig. 12 - Typical on-resistance vs. drain current.

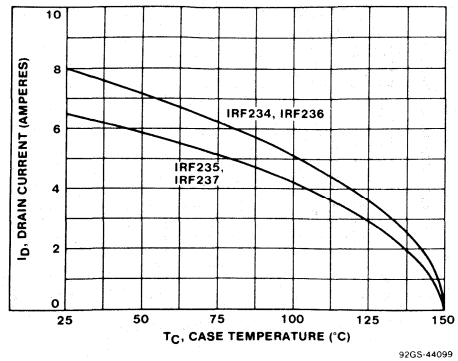


Fig. 13 - Maximum drain current vs. case temperature.

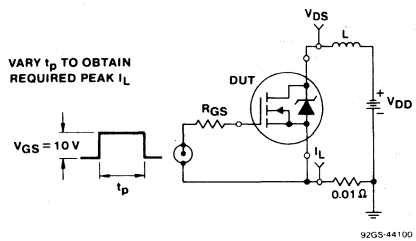


Fig. 14 - Unclamped energy test circuit.

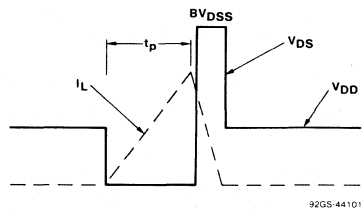


Fig. 15 - Unclamped energy waveforms.

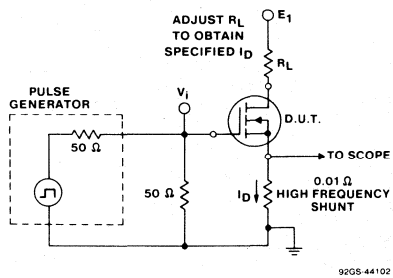


Fig. 16 - Switching time test circuit.

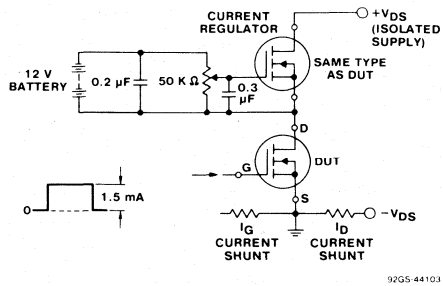


Fig. 17 - Gate charge test circuit.

File Number **2003**

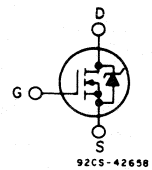
IRF240R, IRF241R
IRF242R, IRF243R

Avalanche Energy Rated N-Channel Power MOSFETs

16A and 18A, 200V, 150V
$r_{DS}(on) = 0.18\Omega$ and 0.22Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

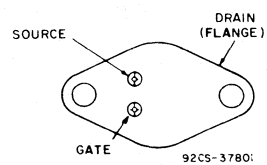


N-CHANNEL ENHANCEMENT MODE

The IRF240R, IRF241R, IRF242R and IRF243R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATION



JEDEC TO-204AE

Absolute Maximum Ratings

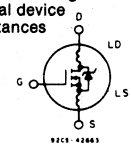
Parameter		IRF240R	IRF241R	IRF242R	IRF243R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	18	18	16	16	A
I_D @ $T_C = 100°C$	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	580				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF240R, IRF241R
IRF242R, IRF243R

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF240R IRF242R	200	—	—	V	$V_{GS} = 0V$
		IRF241R IRF243R	150	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRF240R IRF241R	18	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRF242R IRF243R	16	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF240R IRF241R	—	0.14	0.18	Ω	$V_{GS} = 10V$, $I_D = 10A$
		IRF242R IRF243R	—	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	9.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 10A$
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	500	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} \simeq 75V$, $I_D = 10A$, $Z_0 = 4.7\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	40	80	ns	
t_f	Fall Time	ALL	—	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC	$V_{GS} = 10V$, $I_D = 22A$, $V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	16	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	27	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

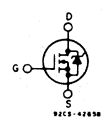


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF240R IRF241R	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF242R IRF243R	—	—	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF240R IRF241R	—	—	72	A	
		IRF242R IRF243R	—	—	64	A	
V_{SD}	Diode Forward Voltage ②	IRF240R IRF241R	—	—	2.0	V	$T_C = 25°C$, $I_S = 18A$, $V_{GS} = 0V$
		IRF242R IRF243R	—	—	1.9	V	$T_C = 25°C$, $I_S = 16A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	$T_J = 150°C$, $I_F = 18A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.1	—	μC	$T_J = 150°C$, $I_F = 18A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 50V$, starting $T_J = 25°C$, L = 2.7 mH, $R_{gs} = 50\Omega$, $I_{peak} = 18A$. See figures 15, 16.

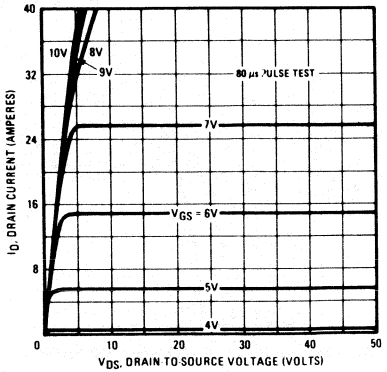


Fig. 1 – Typical Output Characteristics

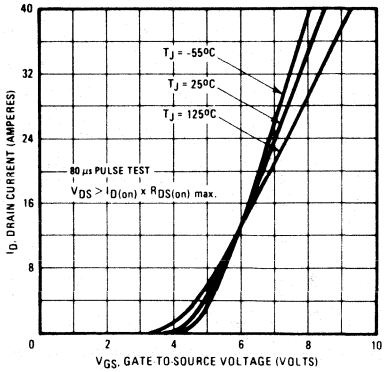


Fig. 2 – Typical Transfer Characteristics

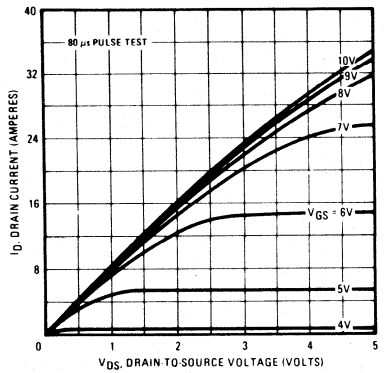


Fig. 3 – Typical Saturation Characteristics

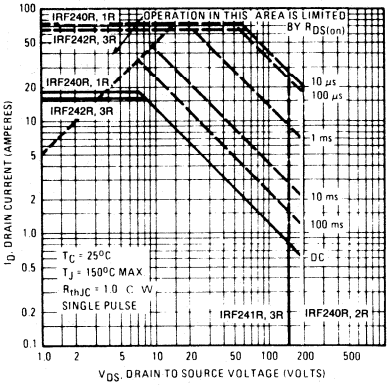


Fig. 4 – Maximum Safe Operating Area

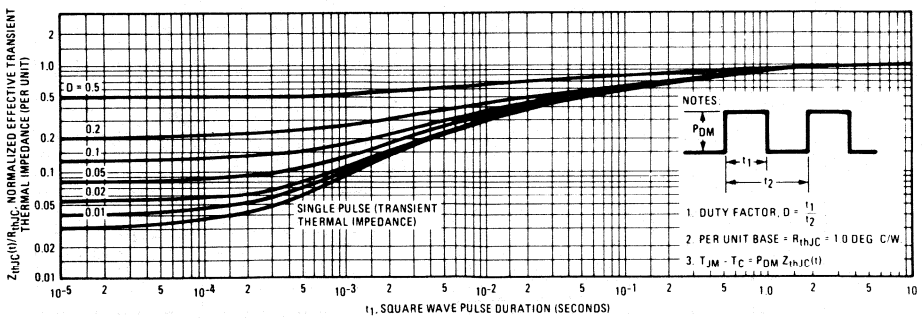


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

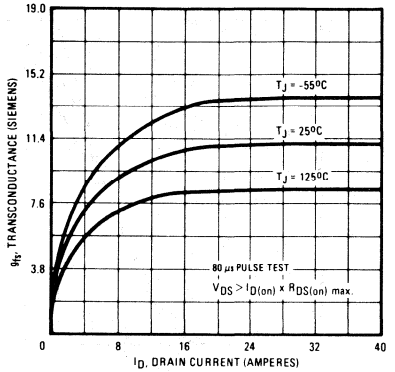


Fig. 6 – Typical Transconductance Vs. Drain Current

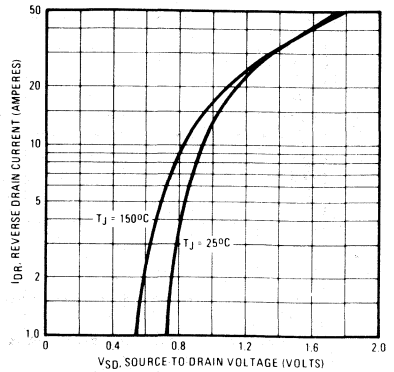


Fig. 7 – Typical Source-Drain Diode Forward Voltage

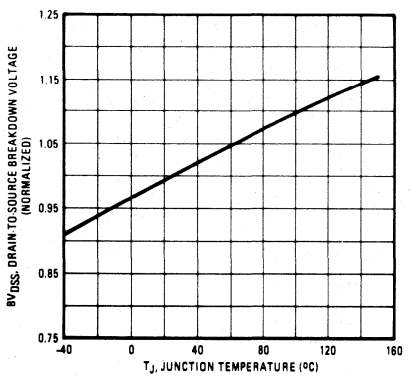


Fig. 8 – Breakdown Voltage Vs. Temperature

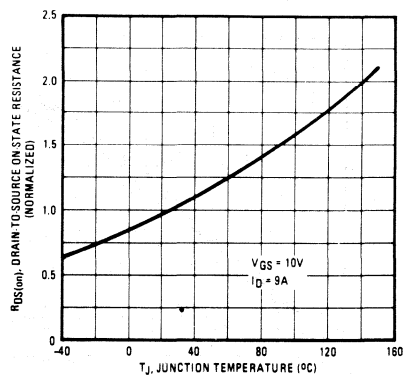


Fig. 9 – Normalized On-Resistance Vs. Temperature

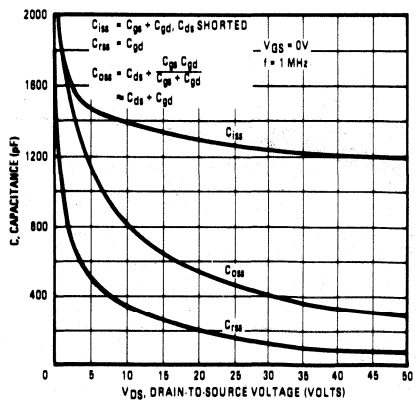


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

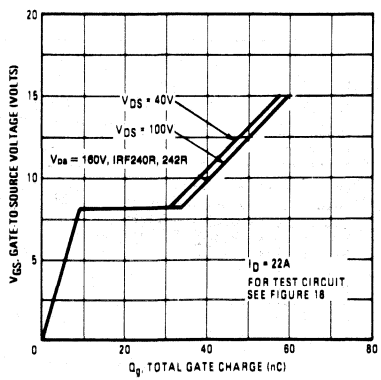


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

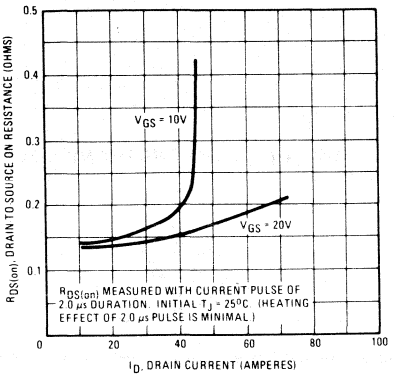


Fig. 12 – Typical On-Resistance Vs. Drain Current

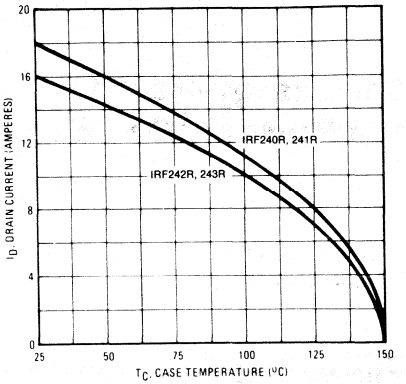


Fig. 13 – Maximum Drain Current Vs. Case Temperature

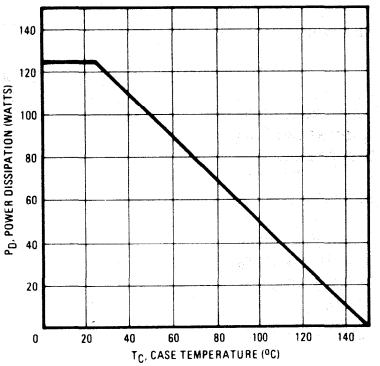


Fig. 14 – Power Vs. Temperature Derating Curve

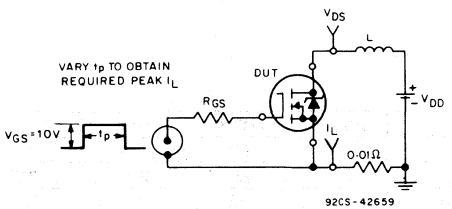


Fig. 15 — Unclamped Energy Test Circuit

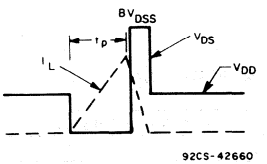


Fig. 16 — Unclamped Energy Waveforms

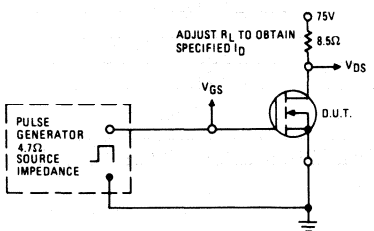


Fig. 17 – Switching Time Test Circuit

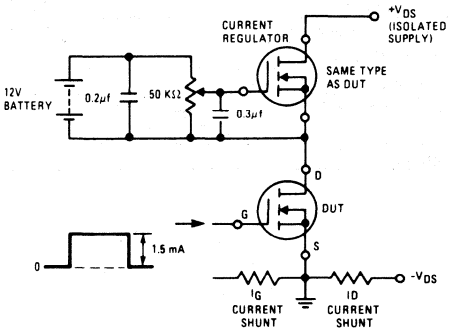


Fig. 18 – Gate Charge Test Circuit

IRF244, IRF245, IRF246, IRF247

File Number **2209**

Avalanche-Energy-Rated N-Channel Power MOSFETs

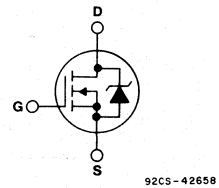
14 A and 13 A, 275 V and 250 V
$r_{DS}(on)$ = 0.28 Ω and 0.34 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250V dc rated - 120V ac line system operation*

The IRF244, IRF245, IRF246 and IRF247 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

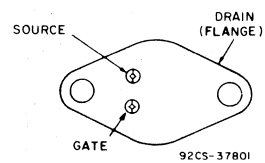
The IRF-types are supplied in the JEDEC TO-204AA steel package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

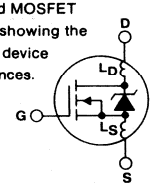
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF244	IRF245	IRF246	IRF247	UNITS
Drain-Source Voltage ①	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	250	250	275	275	V
Continuous Drain Current	I_D @ T_C = 25°C	14	13	14	13	A
Continuous Drain Current	I_D @ T_C = 100°C	8.8	8.0	8.8	8.0	A
Pulsed Drain Current ③	I_{DM}	56	52	56	52	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	125				W
Linear Derating Factor		1.0				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	550				mj
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. (1.6 mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS, At T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF246 IRF247	275	—	—	V	V_{GS} = 0 V
		IRF244 IRF245	250	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS}(th)$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_D(on)$	IRF244 IRF246	14	—	—	A	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., V_{GS} = 10 V
		IRF245 IRF247	13	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS}(on)$	IRF244 IRF246	—	0.20	0.28	Ω	V_{GS} = 10 V, I_D = 10 A
		IRF245 IRF247	—	0.24	0.34	Ω	
Forward Transconductance ②	g_{fs}	ALL	6.7	10	—	S (℧)	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., I_D = 10 A
Input Capacitance	C_{iss}	ALL	—	1300	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	320	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	69	—	pF	
Turn-On Delay Time	$t_d(on)$	ALL	—	16	24	ns	V_{DD} = 90 V, I_D = 10 A, Z_O = 4.7 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	67	100	ns	
Turn-Off Delay Time	$t_d(off)$	ALL	—	53	80	ns	
Fall Time	t_f	ALL	—	49	74	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	39	59	nC	V_{GS} = 10 V, I_D = 22 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	6.6	9.9	nC	
Gate-Drain (("Miller") Charge	Q_{gd}	ALL	—	20	30	nC	
Internal Drain Inductance	L_D	ALL	—	4.5	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

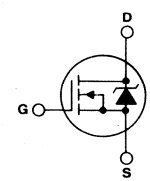


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1.0	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Free air operation.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF244 IRF246	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF245 IRF247	—	—	13	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF244 IRF246	—	—	56	A	
		IRF245 IRF247	—	—	52	A	
Diode Forward Voltage ②	V_{SD}	ALL	—	—	1.8	V	T_C = 25°C, I_S = 14 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	150	300	640	ns	T_J = 150°C, I_F = 14 A, di_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	1.6	3.4	7.2	μC	T_J = 150°C, I_F = 14 A, di_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs. Duty Cycle ≤ 2%

③ Repetitive Rating: Pulse width limited by max. junction temperature See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50 V, Starting T_J = 25°C, L = 4.5 mH, R_G = 25 Ω, Peak I_L = 14 A (See Figs. 14 & 15).

IRF244, IRF245, IRF246, IRF247

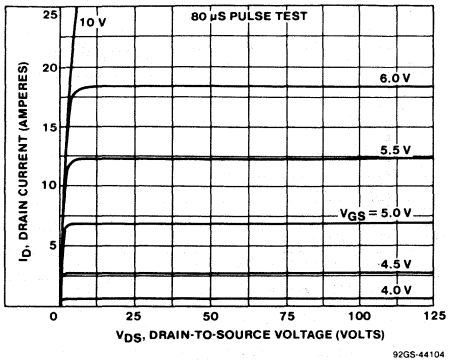


Fig. 1 - Typical output characteristics.

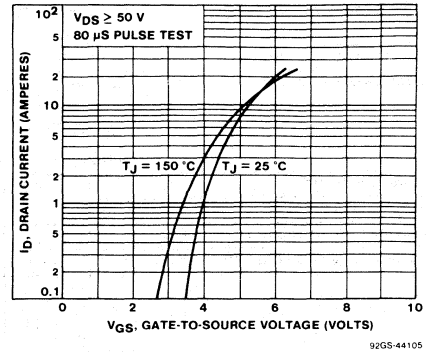


Fig. 2 - Typical transfer characteristics.

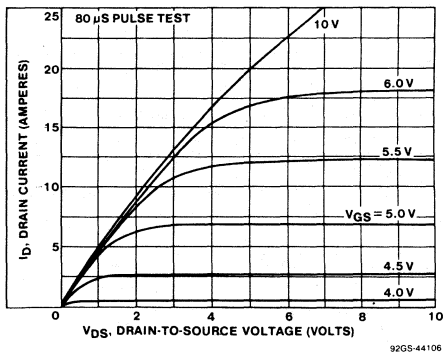


Fig. 3 - Typical saturation characteristics.

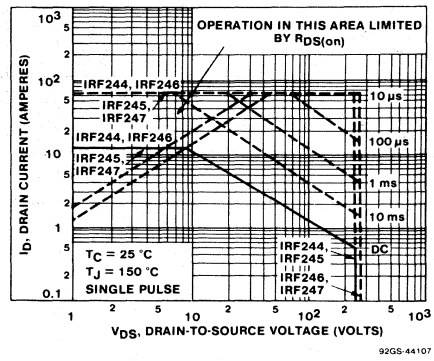


Fig. 4 - Maximum safe operating area.

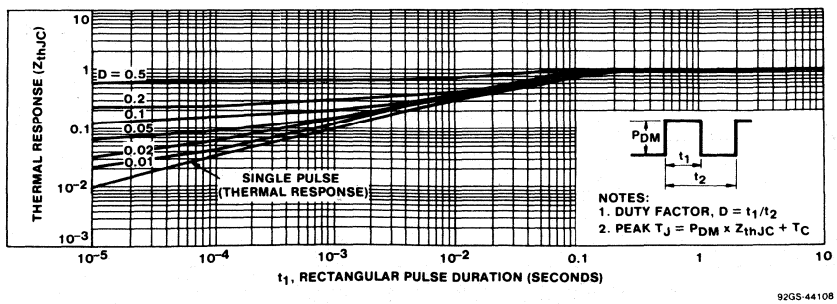


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

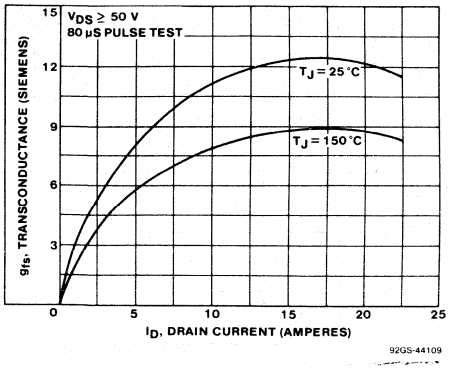


Fig. 6 - Typical transconductance vs. drain current.

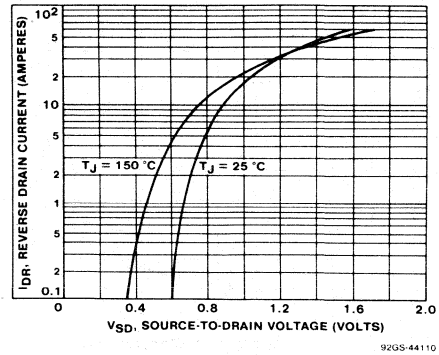


Fig. 7 - Typical source-drain diode forward voltage.

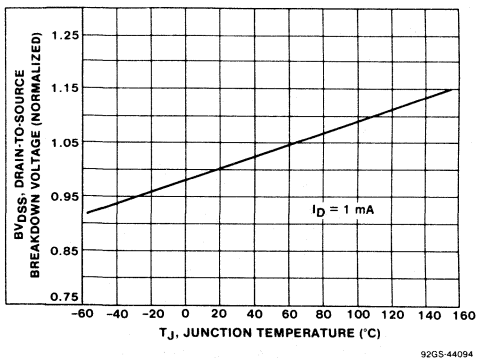


Fig. 8 - Breakdown voltage vs. temperature.

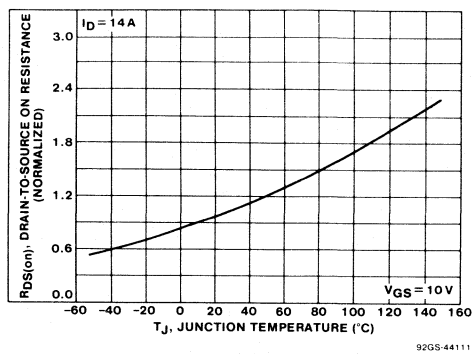


Fig. 9 - Normalized on-resistance vs. temperature.

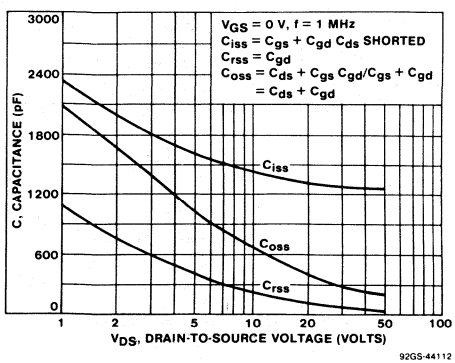


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

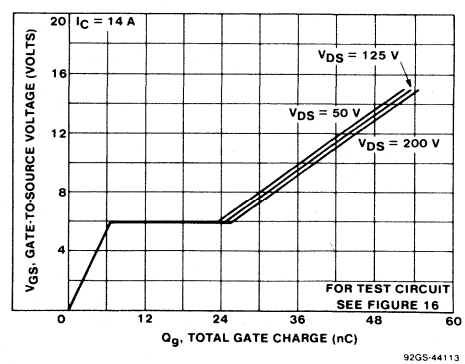


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

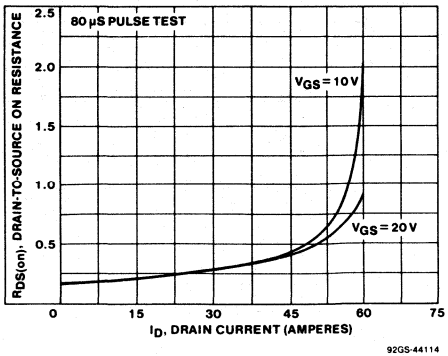


Fig. 12 - Typical on-resistance vs. drain current.

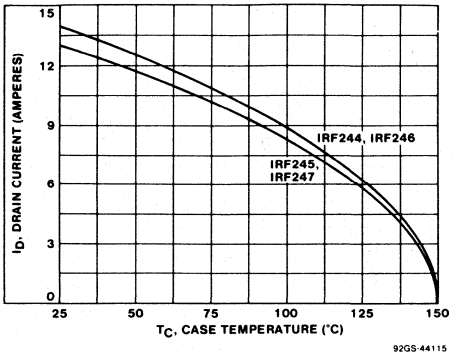


Fig. 13 - Maximum drain current vs. case temperature.

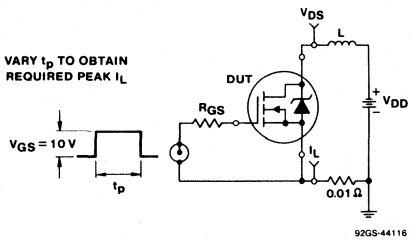


Fig. 14 - Unclamped energy test circuit.

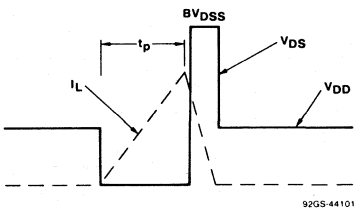


Fig. 15 - Unclamped energy waveforms.

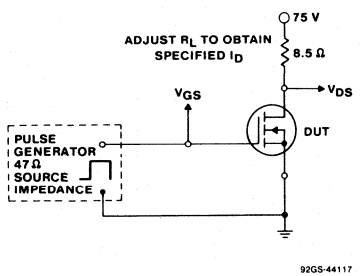


Fig. 16 - Switching time test circuit.

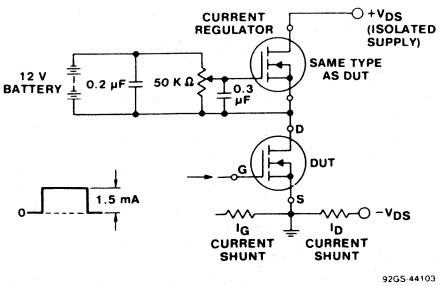


Fig. 17 - Gate charge test circuit.

File Number **2004**

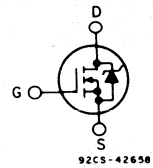
IRF250R, IRF251R, IRF252R, IRF253R

Avalanche Energy Rated N-Channel Power MOSFETs

25A and 30A, 150V-200V
$r_{DS}(on) = 0.085\Omega$ and 0.120Ω

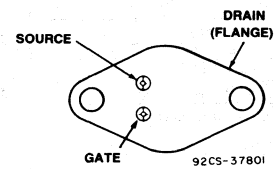
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO - 204AE

The IRF250R, IRF251R, IRF252R and IRF253R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

Absolute Maximum Ratings

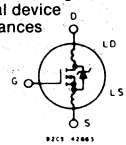
Parameter		IRF250R	IRF251R	IRF252R	IRF253R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	30	30	25	25	A
I_D @ $T_C = 100°C$	Continuous Drain Current	19	19	16	16	A
I_{DM}	Pulsed Drain Current ③	120	120	100	100	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	910				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF250R, IRF251R, IRF252R, IRF253R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF250R IRF252R	200	—	—	V	V_{GS} = 0V
		IRF251R IRF253R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF250R IRF251R	30	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF252R IRF253R	25	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF250R IRF251R	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 16A
		IRF252R IRF253R	—	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 16A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	800	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	300	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 95V, I_D = 16A, Z_0 = 4.7Ω
t_r	Rise Time	ALL	—	—	100	ns	See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	125	ns	
t_f	Fall Time	ALL	—	—	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	37	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	42	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF250R IRF251R	—	—	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF252R IRF253R	—	—	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF250R IRF251R	—	—	120	A	
		IRF252R IRF253R	—	—	100	A	
V_{SD}	Diode Forward Voltage ②	IRF250R IRF251R	—	—	2.0	V	T_C = 25°C, I_S = 30A, V_{GS} = 0V
		IRF252R IRF253R	—	—	1.8	V	T_C = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	750	—	ns	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.7	—	μC	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 1.5 mH, R_{gs} = 50Ω, I_{peak} = 30A. See figures 15, 16.

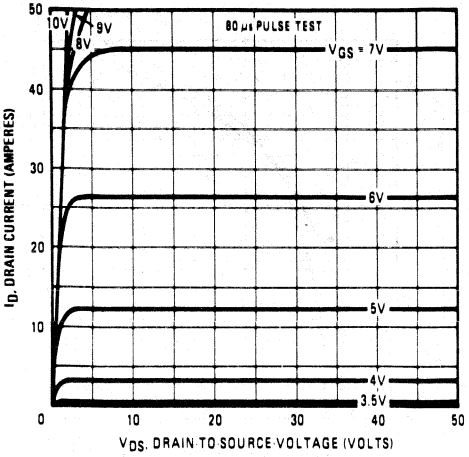


Fig. 1 – Typical Output Characteristics

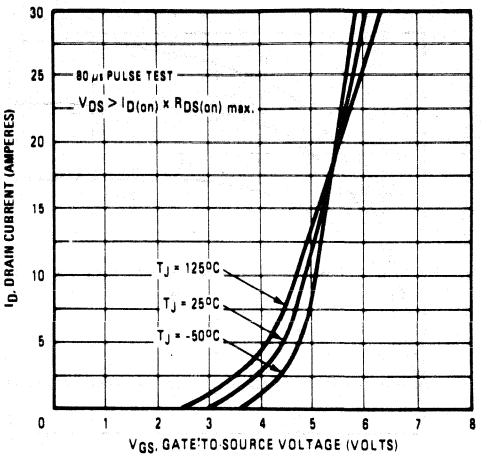


Fig. 2 – Typical Transfer Characteristics

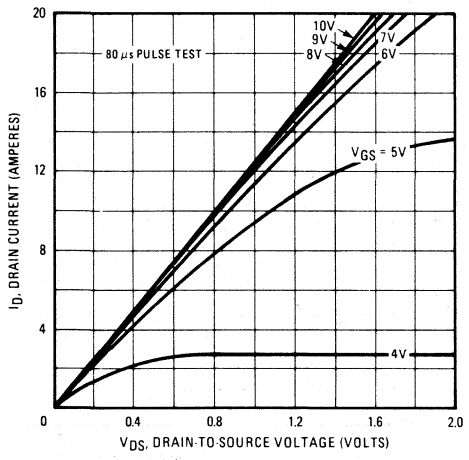


Fig. 3 – Typical Saturation Characteristics

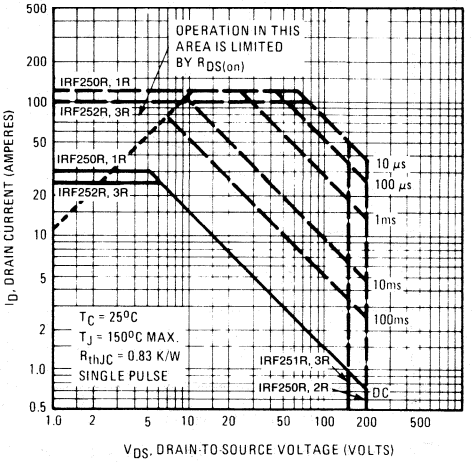


Fig. 4 – Maximum Safe Operating Area

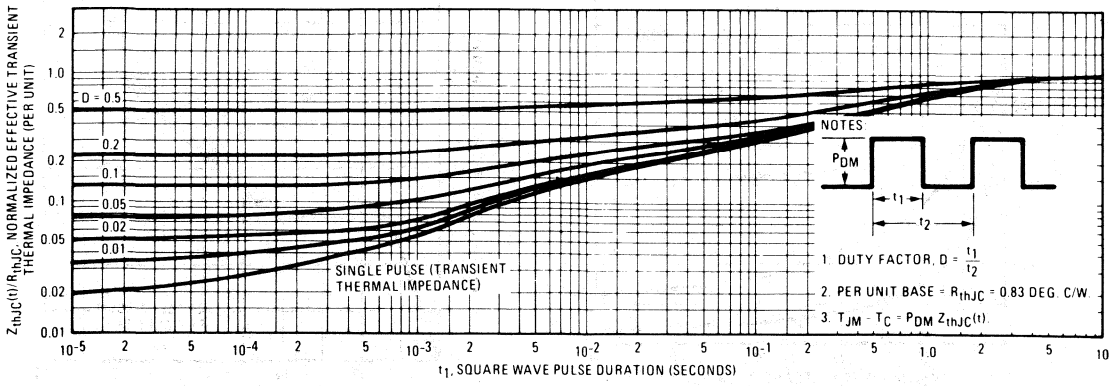


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF250R, IRF251R, IRF252R, IRF253R

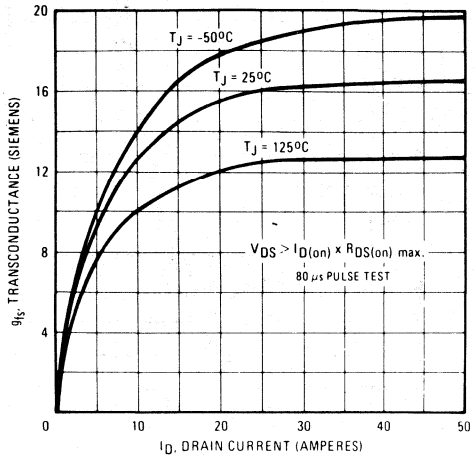


Fig. 6 — Typical Transconductance Vs. Drain Current

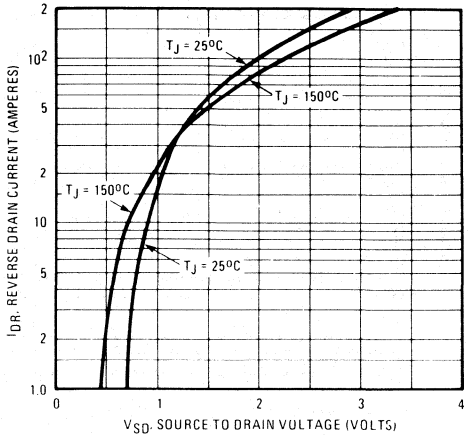


Fig. 7 — Typical Source-Drain Diode Forward Voltage

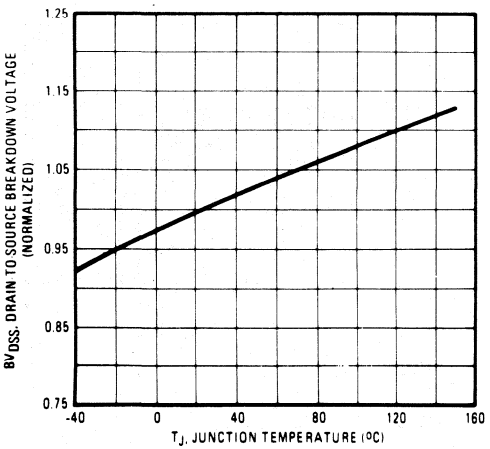


Fig. 8 — Breakdown Voltage Vs. Temperature

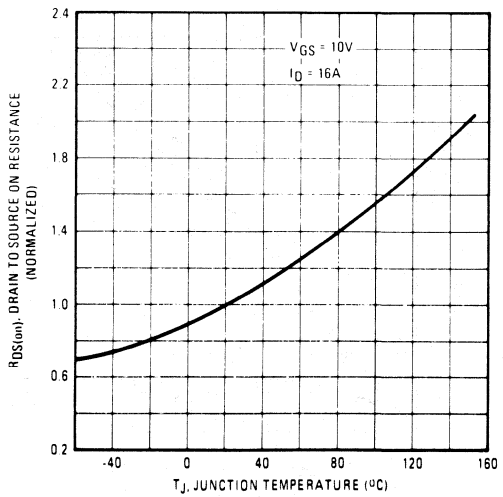


Fig. 9 — Normalized On-Resistance Vs. Temperature

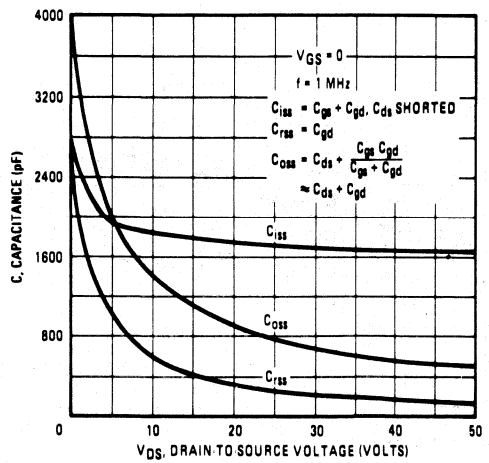


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

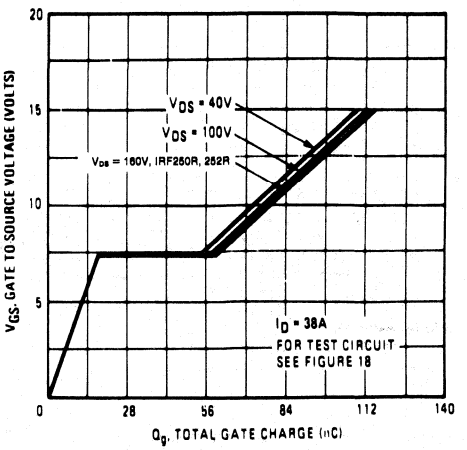


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

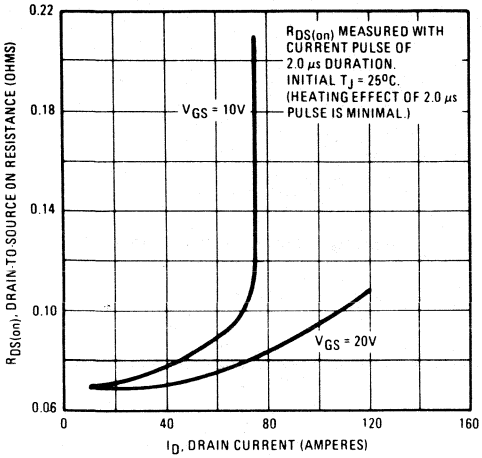


Fig. 12 – Typical On-Resistance Vs. Drain Current

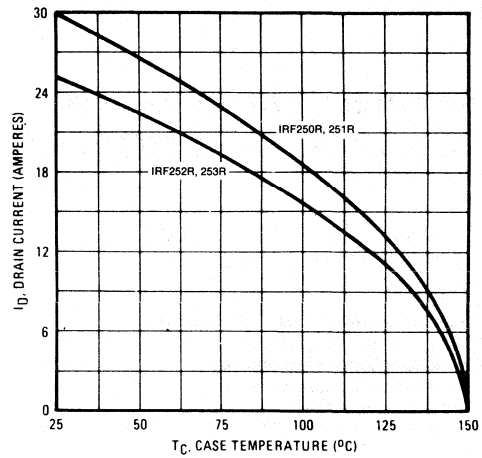


Fig. 13 – Maximum Drain Current Vs. Case Temperature

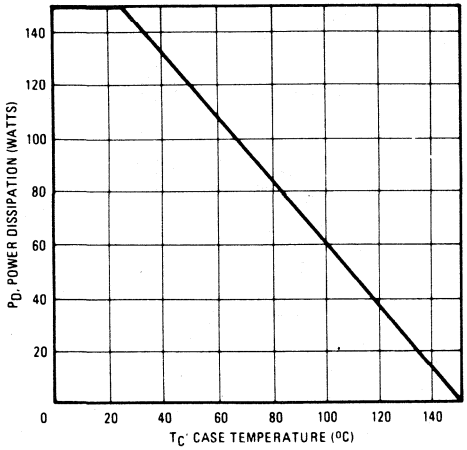


Fig. 14 – Power Vs. Temperature Derating Curve

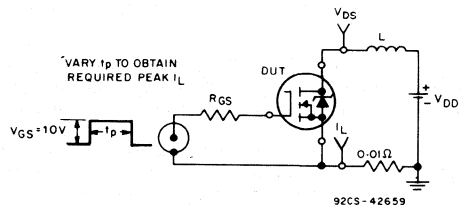


Fig. 15 — Unclamped Energy Test Circuit

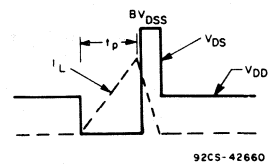


Fig. 16 — Unclamped Energy Waveforms

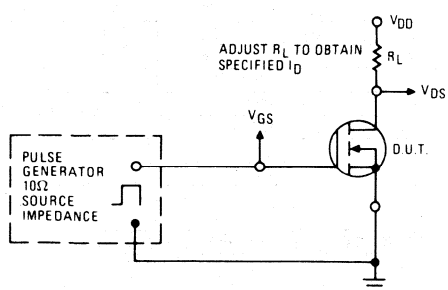


Fig. 17 – Switching Time Test Circuit

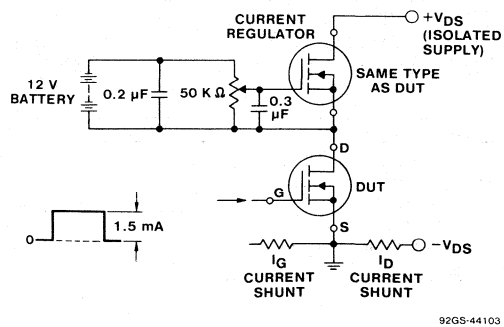


Fig. 18 – Gate Charge Test Circuit

IRF254, IRF255
IRF256, IRF257

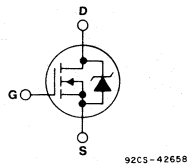
File Number **2300**

Avalanche-Energy-Rated N-Channel Power MOSFETs

22 A and 20 A, 275 V and 250 V
$r_{DS(on)}$ = 0.14 Ω and 0.17 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250 V dc rated - 120 V ac line system operation*

N-CHANNEL ENHANCEMENT MODE

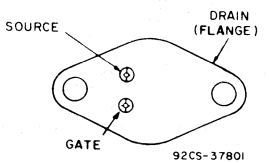


TERMINAL DIAGRAM

The IRF254, IRF255, IRF256 and IRF257 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATION



JEDEC TO-204AE

ABSOLUTE-MAXIMUM RATINGS

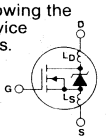
CHARACTERISTIC		IRF254	IRF255	IRF256	IRF257	UNITS
Drain-Source Voltage ①	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	250	250	275	275	V
Continuous Drain Current	I_D @ T_C = 25°C	22	20	22	20	A
Continuous Drain Current	I_D @ T_C = 100°C	14	12	14	12	A
Pulsed Drain Current ③	I_{DM}	88	80	88	80	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	150				W
Linear Derating Factor		1.2				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	1000				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

IRF254, IRF255, IRF256, IRF257

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF256, IRF257	275	—	—	V	V_{GS} = 0 V
		IRF254, IRF255	250	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRF254, IRF256	22	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = 10 V
		IRF255, IRF257	20	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRF254, IRF256	—	0.11	0.14	Ω	V_{GS} = 10 V, I_D = 12 A
		IRF255, IRF257	—	0.14	0.17	Ω	
Forward Transconductance ②	g_{fs}	ALL	11	17	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = 12 A
Input Capacitance	C_{iss}	ALL	—	2700	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	580	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	130	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	19	29	ns	V_{DD} = 125 V, I_D = 22 A, Z_O = 6.2 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	84	130	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	75	110	ns	
Fall Time	t_f	ALL	—	65	98	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	87	130	nC	V_{GS} = 10 V, I_D = 22 A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	14	20	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	73	110	nC	
Internal Drain Inductance	L_D	ALL	—	5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

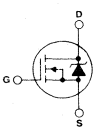


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	0.83	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.12	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	30	°C/W	Free air operation.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF254, IRF256	—	—	22	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF255, IRF257	—	—	22	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF254, IRF256	—	—	88	A	
		IRF255, IRF257	—	—	88	A	
Diode Forward Voltage ②	V_{SD}	ALL	—	—	1.8	V	T_C = 25°C, I_S = 22 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	150	310	650	ns	T_J = 150°C, I_F = 22 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	1.9	4	8.4	μC	T_J = 150°C, I_F = 22 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_J = 25°C, L = 3.3 mH, R_G = 25 Ω, Peak I_L = 22 A (See Figs. 14 & 15).

IRF254, IRF255, IRF256, IRF257

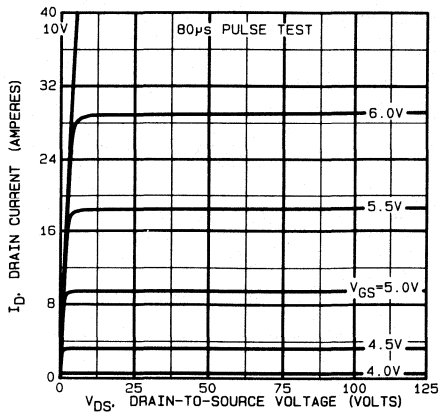


Fig. 1 - Typical output characteristics.

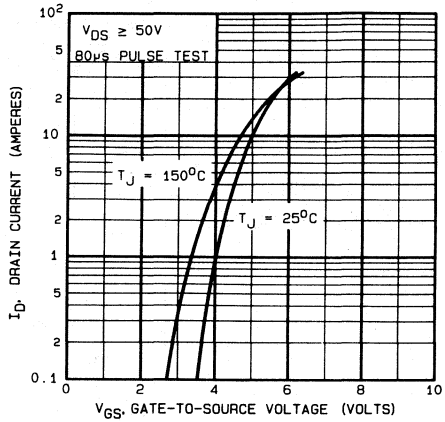


Fig. 2 - Typical transfer characteristics.

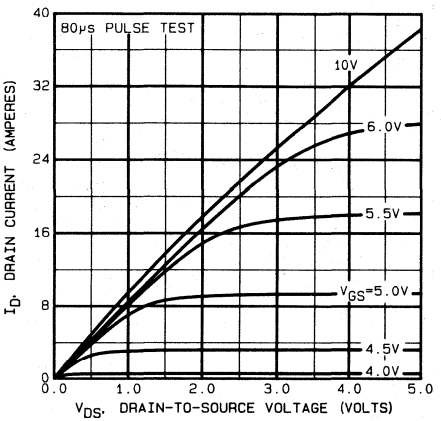


Fig. 3 - Typical saturation characteristics.

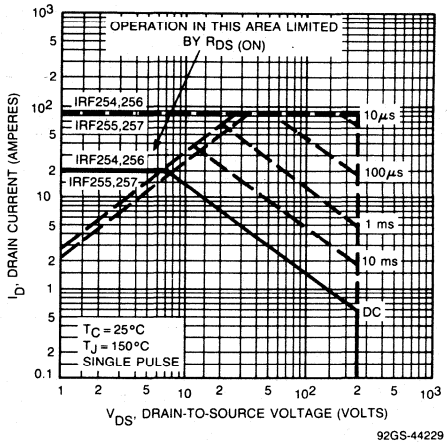


Fig. 4 - Maximum safe operating area.

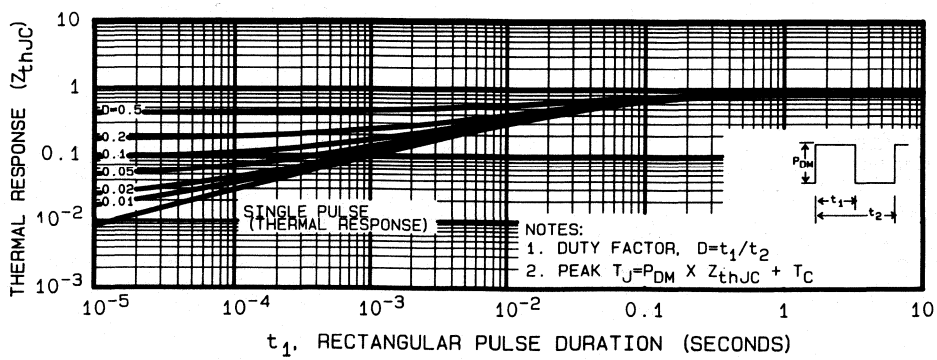


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

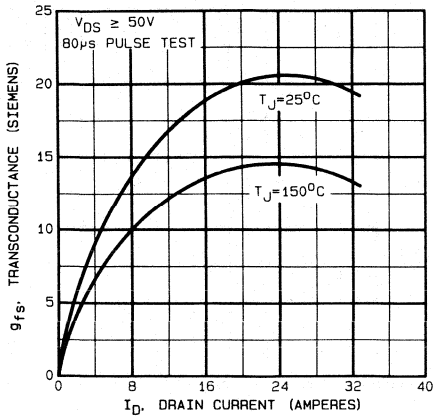


Fig. 6 - Typical transconductance vs. drain current.

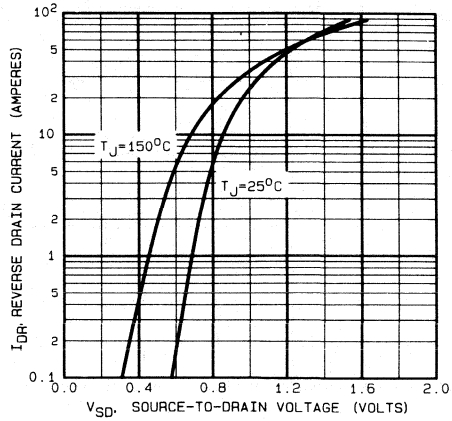


Fig. 7 - Typical source-drain diode forward voltage.

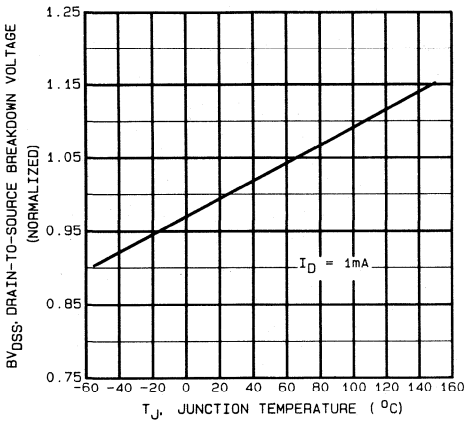


Fig. 8 - Breakdown voltage vs. temperature.

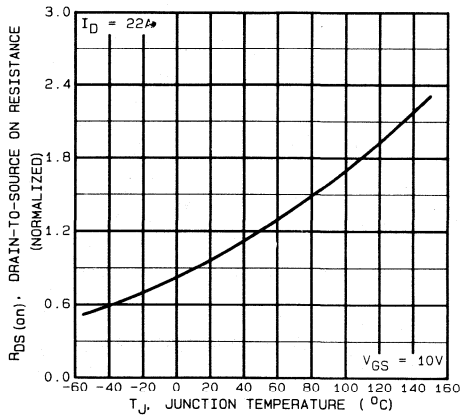


Fig. 9 - Normalized on-resistance vs. temperature.

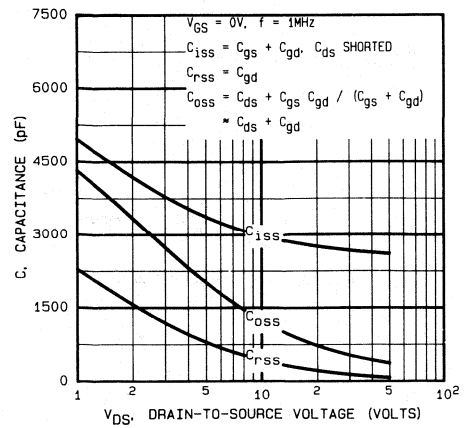


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

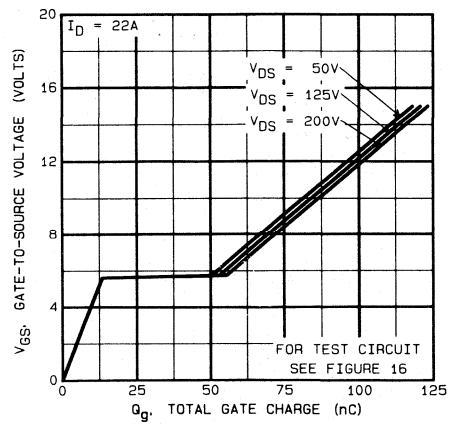


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRF254, IRF255, IRF256, IRF257

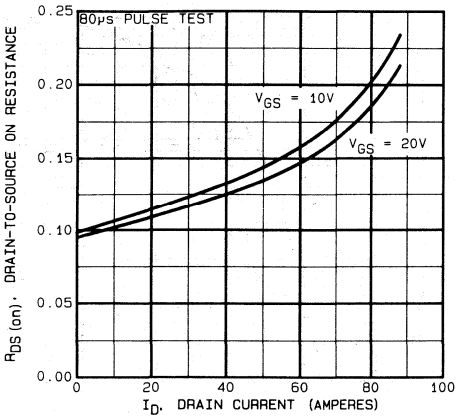


Fig. 12 - Typical on-resistance vs. drain current.

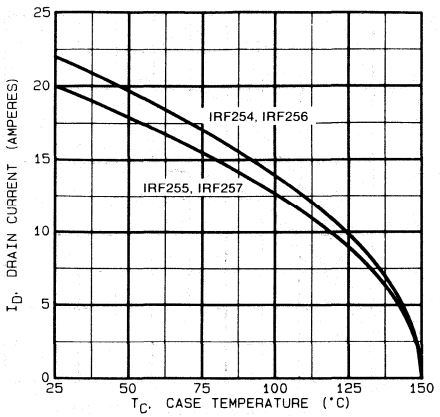


Fig. 13 - Maximum drain current vs. case temperature.

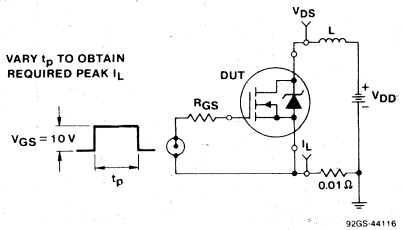


Fig. 14 - Unclamped energy test circuit.

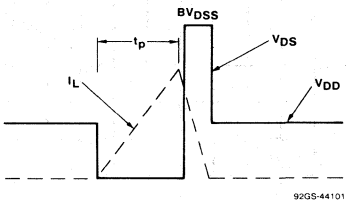


Fig. 15 - Unclamped energy waveforms.

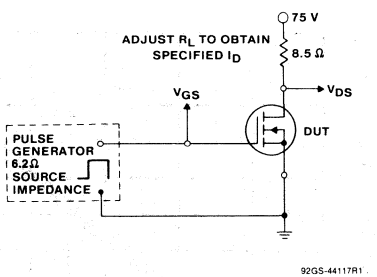


Fig. 17 - Switching time test circuit.

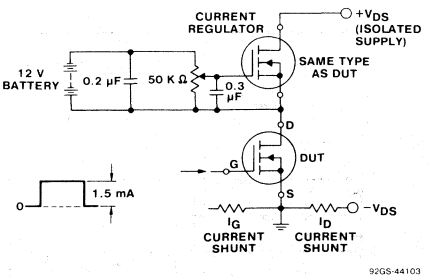


Fig. 18 - Gate charge test circuit.

File Number **2011**

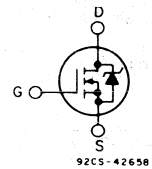
IRF330R, IRF331R, IRF332R, IRF333R

Avalanche Energy Rated N-Channel Power MOSFETs

4.5A and 5.5A, 350V-400V
$r_{DS}(on) = 1.0\Omega$ and 1.5Ω

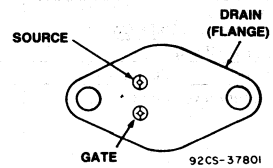
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO - 204AA

The IRF330R, IRF331R, IRF332R and IRF333R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

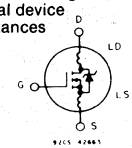
Parameter		IRF330R	IRF331R	IRF332R	IRF333R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
I_D @ $T_C = 25°C$	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ $T_C = 100°C$	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	300				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF330R, IRF331R, IRF332R, IRF333R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF330R IRF332R	400	—	—	V	V_{GS} = 0V
		IRF331R IRF333R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF330R IRF331R	5.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF332R IRF333R	4.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF330R IRF331R	—	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF332R IRF333R	—	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 3.0A
C_{iss}	Input Capacitance	ALL	—	700	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 175V, I_D = 3.0A, Z_0 = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	39	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

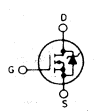


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF330R IRF331R	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF332R IRF333R	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF330R IRF331R	—	—	22	A	
		IRF332R IRF333R	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	IRF330R IRF331R	—	—	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF332R IRF333R	—	—	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 17mH, R_{gs} = 25Ω, I_{peak} = 5.5A. See figures 15, 16.

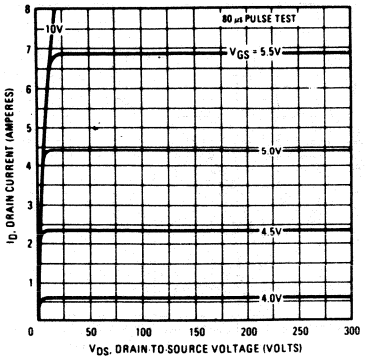


Fig. 1 – Typical Output Characteristics

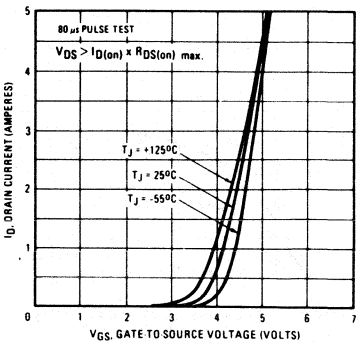


Fig. 2 – Typical Transfer Characteristics

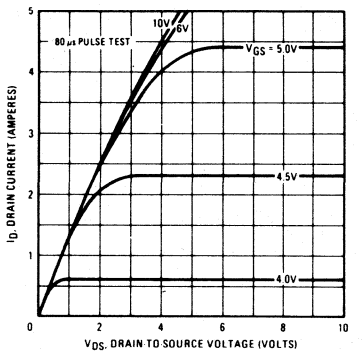


Fig. 3 – Typical Saturation Characteristics

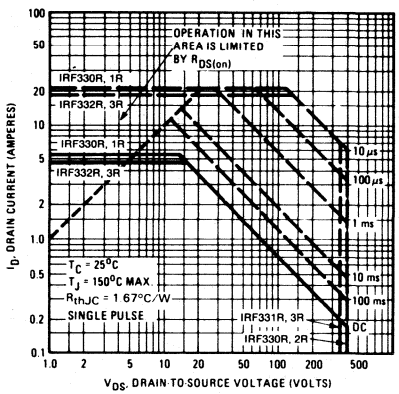


Fig. 4 – Maximum Safe Operating Area

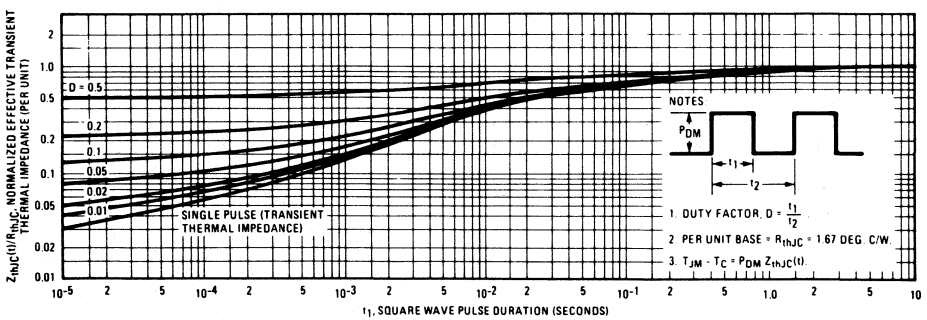


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

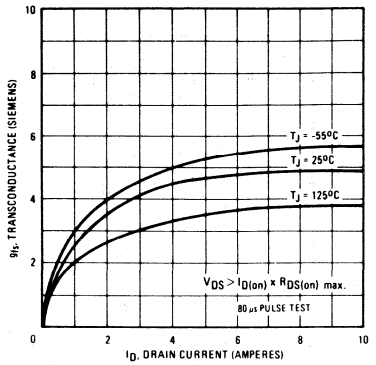


Fig. 6 – Typical Transconductance Vs. Drain Current

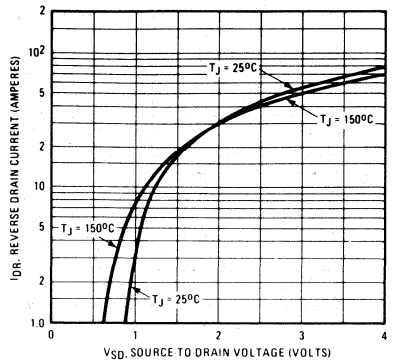


Fig. 7 – Typical Source-Drain Diode Forward Voltage

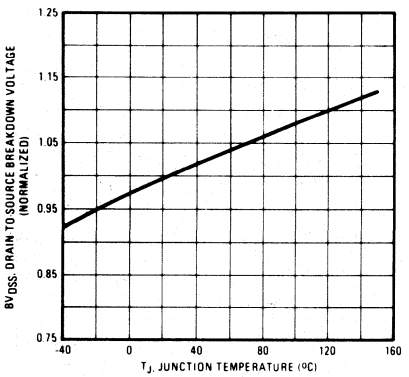


Fig. 8 – Breakdown Voltage Vs. Temperature

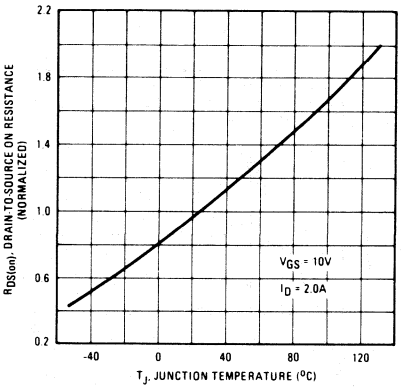


Fig. 9 – Normalized On-Resistance Vs. Temperature

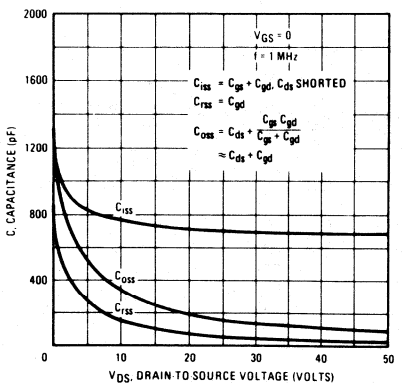


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

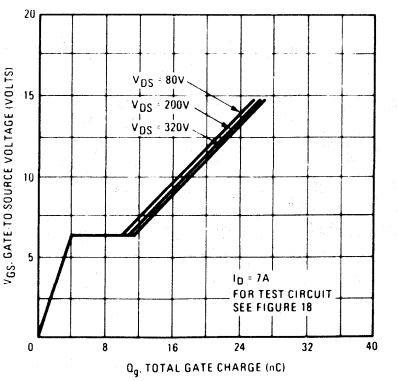


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

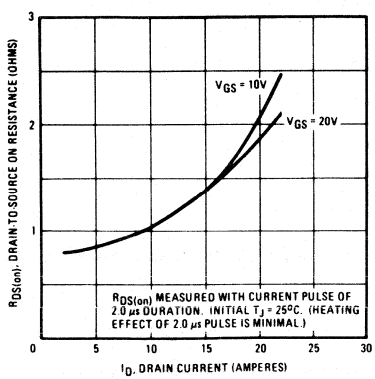


Fig. 12 – Typical On-Resistance Vs. Drain Current

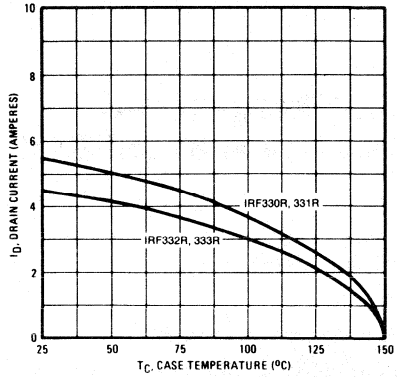


Fig. 13 – Maximum Drain Current Vs. Case Temperature

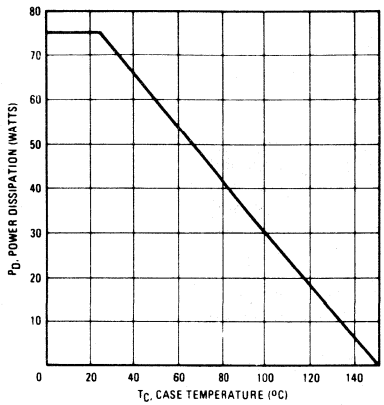


Fig. 14 – Power Vs. Temperature Derating Curve

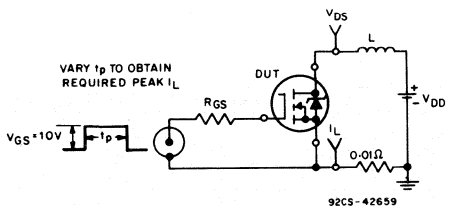


Fig. 15 — Unclamped Energy Test Circuit

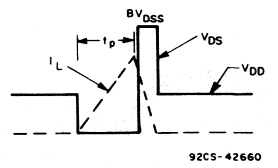


Fig. 16 — Unclamped Energy Waveforms

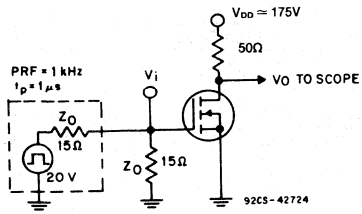


Fig. 17 – Switching Time Test Circuit

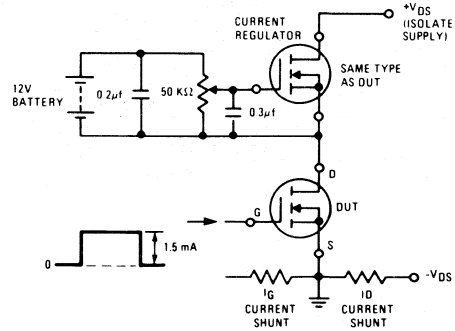


Fig. 18 – Gate Charge Test Circuit

IRF340R, IRF341R, IRF342R, IRF343R

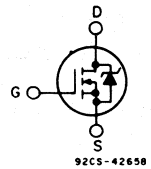
File Number **2005**

Avalanche Energy Rated N-Channel Power MOSFETs

10A and 8A, 400V and 350V
$r_{DS}(on) = 0.55\Omega$ and 0.80Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

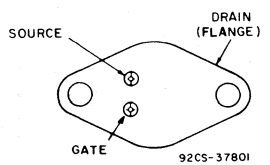


TERMINAL DIAGRAM

The IRF340R, IRF341R, IRF342R and IRF343R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

Absolute Maximum Ratings

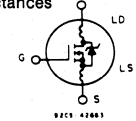
Parameter		IRF340R	IRF341R	IRF342R	IRF343R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
I_D @ $T_C = 25°C$	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
E_{as}	Single Pulse Avalanche Energy Rating ④	520				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF340R, IRF341R, IRF342R, IRF343R

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF340R IRF342R	400	—	—	V	$V_{GS} = 0V$
		IRF341R IRF343R	350	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRF340R IRF341R	10	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRF342R IRF343R	8.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF340R IRF341R	—	0.47	0.55	Ω	$V_{GS} = 10V$, $I_D = 5.0A$
		IRF342R IRF343R	—	0.68	0.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 5.0A$
C_{iss}	Input Capacitance	ALL	—	1250	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	17	35	ns	$V_{DD} \simeq 175V$, $I_D = 5.0A$, $Z_o = 4.7\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5.0	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	45	90	ns	
t_f	Fall Time	ALL	—	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	41	60	nC	$V_{GS} = 10V$, $I_D = 12A$, $V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	18	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	23	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF340R IRF341R	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF342R IRF343R	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF340R IRF341R	—	—	40	A	
		IRF342R IRF343R	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	IRF340R IRF341R	—	—	2.0	V	$T_C = 25°C$, $I_S = 10A$, $V_{GS} = 0V$
		IRF342R IRF343R	—	—	1.9	V	$T_C = 25°C$, $I_S = 8.0A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	$T_J = 150°C$, $I_F = 10A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	5.7	—	μC	$T_J = 150°C$, $I_F = 10A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 50V$, starting $T_J = 25°C$, $L = 9.2$ mH, $R_{gs} = 50\Omega$, $I_{peak} = 10A$. See figures 15, 16.

IRF340R, IRF341R, IRF342R, IRF343R

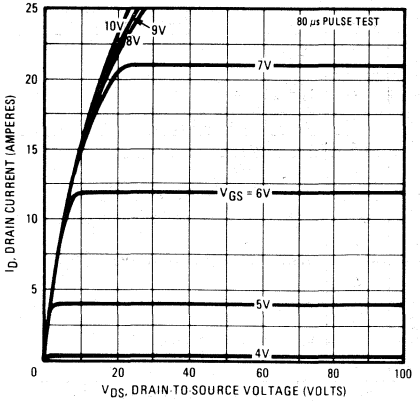


Fig. 1 – Typical Output Characteristics

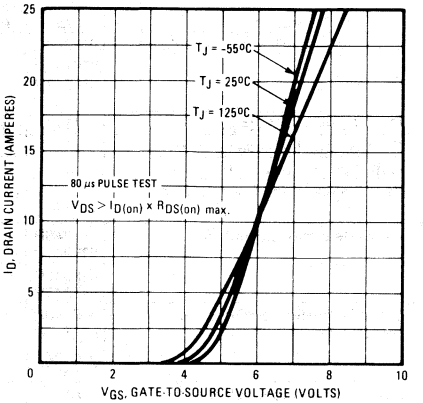


Fig. 2 – Typical Transfer Characteristics

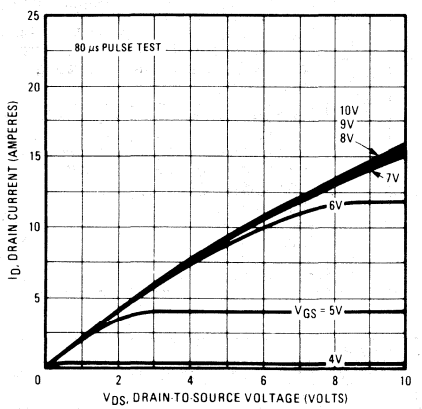


Fig. 3 – Typical Saturation Characteristics

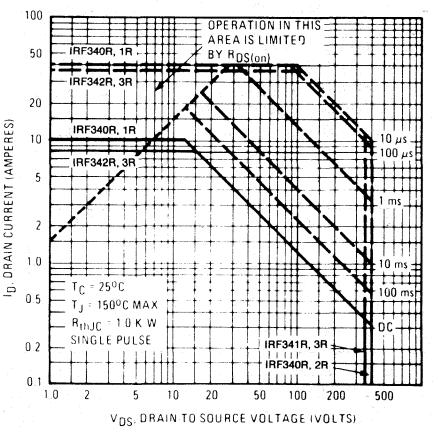


Fig. 4 – Maximum Safe Operating Area

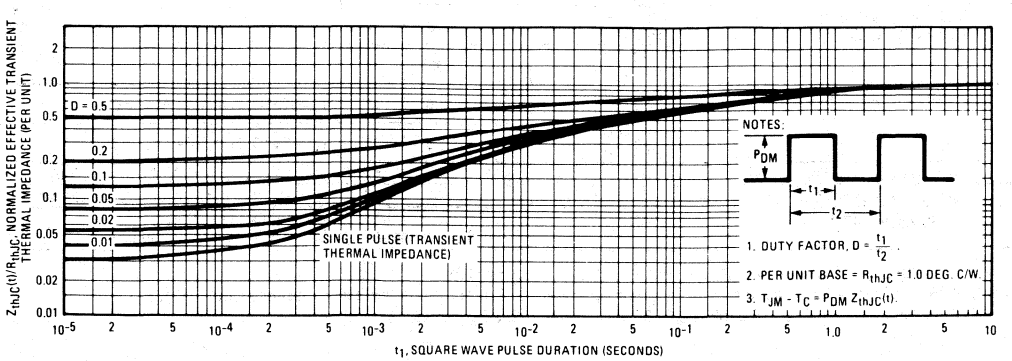


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

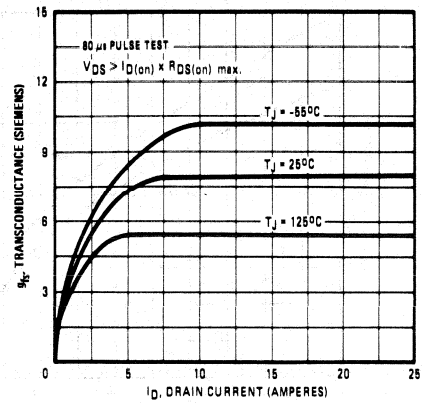


Fig. 6 – Typical Transconductance Vs. Drain Current

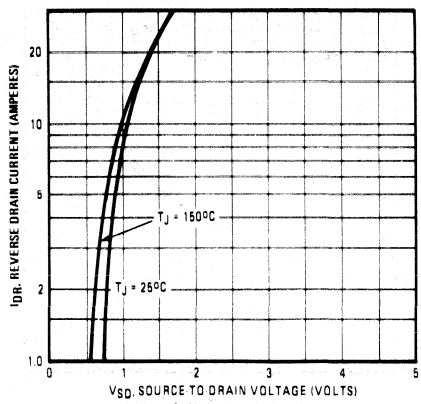


Fig. 7 – Typical Source-Drain Diode Forward Voltage

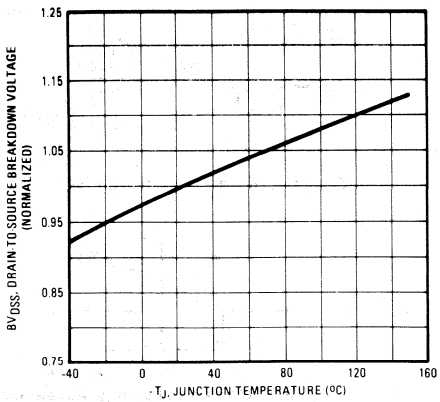


Fig. 8 – Breakdown Voltage Vs. Temperature

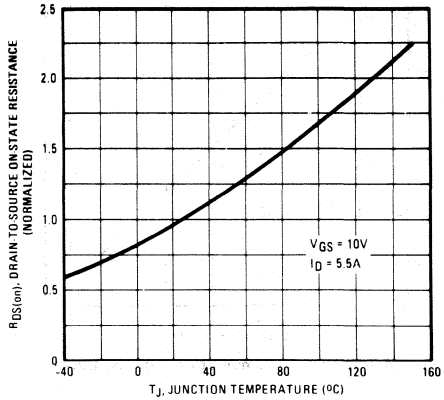


Fig. 9 – Normalized On-Resistance Vs. Temperature

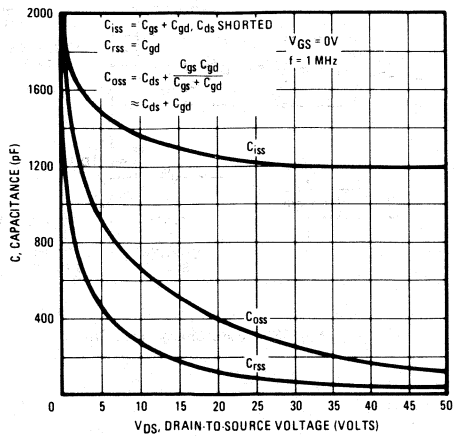


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

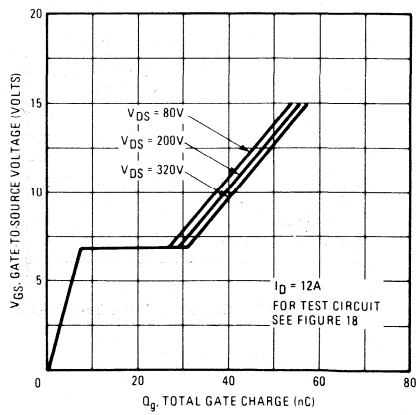


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF340R, IRF341R, IRF342R, IRF343R

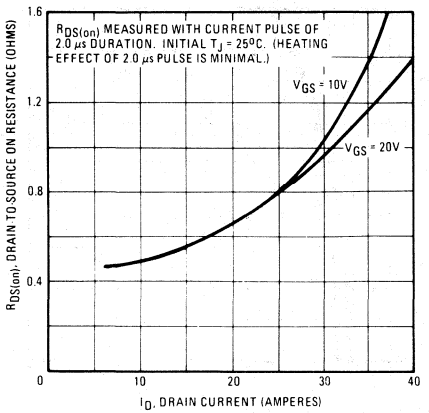


Fig. 12 – Typical On-Resistance Vs. Drain Current

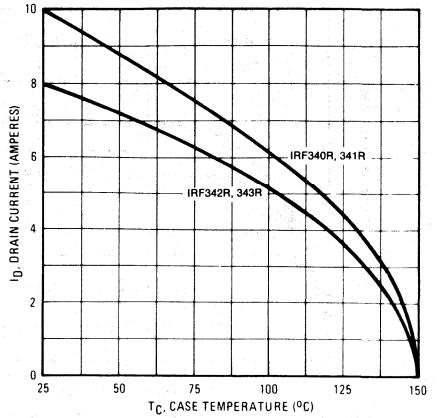


Fig. 13 – Maximum Drain Current Vs. Case Temperature

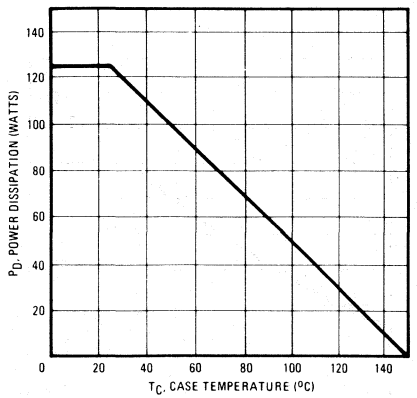


Fig. 14 – Power Vs. Temperature Derating Curve

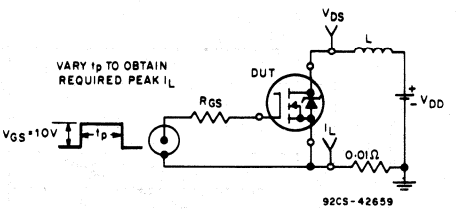


Fig. 15 — Unclamped Energy Test Circuit

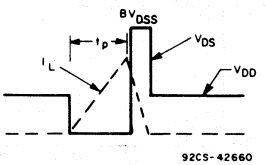


Fig. 16 — Unclamped Energy Waveforms

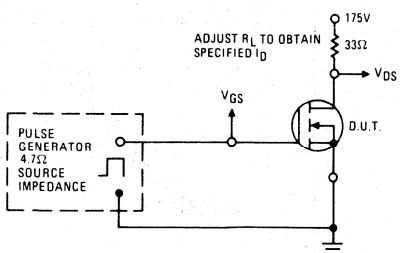


Fig. 17 – Switching Time Test Circuit

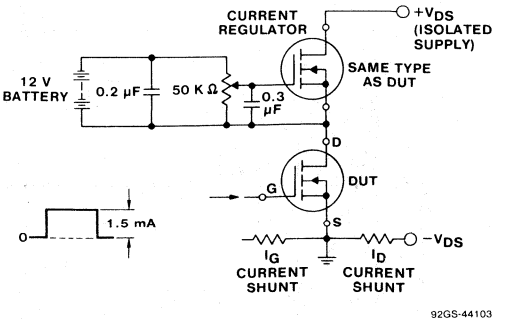


Fig. 18 – Gate Charge Test Circuit

File Number **2006**

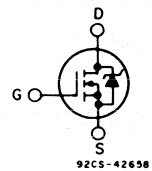
IRF350R, IRF351R, IRF352R, IRF353R

Avalanche Energy Rated N-Channel Power MOSFETs

13A and 15A, 350V-400V
$r_{DS}(on) = 0.3\Omega$ and 0.4Ω

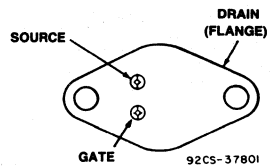
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO - 204AA

The IRF350R, IRF351R, IRF352R and IRF353R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA metal package.

Absolute Maximum Ratings

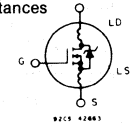
Parameter		IRF350R	IRF351R	IRF352R	IRF353R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
I_D @ $T_C = 25°C$	Continuous Drain Current	15	15	13	13	A
I_D @ $T_C = 100°C$	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	60	60	52	52	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	700				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF350R, IRF351R, IRF352R, IRF353R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF350R IRF352R	400	—	—	V	V_{GS} = 0V
		IRF351R IRF353R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF350R IRF351R	15	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF352R IRF353R	13	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF350R IRF351R	—	0.25	0.3	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF352R IRF353R	—	0.3	0.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	10	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 8.0A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 180V, I_D = 8.0A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	65	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	150	ns	
t_f	Fall Time	ALL	—	—	75	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	38	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	41	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

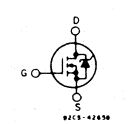


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF350R IRF351R	—	—	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF352R IRF353R	—	—	13	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF350R IRF351R	—	—	60	A	
		IRF352R IRF353R	—	—	52	A	
V_{SD}	Diode Forward Voltage ②	IRF350R IRF351R	—	—	1.6	V	T_C = 25°C, I_S = 15A, V_{GS} = 0V
		IRF352R IRF353R	—	—	1.5	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1000	—	ns	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.6	—	μC	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 40V, starting T_J = 25°C, L = 5.66mH, R_{gs} = 50Ω, I_{peak} = 15A. See figures 15, 16.

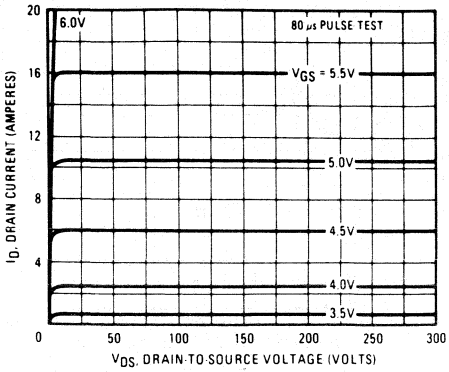


Fig. 1 — Typical Output Characteristics

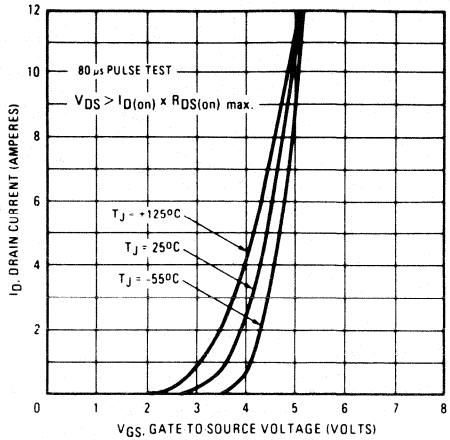


Fig. 2 — Typical Transfer Characteristics

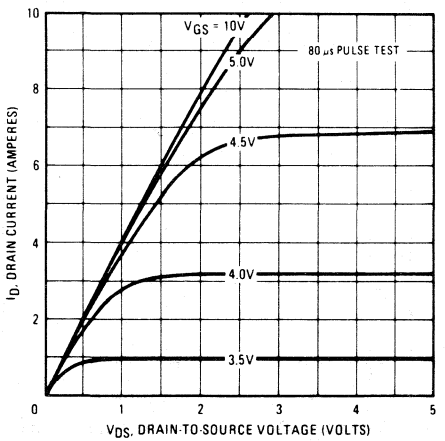


Fig. 3 — Typical Saturation Characteristics

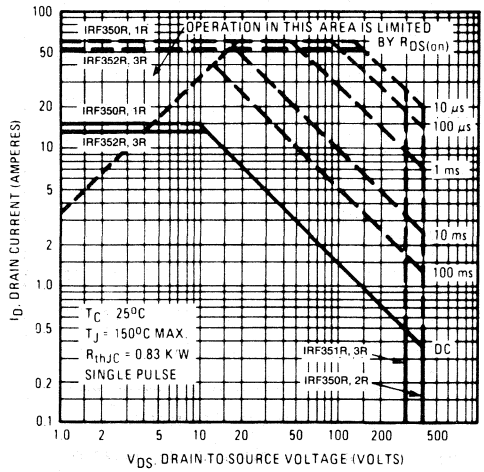


Fig. 4 — Maximum Safe Operating Area

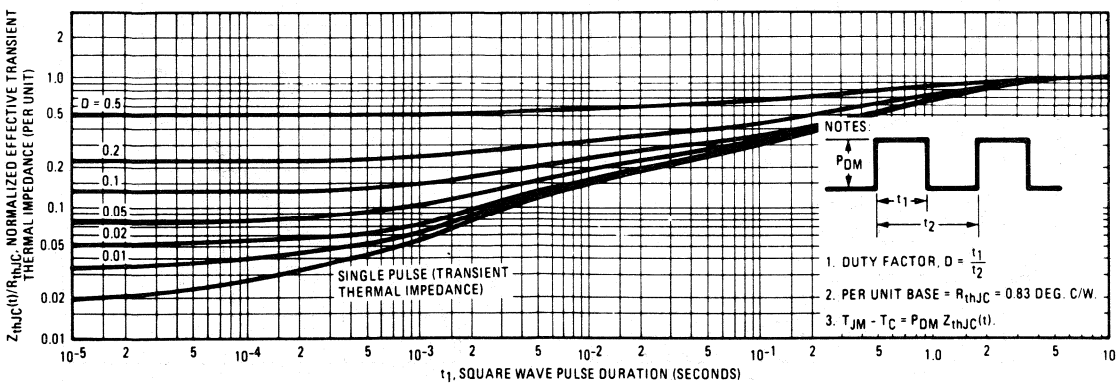


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

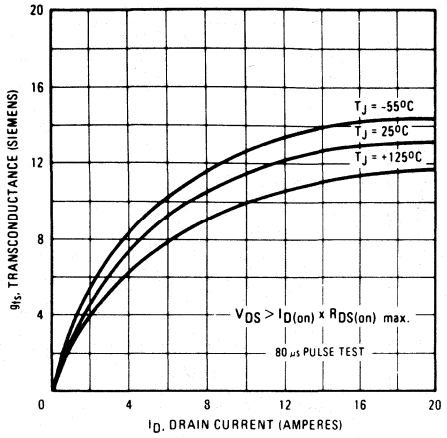


Fig. 6 – Typical Transconductance Vs. Drain Current

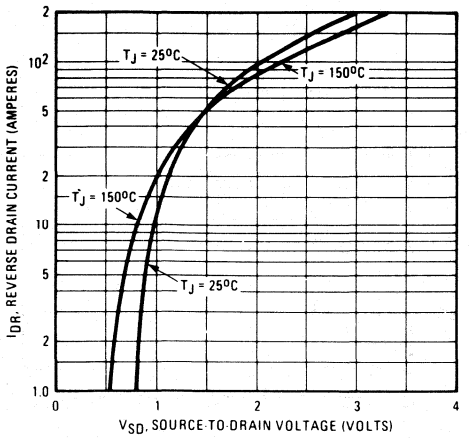


Fig. 7 – Typical Source-Drain Diode Forward Voltage

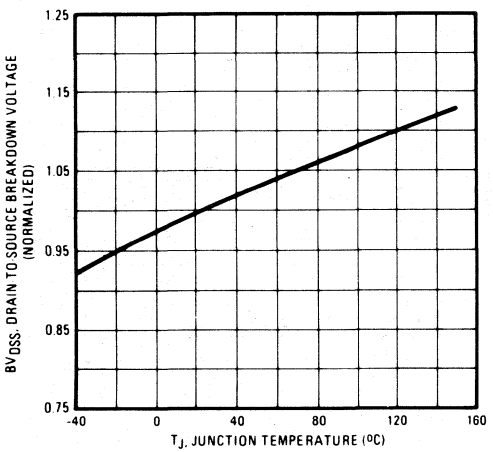


Fig. 8 – Breakdown Voltage Vs. Temperature

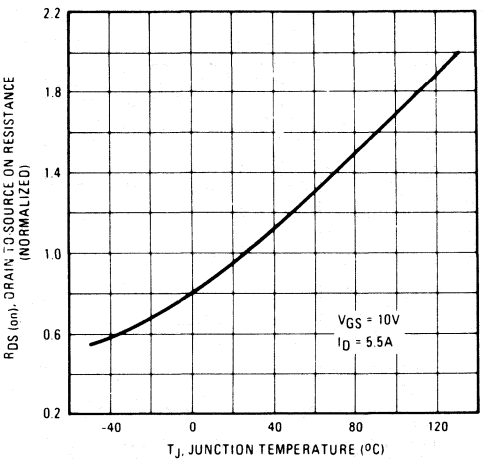


Fig. 9 – Normalized On-Resistance Vs. Temperature

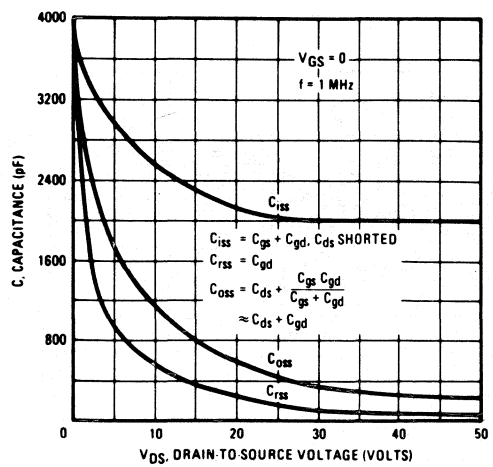


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

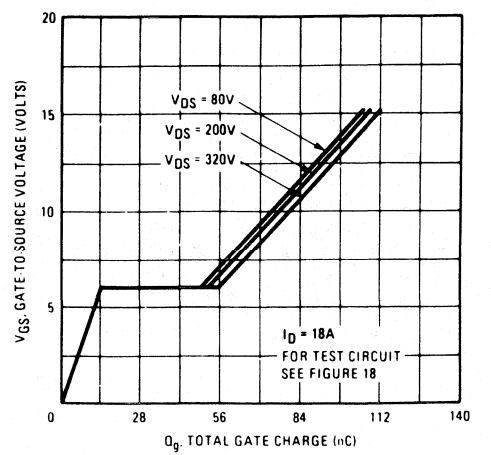


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

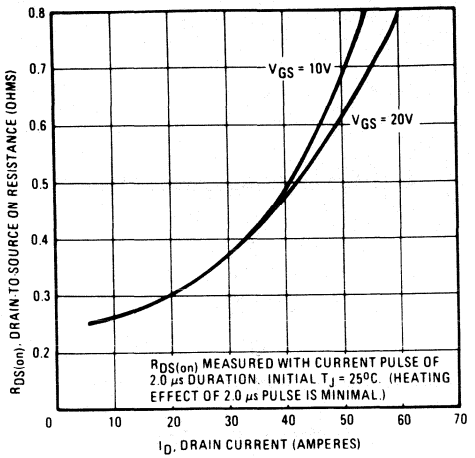


Fig. 12 – Typical On-Resistance Vs. Drain Current

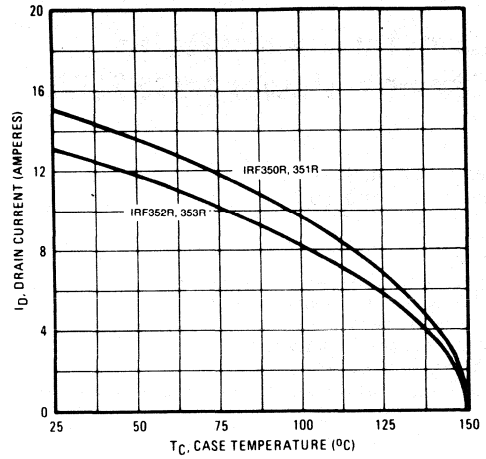
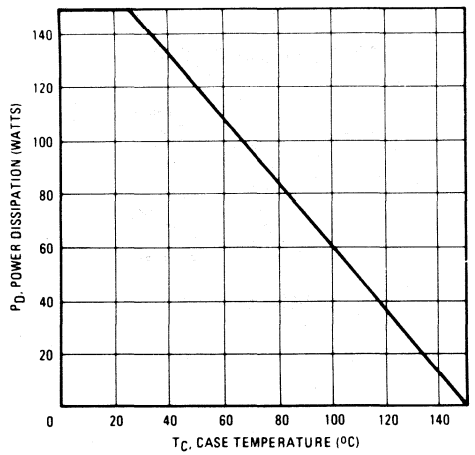


Fig. 13 – Maximum Drain Current Vs. Case Temperature



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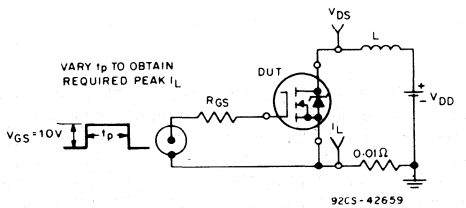


Fig. 15 — Unclamped Energy Test Circuit

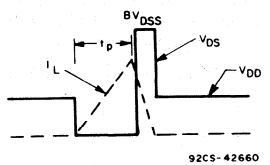


Fig. 16 — Unclamped Energy Waveforms

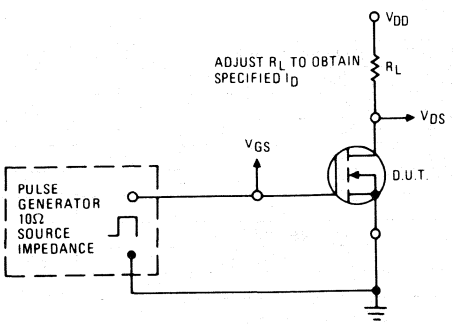


Fig. 17 – Switching Time Test Circuit

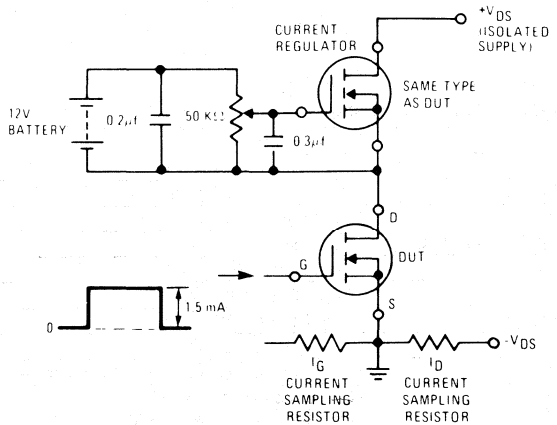


Fig. 18 – Gate Charge Test Circuit

IRF430R, IRF431R, IRF432R, IRF433R

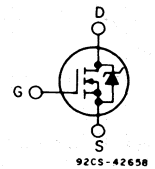
File Number **1996**

Avalanche Energy Rated N-Channel Power MOSFETs

4.0A and 4.5A, 450V-500V
$r_{DS}(on) = 1.5\Omega$ and 2.0Ω

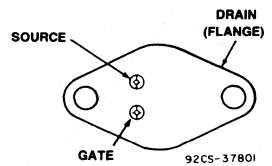
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO - 204AA

The IRF430R, IRF431R, IRF432R and IRF433R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

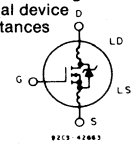
Absolute Maximum Ratings

Parameter		IRF430R	IRF431R	IRF432R	IRF433R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	300				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF430R IRF432R	500	—	—	V	V_{GS} = 0V
		IRF431R IRF433R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF430R IRF431R	4.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF432R IRF433R	4.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF430R IRF431R	—	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF432R IRF433R	—	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.2	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 2.5A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 225V, I_D = 2.5A, Z_0 = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	39	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	11	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

$R_{th}JC$	Junction-to-Case	ALL	—	—	1.67	°C/W	
$R_{th}CS$	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{th}JA$	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF430R IRF431R	—	—	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF432R IRF433R	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF430R IRF431R	—	—	18	A	
		IRF432R IRF433R	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	IRF430R IRF431R	—	—	1.4	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF432R IRF433R	—	—	1.3	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 25mH, R_{gs} = 25Ω, I_{peak} = 4.5A. See figures 15, 16.

IRF430R, IRF431R, IRF432R, IRF433R

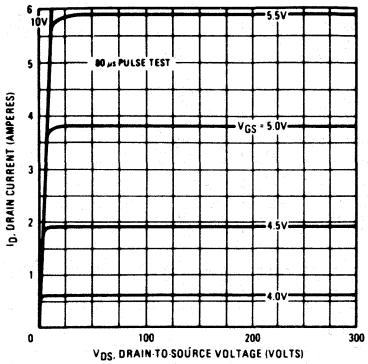


Fig. 1 – Typical Output Characteristics

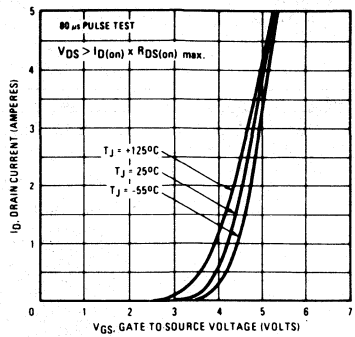


Fig. 2 – Typical Transfer Characteristics

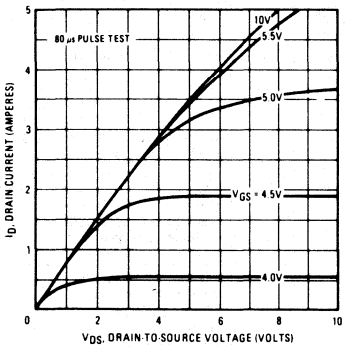


Fig. 3 – Typical Saturation Characteristics

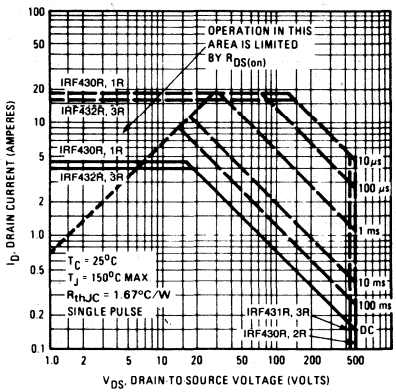


Fig. 4 – Maximum Safe Operating Area

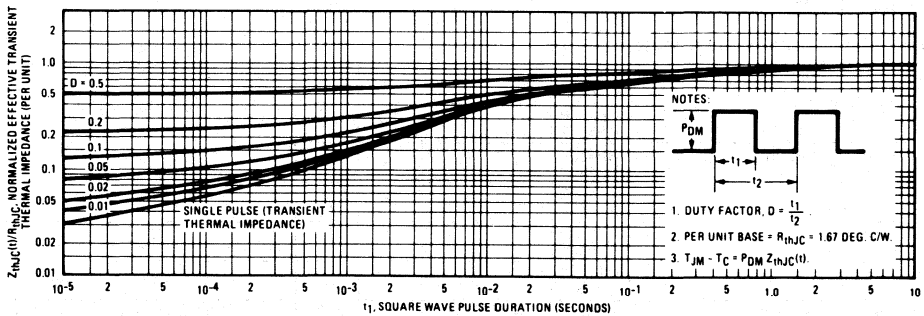


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

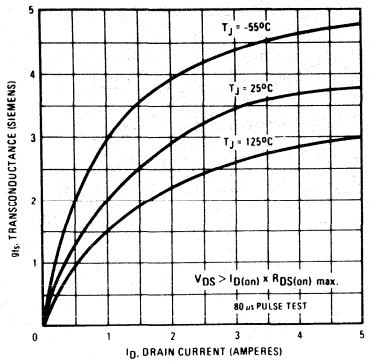


Fig. 6 – Typical Transconductance Vs. Drain Current

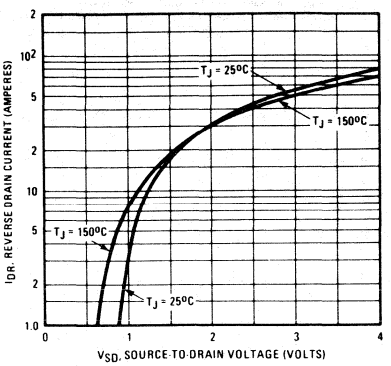


Fig. 7 – Typical Source-Drain Diode Forward Voltage

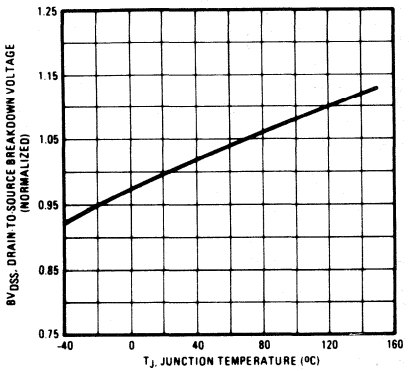


Fig. 8 – Breakdown Voltage Vs. Temperature

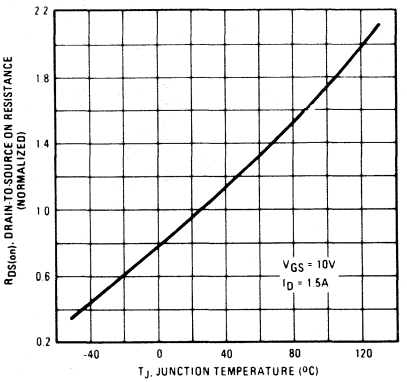


Fig. 9 – Normalized On-Resistance Vs. Temperature

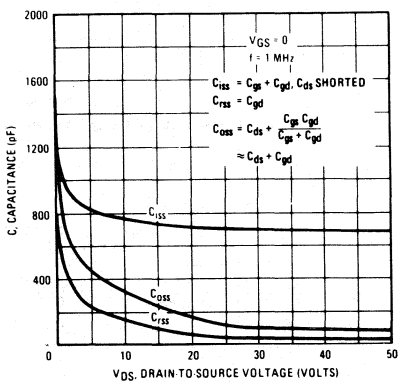


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

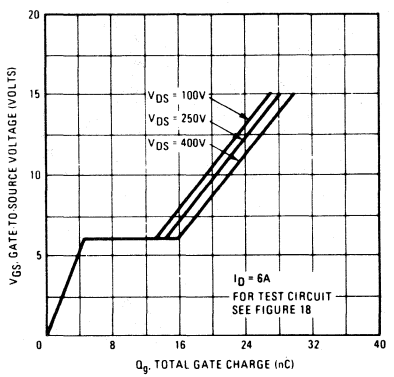


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

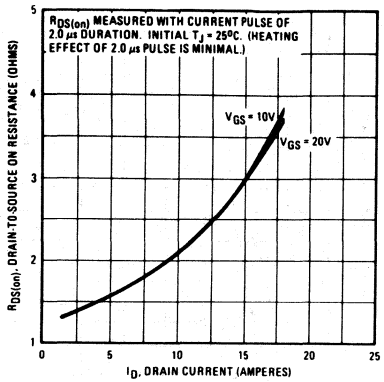


Fig. 12 — Typical On-Resistance Vs. Drain Current

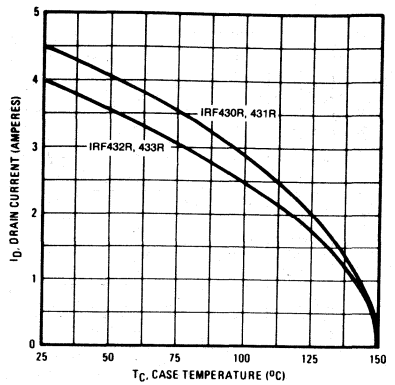


Fig. 13 — Maximum Drain Current Vs. Case Temperature

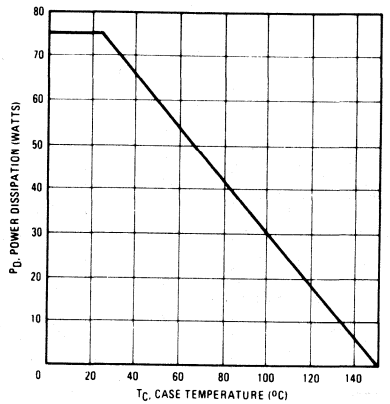


Fig. 14 — Power Vs. Temperature Derating Curve

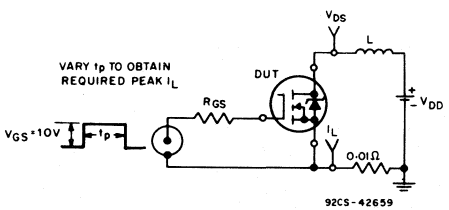


Fig. 15 — Unclamped Energy Test Circuit

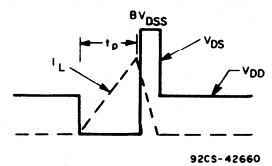


Fig. 16 — Unclamped Energy Waveforms

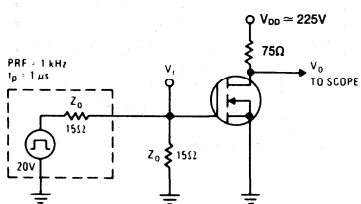


Fig. 17 — Switching Time Test Circuit

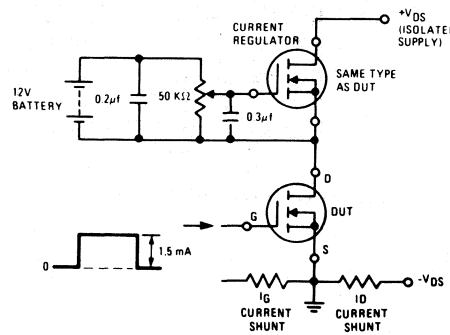


Fig. 18 — Gate Charge Test Circuit

File Number **2007**

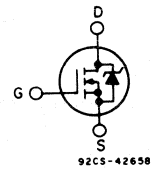
IRF440R, IRF441R, IRF442R, IRF443R

Avalanche Energy Rated N-Channel Power MOSFETs

8A and 7A, 500V-400V
$r_{DS}(on) = 0.85\Omega$ and 1.1Ω

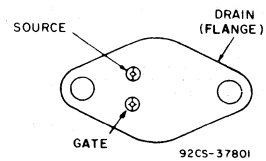
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

The IRF440R, IRF441R, IRF442R and IRF443R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

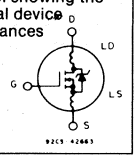
Parameter		IRF440R	IRF441R	IRF442R	IRF443R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	510				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF440R, IRF441R, IRF442R, IRF443R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF440R IRF442R	500	—	—	V	V_{GS} = 0V
		IRF441R IRF443R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF440R IRF441R	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF442R IRF443R	7.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF440R IRF441R	—	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF442R IRF443R	—	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 4.0A
C_{iss}	Input Capacitance	ALL	—	1225	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	85	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	17	35	ns	$V_{DD} \simeq$ 200V, I_D = 4.0A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	42	90	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	20	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	22	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF440R IRF441R	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF442R IRF443R	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF440R IRF441R	—	—	32	A	
		IRF442R IRF443R	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	IRF440R IRF441R	—	—	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF442R IRF443R	—	—	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1100	—	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.4	—	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 14 mH, R_{gs} = 50Ω, I_{peak} = 8A. See figures 15, 16.

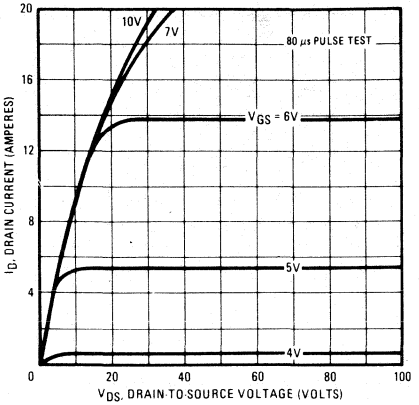


Fig. 1 – Typical Output Characteristics

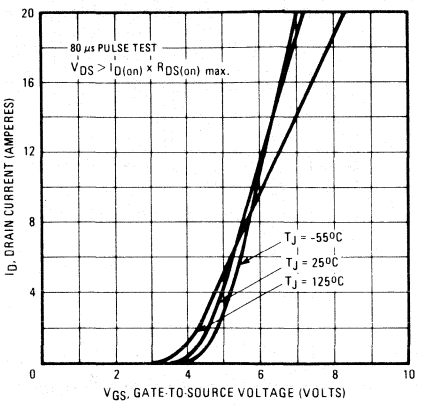


Fig. 2 – Typical Transfer Characteristics

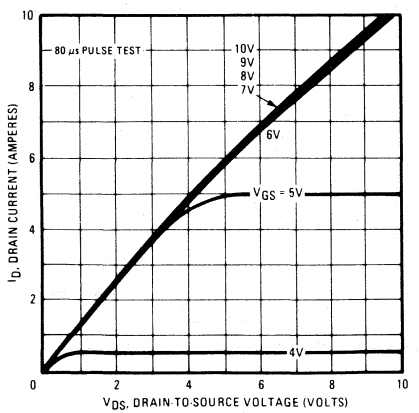


Fig. 3 – Typical Saturation Characteristics

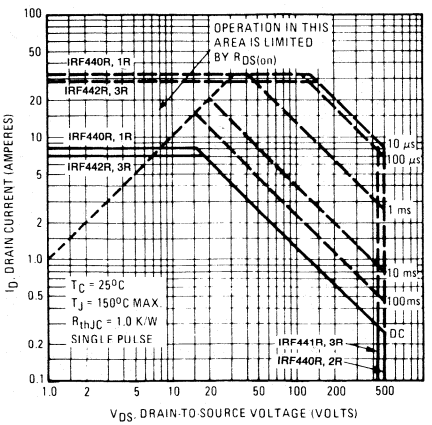


Fig. 4 – Maximum Safe Operating Area

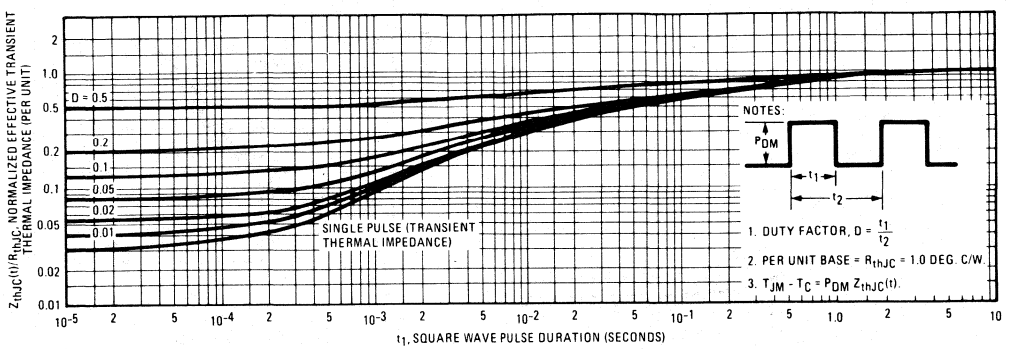


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF440R, IRF441R, IRF442R, IRF443R

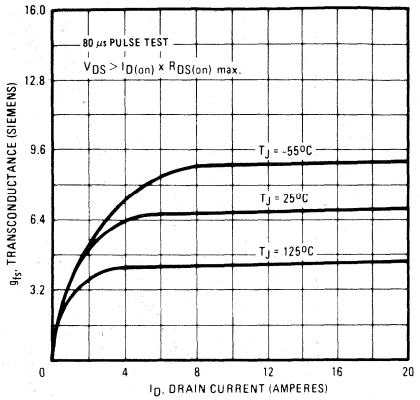


Fig. 6 – Typical Transconductance Vs. Drain Current

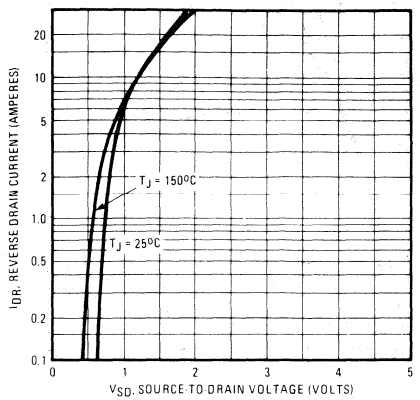


Fig. 7 – Typical Source-Drain Diode Forward Voltage

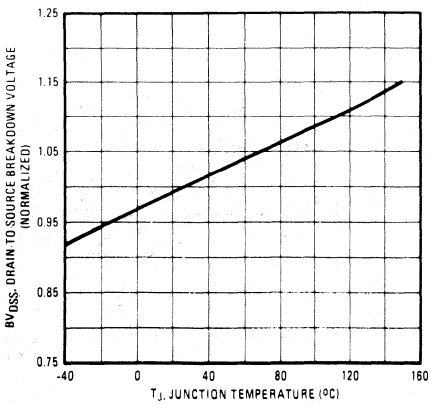


Fig. 8 – Breakdown Voltage Vs. Temperature

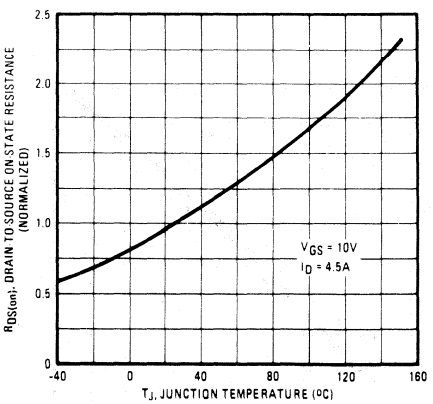


Fig. 9 – Normalized On-Resistance Vs. Temperature

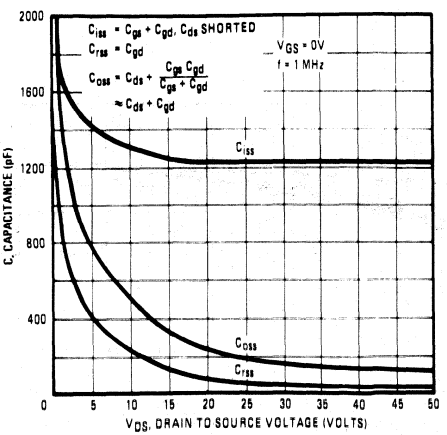


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

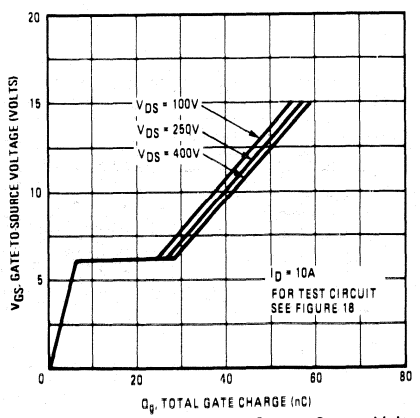


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

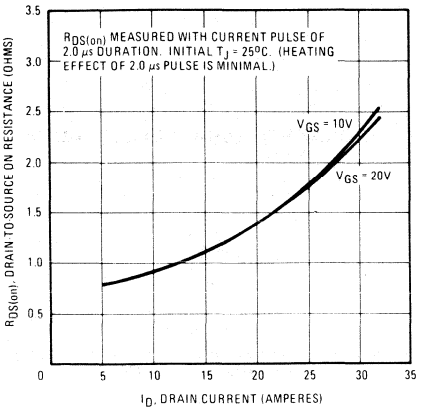


Fig. 12 – Typical On-Resistance Vs. Drain Current

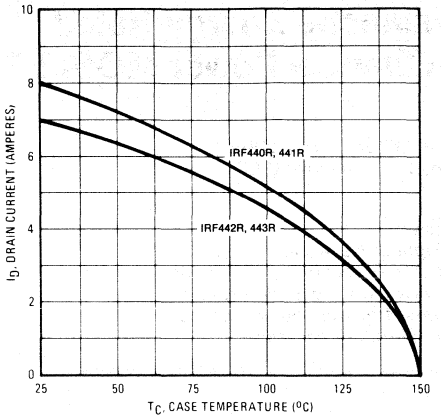


Fig. 13 – Maximum Drain Current Vs. Case Temperature

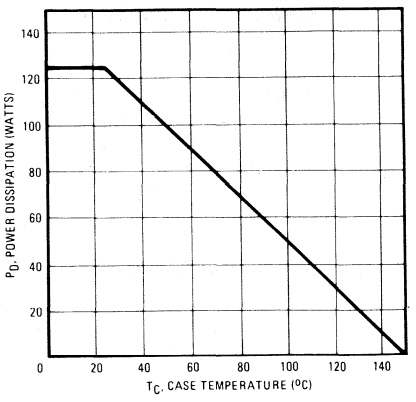


Fig. 14 – Power Vs. Temperature Derating Curve

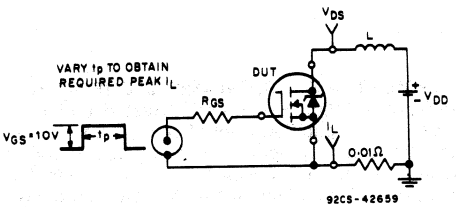


Fig. 15 — Unclamped Energy Test Circuit

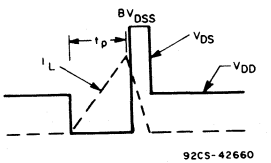


Fig. 16 — Unclamped Energy Waveforms

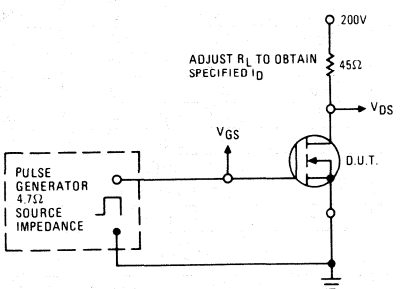


Fig. 17 – Switching Time Test Circuit

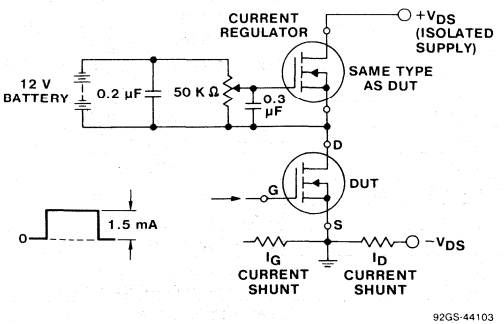


Fig. 18 – Gate Charge Test Circuit

IRF450R, IRF451R, IRF452R, IRF453R

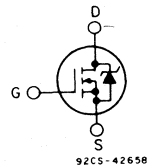
File Number **2008**

Avalanche Energy Rated N-Channel Power MOSFETs

12A and 13A, 450V-500V
$r_{DS}(on) = 0.4\Omega$ and 0.5Ω

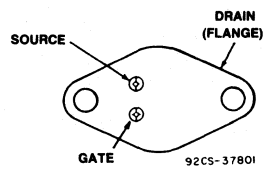
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO- 204AA

The IRF450R, IRF451R, IRF452R and IRF453R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA metal package.

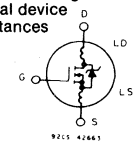
Absolute Maximum Ratings

Parameter		IRF450R	IRF451R	IRF452R	IRF453R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	13	13	12	12	A
I_D @ $T_C = 100°C$	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	860				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF450R, IRF452R	500	—	—	V	V_{GS} = 0V
		IRF451R, IRF453R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF450R, IRF451R	13	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF452R, IRF453R	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF450R, IRF451R	—	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		IRF452R, IRF453R	—	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 7.0A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 210V, I_D = 7.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	150	ns	
t_f	Fall Time	ALL	—	—	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	82	140	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	40	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	42	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF450R, IRF451R	—	—	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF452R, IRF453R	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF450R, IRF451R	—	—	52	A	
		IRF452R, IRF453R	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	IRF450R, IRF451R	—	—	1.4	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
		IRF452R, IRF453R	—	—	1.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1300	—	ns	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	7.5	—	μC	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_J = 25°C, L = 9.2mH, R_{gs} = 25Ω, I_{peak} = 13A. See figures 15, 16.

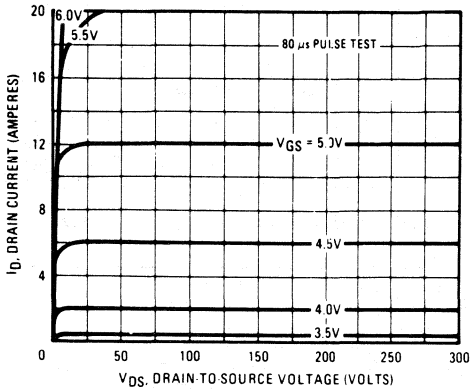


Fig. 1 — Typical Output Characteristics

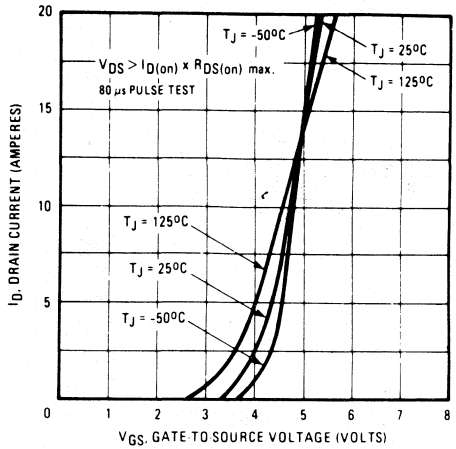


Fig. 2 — Typical Transfer Characteristics

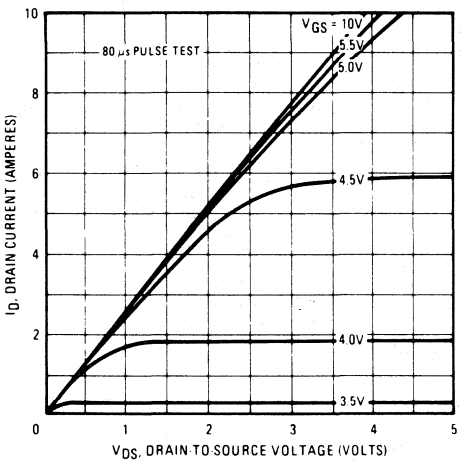


Fig. 3 — Typical Saturation Characteristics

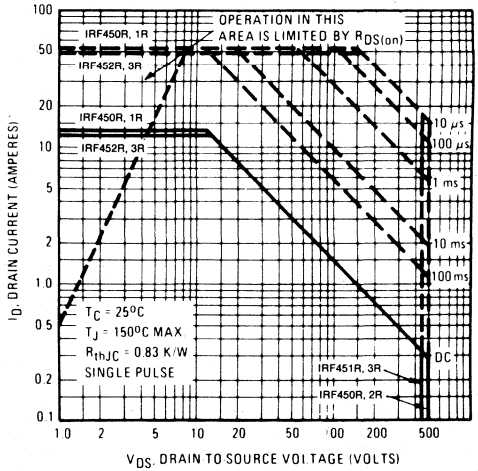


Fig. 4 — Maximum Safe Operating Area

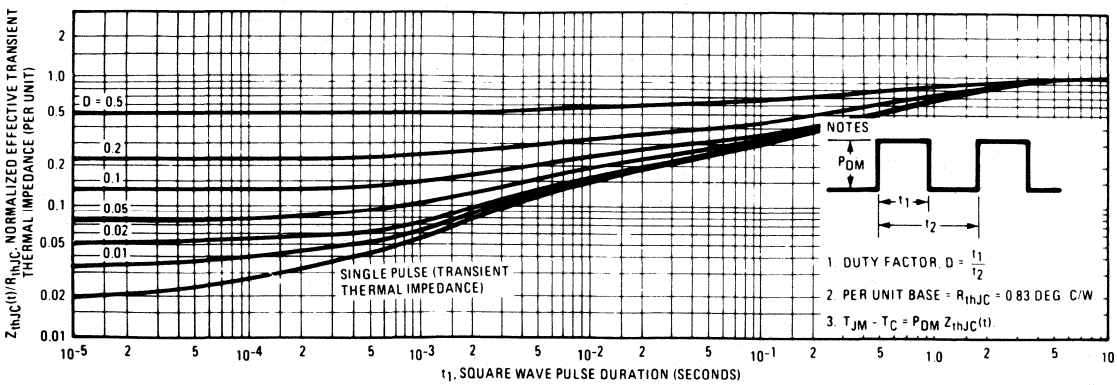


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

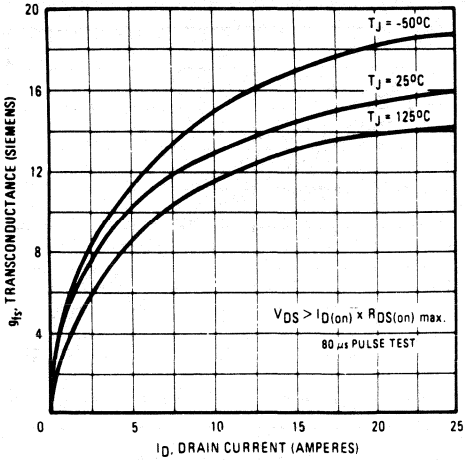


Fig. 6 — Typical Transconductance Vs. Drain Current

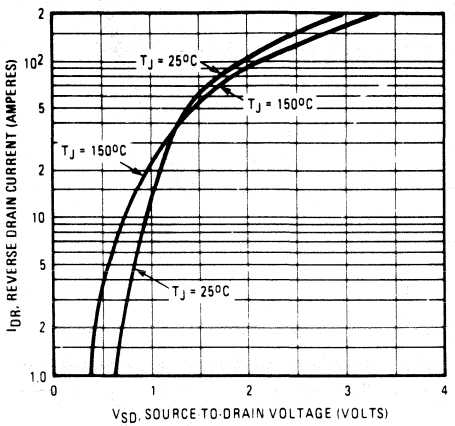


Fig. 7 — Typical Source-Drain Diode Forward Voltage

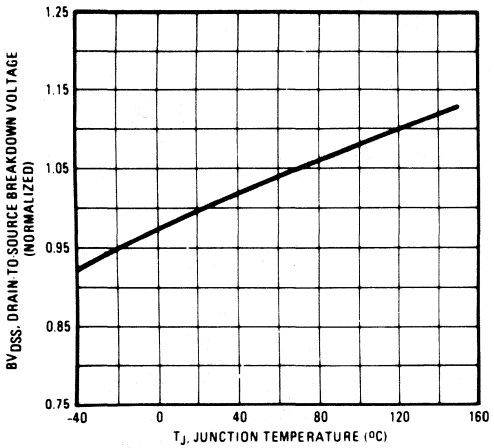


Fig. 8 — Breakdown Voltage Vs. Temperature

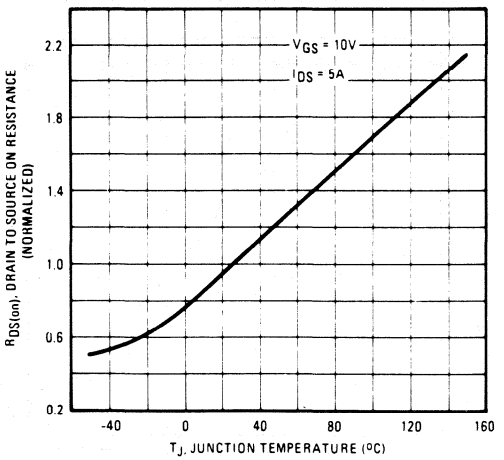


Fig. 9 — Normalized On-Resistance Vs. Temperature

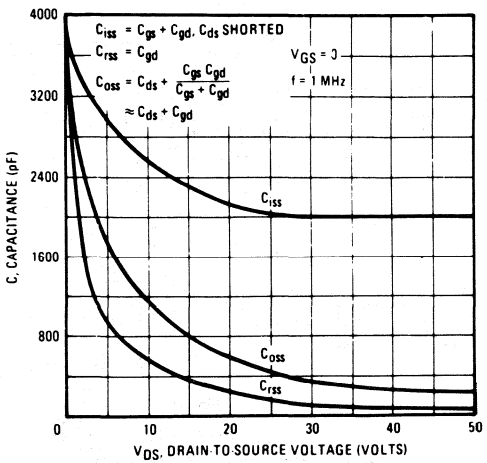


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

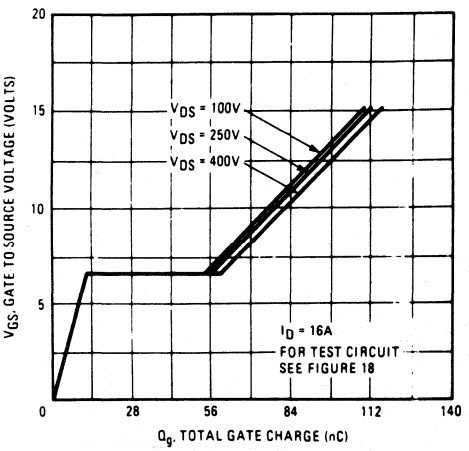


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

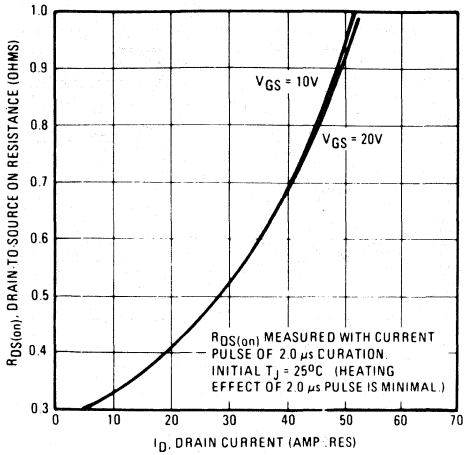


Fig. 12 – Typical On-Resistance Vs. Drain Current

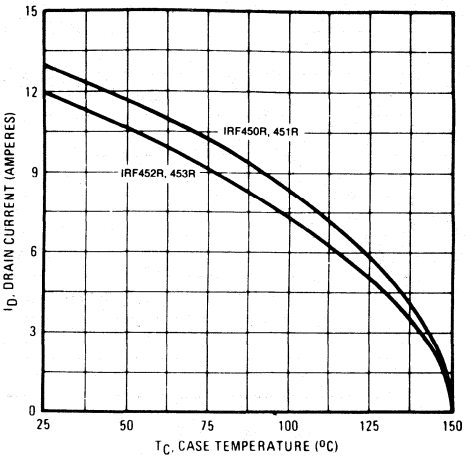


Fig. 13 – Maximum Drain Current Vs. Case Temperature

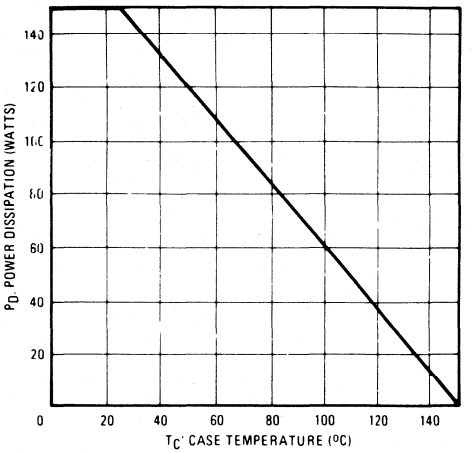


Fig. 14 – Power Vs. Temperature Derating Curve

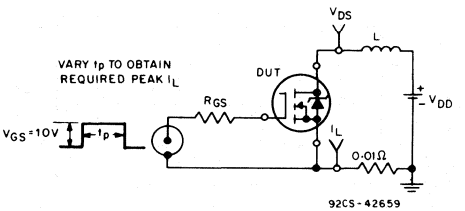


Fig. 15 — Unclamped Energy Test Circuit

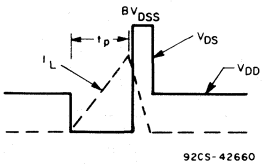


Fig. 16 — Unclamped Energy Waveforms

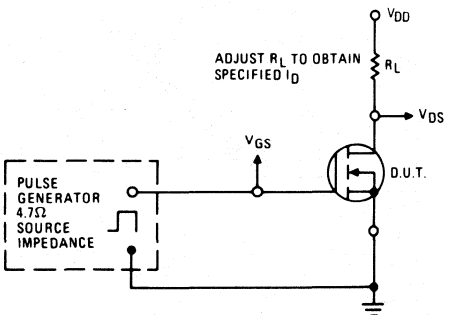


Fig. 17 – Switching Time Test Circuit

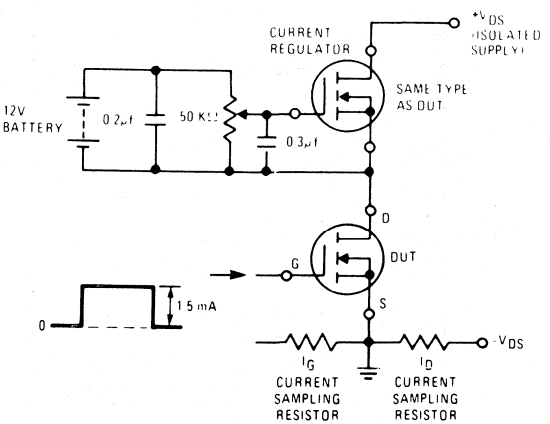


Fig. 18 – Gate Charge Test Circuit

File Number **1995**

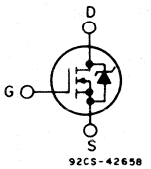
IRF510R, IRF511R, IRF512R, IRF513R

Avalanche Energy Rated N-Channel Power MOSFETs

3.5A and 4.0A, 60V-100V
$r_{DS}(on) = 0.6\Omega$ and 0.8Ω

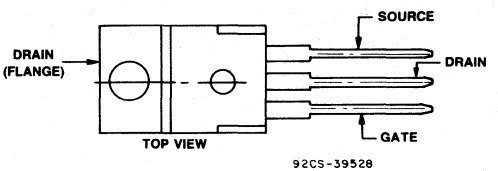
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF510R, IRF511R, IRF512R and IRF513R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

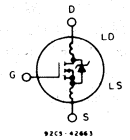
Parameter		IRF510R	IRF511R	IRF512R	IRF513R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	4.0	4.0	3.5	3.5	A
I_D @ $T_C = 100°C$	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	16	16	14	14	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	19				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF510R, IRF511R, IRF512R, IRF513R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF510R IRF512R	100	—	—	V	V_{GS} = 0V
		IRF511R IRF513R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF510R IRF511R	4.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF512R IRF513R	3.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF510R IRF511R	—	0.5	0.6	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF512R IRF513R	—	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 2.0A
C_{iss}	Input Capacitance	ALL	—	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	80	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_o = 50Ω
t_r	Rise Time	ALL	—	15	25	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	11	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

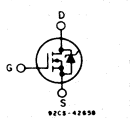


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF510R IRF511R	—	—	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF512R IRF513R	—	—	3.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF510R IRF511R	—	—	16	A	
		IRF512R IRF513R	—	—	14	A	
V_{SD}	Diode Forward Voltage ②	IRF510R IRF511R	—	—	2.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
		IRF512R IRF513R	—	—	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	230	—	ns	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.4	—	μC	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_j = 25°C, L = 910μH, R_{gs} = 25Ω, I_{peak} = 5.6Ω. See figures 15, 16

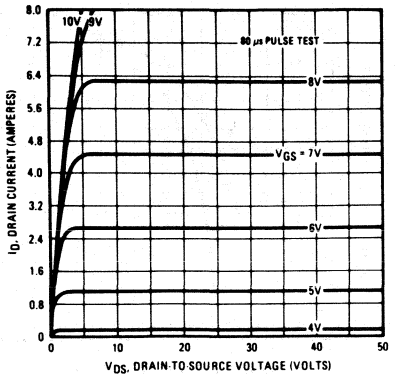


Fig. 1 – Typical Output Characteristics

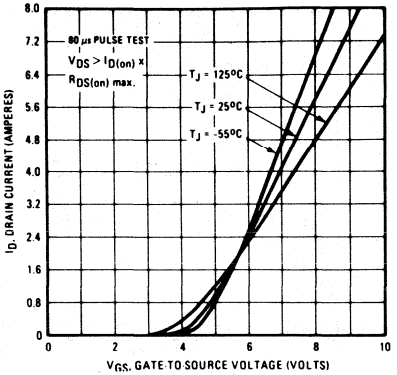


Fig. 2 – Typical Transfer Characteristics

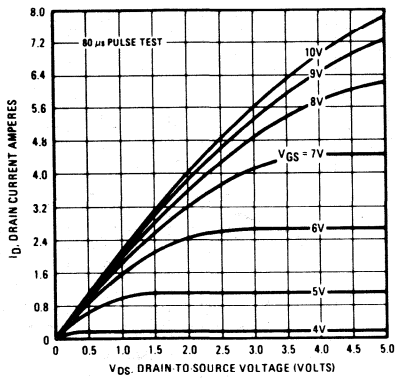


Fig. 3 – Typical Saturation Characteristics

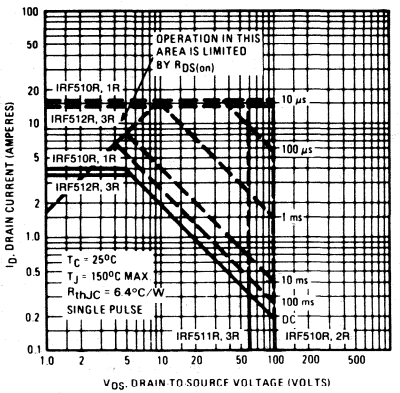


Fig. 4 – Maximum Safe Operating Area

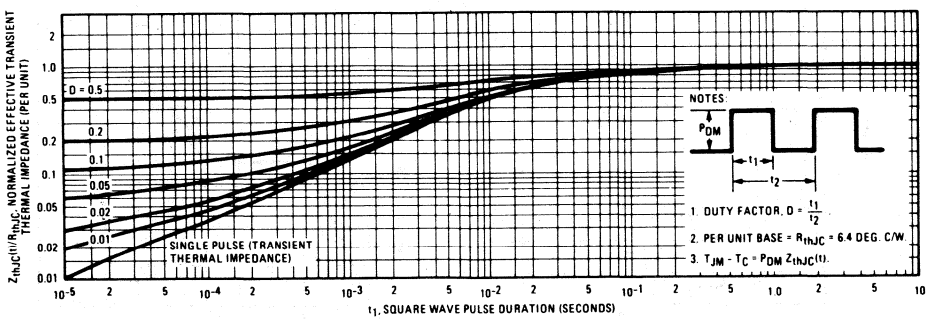


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

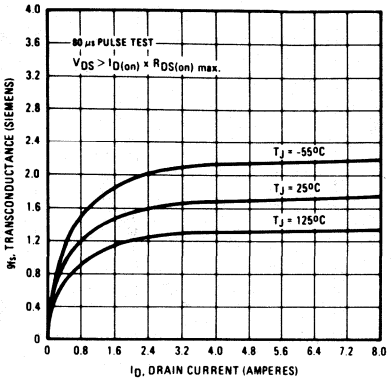


Fig. 6 – Typical Transconductance Vs. Drain Current

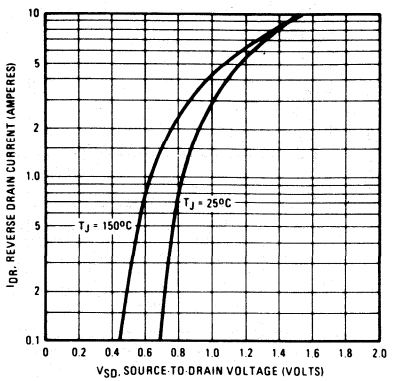


Fig. 7 – Typical Source-Drain Diode Forward Voltage

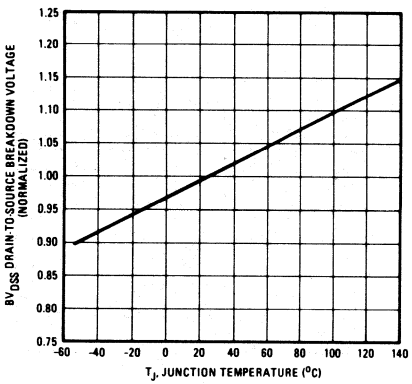


Fig. 8 – Breakdown Voltage Vs. Temperature

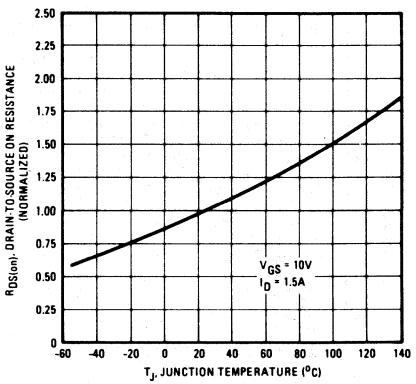


Fig. 9 – Normalized On-Resistance Vs. Temperature

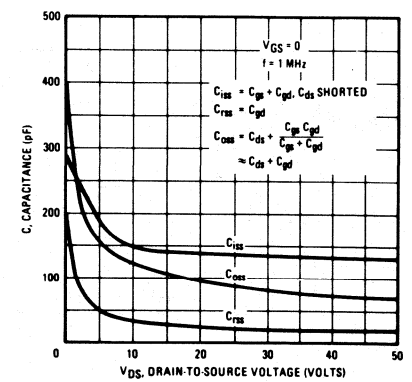


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

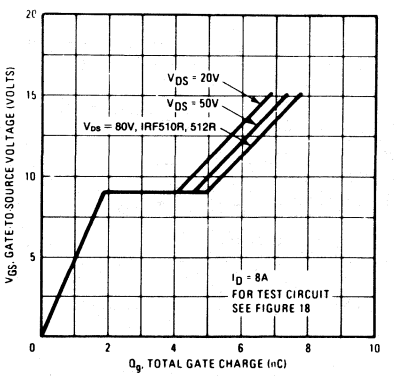


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

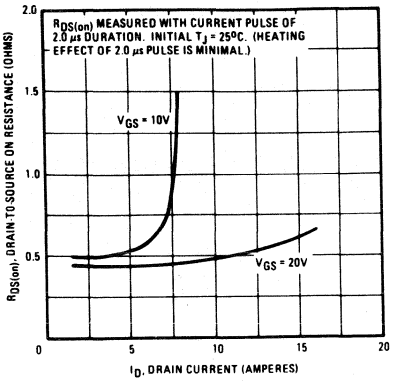


Fig. 12 – Typical On-Resistance Vs. Drain Current

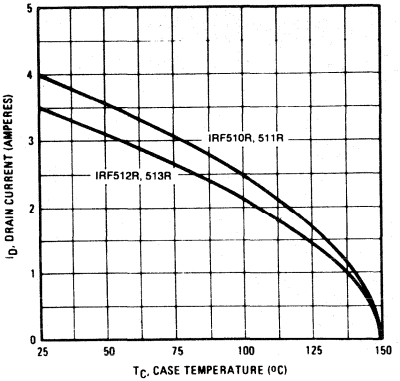


Fig. 13 – Maximum Drain Current Vs. Case Temperature

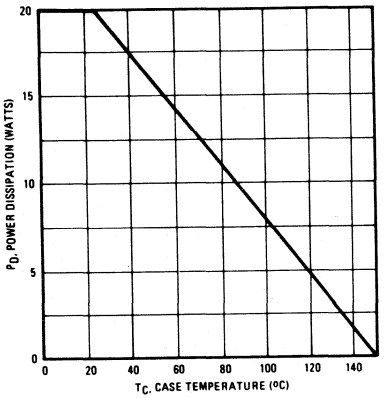


Fig. 14 – Power Vs. Temperature Derating Curve

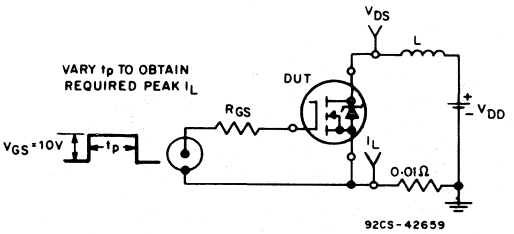


Fig. 15 — Unclamped Energy Test Circuit

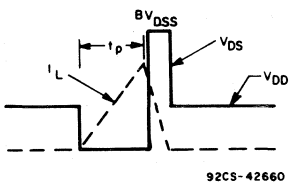


Fig. 16 — Unclamped Energy Waveforms

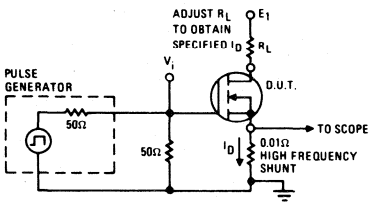


Fig. 17 – Switching Time Test Circuit

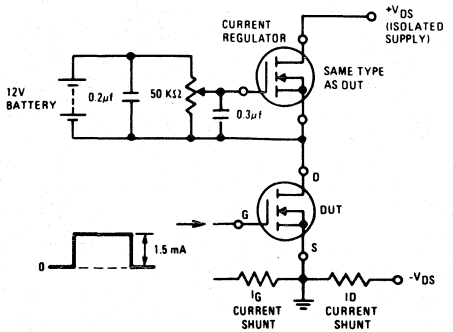


Fig. 18 – Gate Charge Test Circuit

IRF520R, IRF521R, IRF522R, IRF523R

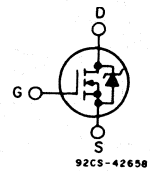
File Number **1994**

Avalanche Energy Rated N-Channel Power MOSFETs

7.0A and 8.0A, 60V-100V
$r_{DS}(on) = 0.30\Omega$ and 0.40Ω

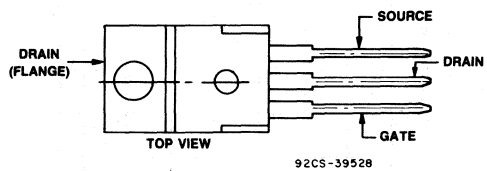
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF520R, IRF521R, IRF522R and IRF523R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

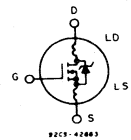
Absolute Maximum Ratings

Parameter		IRF520R	IRF521R	IRF522R	IRF523R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	36				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF520R IRF522R	100	—	—	V	V_{GS} = 0V
		IRF521R IRF523R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF520R IRF521R	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF522R IRF523R	7.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF520R IRF521R	—	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF522R IRF523R	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 4.0A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_0 = 50Ω
t_r	Rise Time	ALL	—	35	70	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	—	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	18	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

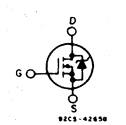


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF520R IRF521R	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF522R IRF523R	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF520R IRF521R	—	—	32	A	
		IRF522R IRF523R	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	IRF520R IRF521R	—	—	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF522R IRF523R	—	—	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_j = 25°C, L = 640μH, R_{gs} = 25Ω, I_{peak} = 9.2A. See figures 15, 16.

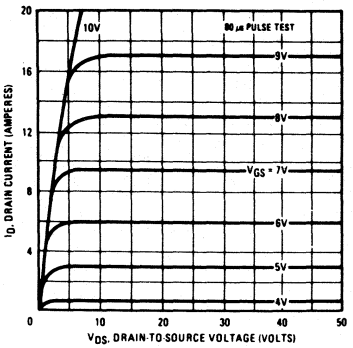


Fig. 1 – Typical Output Characteristics

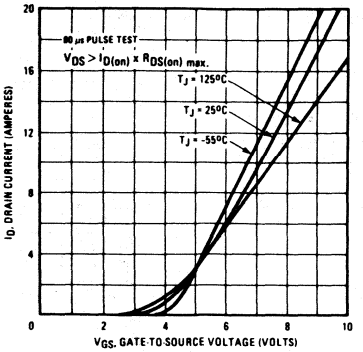


Fig. 2 – Typical Transfer Characteristics

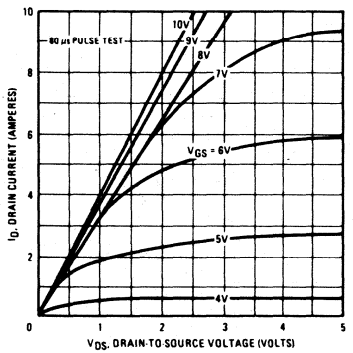


Fig. 3 – Typical Saturation Characteristics

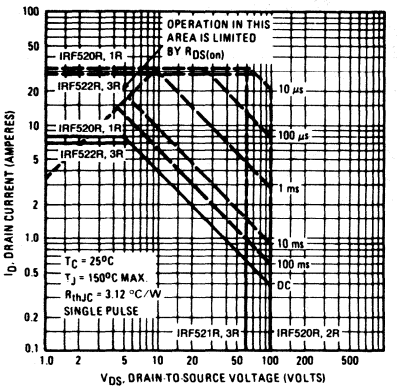


Fig. 4 – Maximum Safe Operating Area

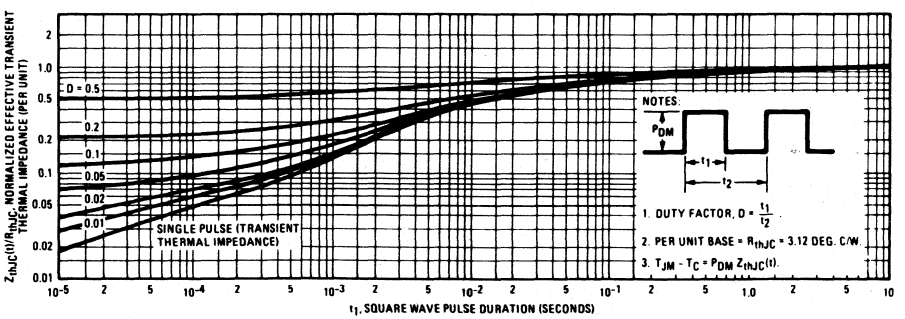


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

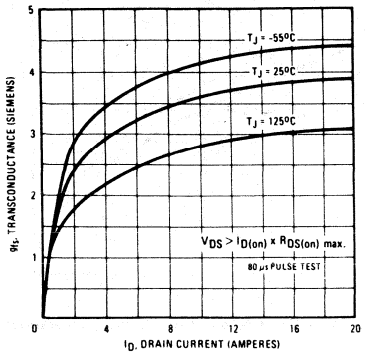


Fig. 6 – Typical Transconductance Vs. Drain Current

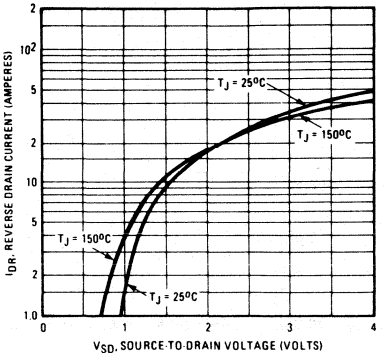


Fig. 7 – Typical Source-Drain Diode Forward Voltage

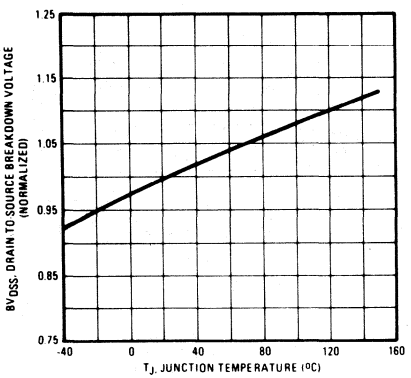


Fig. 8 – Breakdown Voltage Vs. Temperature

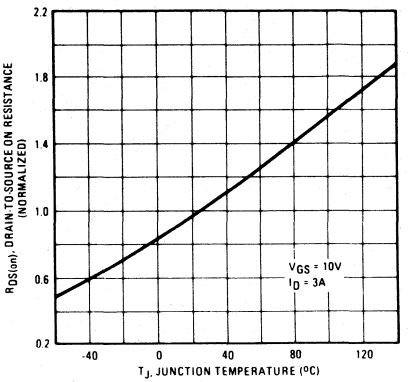


Fig. 9 – Normalized On-Resistance Vs. Temperature

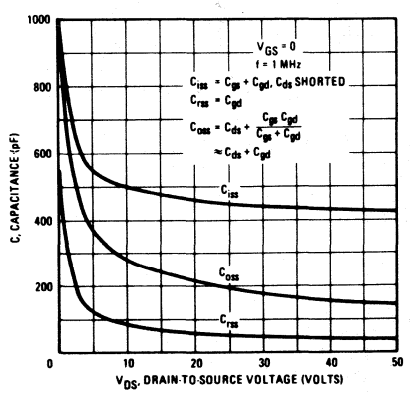


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

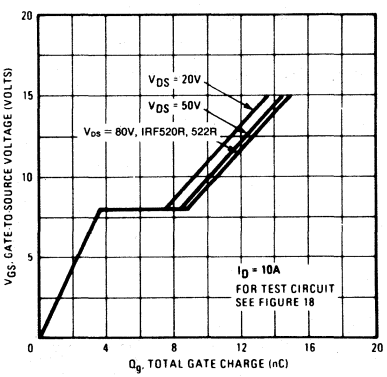


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF520R, IRF521R, IRF522R, IRF523R

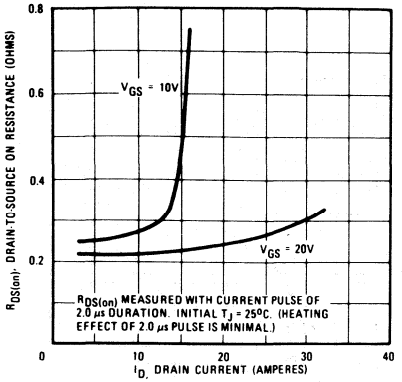


Fig. 12 – Typical On-Resistance Vs. Drain Current

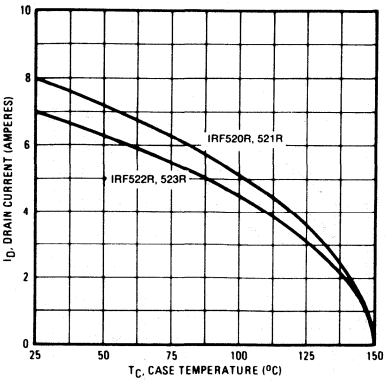


Fig. 13 – Maximum Drain Current Vs. Case Temperature

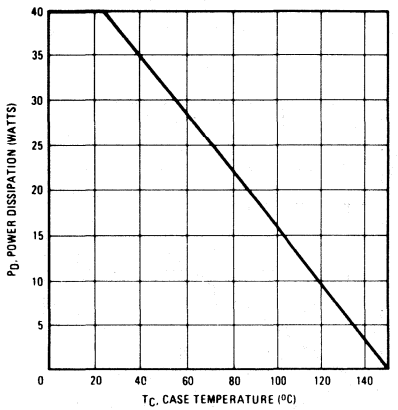


Fig. 14 – Power Vs. Temperature Derating Curve

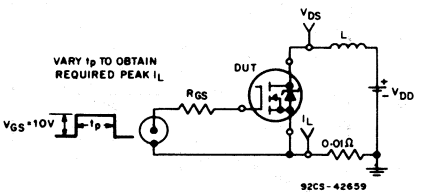


Fig. 15 — Unclamped Energy Test Circuit

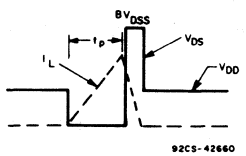


Fig. 16 — Unclamped Energy Waveforms

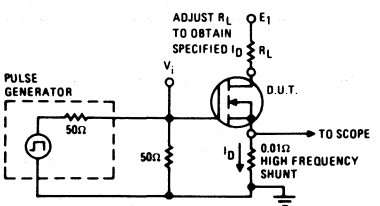


Fig. 17 – Switching Time Test Circuit

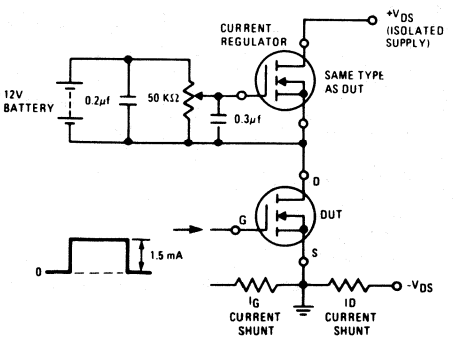


Fig. 18 – Gate Charge Test Circuit

File Number **1993**

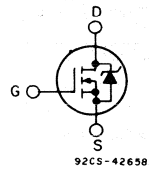
IRF530R, IRF531R, IRF532R, IRF533R

Avalanche Energy Rated N-Channel Power MOSFETs

12A and 14A, 60V-100V
$r_{DS}(on) = 0.18\Omega$ and 0.25Ω

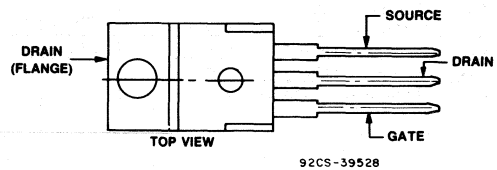
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF530R, IRF531R, IRF532R and IRF533R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

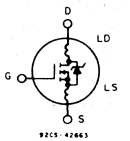
Parameter		IRF530R	IRF531R	IRF532R	IRF533R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	69				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF530R, IRF531R, IRF532R, IRF533R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF530R IRF532R	100	—	—	V	V_{GS} = 0V
		IRF531R IRF533R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF530R IRF531R	14	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF532R IRF533R	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF530R IRF531R	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF532R IRF533R	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 8.0A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} = 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	40	ns	
t_f	Fall Time	ALL	—	—	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

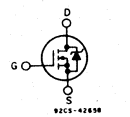


Thermal Resistance

$R_{th}JC$	Junction-to-Case	ALL	—	—	1.67	°C/W	
$R_{th}CS$	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{th}JA$	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF530R IRF531R	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF532R IRF533R	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF530R IRF531R	—	—	56	A	
		IRF532R IRF533R	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	IRF530R IRF531R	—	—	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF532R IRF533R	—	—	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_j = 25°C, L = 530μH, R_{gs} = 25Ω, I_{peak} = 14A. See figures 15, 16.

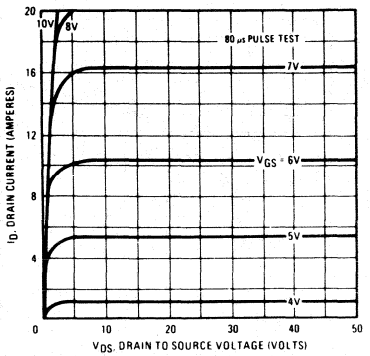


Fig. 1 – Typical Output Characteristics

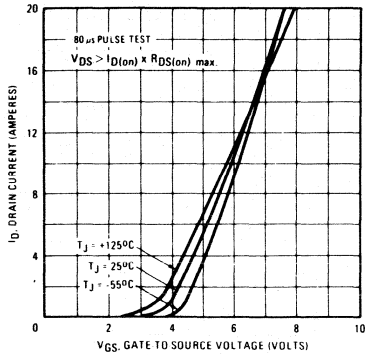


Fig. 2 – Typical Transfer Characteristics

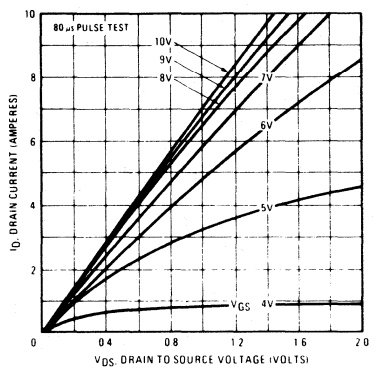


Fig. 3 – Typical Saturation Characteristics

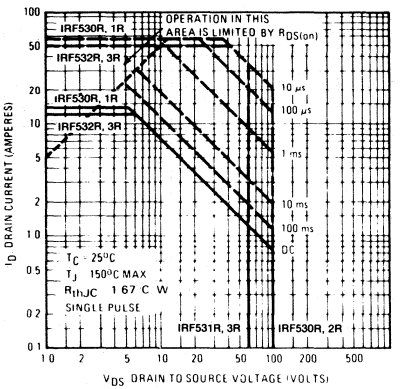


Fig. 4 – Maximum Safe Operating Area

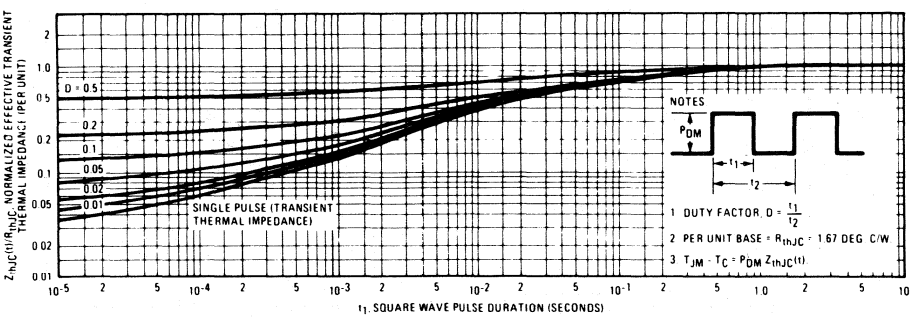


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

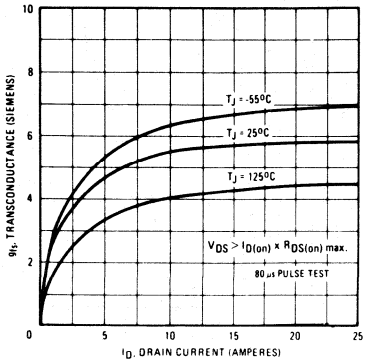


Fig. 6 – Typical Transconductance Vs. Drain Current

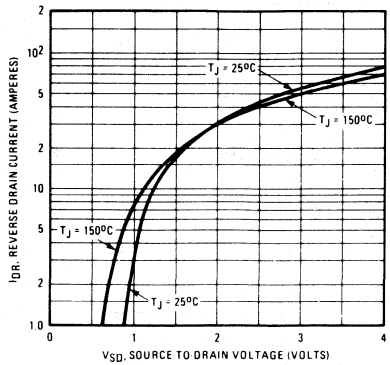


Fig. 7 – Typical Source-Drain Diode Forward Voltage

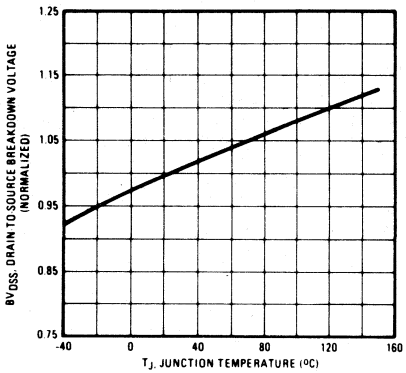


Fig. 8 – Breakdown Voltage Vs. Temperature

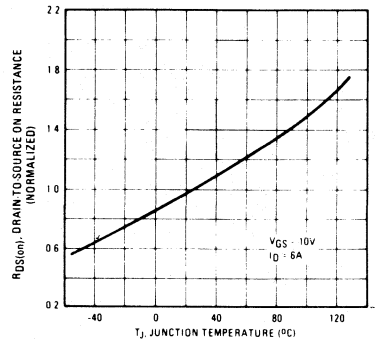


Fig. 9 – Normalized On-Resistance Vs. Temperature

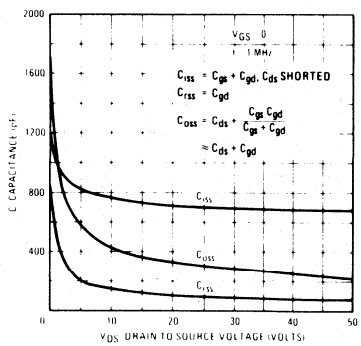


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

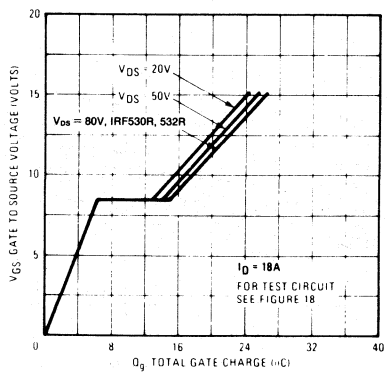


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

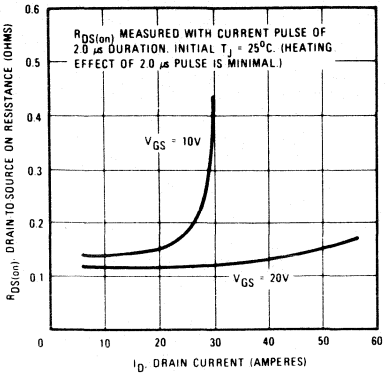


Fig. 12 – Typical On-Resistance Vs. Drain Current

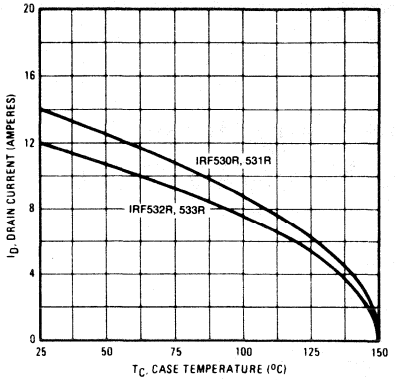


Fig. 13 – Maximum Drain Current Vs. Case Temperature

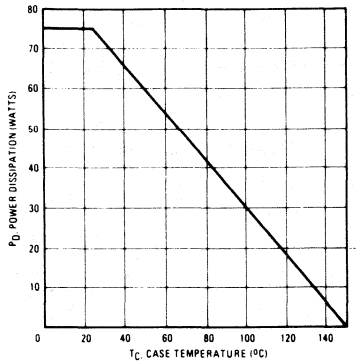


Fig. 14 – Power Vs. Temperature Derating Curve

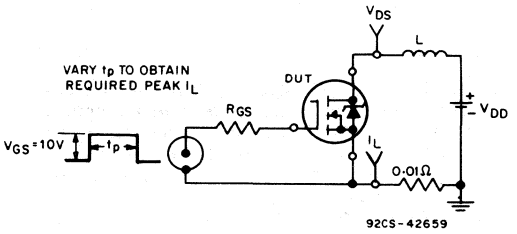


Fig. 15 — Unclamped Energy Test Circuit

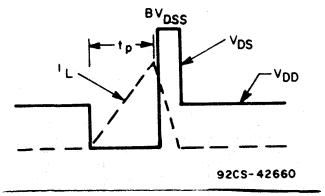


Fig. 16 — Unclamped Energy Waveforms

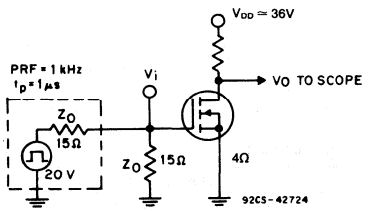


Fig. 17 – Switching Time Test Circuit

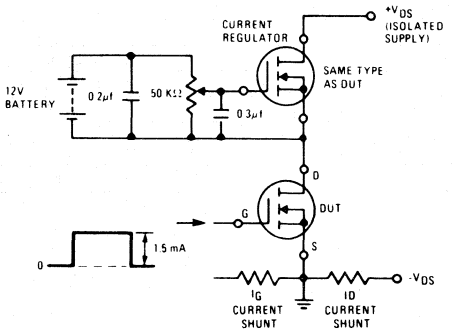


Fig. 18 – Gate Charge Test Circuit

IRF540R, IRF541R
IRF542R, IRF543R

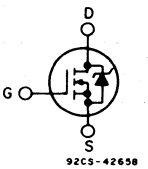
File Number **2009**

Avalanche Energy Rated N-Channel Power MOSFETs

27A and 24A, 100V-60V
$r_{DS}(on) = 0.085\Omega$ and 0.11Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

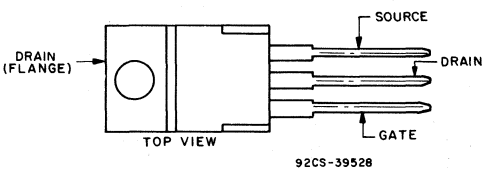


N-CHANNEL ENHANCEMENT MODE

The IRF540R, IRF541R, IRF542R and IRF543R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

Absolute Maximum Ratings

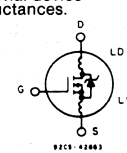
Parameter		IRF540R	IRF541R	IRF542R	IRF543R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	27	27	24	24	A
I_D @ $T_C = 100°C$	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	230				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF540R, IRF541R
IRF542R, IRF543R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF540R IRF542R	100	—	—	V	V_{GS} = 0V
		IRF541R IRF543R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF540R IRF541R	27	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF542R IRF543R	24	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF540R IRF541R	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		IRF542R IRF543R	—	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 15A
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	550	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} \simeq$ 30V, I_D = 15A, Z_0 = 4.7Ω
t_r	Rise Time	ALL	—	27	60	ns	See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	38	80	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	17	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	21	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF540R IRF541R	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF542R IRF543R	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF540R IRF541R	—	—	108	A	
		IRF542R IRF543R	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	IRF540R IRF541R	—	—	2.5	V	T_C = 25°C, I_S = 27A, V_{GS} = 0V
		IRF542R IRF543R	—	—	2.3	V	T_C = 25°C, I_S = 24A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_J = 25°C, L = 440 μH, R_{GS} = 50Ω, I_{peak} = 28A. See figures 15, 16.

IRF540R, IRF541R
IRF542R, IRF543R

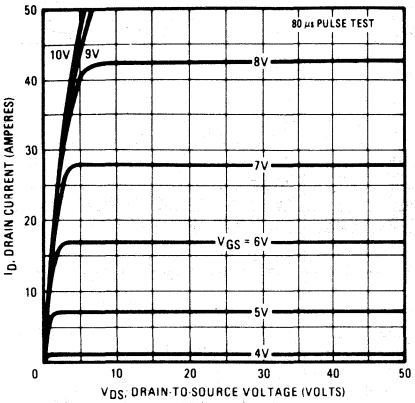


Fig. 1 – Typical Output Characteristics

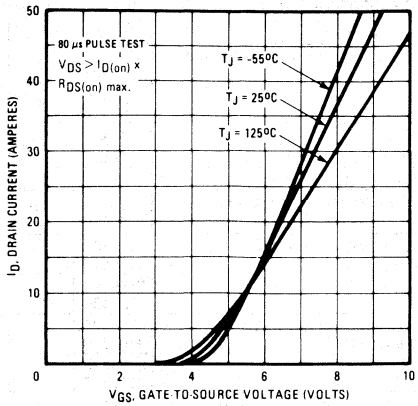


Fig. 2 – Typical Transfer Characteristics

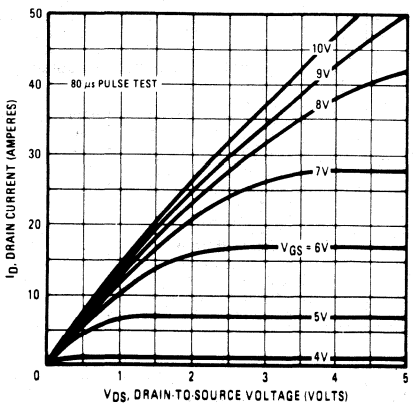


Fig. 3 – Typical Saturation Characteristics

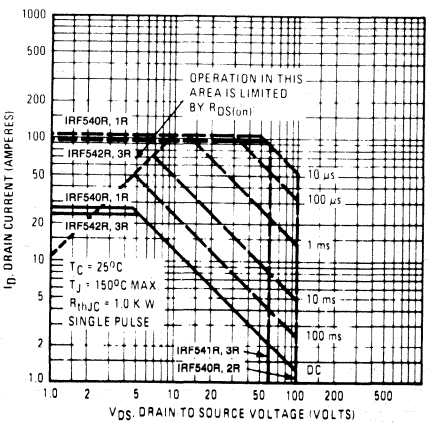


Fig. 4 – Maximum Safe Operating Area

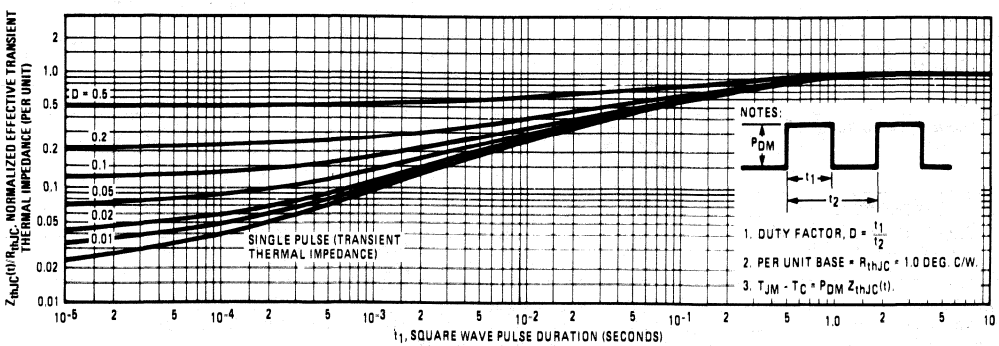


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

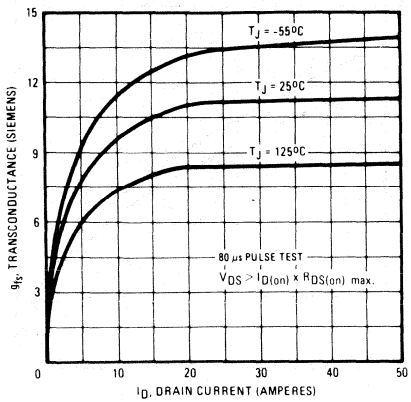


Fig. 6 – Typical Transconductance Vs. Drain Current

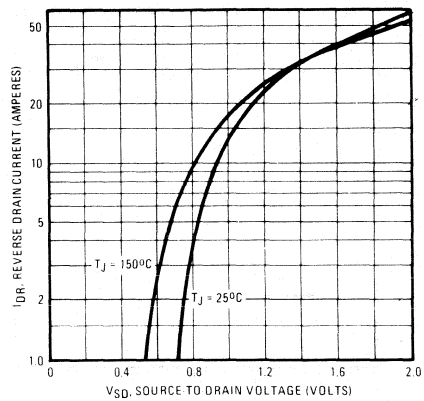


Fig. 7 – Typical Source-Drain Diode Forward Voltage

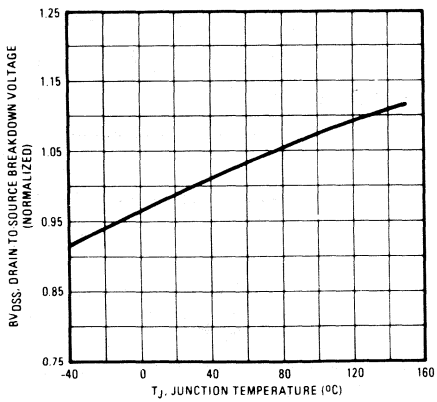


Fig. 8 – Breakdown Voltage Vs. Temperature

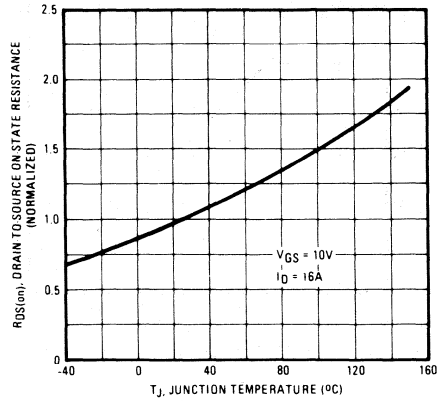


Fig. 9 – Normalized On-Resistance Vs. Temperature

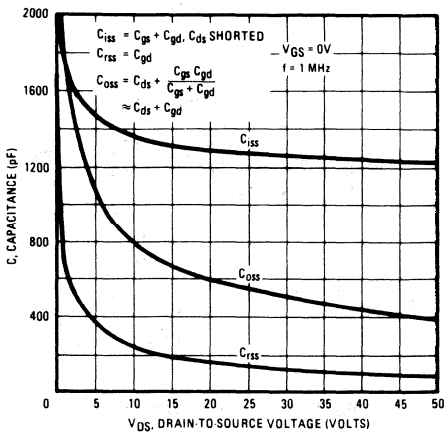


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

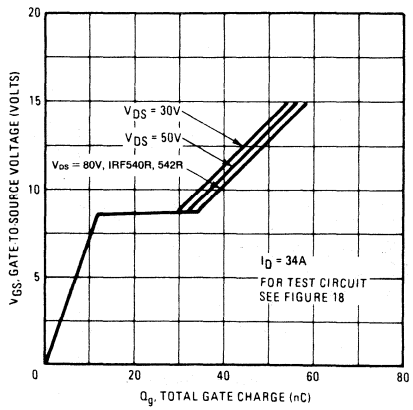


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

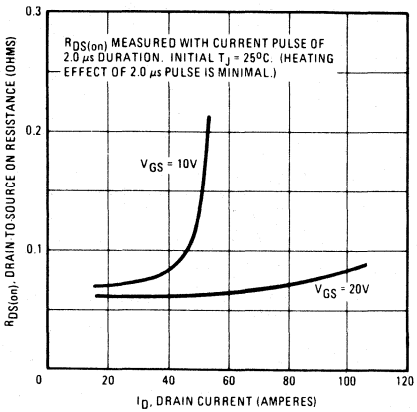


Fig. 12 — Typical On-Resistance Vs. Drain Current

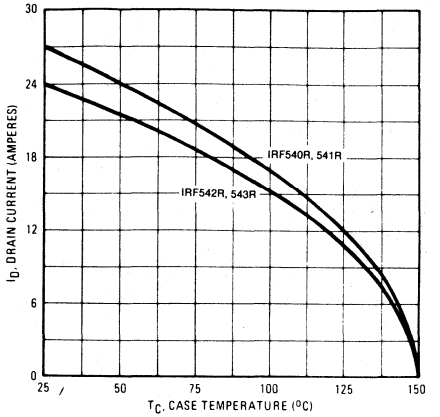


Fig. 13 — Maximum Drain Current Vs. Case Temperature

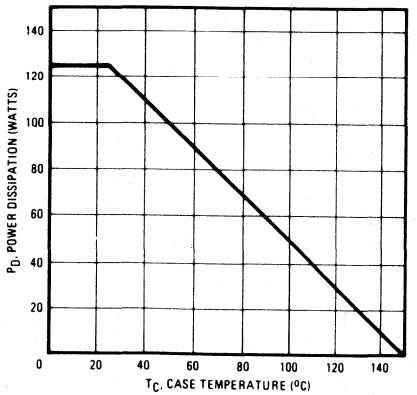


Fig. 14 — Power Vs. Temperature Derating Curve

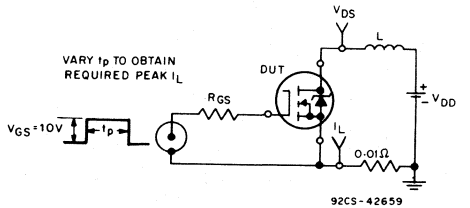


Fig. 15 — Unclamped Energy Test Circuit

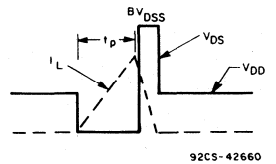


Fig. 16 — Unclamped Energy Waveforms

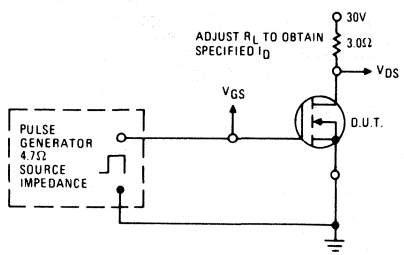


Fig. 17 — Switching Time Test Circuit

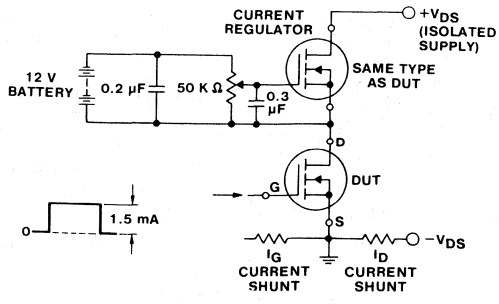


Fig. 18 — Gate Charge Test Circuit

File Number **1988**

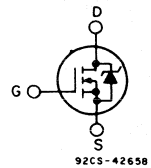
IRF610R, IRF611R, IRF612R, IRF613R

Avalanche Energy Rated N-Channel Power MOSFETs

2.0A and 2.5A, 150V-200V
$r_{DS}(on) = 1.5\Omega$ and 2.4Ω

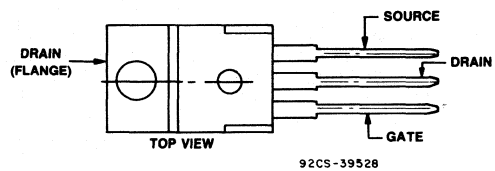
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF610R, IRF611R, IRF612R and IRF613R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

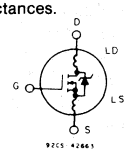
Parameter		IRF610R	IRF611R	IRF612R	IRF613R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	1.5	1.5	1.25	1.25	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	30				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF610R, IRF611R, IRF612R, IRF613R

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF610R IRF612R	200	—	—	V	$V_{GS} = 0V$
		IRF611R IRF613R	150	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRF610R IRF611R	2.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, $V_{GS} = 10V$
		IRF612R IRF613R	2.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF610R IRF611R	—	1.0	1.5	Ω	$V_{GS} = 10V$, $I_D = 1.25A$
		IRF612R IRF613R	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 1.25A$
C_{iss}	Input Capacitance	ALL	—	135	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	60	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	16	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	$V_{DD} \simeq 0.5BV_{DSS}$, $I_D = 1.25A$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	$V_{GS} = 10V$, $I_D = 3.0A$, $V_{DS} = 0.8V$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

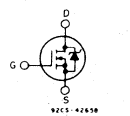


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF610R IRF611R	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF612R IRF613R	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF610R IRF611R	—	—	10	A	
		IRF612R IRF613R	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF610R IRF611R	—	—	2.0	V	$T_C = 25°C$, $I_S = 2.5A$, $V_{GS} = 0V$
		IRF612R IRF533R	—	—	1.8	V	$T_C = 25°C$, $I_S = 2.0A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	$T_J = 150°C$, $I_F = 2.5A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	$T_J = 150°C$, $I_F = 2.5A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 20V$, starting $T_J = 25°C$, L = 8.73mH, $R_{gs} = 50\Omega$, $I_{peak} = 2.5A$. See figures 15, 16.

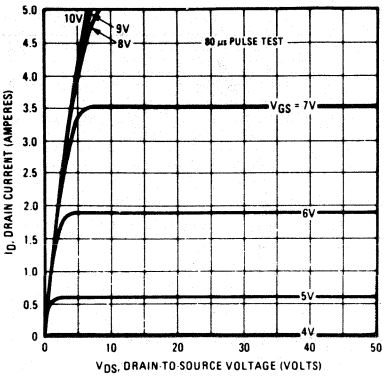


Fig. 1 – Typical Output Characteristics.

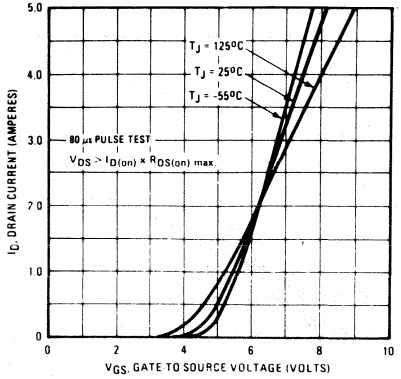


Fig. 2 – Typical Transfer Characteristics

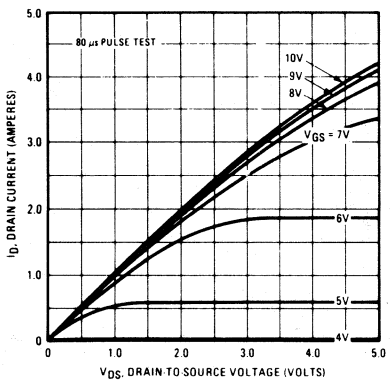


Fig. 3 – Typical Saturation Characteristics

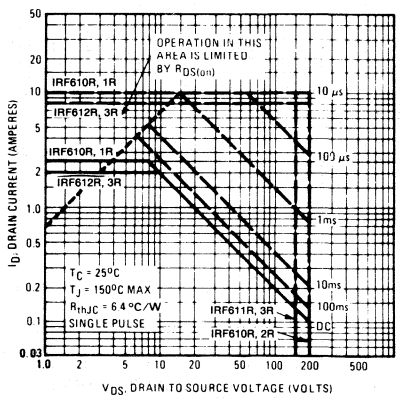


Fig. 4 – Maximum Safe Operating Area

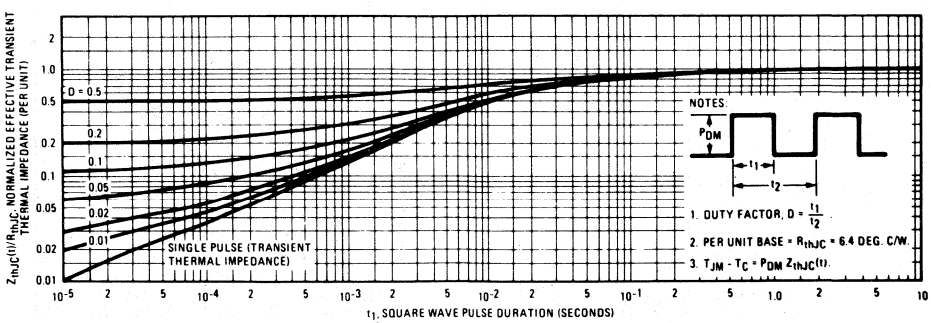


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

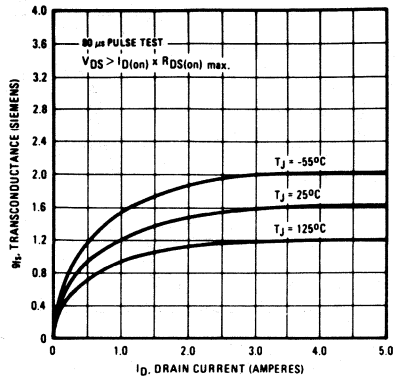


Fig. 6 – Typical Transconductance Vs. Drain Current

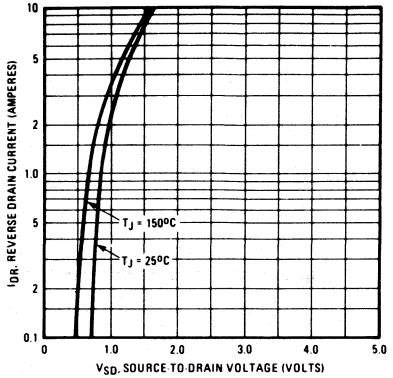


Fig. 7 – Typical Source-Drain Diode Forward Voltage

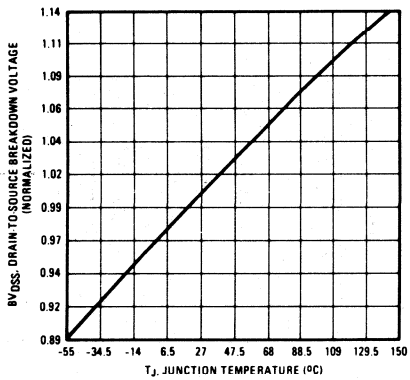


Fig. 8 – Breakdown Voltage Vs. Temperature

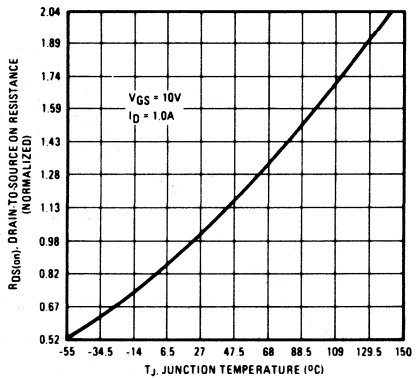


Fig. 9 – Normalized On-Resistance Vs. Temperature

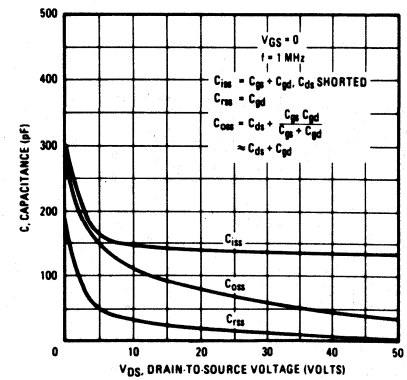


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

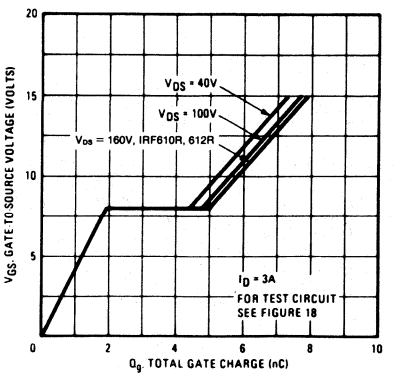


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

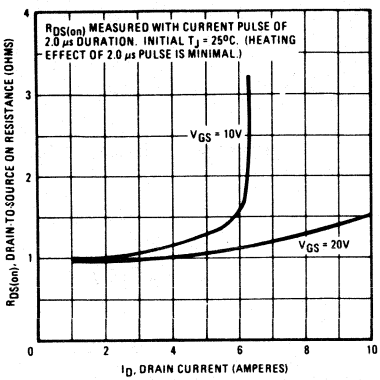


Fig. 12 – Typical On-Resistance Vs. Drain Current

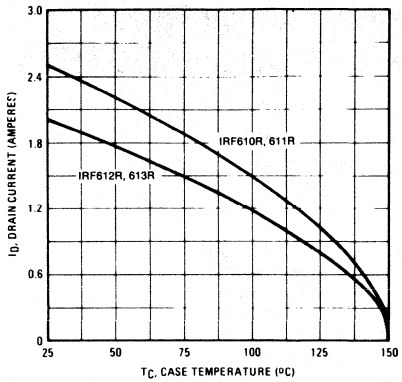


Fig. 13 – Maximum Drain Current Vs. Case Temperature

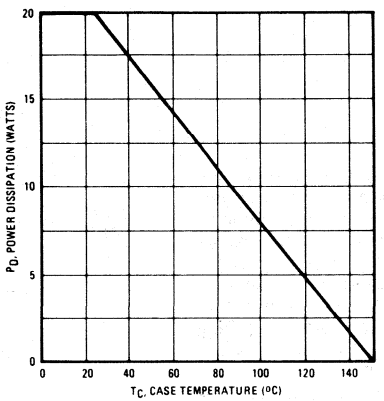


Fig. 14 – Power Vs. Temperature Derating Curve

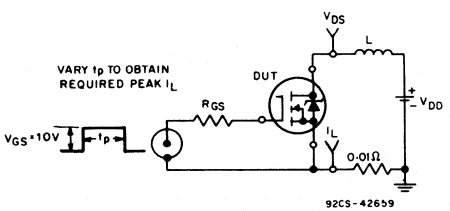


Fig. 15 — Unclamped Energy Test Circuit

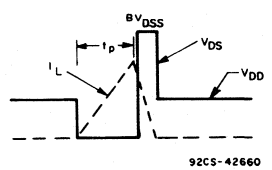


Fig. 16 — Unclamped Energy Waveforms

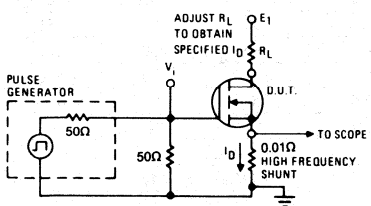


Fig. 17 – Switching Time Test Circuit

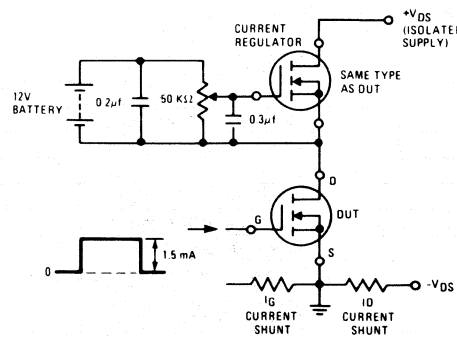


Fig. 18 – Gate Charge Test Circuit

IRF620R, IRF621R, IRF622R, IRF623R

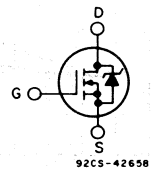
File Number **1989**

Avalanche Energy Rated N-Channel Power MOSFETs

4.0A and 5.0A, 150V-200V
$r_{DS}(on) = 0.8\Omega$ and 1.2Ω

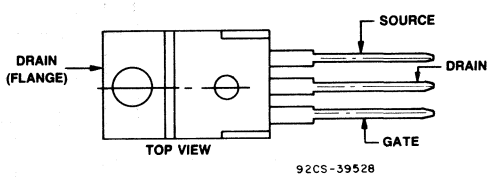
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF620R, IRF621R, IRF622R and IRF623R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

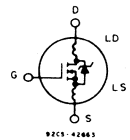
Absolute Maximum Ratings

Parameter		IRF620R	IRF621R	IRF622R	IRF623R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	85				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF620R IRF622R	200	—	—	V	V_{GS} = 0V
		IRF621R IRF623R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF620R IRF621R	5.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF622R IRF623R	4.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF620R IRF621R	—	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF622R IRF623R	—	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 2.5A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	V_{DD} = 2.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω
t_r	Rise Time	ALL	—	30	60	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	—	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

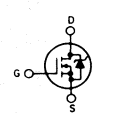


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF620R IRF621R	—	—	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF622R IRF623R	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF620R IRF621R	—	—	20	A	
		IRF622R IRF623R	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	IRF620R IRF621R	—	—	1.8	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF622R IRF623R	—	—	1.4	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 10V, starting T_j = 25°C, L = 6.18mH, R_{gs} = 50Ω, I_{peak} = 5A. See figures 15, 16.

IRF620R, IRF621R, IRF622R, IRF623R

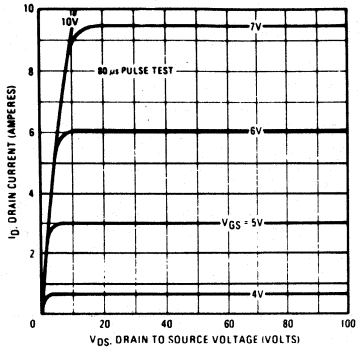


Fig. 1 – Typical Output Characteristics

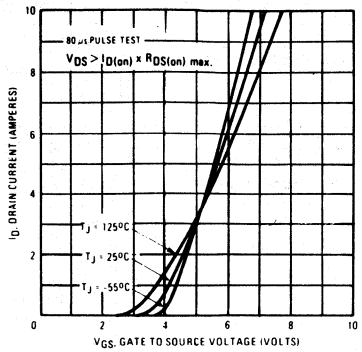


Fig. 2 – Typical Transfer Characteristics

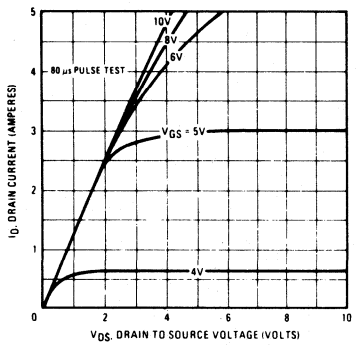


Fig. 3 – Typical Saturation Characteristics

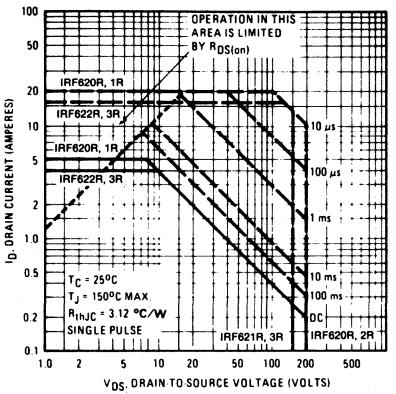


Fig. 4 – Maximum Safe Operating Area

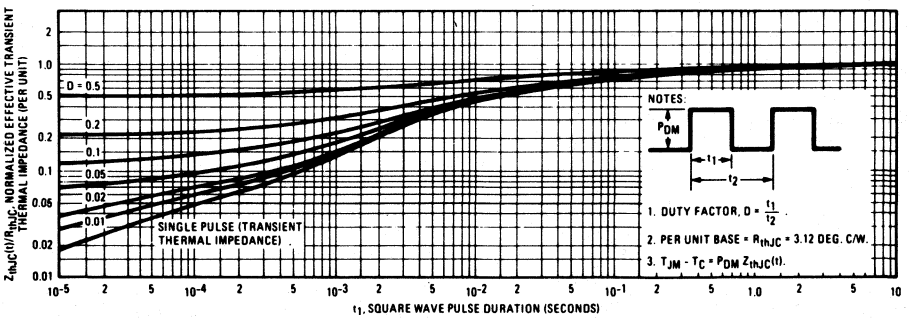


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

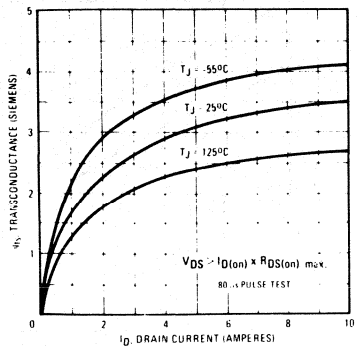


Fig. 6 – Typical Transconductance Vs. Drain Current

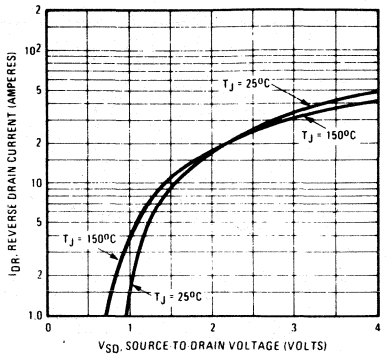


Fig. 7 – Typical Source-Drain Diode Forward Voltage

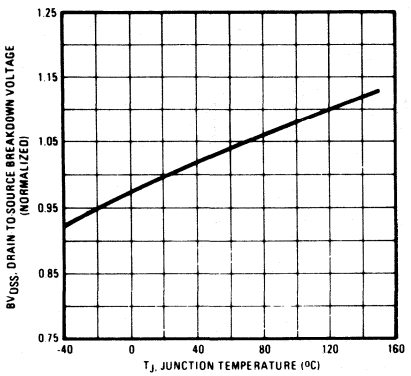


Fig. 8 – Breakdown Voltage Vs. Temperature

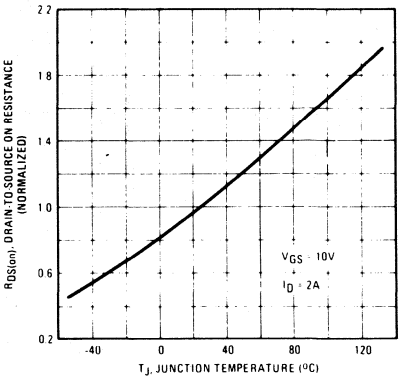


Fig. 9 – Normalized On-Resistance Vs. Temperature

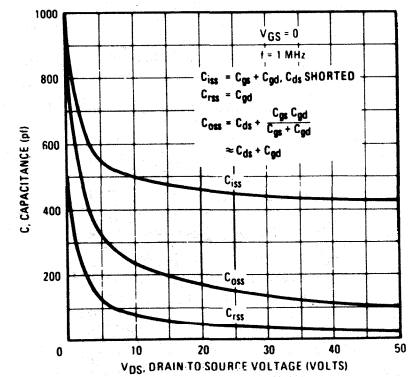


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

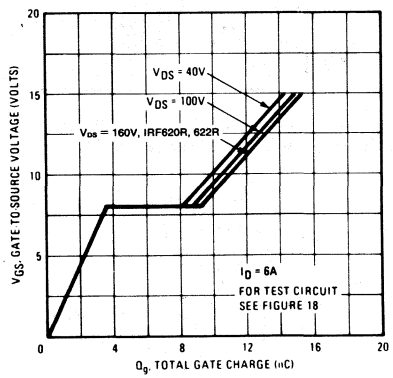


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

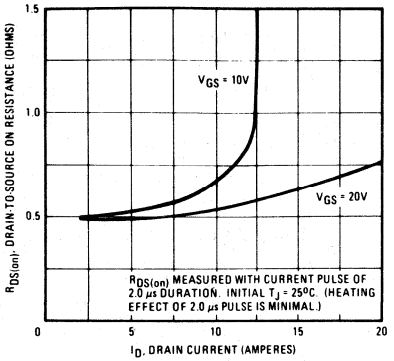


Fig. 12 — Typical On-Resistance Vs. Drain Current

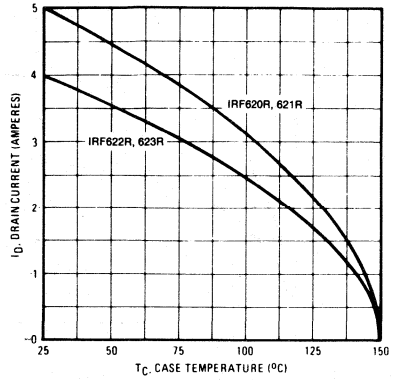


Fig. 13 — Maximum Drain Current Vs. Case Temperature

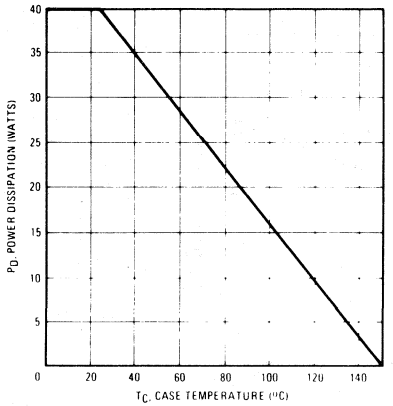


Fig. 14 — Power Vs. Temperature Derating Curve

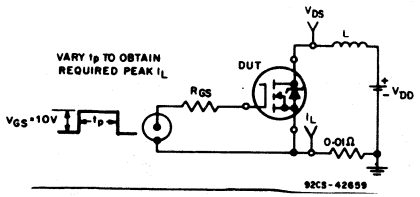


Fig. 15 — Unclamped Energy Test Circuit

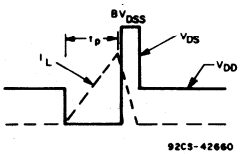


Fig. 16 — Unclamped Energy Waveforms

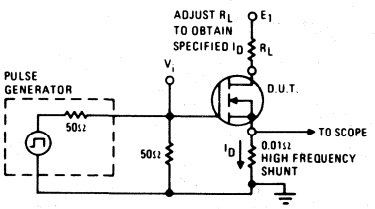


Fig. 17 — Switching Time Test Circuit

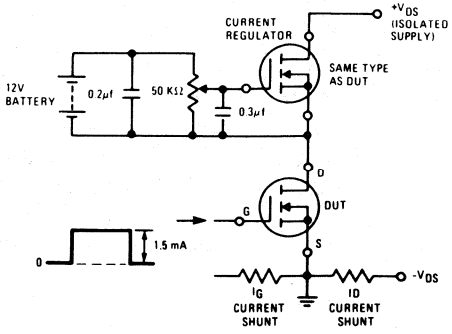


Fig. 18 — Gate Charge Test Circuit

File Number **2167**

IRF624, IRF625, IRF626, IRF627

Avalanche Energy Rated N-Channel Power MOSFETs

3.8A, and 3.3A, 275, 250V
r_{DS} (on) = 1.1Ω, and 1.5Ω

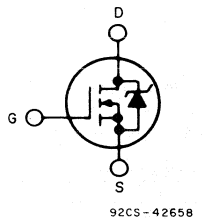
Features:

- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *250/275V DC rating - 120V AC line system operation*

The IRF624, IRF625, IRF626, and IRF627 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

All types are supplied in the JEDEC TO-220AB plastic package.

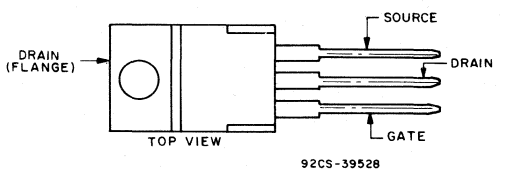
N-CHANNEL ENHANCEMENT MODE



92CS-42658

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

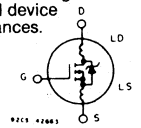
Parameter		IRF624	IRF625	IRF626	IRF627	Units
V_{DS}	Drain - Source Voltage ①	250	250	275	275	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	250	250	275	275	V
I_D @ T_C = 25°C	Continuous Drain Current	3.8	3.3	3.8	3.3	A
I_D @ T_C = 100°C	Continuous Drain Current	2.4	2.1	2.4	2.1	A
I_{DM}	Pulsed Drain Current ③	15	13	15	13	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40				W
	Linear Derating Factor	0.32				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	120				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]				°C

IRF624, IRF625, IRF626, IRF627

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRF626 IRF627	275	—	—	V	V_{GS} = 0V
	IRF624 IRF625	250	—	—	V	I_D = 250μA
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = 20V
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$ On-State Drain Current ②	IRF624 IRF626	3.8	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, V_{GS} = 10V
	IRF625 IRF627	3.3	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF624 IRF626	—	0.8	1.1	Ω	V_{GS} = 10V, I_D = 2.1A
	IRF625 IRF627	—	1.05	1.5	Ω	
g_{fs} Forward Transconductance ②	ALL	1.4	2.1	—	S(Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 1.9A
C_{iss} Input Capacitance	ALL	—	340	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss} Output Capacitance	ALL	—	110	—	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	32	—	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	11	17	ns	V_{DD} = 125V, I_D = 3.8A, R_g = 18Ω
t_r Rise Time	ALL	—	24	36	ns	See Fig. 16 R_L = 32Ω
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	21	40	ns	(MOSFET switching times are essentially
t_f Fall Time	ALL	—	13	20	ns	independent of operating temperature.)
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	15	22	nC	V_{GS} = 10V, I_D = 3.8A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	4.0	6.0	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	7.2	11	nC	
L_D Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

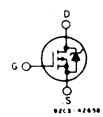


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF624 IRF626	—	—	3.8	A	Modified MOSFET symbol showing the integral reverse◆P-N junction rectifier.
		IRF625 IRF627	—	—	3.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF624 IRF626	—	—	15	A	
		IRF625 IRF627	—	—	13	A	
V_{SD}	Diode Forward Voltage ②	ALL	—	—	1.8	V	T_C = 25°C, I_S = 3.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	81	180	370	ns	T_J = 150°C, I_F = 3.8A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	0.44	0.93	2.0	μC	T_J = 150°C, I_F = 3.8A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_j = 25°C, L = 13.6MH, R_{gs} = 25Ω, I_{peak} = 3.8A. See figures 14, 15.

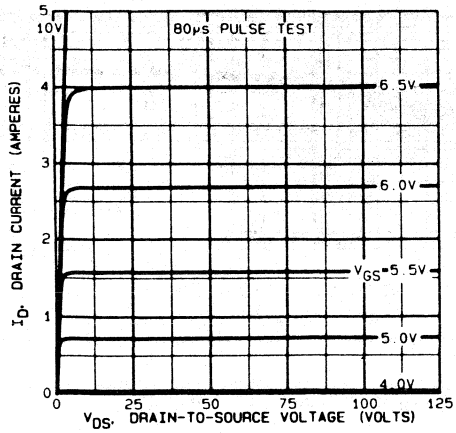


Fig. 1 — Typical Output Characteristics

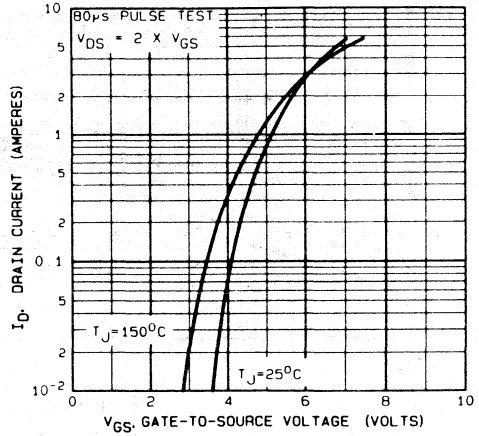


Fig. 2 — Typical Transfer Characteristics

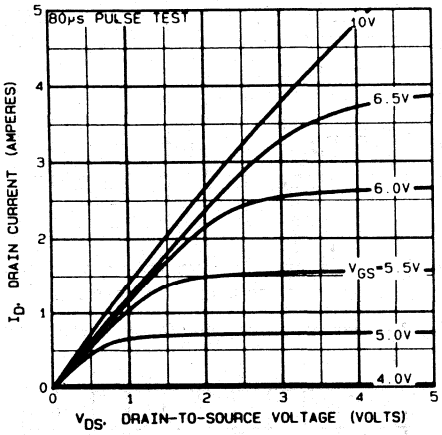


Fig. 3 — Typical Saturation Characteristics

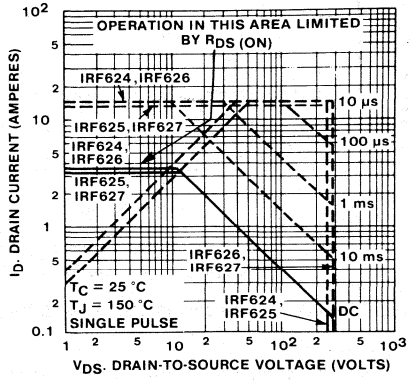


Fig. 4 — Maximum Safe Operating Area

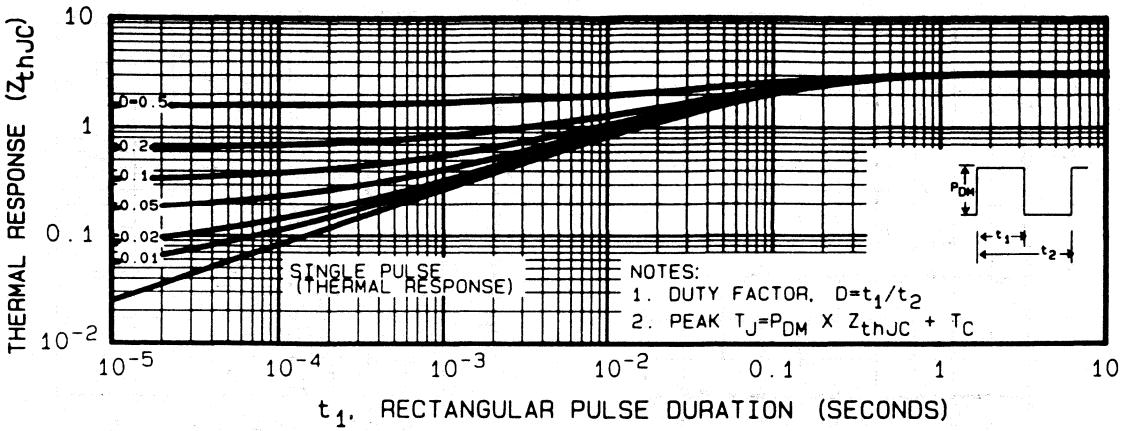


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

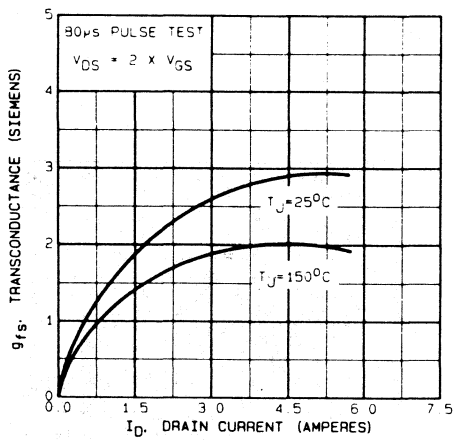


Fig. 6 — Typical Transconductance Vs. Drain Current

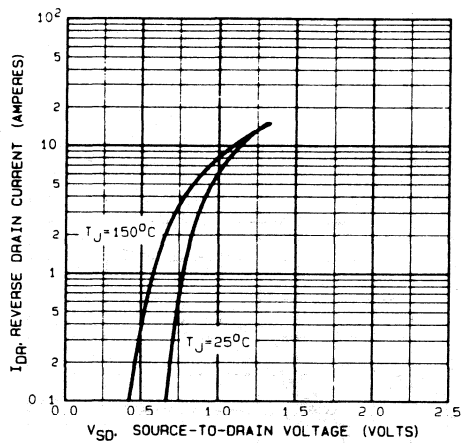


Fig. 7 — Typical Source-Drain Diode Forward Voltage

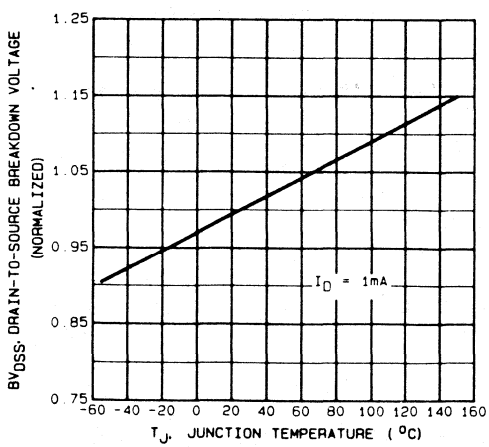


Fig. 8 — Breakdown Voltage Vs. Temperature

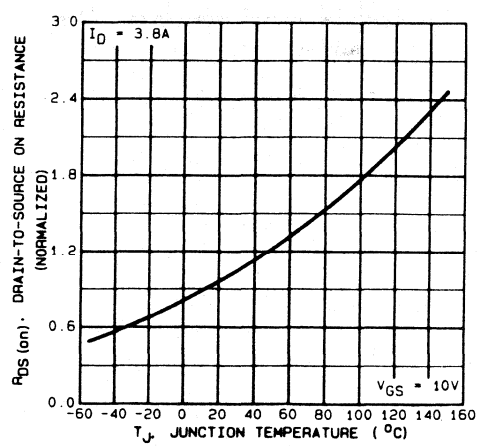


Fig. 9 — Normalized On-Resistance Vs. Temperature

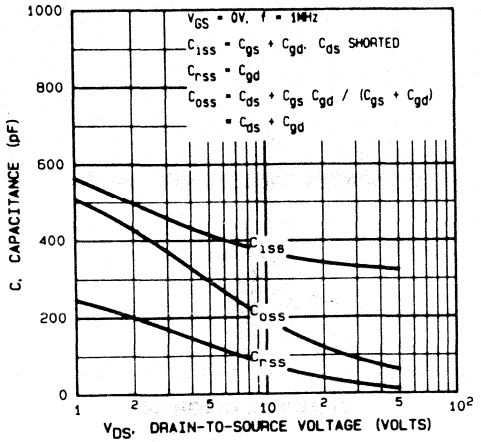


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

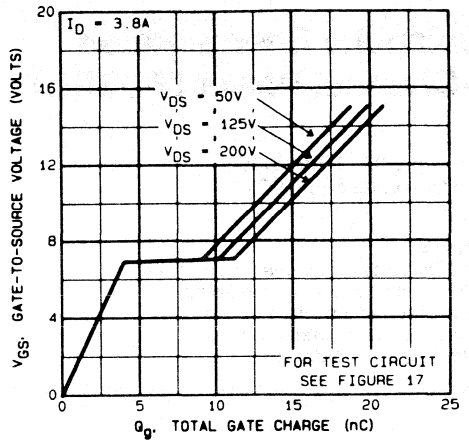


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

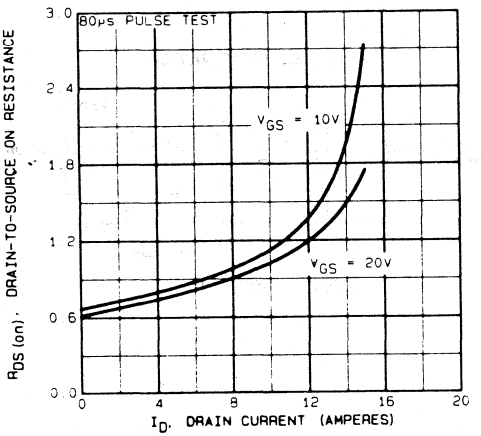


Fig. 12 — Typical On-Resistance Vs. Drain Current

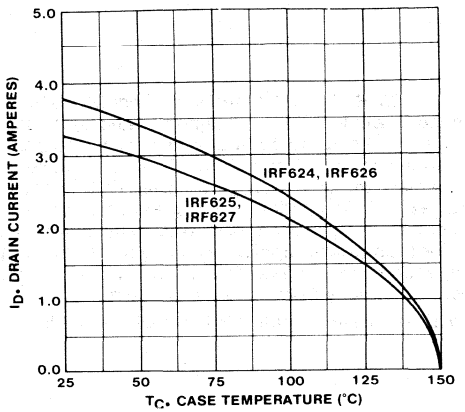


Fig. 13 — Maximum Drain Current Vs. Case Temperature

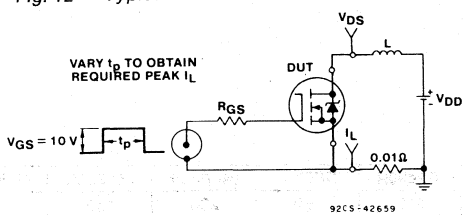


Fig. 14 — Unclamped Energy Test Circuit

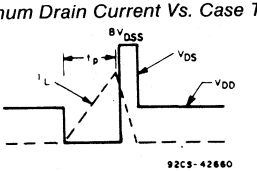


Fig. 15 — Unclamped Energy Waveforms

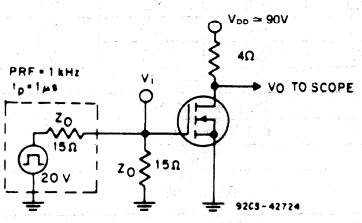


Fig. 16 — Switching Time Test Circuit

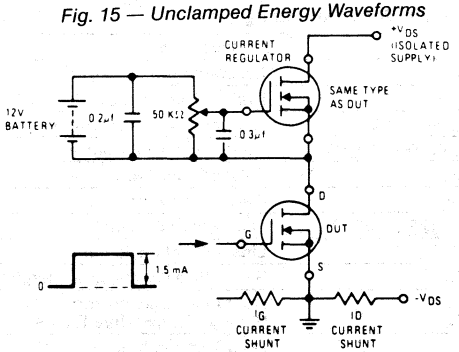


Fig. 17 — Gate Charge Test Circuit

IRF630R, IRF631R, IRF632R, IRF633R

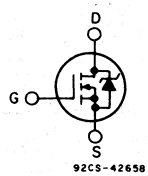
File Number **1990**

Avalanche Energy Rated N-Channel Power MOSFETs

8.0A and 9.0A, 150V-200V
$r_{DS}(on) = 0.4\Omega$ and 0.6Ω

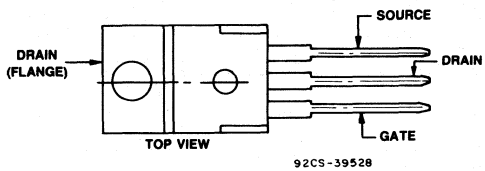
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF630R, IRF631R, IRF632R and IRF633R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

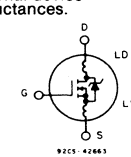
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

Parameter		IRF630R	IRF631R	IRF632R	IRF633R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	150				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF630R IRF632R	200	—	—	V	V_{GS} = 0V
		IRF631R IRF633R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF630R IRF631R	9.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF632R IRF633R	8.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF630R IRF631R	—	0.25	0.1	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF632R IRF633R	—	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 5.0A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	250	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} = 90V, I_D = 5.0A, Z_0 = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	50	ns	
t_f	Fall Time	ALL	—	—	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	10	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

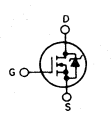


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF630R IRF631R	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF632R IRF633R	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF630R IRF631R	—	—	36	A	
		IRF632R IRF633R	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	IRF630R IRF631R	—	—	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF632R IRF633R	—	—	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 20V, starting T_j = 25°C, L = 3.37mH, R_{gs} = 50Ω, I_{peak} = 9A. See figures 15, 16.

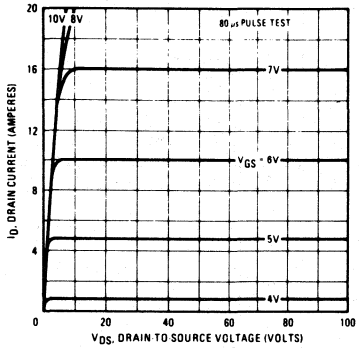


Fig. 1 – Typical Output Characteristics

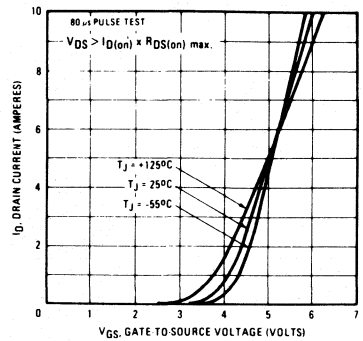


Fig. 2 – Typical Transfer Characteristics

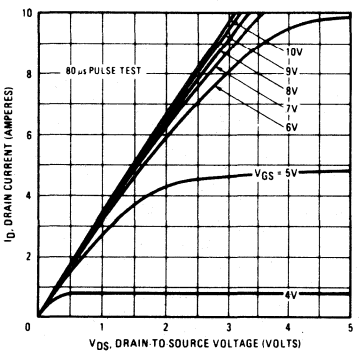


Fig. 3 – Typical Saturation Characteristics

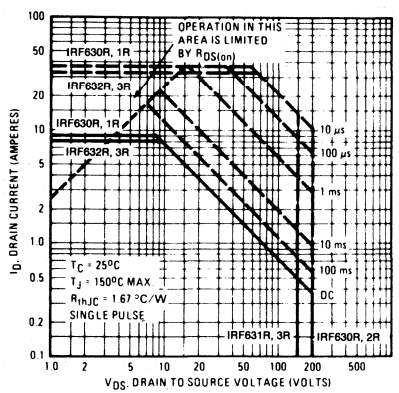


Fig. 4 – Maximum Safe Operating Area

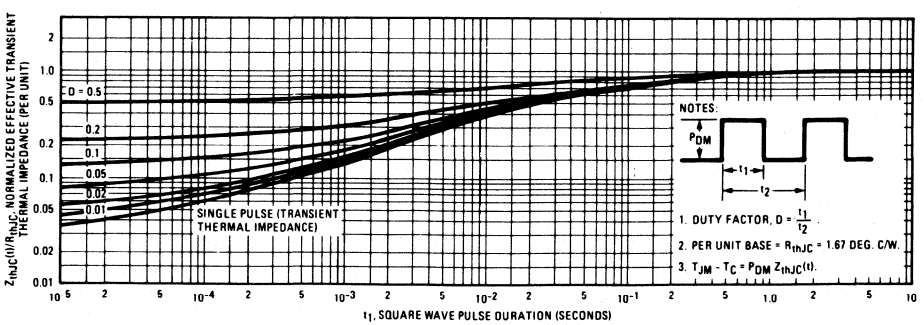


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

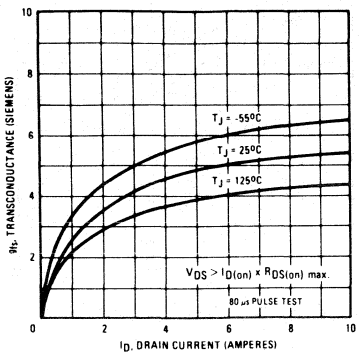


Fig. 6 – Typical Transconductance Vs. Drain Current

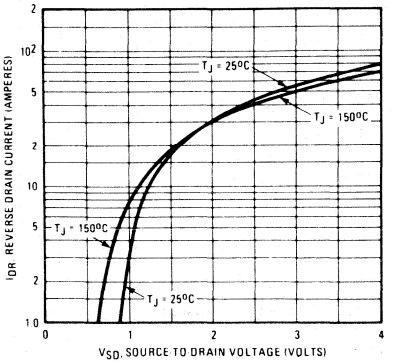


Fig. 7 – Typical Source-Drain Diode Forward Voltage

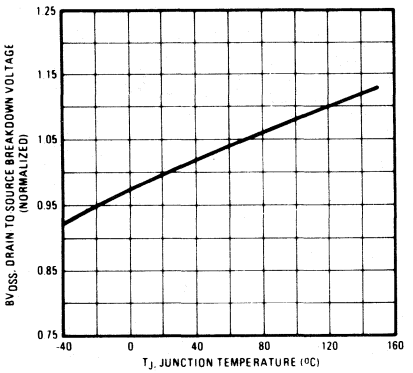


Fig. 8 – Breakdown Voltage Vs. Temperature

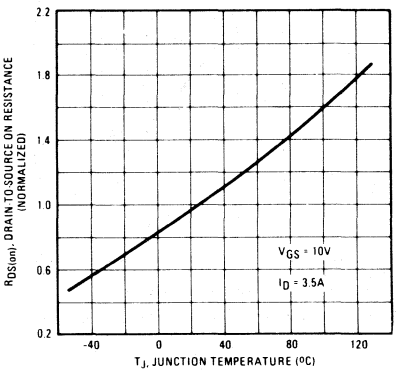


Fig. 9 – Normalized On-Resistance Vs. Temperature

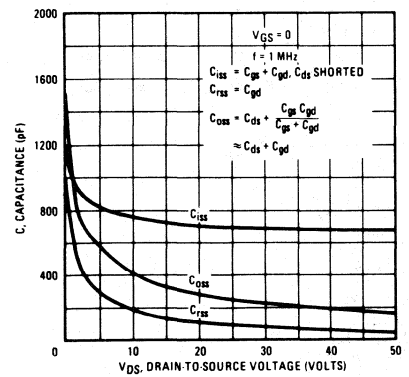


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

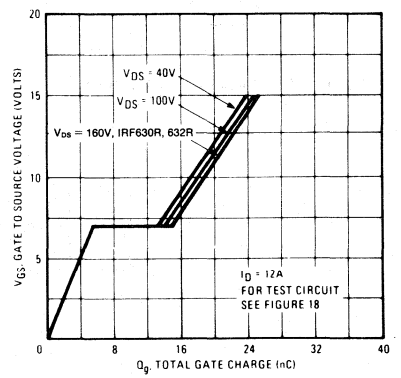


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

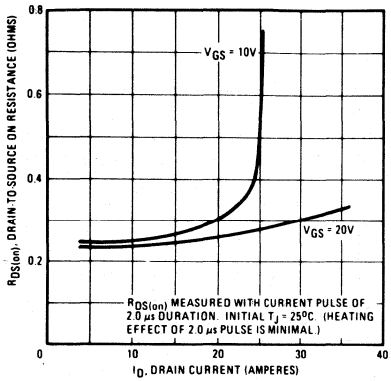


Fig. 12 – Typical On-Resistance Vs. Drain Current

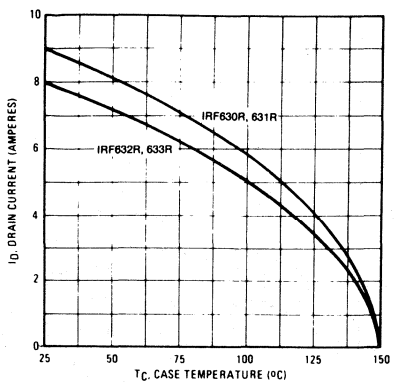


Fig. 13 – Maximum Drain Current Vs. Case Temperature

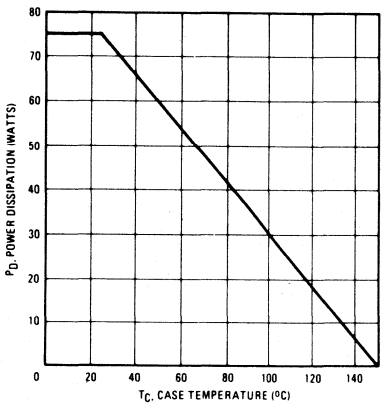


Fig. 14 – Power Vs. Temperature Derating Curve

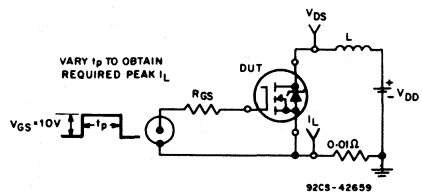


Fig. 15 — Unclamped Energy Test Circuit

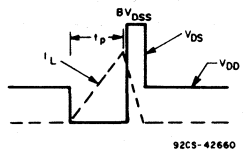


Fig. 16 — Unclamped Energy Waveforms

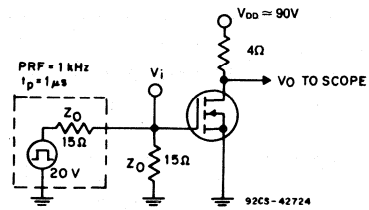


Fig. 17 – Switching Time Test Circuit

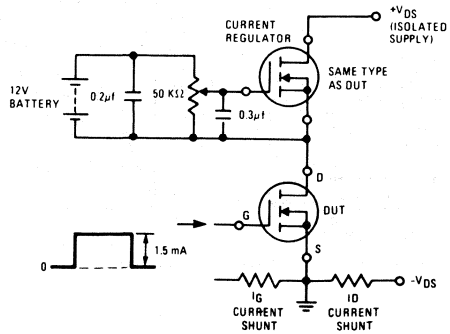


Fig. 18 – Gate Charge Test Circuit

File Number **2168**

IRF634, IRF635, IRF636, IRF637

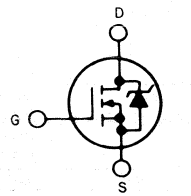
Avalanche Energy Rated N-Channel Power MOSFETs

N-CHANNEL ENHANCEMENT MODE

8.1A, and 6.5A, 275, 250V
r_{DS} (on) = 0.45Ω, 0.68Ω

Features:

- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250V rating - 120V AC line system operation*



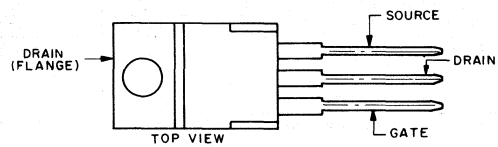
92CS-42658

TERMINAL DIAGRAM

The IRF634, IRF635, IRF636, and IRF637 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

All types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

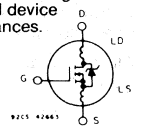
Parameter		IRF634	IRF635	IRF636	IRF637	Units
V_{DS}	Drain - Source Voltage ①	250	250	275	275	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	250	250	275	275	V
I_D @ T_C = 25°C	Continuous Drain Current	8.1	6.5	8.1	6.5	A
I_D @ T_C = 100°C	Continuous Drain Current	5.1	4.1	5.1	4.1	A
I_{DM}	Pulsed Drain Current ③	32	26	32	26	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75				W
	Linear Derating Factor	0.6				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	180				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]				°C

IRF634, IRF635
IRF636, IRF637

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRF636 IRF637	275	—	—	V	V_{GS} = 0V
	IRF634 IRF635	250	—	—	V	I_D = 250μA
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = 20V
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$ On-State Drain Current ②	IRF634 IRF636	8.1	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, V_{GS} = 10V
	IRF635 IRF637	6.5	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF634 IRF636	—	0.32	0.45	Ω	V_{GS} = 10V, I_D = 4.1A
	IRF635 IRF637	—	0.48	0.68	Ω	
g_{fs} Forward Transconductance ②	ALL	2.9	4.3	—	S(Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 4.1
C_{iss} Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss} Output Capacitance	ALL	—	180	—	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	52	—	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	9.1	14	ns	V_{DD} = 90V, I_D = 5.0A, Z_D = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	—	23	35	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	31	47	ns	
t_f Fall Time	ALL	—	19	29	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	24	35	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	5.1	7.7	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	12	18	nC	
L_D Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS} Case-to-Sink	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRF634 IRF636	—	—	8.1	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF635 IRF637	—	—	6.5	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRF634 IRF636	—	—	32	A	
	IRF635 IRF637	—	—	26	A	
V_{SD} Diode Forward Voltage ②	ALL	—	—	2.0	V	T_C = 25°C, I_S = 8.1A, V_{GS} = 0V
t_{rr} Reverse Recovery Time	ALL	92	180	390	ns	T_J = 150°C, I_F = 8.1A, dI_F/dt = 100A/μs
Q_{RR} Reverse Recovered Charge	ALL	0.63	1.3	2.7	μC	T_J = 150°C, I_F = 8.1A, dI_F/dt = 100A/μs
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_j = 25°C, L = 4.5MH, R_{gs} = 25Ω, I_{peak} = 8.1A. See figures 14, 15.

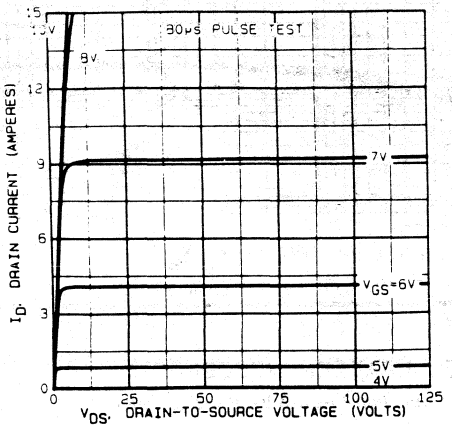


Fig. 1 — Typical Output Characteristics

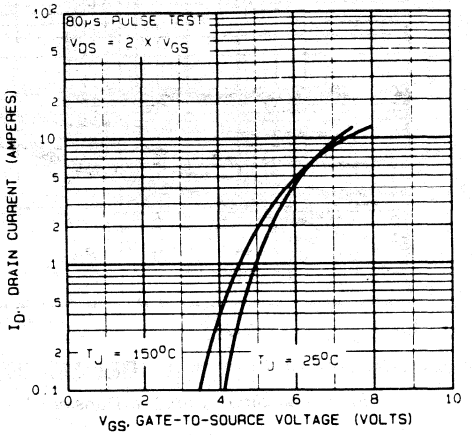


Fig. 2 — Typical Transfer Characteristics

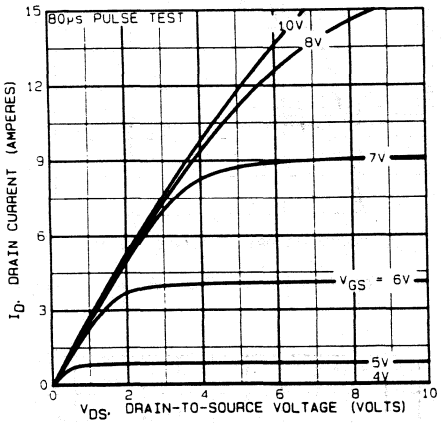


Fig. 3 — Typical Saturation Characteristics

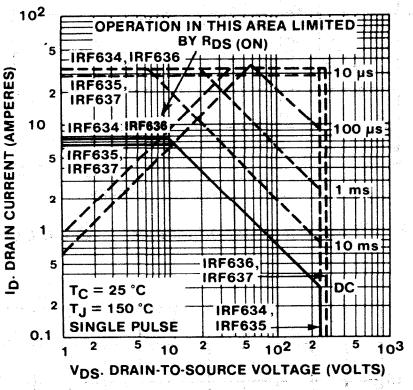


Fig. 4 — Maximum Safe Operating Area

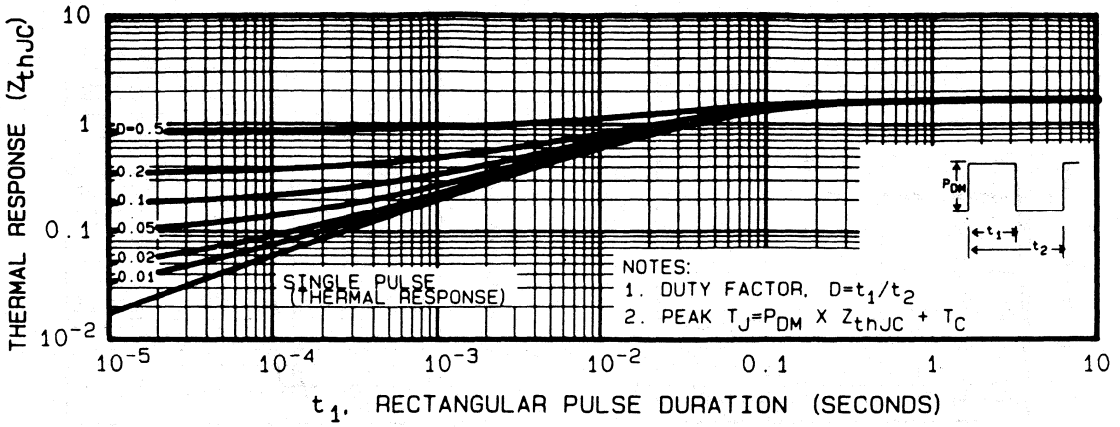


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

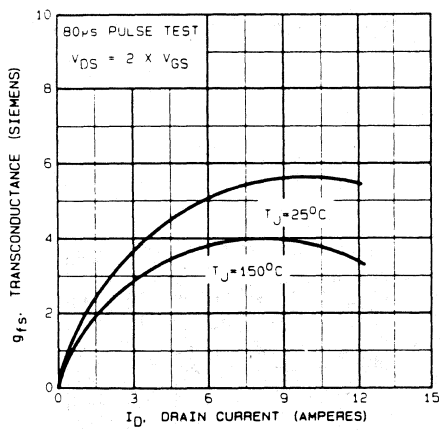


Fig. 6 — Typical Transconductance Vs. Drain Current

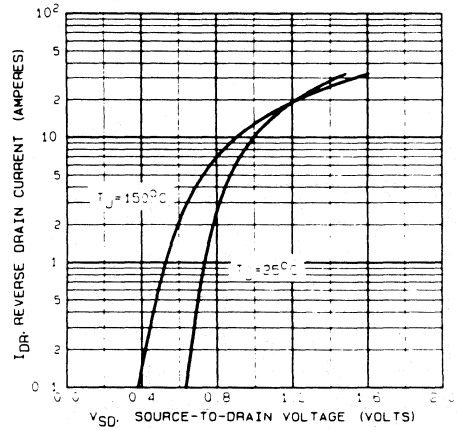


Fig. 7 — Typical Source-Drain Diode Forward Voltage

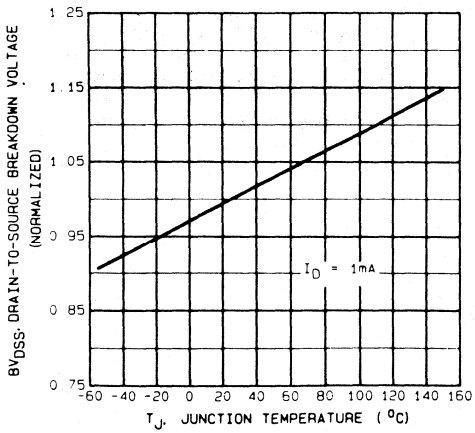


Fig. 8 — Breakdown Voltage Vs. Temperature

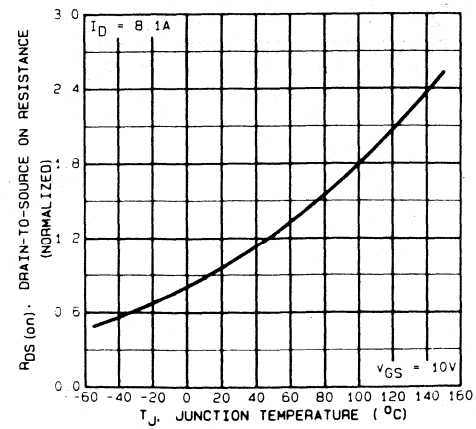


Fig. 9 — Normalized On-Resistance Vs. Temperature

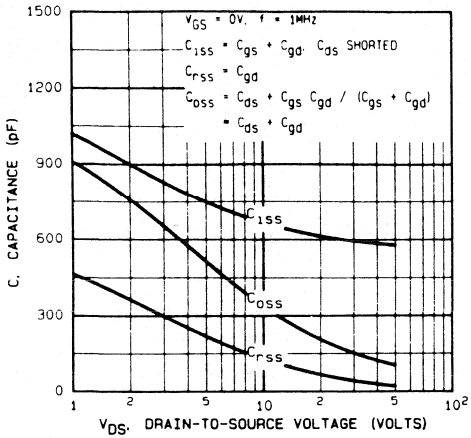


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

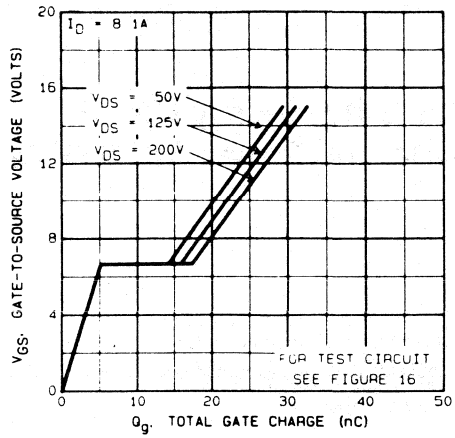


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

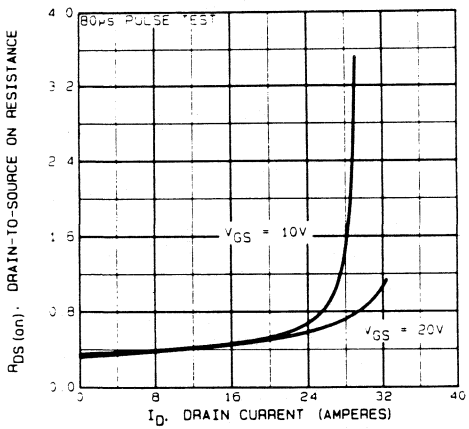


Fig. 12 — Typical On-Resistance Vs. Drain Current

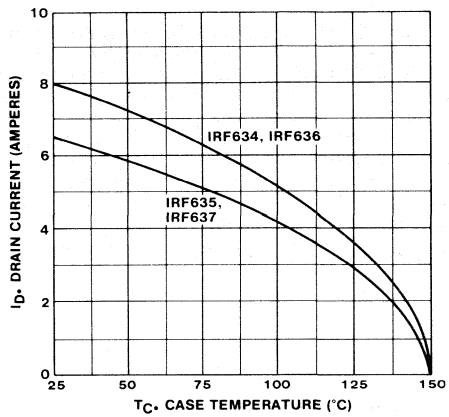


Fig. 13 — Maximum Drain Current Vs. Case Temperature

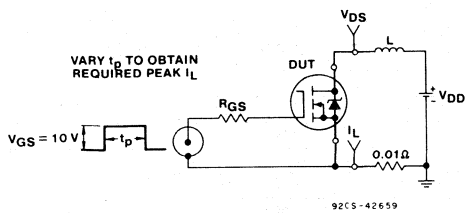


Fig. 14 — Unclamped Energy Test Circuit

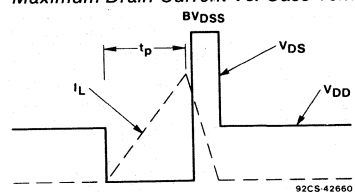


Fig. 15 — Unclamped Energy Waveforms

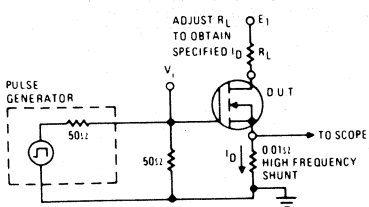


Fig. 16 — Switching Time Test Circuit

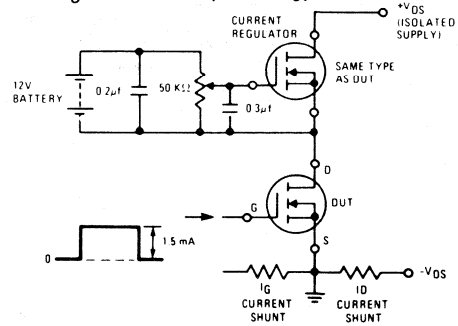


Fig. 17 — Gate Charge Test Circuit

IRF640R, IRF641R, IRF642R, IRF643R

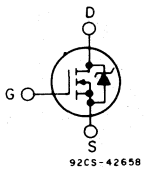
File Number **2010**

Avalanche Energy Rated N-Channel Power MOSFETs

16A and 18A, 200V, 150V
$r_{DS}(on) = 0.18\Omega$ and 0.22Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

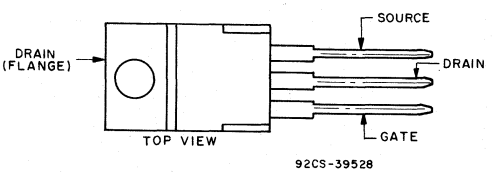


TERMINAL DIAGRAM

The IRF640R, IRF641R, IRF642R and IRF643R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

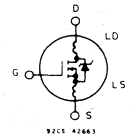
Absolute Maximum Ratings

Parameter		IRF640R	IRF641R	IRF642R	IRF643R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	580				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF640R IRF642R	200	—	—	V	V_{GS} = 0V
		IRF641R IRF643R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF640R IRF641R	18	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF642R IRF643R	16	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF640R IRF641R	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRF642R IRF643R	—	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 10A
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	500	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} \simeq$ 75V, I_D = 10A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	40	80	ns	
t_f	Fall Time	ALL	—	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit: (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	16	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	27	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

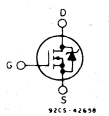


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF640R IRF641R	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF642R IRF643R	—	—	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF640R IRF641R	—	—	72	A	
		IRF642R IRF643R	—	—	64	A	
V_{SD}	Diode Forward Voltage ②	IRF640R IRF641R	—	—	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRF642R IRF643R	—	—	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.1	—	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 2.7 mH, R_{gs} = 50Ω, I_{peak} = 18A. See figures 15, 16.

IRF640R, IRF641R, IRF642R, IRF643R

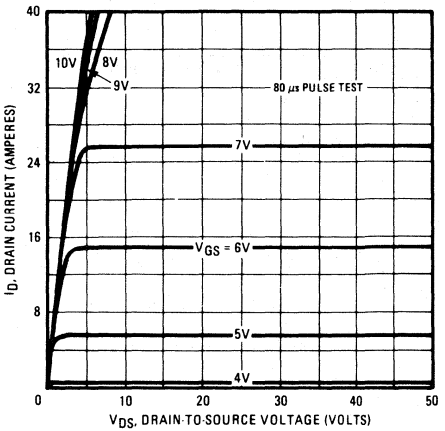


Fig. 1 — Typical Output Characteristics

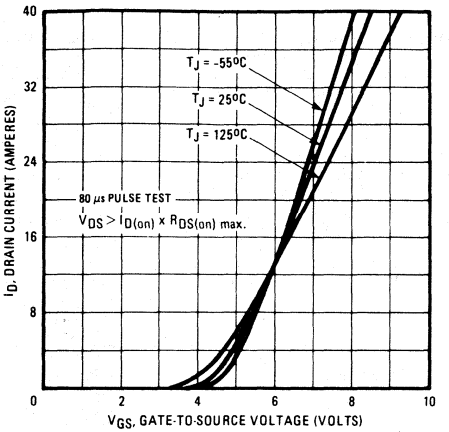


Fig. 2 — Typical Transfer Characteristics

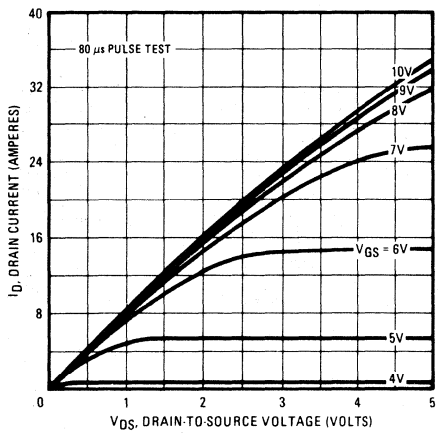


Fig. 3 — Typical Saturation Characteristics

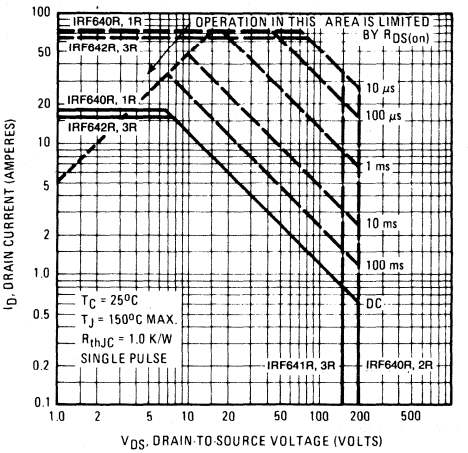


Fig. 4 — Maximum Safe Operating Area

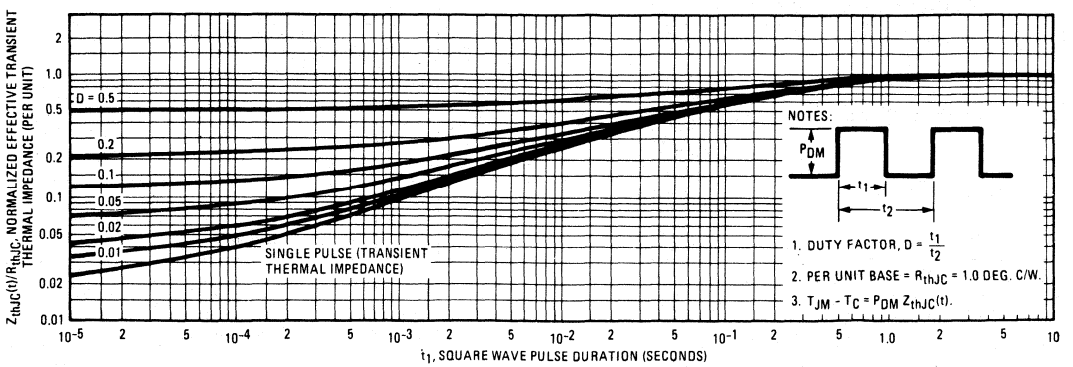


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

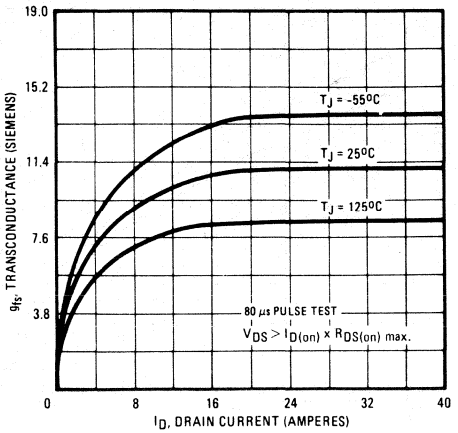


Fig. 6 — Typical Transconductance Vs. Drain Current

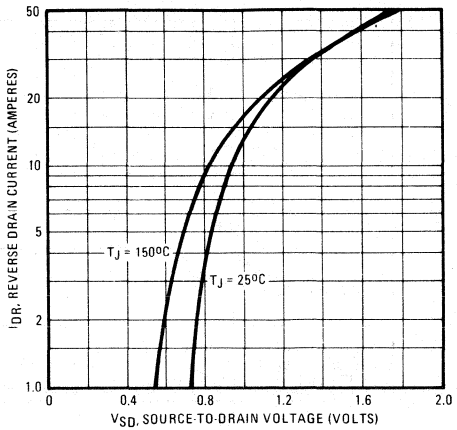


Fig. 7 — Typical Source-Drain Diode Forward Voltage

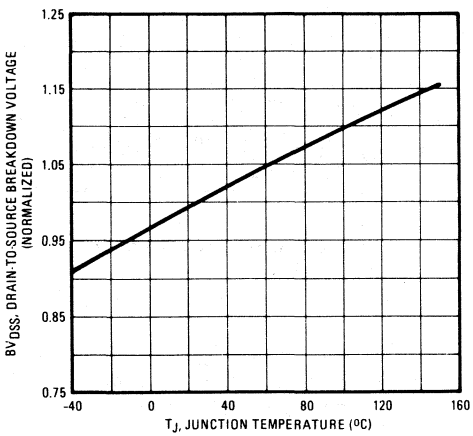


Fig. 8 — Breakdown Voltage Vs. Temperature

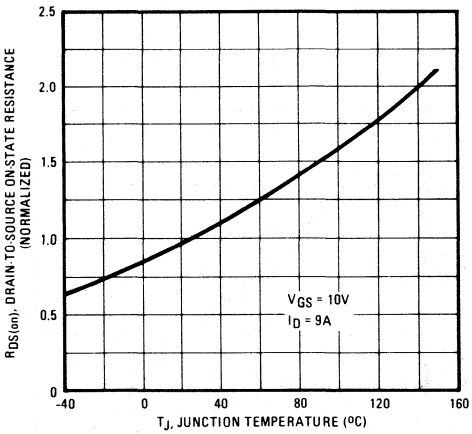


Fig. 9 — Normalized On-Resistance Vs. Temperature

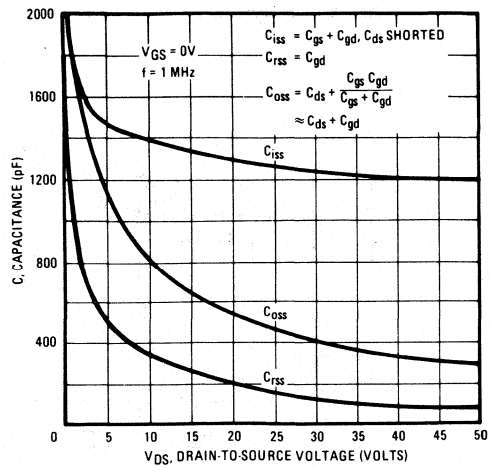


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

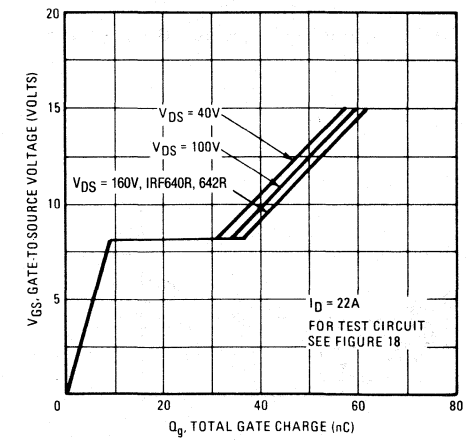


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF640R, IRF641R, IRF642R, IRF643R

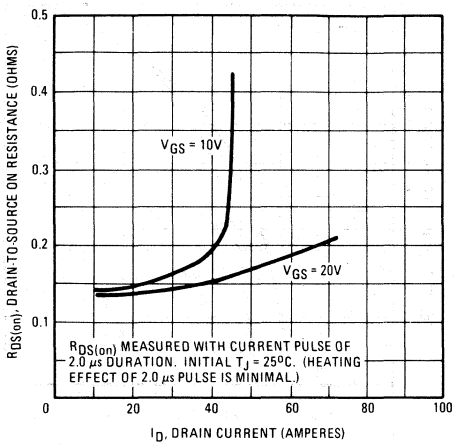


Fig. 12 – Typical On-Resistance Vs. Drain Current

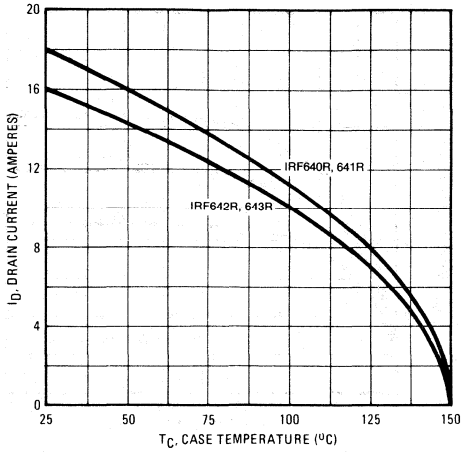


Fig. 13 – Maximum Drain Current Vs. Case Temperature

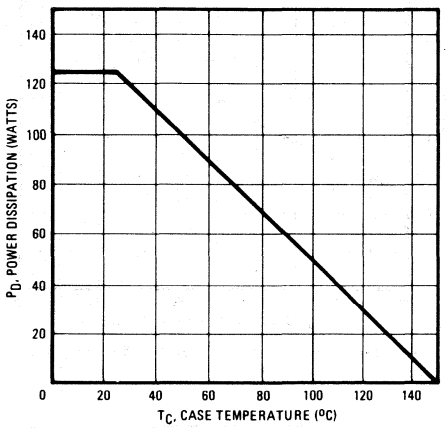


Fig. 14 – Power Vs. Temperature Derating Curve

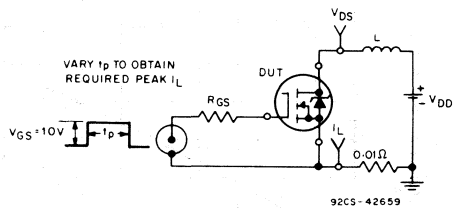


Fig. 15 - Unclamped Energy Test Circuit

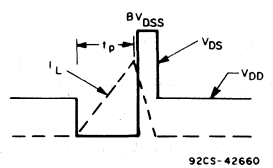


Fig. 16 — Unclamped Energy Waveforms

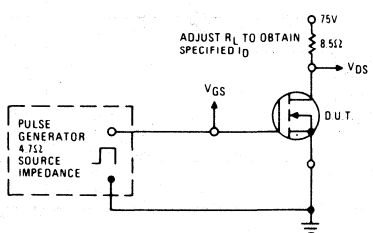


Fig. 17 - Switching Time Test Circuit

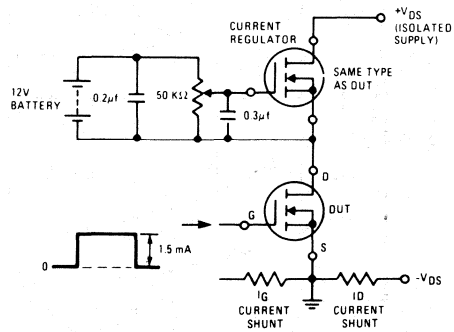


Fig. 18 - Gate Charge Test Circuit

File Number **2169**

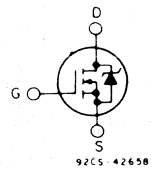
IRF644, IRF645, IRF646, IRF647

Avalanche Energy Rated N-Channel Power MOSFETs

N-CHANNEL ENHANCEMENT MODE

14A, and 13A, 275V, 250V
r_{DS} (on) = 0.28Ω, 0.34Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275V, 250V DC rated - 120V AC line system operation*

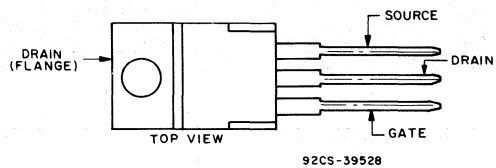


TERMINAL DIAGRAM

The IRF644, IRF645, IRF646, and IRF647 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

All types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

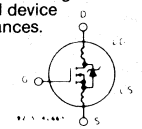
Absolute Maximum Ratings

Parameter		IRF644	IRF645	IRF646	IRF647	Units
V_{DS}	Drain - Source Voltage ①	250	250	275	275	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	250	250	275	275	V
I_D @ T_C = 25°C	Continuous Drain Current	14	13	14	13	A
I_D @ T_C = 100°C	Continuous Drain Current	8.8	8.0	8.8	8.0	A
I_{DM}	Pulsed Drain Current ③	56	52	56	52	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125				W
	Linear Derating Factor	1.0				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	550				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRF646 IRF647	275	—	—	V	V_{GS} = 0V
	IRF644 IRF645	250	—	—	V	I_D = 250μA
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = 20V
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$ On-State Drain Current ②	IRF644 IRF646	14	—	—	A	V_{DS} > $I_{D(on)}$ X $R_{DS(on)max.}$, V_{GS} = 10V
	IRF645 IRF647	13	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF644 IRF646	—	0.20	0.28	Ω	V_{GS} = 10V, I_D = 10A
	IRF645 IRF647	—	0.24	0.34	Ω	
g_{fs} Forward Transconductance ②	ALL	6.7	10	—	S(Ω)	V_{DS} > $I_{D(on)}$ X $R_{DS(on)max.}$, I_D = 10A
C_{iss} Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss} Output Capacitance	ALL	—	320	—	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	69	—	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	16	24	ns	V_{DD} = 90V, I_D = 10A, Z_D = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	—	67	100	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	53	80	ns	
t_f Fall Time	ALL	—	49	74	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	39	59	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	6.6	9.9	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	20	30	nC	
L_D Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

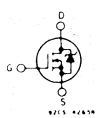


Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS} Case-to-Sink	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRF644 IRF646	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF645 IRF647	—	—	13	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRF644 IRF646	—	—	56	A	
	IRF645 IRF647	—	—	52	A	
V_{SD} Diode Forward Voltage ②	ALL	—	—	1.8	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
t_{rr} Reverse Recovery Time	ALL	150	300	640	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR} Reverse Recovered Charge	ALL	1.6	3.4	7.2	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_j = 25°C, L = 4.5MH, R_{gs} = 25Ω, I_{peak} = 14 A. See figures 14, 15.

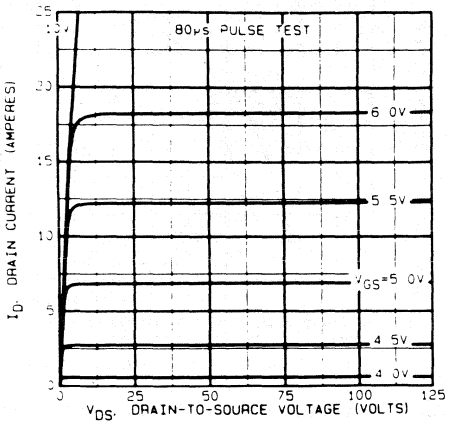


Fig. 1 — Typical Output Characteristics

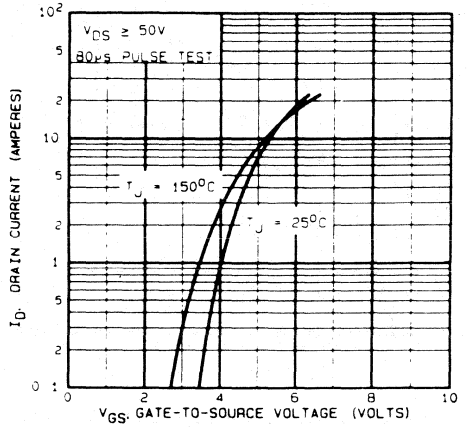


Fig. 2 — Typical Transfer Characteristics

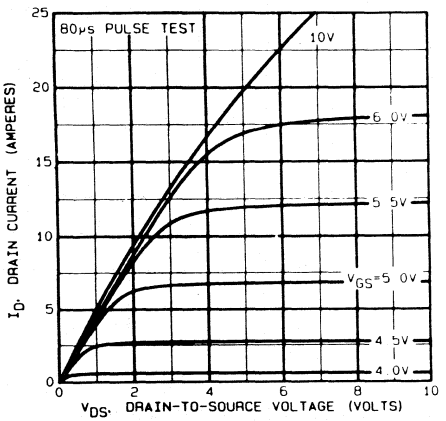


Fig. 3 — Typical Saturation Characteristics

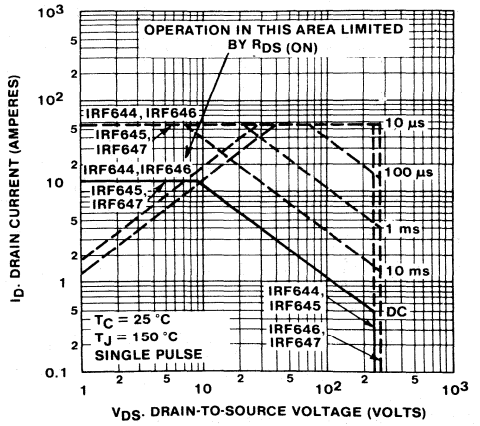


Fig. 4 — Maximum Safe Operating Area

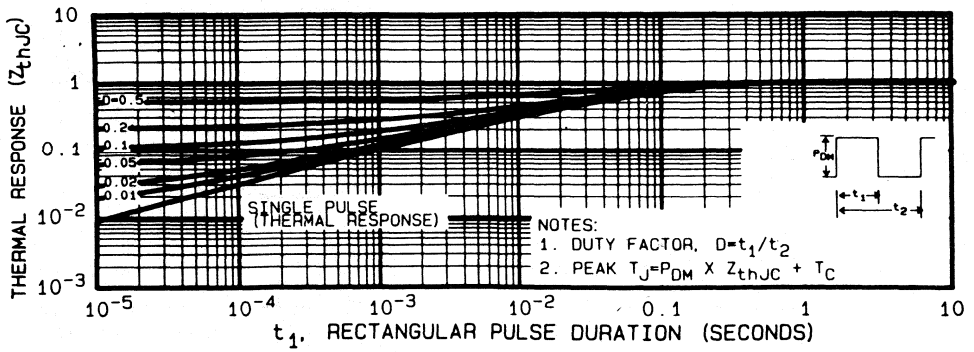


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

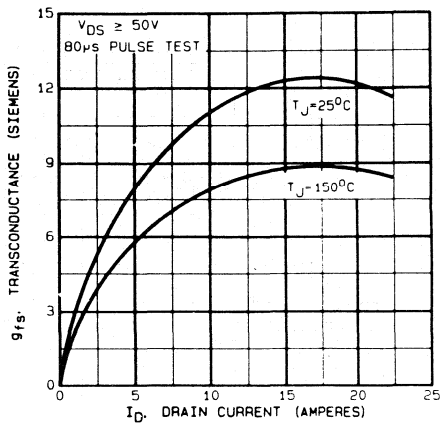


Fig. 6 — Typical Transconductance Vs. Drain Current

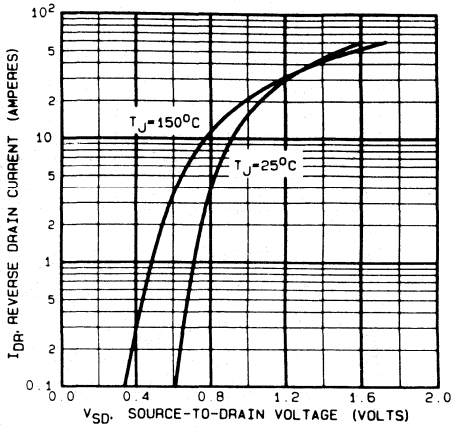


Fig. 7 — Typical Source-Drain Diode Forward Voltage

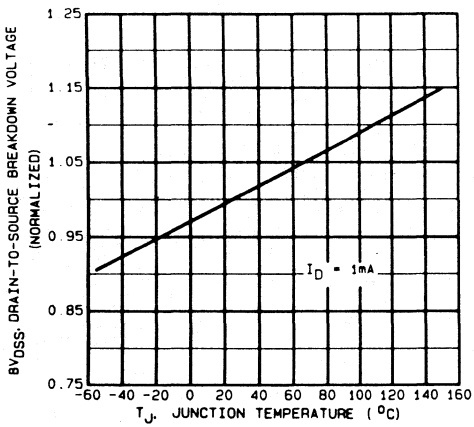


Fig. 8 — Breakdown Voltage Vs. Temperature

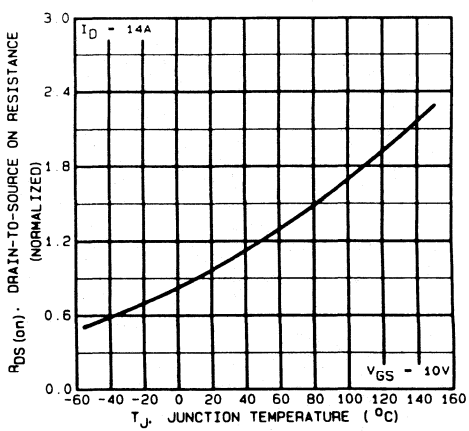


Fig. 9 — Normalized On-Resistance Vs. Temperature

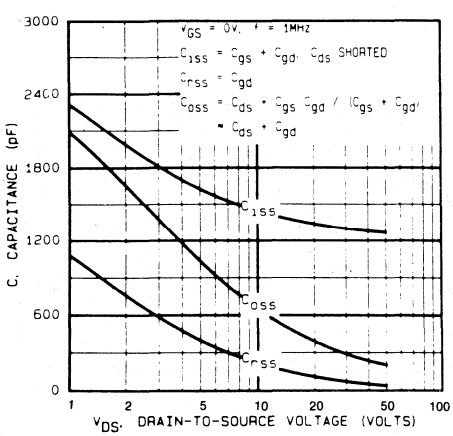


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

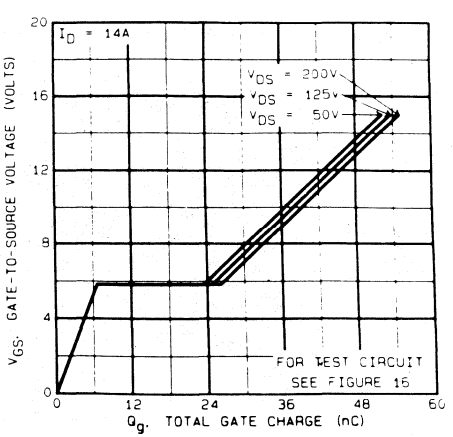


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

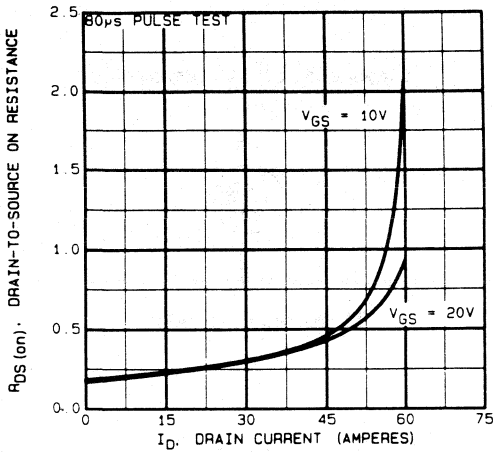


Fig. 12 — Typical On-Resistance Vs. Drain Current

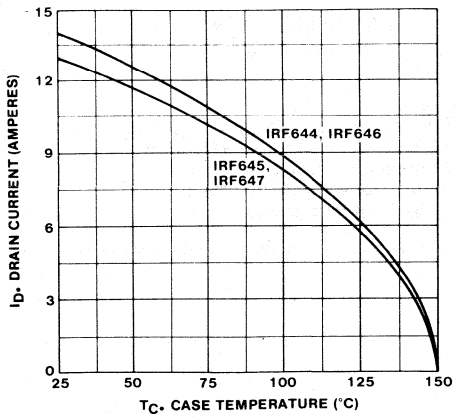


Fig. 13 — Maximum Drain Current Vs. Case Temperature

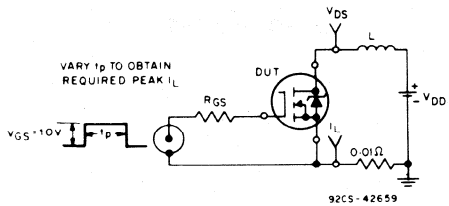


Fig. 14 — Unclamped Energy Test Circuit

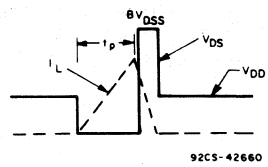


Fig. 15 — Unclamped Energy Waveforms

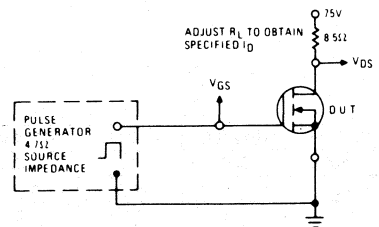


Fig. 16 — Switching Time Test Circuit

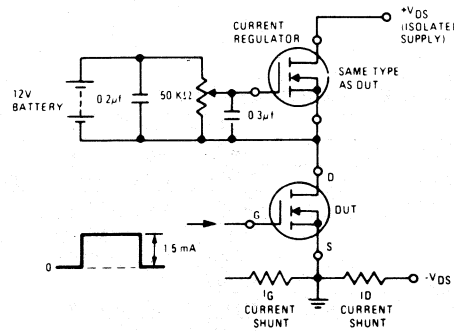


Fig. 17 — Gate Charge Test Circuit

IRF710R, IRF711R, IRF712R, IRF713R

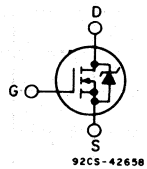
File Number **2000**

Avalanche Energy Rated N-Channel Power MOSFETs

1.5A and 1.3A, 400V-350V
$r_{DS}(on)$ = 3.6Ω and 5.0Ω

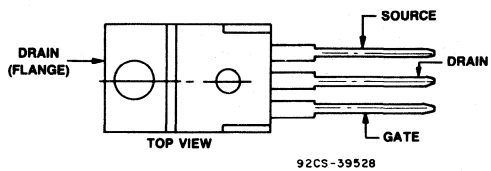
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF710R, IRF711R, IRF712R and IRF713R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

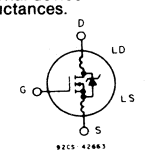
Absolute Maximum Ratings

Parameter		IRF710R	IRF711R	IRF712R	IRF713R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	1.5	1.5	1.3	1.3	A
I_D @ T_C = 100°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current ③	6.0	6.0	5.0	5.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	120				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF710R IRF712R	400	—	—	V	$V_{GS} = 0V$
		IRF711R IRF713R	350	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRF710R IRF711R	1.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRF712R IRF713R	1.3	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF710R IRF711R	—	3.3	3.6	Ω	$V_{GS} = 10V$, $I_D = 0.8A$
		IRF712R IRF713R	—	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 0.8A$
C_{iss}	Input Capacitance	ALL	—	135	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	35	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	8.0	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	3.0	10	ns	$V_{DD} \simeq 0.5BV_{DSS}$, $I_D = 0.8A$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	5.0	10	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	$V_{GS} = 10V$, $I_D = 2.0A$, $V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	3.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

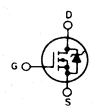


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF710R IRF711R	—	—	1.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF712R IRF713R	—	—	1.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF710R IRF711R	—	—	6.0	A	
		IRF712R IRF713R	—	—	5.0	A	
V_{SD}	Diode Forward Voltage ②	IRF710R IRF711R	—	—	1.6	V	$T_C = 25°C$, $I_S = 1.5A$, $V_{GS} = 0V$
		IRF712R IRF713R	—	—	1.5	V	$T_C = 25°C$, $I_S = 1.3A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	$T_J = 150°C$, $I_F = 1.5A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.7	—	μC	$T_J = 150°C$, $I_F = 1.5A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 50V$, starting $T_J = 25°C$, L = 53 mH, $R_{gs} = 50\Omega$, $I_{peak} = 2A$. See figures 15, 16.

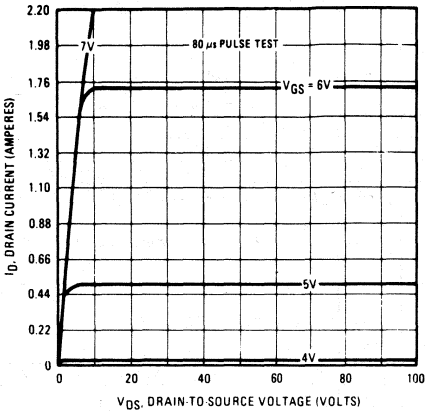


Fig. 1 – Typical Output Characteristics

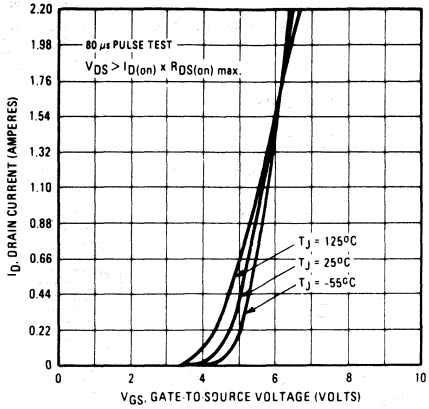


Fig. 2 – Typical Transfer Characteristics

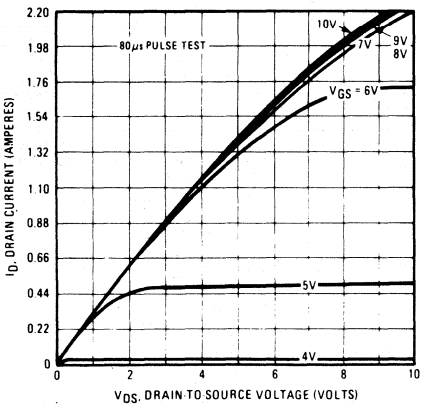


Fig. 3 – Typical Saturation Characteristics

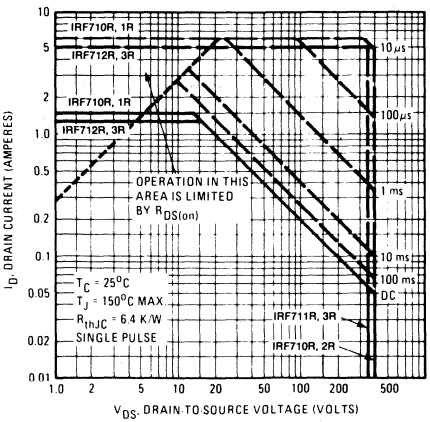


Fig. 4 – Maximum Safe Operating Area

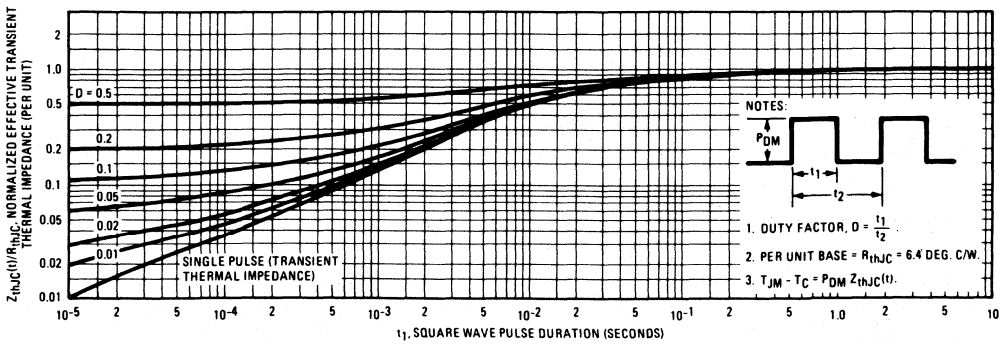


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

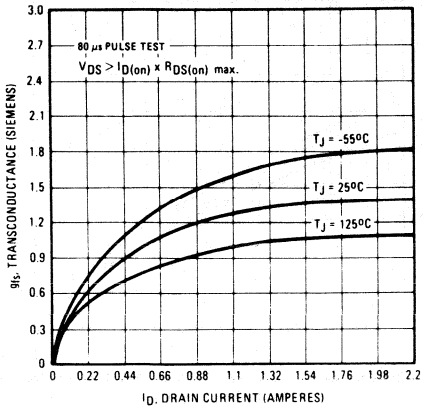


Fig. 6 – Typical Transconductance Vs. Drain Current

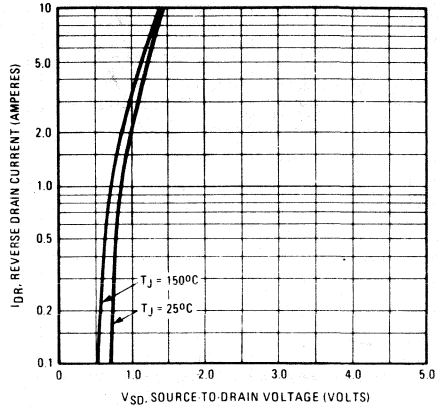


Fig. 7 – Typical Source-Drain Diode Forward Voltage

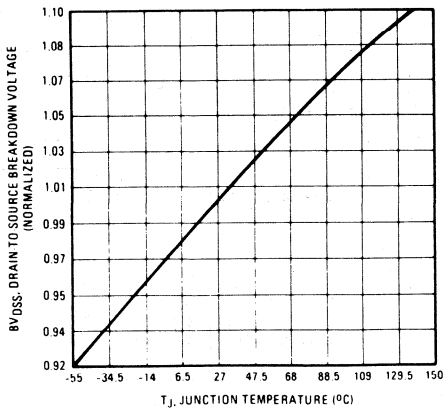


Fig. 8 – Breakdown Voltage Vs. Temperature

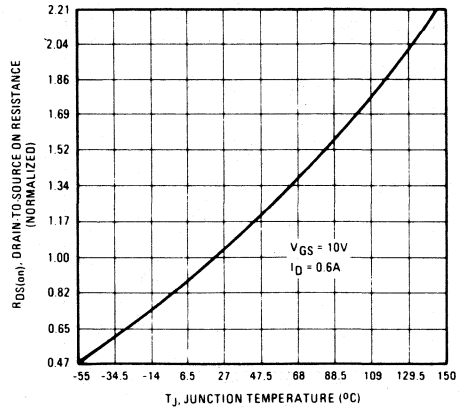


Fig. 9 – Normalized On-Resistance Vs. Temperature

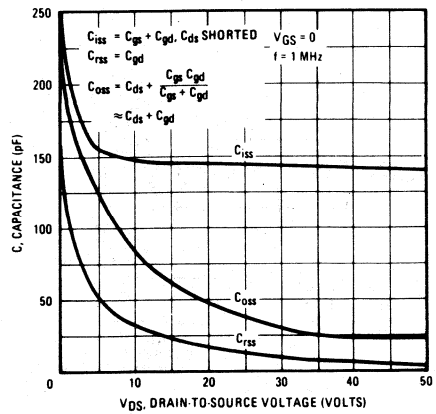


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

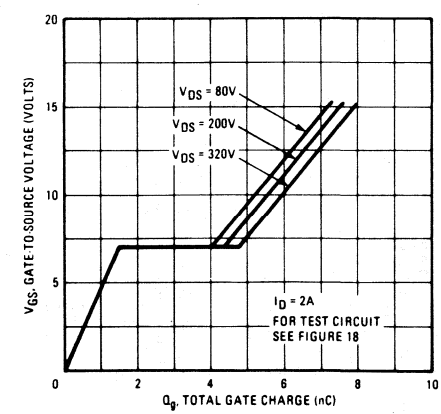


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF710R, IRF711R, IRF712R, IRF713R

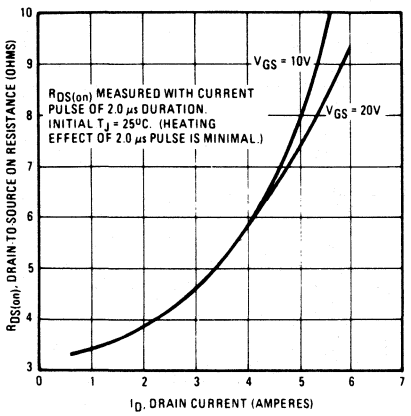


Fig. 12 – Typical On-Resistance Vs. Drain Current

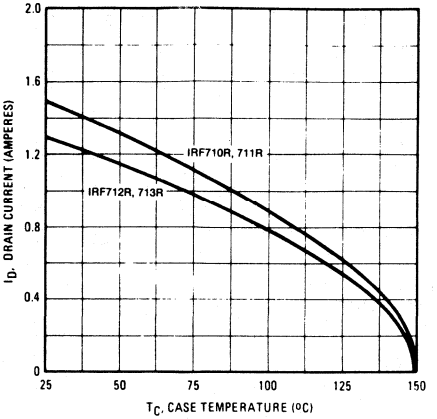


Fig. 13 – Maximum Drain Current Vs. Case Temperature

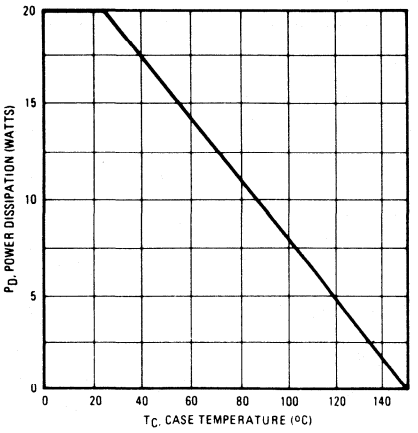


Fig. 14 – Power Vs. Temperature Derating Curve

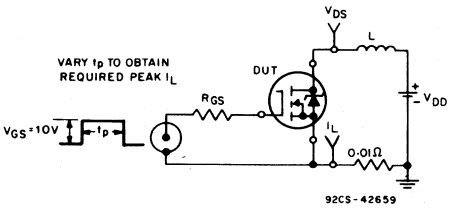


Fig. 15 — Unclamped Energy Test Circuit

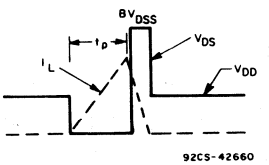


Fig. 16 — Unclamped Energy Waveforms

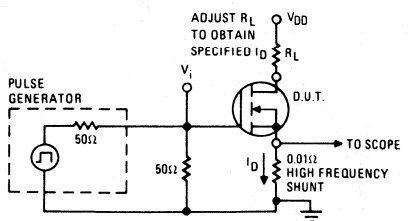


Fig. 17 – Switching Time Test Circuit

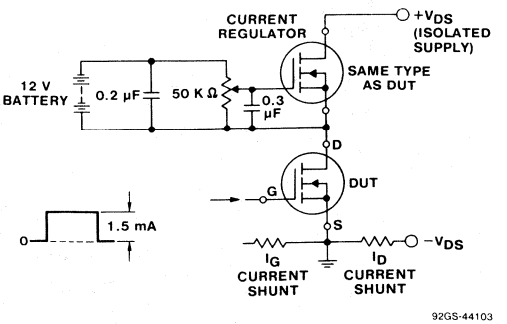


Fig. 18 – Gate Charge Test Circuit

File Number **1991**

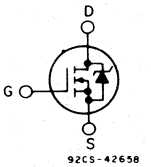
IRF720R, IRF721R IRF722R, IRF723R

Avalanche Energy Rated N-Channel Power MOSFETs

2.5A and 3.0A, 350V-400V
$r_{DS}(on) = 1.8\Omega$ and 2.5Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

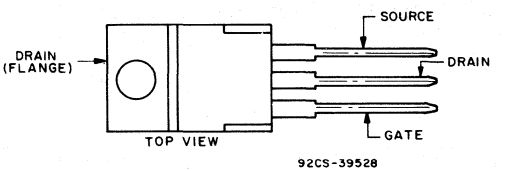


N-CHANNEL ENHANCEMENT MODE

The IRF720R, IRF721R, IRF722R and IRF723R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

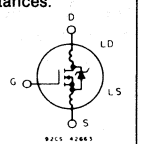
Absolute Maximum Ratings

Parameter		IRF720R	IRF721R	IRF722R	IRF723R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	190				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF720R, IRF721R
IRF722R, IRF723R

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF720R IRF722R	400	—	—	V	$V_{GS} = 0V$
		IRF721R IRF723R	350	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRF720R IRF721R	3.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRF722R IRF723R	2.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF720R IRF721R	—	1.5	1.8	Ω	$V_{GS} = 10V$, $I_D = 1.5A$
		IRF722R IRF723R	—	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 1.5A$
C_{iss}	Input Capacitance	ALL	—	450	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \simeq 0.5BV_{DSS}$, $I_D = 1.5A$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	$V_{GS} = 10V$, $I_D = 4.0A$, $V_{DS} = 0.8V$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

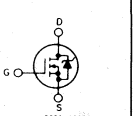


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF720R IRF721R	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF722R IRF723R	—	—	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF720R IRF721R	—	—	12	A	
		IRF722R IRF723R	—	—	10	A	
V_{SD}	Diode Forward Voltage ②	IRF720R IRF721R	—	—	1.6	V	$T_C = 25°C$, $I_S = 3.0A$, $V_{GS} = 0V$
		IRF722R IRF723R	—	—	1.5	V	$T_C = 25°C$, $I_S = 2.5A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150°C$, $I_F = 3.0A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	$T_J = 150°C$, $I_F = 3.0A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 50V$, starting $T_J = 25°C$, L = 31 mH, $R_{gs} = 50\Omega$, $I_{peak} = 3.3A$. See figures 15, 16.

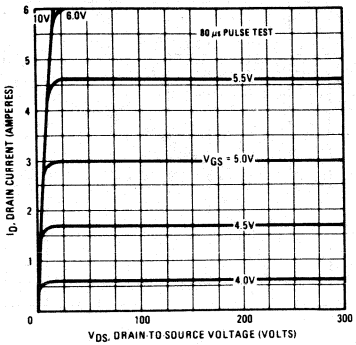


Fig. 1 – Typical Output Characteristics

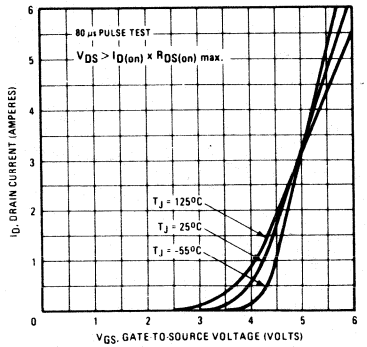


Fig. 2 – Typical Transfer Characteristics

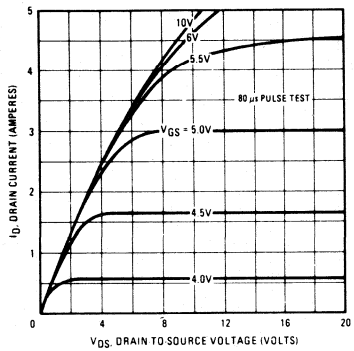


Fig. 3 – Typical Saturation Characteristics

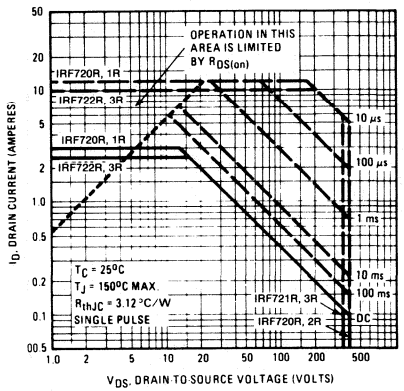


Fig. 4 – Maximum Safe Operating Area

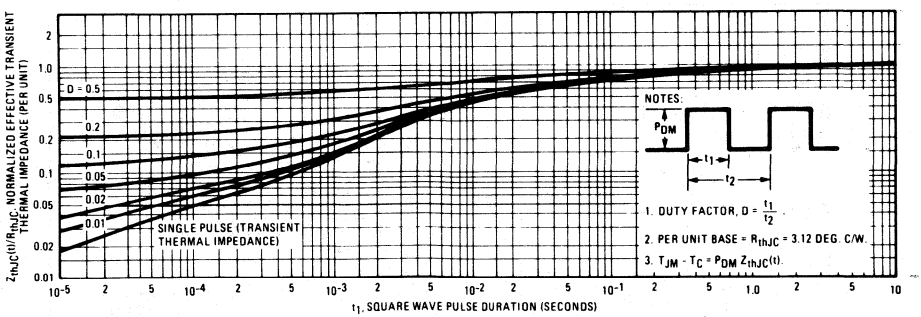


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

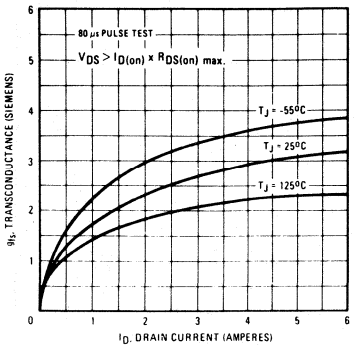


Fig. 6 — Typical Transconductance Vs. Drain Current

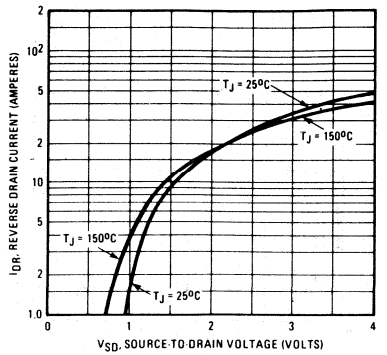


Fig. 7 — Typical Source-Drain Diode Forward Voltage

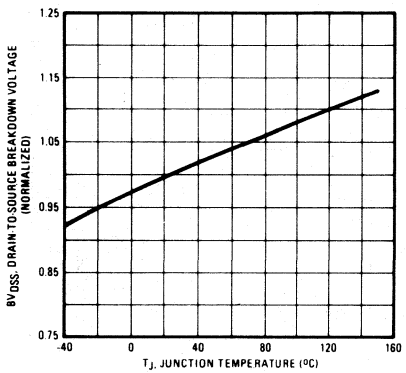


Fig. 8 — Breakdown Voltage Vs. Temperature

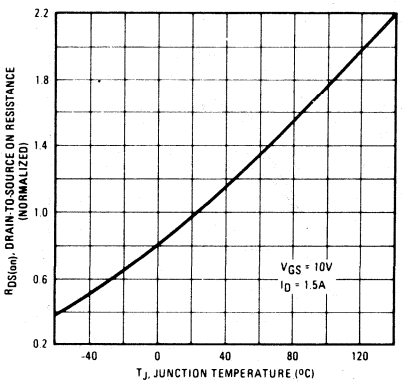


Fig. 9 — Normalized On-Resistance Vs. Temperature

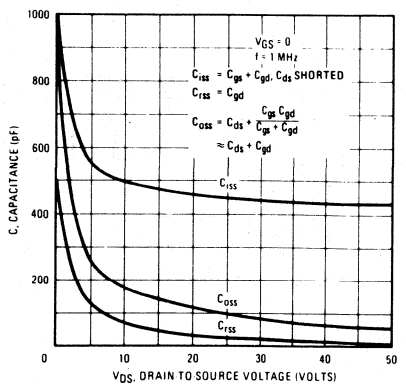


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

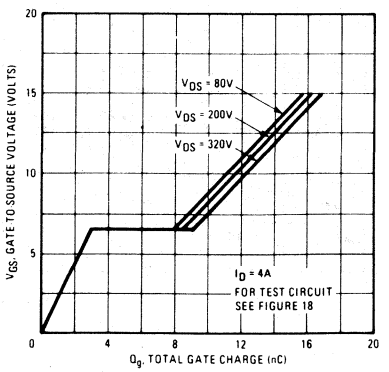


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

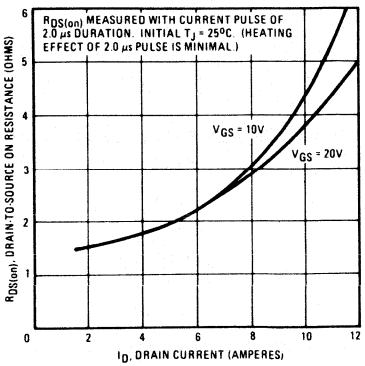


Fig. 12 – Typical On-Resistance Vs. Drain Current

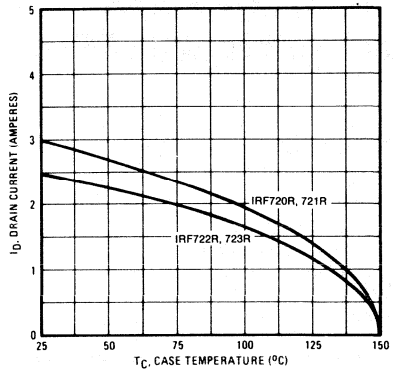


Fig. 13 – Maximum Drain Current Vs. Case Temperature

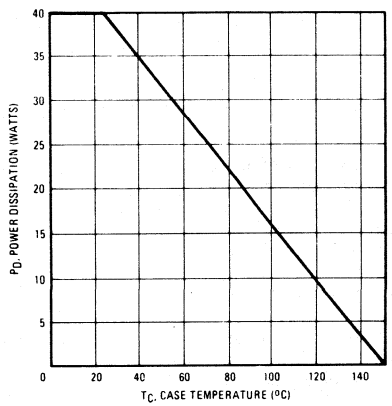


Fig. 14 – Power Vs. Temperature Derating Curve

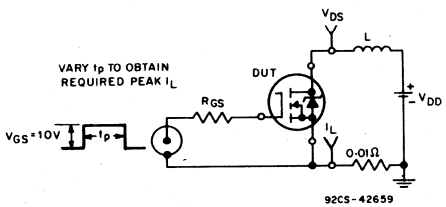


Fig. 15 — Unclamped Energy Test Circuit

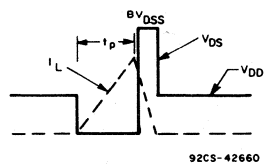


Fig. 16 — Unclamped Energy Waveforms

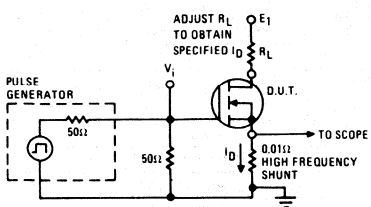


Fig. 17 – Switching Time Test Circuit

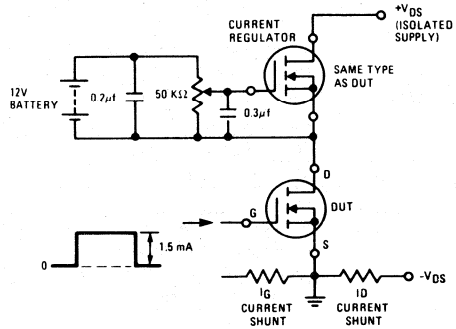


Fig. 18 – Gate Charge Test Circuit

IRF730R, IRF731R, IRF732R, IRF733R

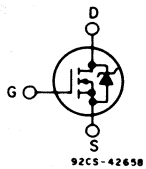
File Number **2019**

Avalanche Energy Rated N-Channel Power MOSFETs

4.5A and 5.5A, 350V-400V
$r_{DS}(on) = 1.0\Omega$ and 1.5Ω

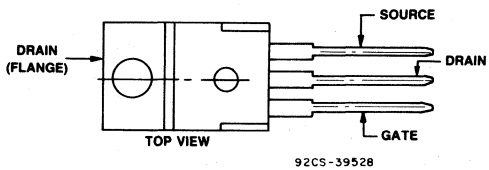
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF730R, IRF731R, IRF732R and IRF733R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

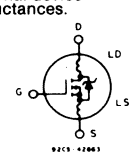
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

Parameter		IRF730R	IRF731R	IRF732R	IRF733R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	300				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF730R IRF732R	400	—	—	V	V_{GS} = 0V
		IRF731R IRF733R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF730R IRF731R	5.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF732R IRF733R	4.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF730R IRF731R	—	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF732R IRF733R	—	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 3.0A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	39	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

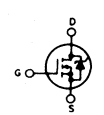


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF730R IRF731R	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF732R IRF733R	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF730R IRF731R	—	—	22	A	
		IRF732R IRF733R	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	IRF730R IRF731R	—	—	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF732R IRF733R	—	—	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 17mH, R_{gs} = 25Ω, I_{peak} = 5.5A.

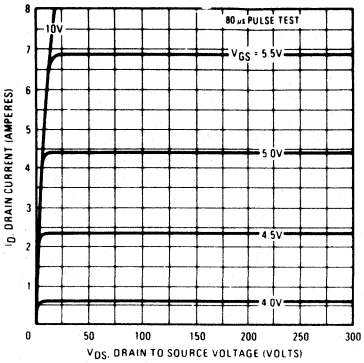


Fig. 1 – Typical Output Characteristics

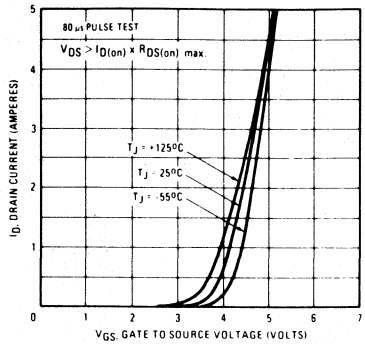


Fig. 2 – Typical Transfer Characteristics

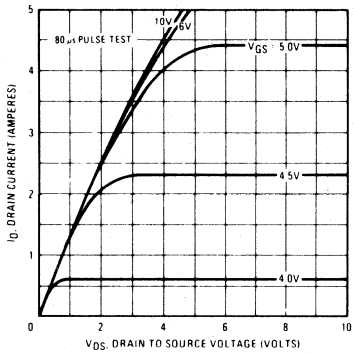


Fig. 3 – Typical Saturation Characteristics

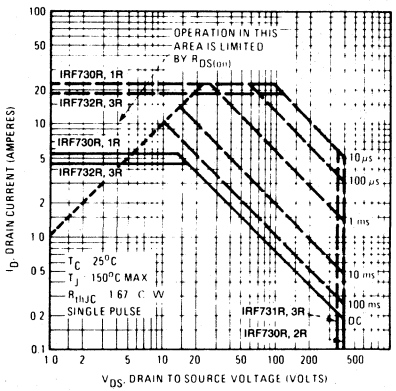


Fig. 4 – Maximum Safe Operating Area

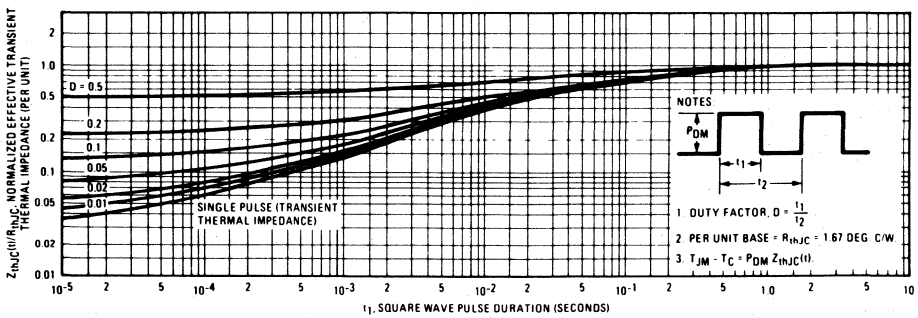


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

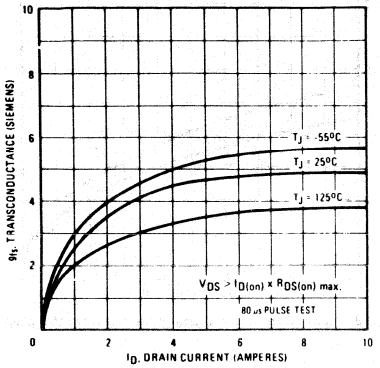


Fig. 6 – Typical Transconductance Vs. Drain Current

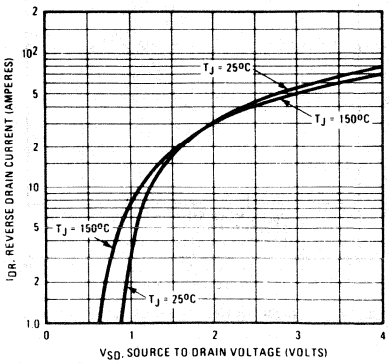


Fig. 7 – Typical Source-Drain Diode Forward Voltage

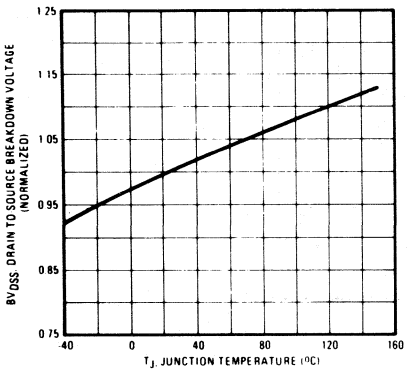


Fig. 8 – Breakdown Voltage Vs. Temperature

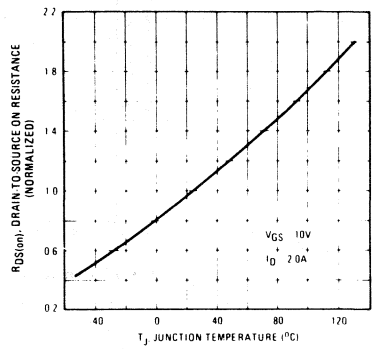


Fig. 9 – Normalized On-Resistance Vs. Temperature

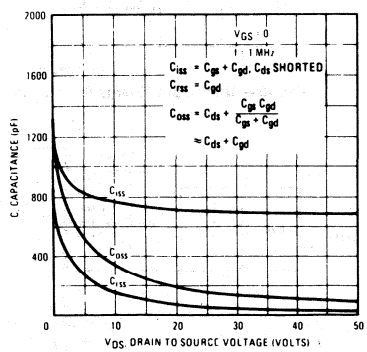


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

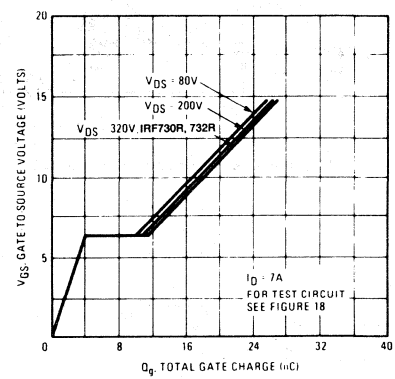


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

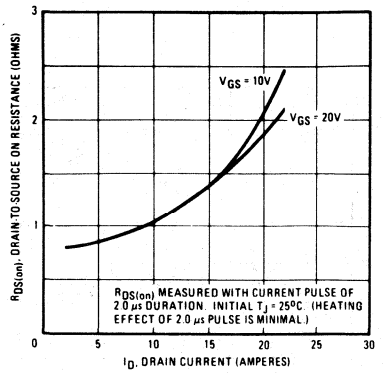


Fig. 12 – Typical On-Resistance Vs. Drain Current

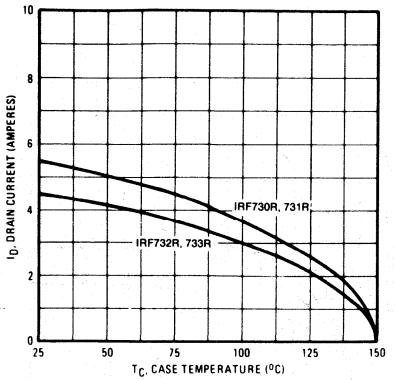


Fig. 13 – Maximum Drain Current Vs. Case Temperature

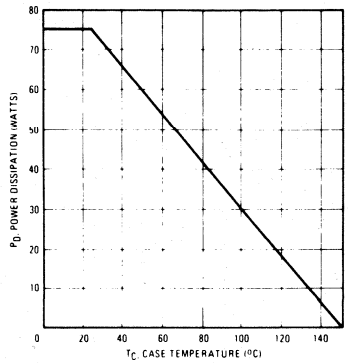


Fig. 14 – Power Vs. Temperature Derating Curve

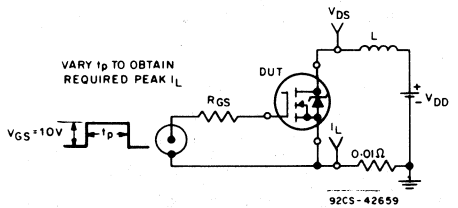


Fig. 15 — Unclamped Energy Test Circuit

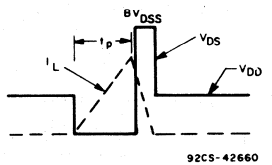


Fig. 16 — Unclamped Energy Waveforms

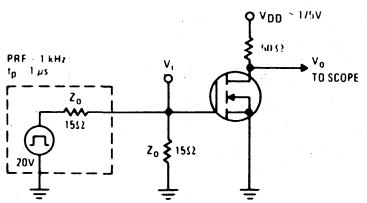


Fig. 17 – Switching Time Test Circuit

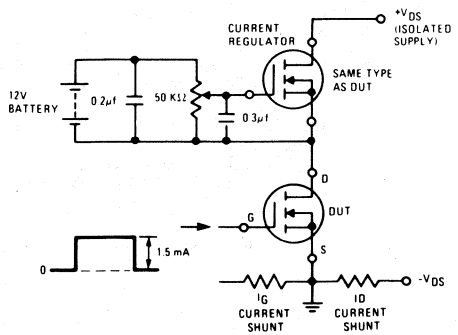


Fig. 18 – Gate Charge Test Circuit

File Number **2033**

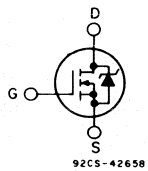
IRF740R, IRF741R
IRF742R, IRF743R

Avalanche Energy Rated N-Channel Power MOSFETs

10A and 8A, 400V-300V
$r_{DS}(on) = 0.55\Omega$ and 0.8Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

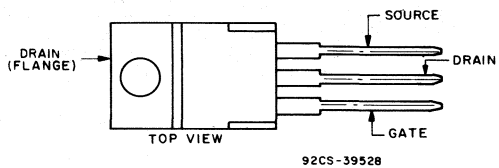


N-CHANNEL ENHANCEMENT MODE

The IRF740R, IRF741R, IRF742R and IRF743R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

Absolute Maximum Ratings

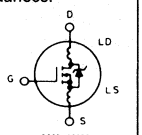
Parameter		IRF740R	IRF741R	IRF742R	IRF743R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	520				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF840R, IRF841R
IRF842R, IRF843R

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF840R IRF842R	500	—	—	V	$V_{GS} = 0V$
		IRF841R IRF843R	450	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRF840R IRF841R	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRF842R IRF843R	7.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF840R IRF841R	—	0.8	0.85	Ω	$V_{GS} = 10V$, $I_D = 4.0A$
		IRF842R IRF843R	—	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 4.0A$
C_{iss}	Input Capacitance	ALL	—	1225	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	85	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	17	35	ns	$V_{DD} \simeq 200V$, $I_D = 4.0A$, $Z_o = 4.7\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	42	90	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	42	60	nC	$V_{GS} = 10V$, $I_D = 10A$, $V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	20	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	22	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

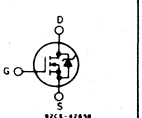


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF840R IRF841R	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF842R IRF843R	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF840R IRF841R	—	—	32	A	
		IRF842R IRF843R	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	IRF840R IRF841R	—	—	2.0	V	$T_C = 25°C$, $I_S = 8.0A$, $V_{GS} = 100A/\mu s$
		IRF842R IRF843R	—	—	1.9	V	$T_C = 25°C$, $I_S = 7.0A$, $V_{GS} = 100A/\mu s$
t_{rr}	Reverse Recovery Time	ALL	—	1100	—	ns	$T_J = 150°C$, $I_F = 8.0A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	6.4	—	μC	$T_J = 150°C$, $I_F = 8.0A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 50V$, starting $T_J = 25°C$, L = 9.1 mH, $R_{gs} = 50\Omega$, $I_{peak} = 10A$. See figures 15, 16.

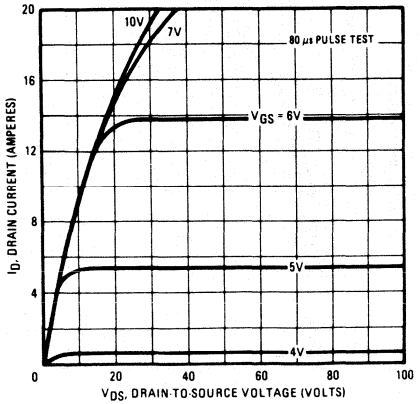


Fig. 1 – Typical Output Characteristics

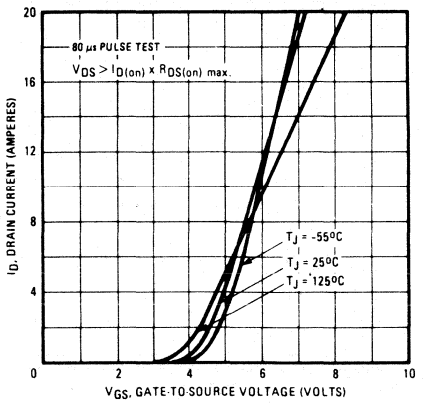


Fig. 2 – Typical Transfer Characteristics

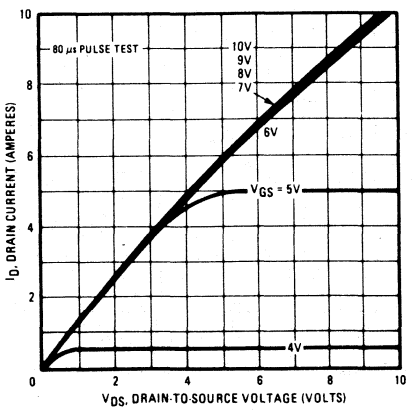


Fig. 3 – Typical Saturation Characteristics

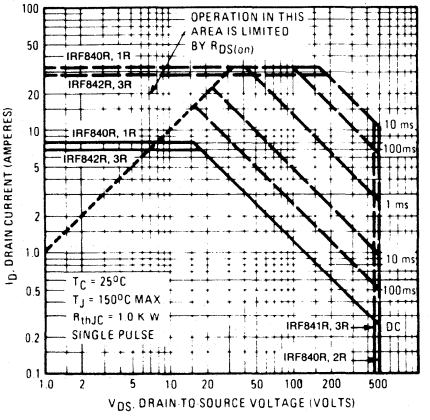


Fig. 4 – Maximum Safe Operating Area

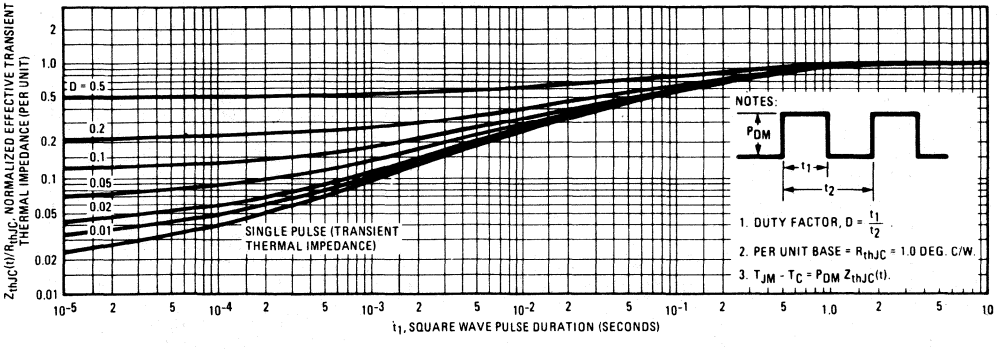


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

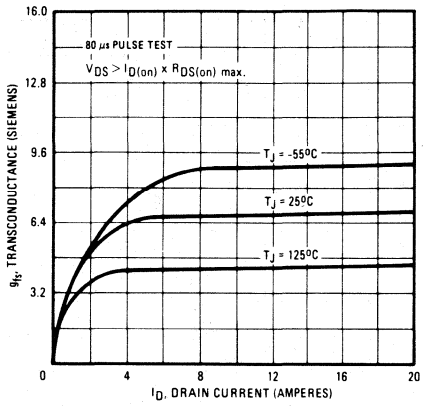


Fig. 6 – Typical Transconductance Vs. Drain Current

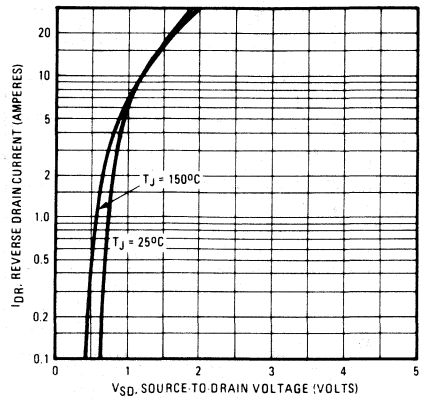


Fig. 7 – Typical Source-Drain Diode Forward Voltage

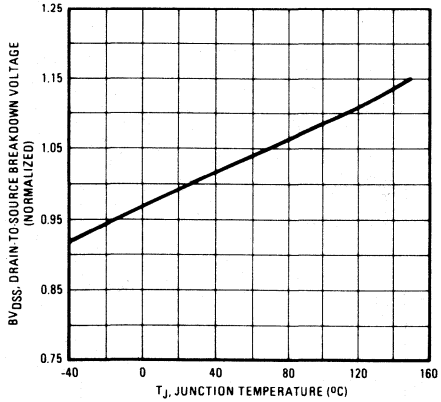


Fig. 8 – Breakdown Voltage Vs. Temperature

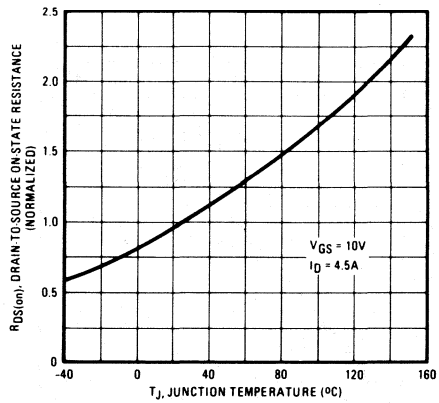


Fig. 9 – Normalized On-Resistance Vs. Temperature

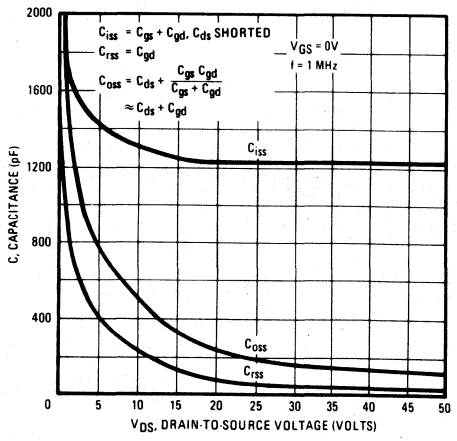


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

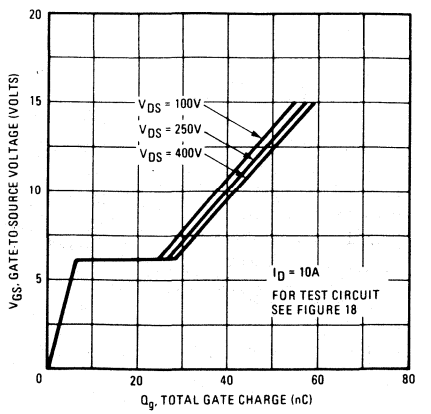


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

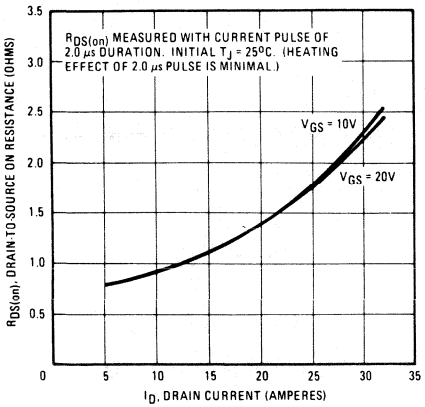


Fig. 12 — Typical On-Resistance Vs. Drain Current

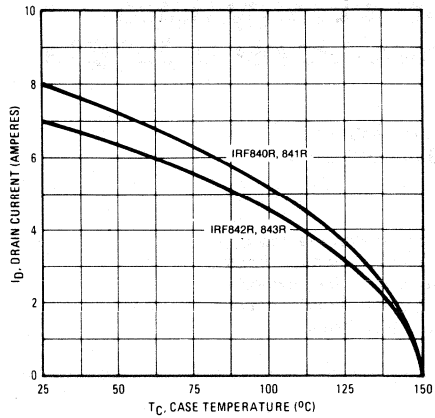


Fig. 13 — Maximum Drain Current Vs. Case Temperature

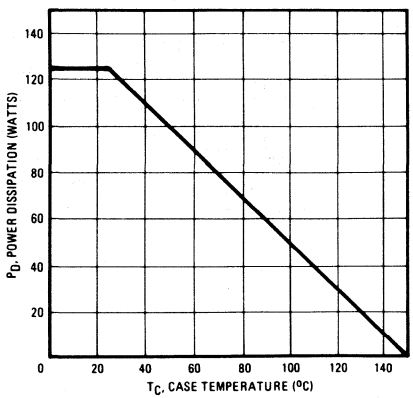


Fig. 14 — Power Vs. Temperature Derating Curve

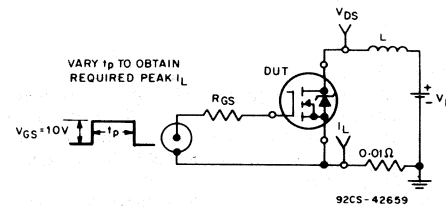


Fig. 15 — Unclamped Energy Test Circuit

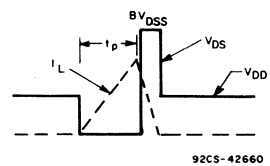


Fig. 16 — Unclamped Energy Waveforms

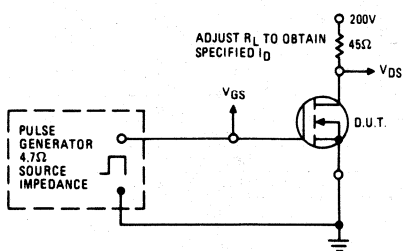


Fig. 17 — Switching Time Test Circuit

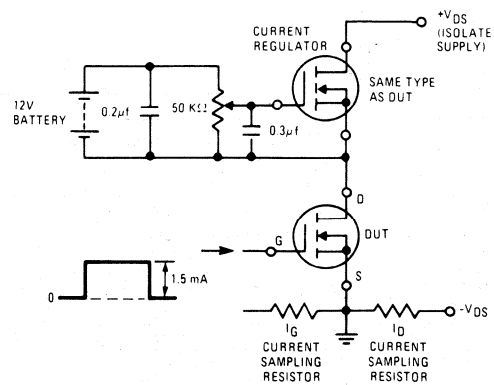


Fig. 18 — Gate Charge Test Circuit

IRF820R, IRF821R, IRF822R, IRF823R

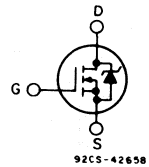
File Number **2020**

Avalanche Energy Rated N-Channel Power MOSFETs

2.0A and 2.5A, 450V-500V
$r_{DS}(on) = 3.0\Omega$ and 4.0Ω

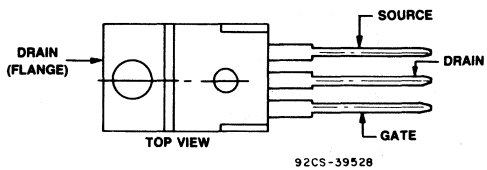
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF820R, IRF821R, IRF822R and IRF823R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

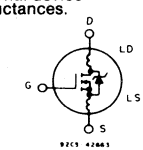
Absolute Maximum Ratings

Parameter		IRF820R	IRF821R	IRF822R	IRF823R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	210				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF820R IRF822R	500	—	—	V	V_{GS} = 0V
		IRF821R IRF823R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF820R IRF821R	2.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF822R IRF823R	2.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF820R IRF821R	—	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF822R IRF823R	—	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 1.0A
C_{iss}	Input Capacitance	ALL	—	300	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	75	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	30	60	ns	
t_f	Fall Time	ALL	—	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	26	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF820R IRF821R	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF822R IRF823R	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF820R IRF821R	—	—	10	A	
		IRF822R IRF823R	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF820R IRF821R	—	—	1.6	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF822R IRF823R	—	—	1.5	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.5	—	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 5V, starting T_J = 25°C, L = 60mH, R_{gs} = 25Ω, I_{peak} = 2.5A. See figures 15, 16.

IRF820R, IRF821R, IRF822R, IRF823R

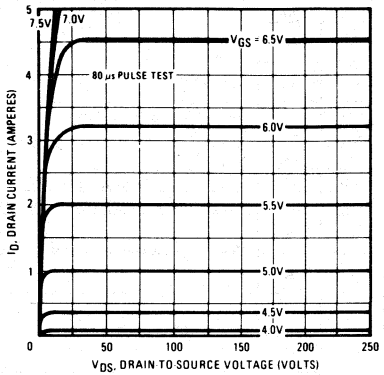


Fig. 1 – Typical Output Characteristics

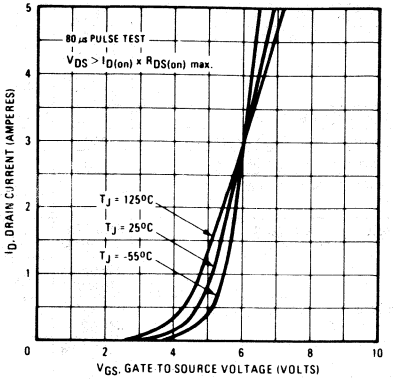


Fig. 2 – Typical Transfer Characteristics

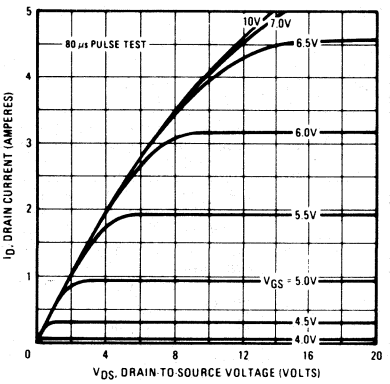


Fig. 3 – Typical Saturation Characteristics

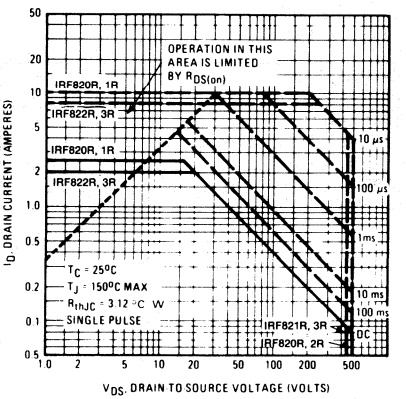


Fig. 4 – Maximum Safe Operating Area

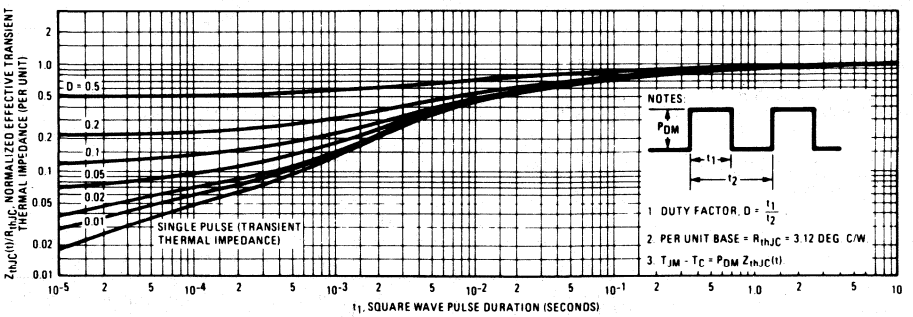


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

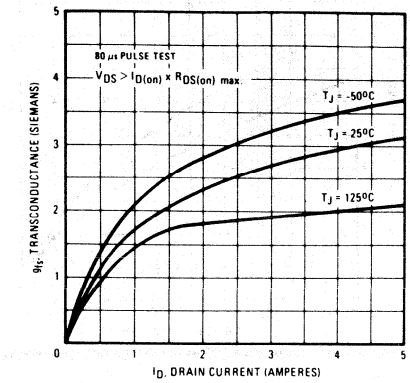


Fig. 6 – Typical Transconductance Vs. Drain Current

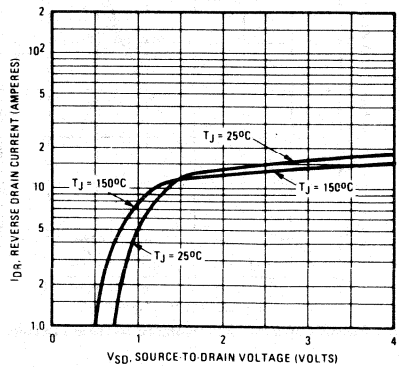


Fig. 7 – Typical Source-Drain Diode Forward Voltage

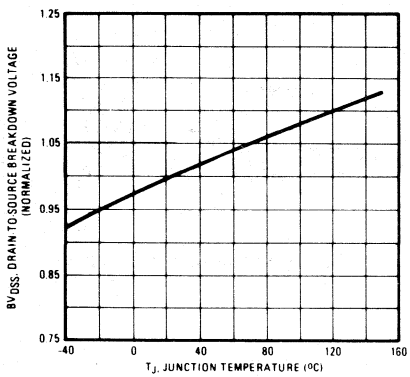


Fig. 8 – Breakdown Voltage Vs. Temperature

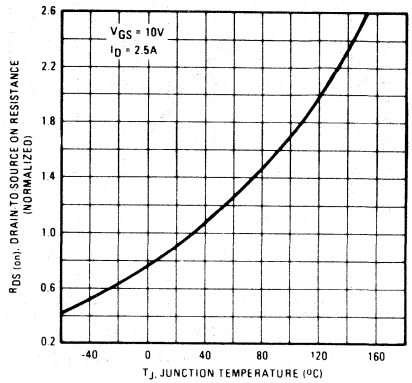


Fig. 9 – Normalized On-Resistance Vs. Temperature

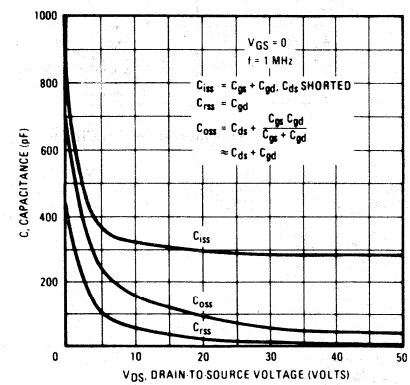


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

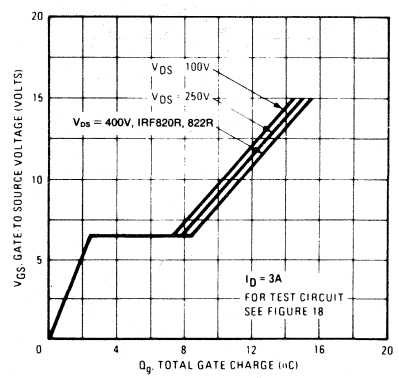


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

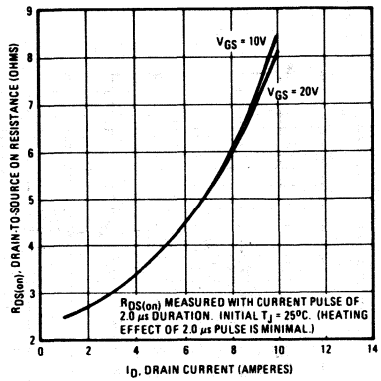


Fig. 12 – Typical On-Resistance Vs. Drain Current

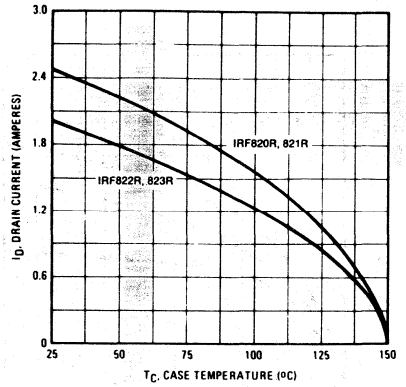


Fig. 13 – Maximum Drain Current Vs. Case Temperature

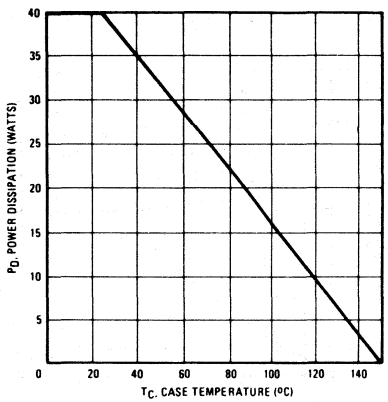


Fig. 14 – Power Vs. Temperature Derating Curve

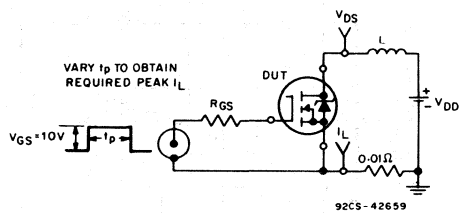


Fig. 15 — Unclamped Energy Test Circuit

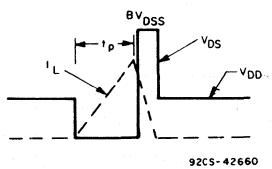


Fig. 16 — Unclamped Energy Waveforms

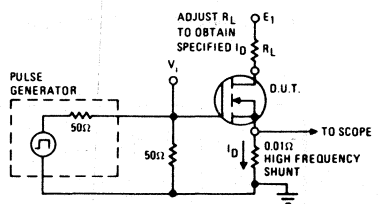


Fig. 17 – Switching Time Test Circuit

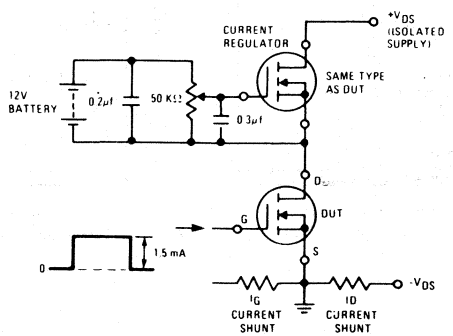


Fig. 18 – Gate Charge Test Circuit

File Number **2021**

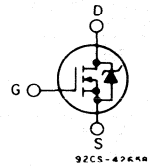
IRF830R, IRF831R, IRF832R, IRF833R

Avalanche Energy Rated N-Channel Power MOSFETs

4.0A and 4.5A, 450V-500V
$r_{DS}(on) = 1.5\Omega$ and 2.0Ω

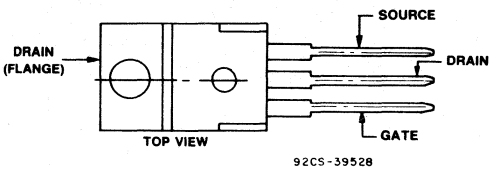
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF830R, IRF831R, IRF832R and IRF833R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

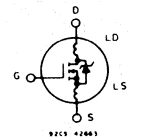
Absolute Maximum Ratings

	Parameter	IRF830R	IRF831R	IRF832R	IRF833R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	300				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF830R, IRF831R, IRF832R, IRF833R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF830R IRF832R	500	—	—	V	V_{GS} = 0V
		IRF831R IRF833R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF830R IRF831R	4.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF832R IRF833R	4.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF830R IRF831R	—	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF832R IRF833R	—	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.25	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 2.5A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 225V, I_D = 2.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	39	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	11	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

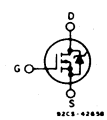


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF830R IRF831R	—	—	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF832R IRF833R	—	—	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF830R IRF831R	—	—	18	A	
		IRF832R IRF833R	—	—	16	A	
V_{SD}	Diode Forward Voltage ②	IRF830R IRF831R	—	—	1.6	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF832R IRF833R	—	—	1.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 25mH, R_{gs} = 25Ω, I_{peak} = 4.5A. See figures 15, 16.

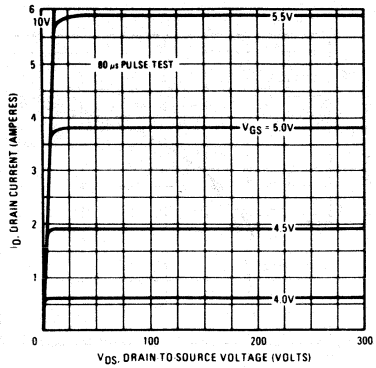


Fig. 1 – Typical Output Characteristics

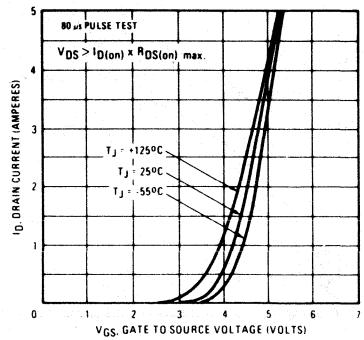


Fig. 2 – Typical Transfer Characteristics

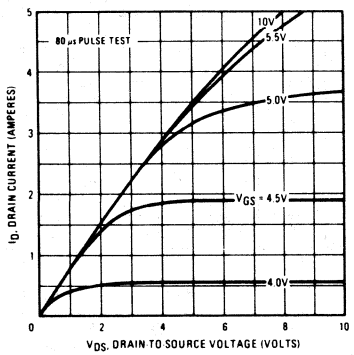


Fig. 3 – Typical Saturation Characteristics

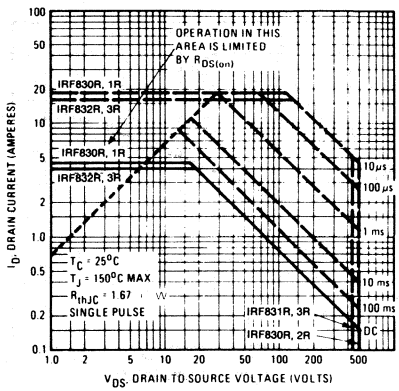


Fig. 4 – Maximum Safe Operating Area

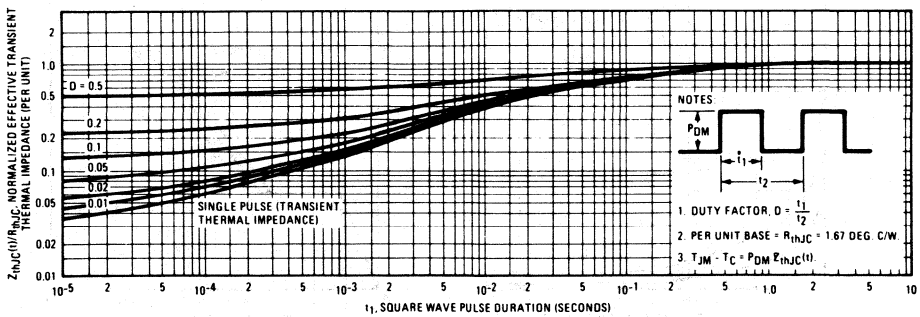


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

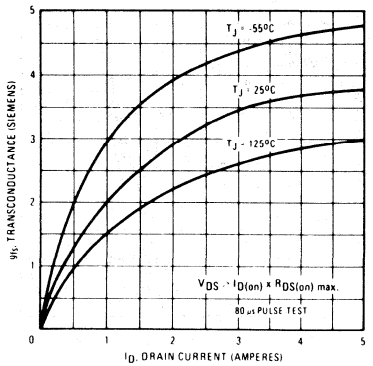


Fig. 6 – Typical Transconductance Vs. Drain Current

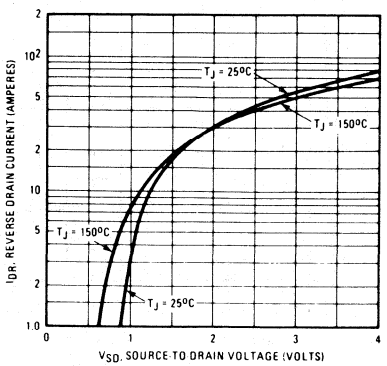


Fig. 7 – Typical Source-Drain Diode Forward Voltage

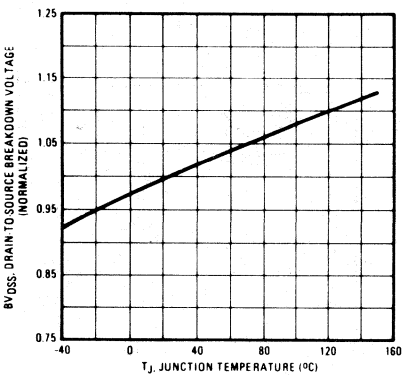


Fig. 8 – Breakdown Voltage Vs. Temperature

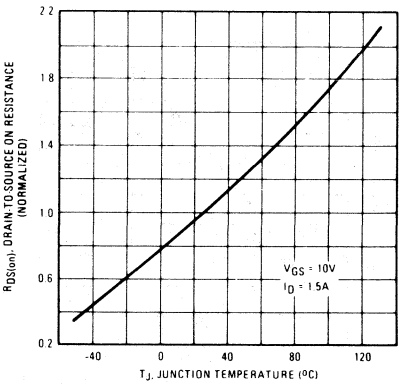


Fig. 9 – Normalized On-Resistance Vs. Temperature

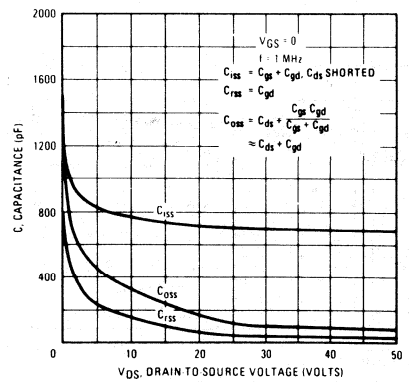


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

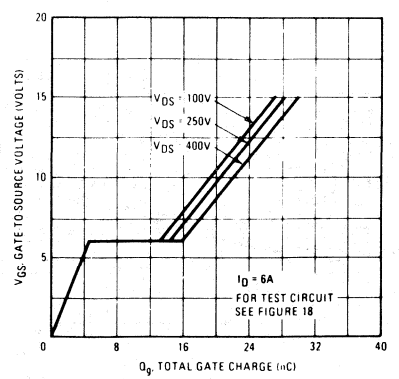


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

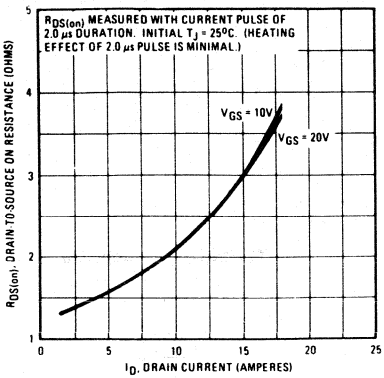


Fig. 12 – Typical On-Resistance Vs. Drain Current

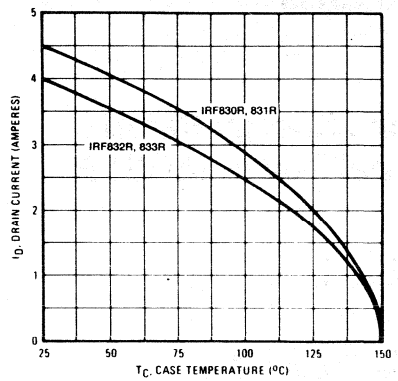


Fig. 13 – Maximum Drain Current Vs. Case Temperature

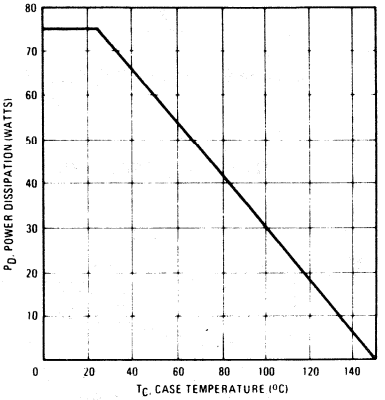


Fig. 14 – Power Vs. Temperature Derating Curve

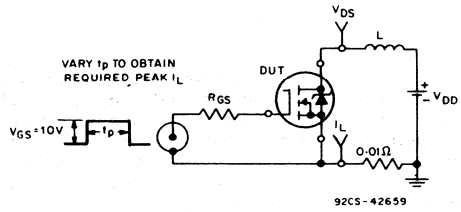


Fig. 15 — Unclamped Energy Test Circuit

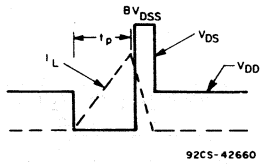


Fig. 16 — Unclamped Energy Waveforms

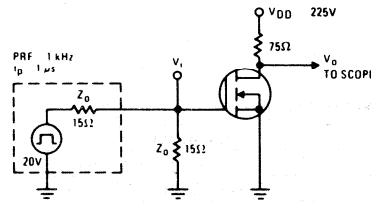


Fig. 17 – Switching Time Test Circuit

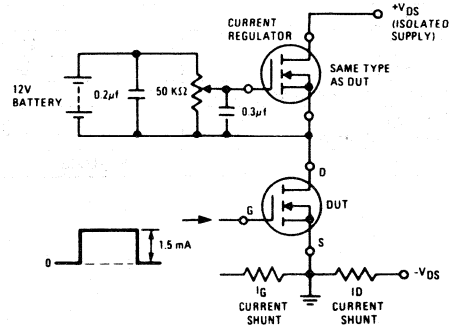


Fig. 18 – Gate Charge Test Circuit

IRF840R, IRF841R
IRF842R, IRF843R

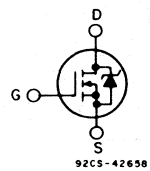
File Number **2034**

Avalanche Energy Rated N-Channel Power MOSFETs

8A and 7A, 500V-400V
$r_{DS}(on) = 0.85\Omega$ and 1.1Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

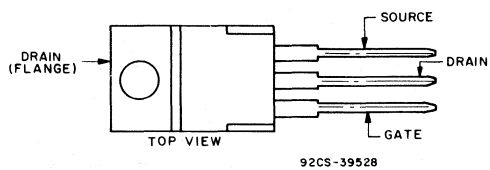


N-CHANNEL ENHANCEMENT MODE

The IRF840R, IRF841R, IRF842R and IRF843R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



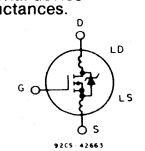
JEDEC TO-220AB

Absolute Maximum Ratings

Parameter		IRF840R	IRF841R	IRF842R	IRF843R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	510				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF740R IRF742R	400	—	—	V	V_{GS} = 0V
		IRF741R IRF743R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF740R IRF741R	10	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF742R IRF743R	8.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF740R IRF741R	—	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF742R IRF743R	—	.68	.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 5.0A
C_{iss}	Input Capacitance	ALL	—	1250	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	17	35	ns	V_{DD} = 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5.0	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	45	90	ns	
t_f	Fall Time	ALL	—	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	18	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	23	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

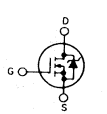


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF740R IRF741R	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF742R IRF743R	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF740R IRF741R	—	—	40	A	
		IRF742R IRF743R	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	IRF740R IRF741R	—	—	2.0	V	T_C = 25°C, I_S = 10A, V_{GS} = 0V
		IRF742R IRF743R	—	—	1.9	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	5.7	—	μC	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 14 mH, R_{gs} = 50Ω, I_{peak} = 8A. See figures 15, 16.

IRF740R, IRF741R
IRF742R, IRF743R

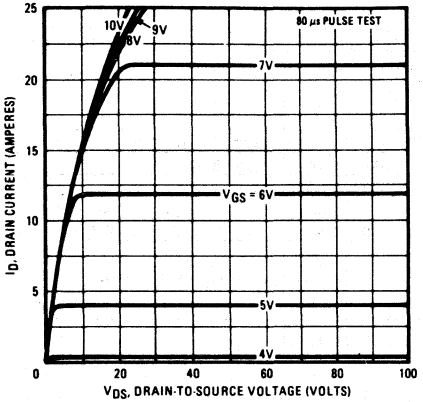


Fig. 1 — Typical Output Characteristics

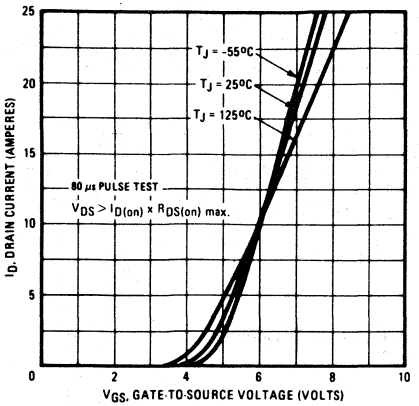


Fig. 2 — Typical Transfer Characteristics

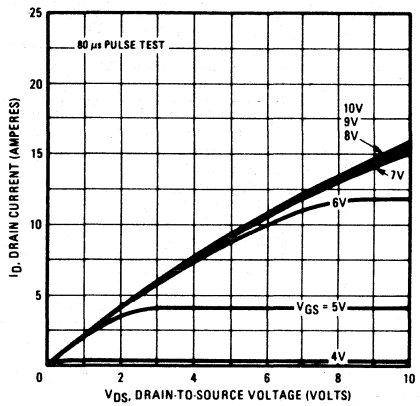


Fig. 3 — Typical Saturation Characteristics

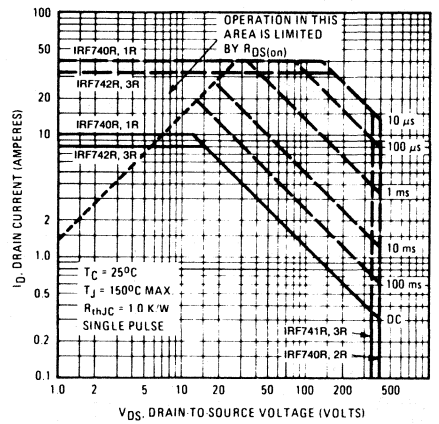


Fig. 4 — Maximum Safe Operating Area

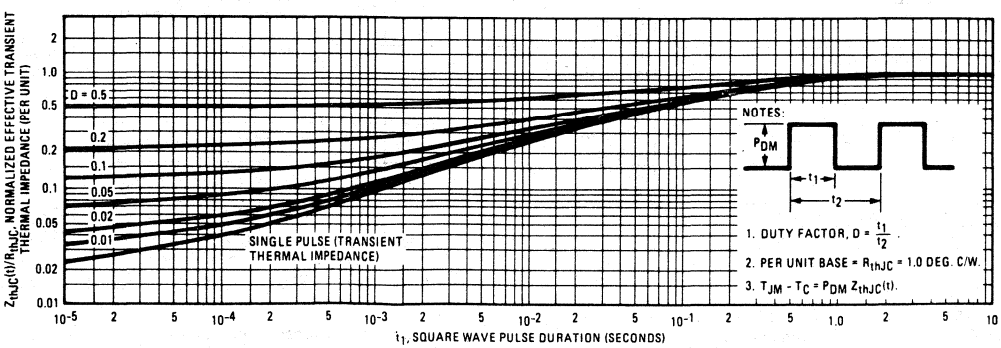


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

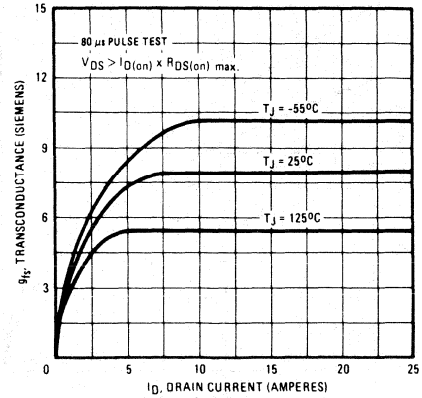


Fig. 6 – Typical Transconductance Vs. Drain Current

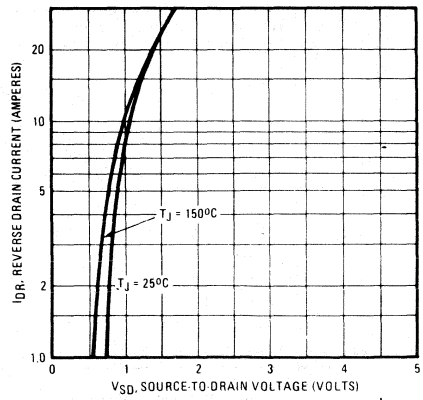


Fig. 7 – Typical Source-Drain Diode Forward Voltage

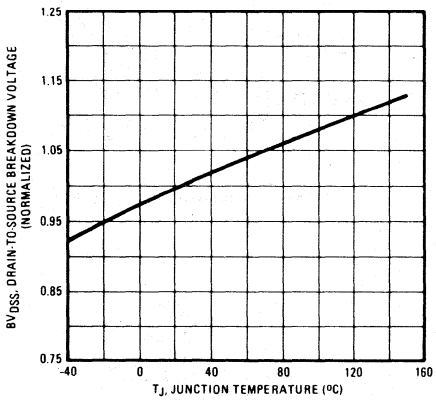


Fig. 8 – Breakdown Voltage Vs. Temperature

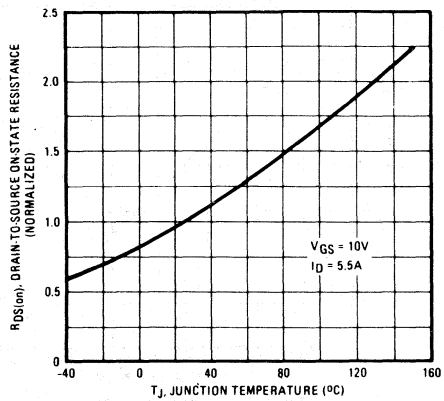


Fig. 9 – Normalized On-Resistance Vs. Temperature

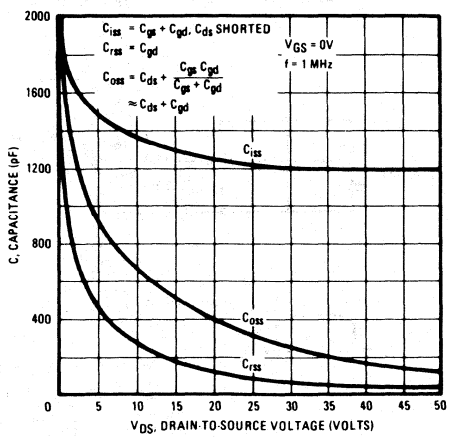


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

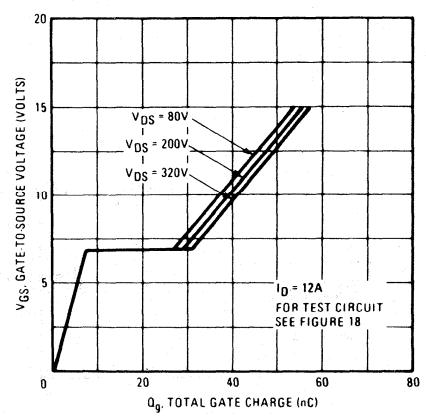


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

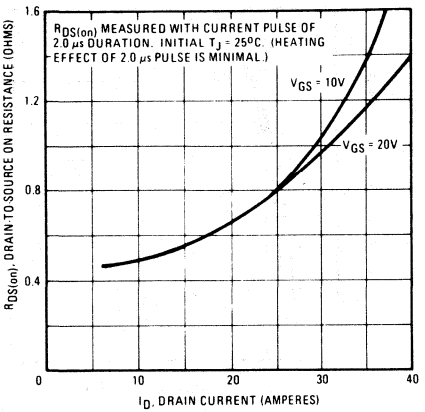


Fig. 12 — Typical On-Resistance Vs. Drain Current

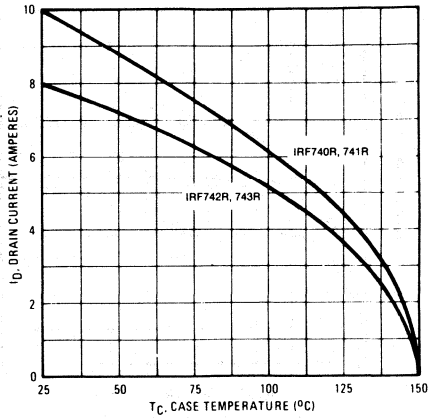


Fig. 13 — Maximum Drain Current Vs. Case Temperature

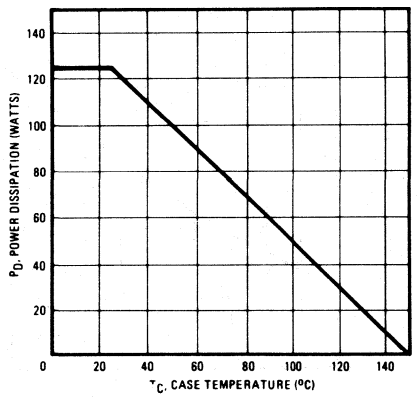


Fig. 14 — Power Vs. Temperature Derating Curve

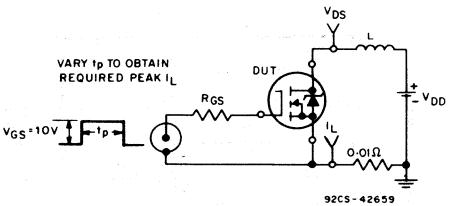


Fig. 15 — Unclamped Energy Test Circuit

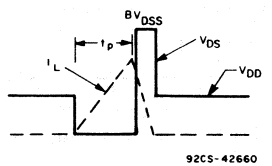


Fig. 16 — Unclamped Energy Waveforms

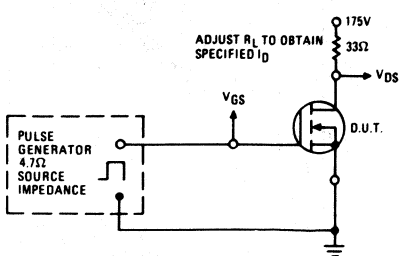


Fig. 17 — Switching Time Test Circuit

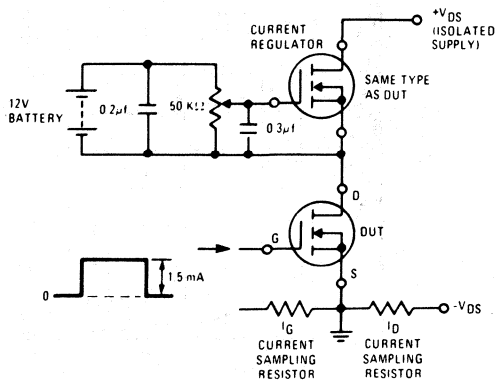


Fig. 18 — Gate Charge Test Circuit

File Number **2156**

IRFAC40R, IRFAC42R

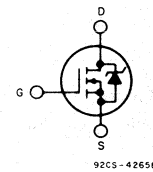
Avalanche-Energy-Rated N-Channel Power MOSFETs

6.2A and 5.4A, 600V
$r_{DS(on)} = 1.2\Omega$ and 1.6Ω

Features:

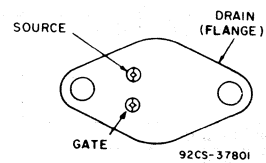
- *Repetitive Avalanche Ratings*
- *Simple Drive Requirements*
- *Ease of Paralleling*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

The IRFAC40R and IRFAC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFAC-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

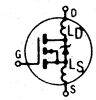
Parameter		IRFAC40R	IRFAC42R	Units
I_D @ T_C = 25°C	Continuous Drain Current	6.2	5.4	A
I_D @ T_C = 100°C	Continuous Drain Current	3.9	3.4	A
I_{DM}	Pulsed Drain Current ①	25	22	A
P_D @ T_C = 25°C	Max. Power Dissipation	125		W
	Linear Derating Factor	1.0		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	570 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ① (Repetitive or Non-Repetitive)	6.2 (See E_{AR})		A
E_{AR}	Repetitive Avalanche Energy ①	13 (See I_{AR})		mJ
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]		°C

IRFAC40R, IRFAC42R

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFAC40R IRFAC42R	600	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFAC40R IRFAC42R	— —	0.97 1.2	1.2 1.6	Ω	V_{GS} = 10V, I_D = 3.4A
$I_{D(on)}$	On-State Drain Current ③	IRFAC40R IRFAC42R	6.2 5.4	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	4.7	70	—	S(℧)	$V_{DS} \geq 50V$, I_{DS} = 3.4A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	— —	— —	250 1000	μA	V_{DS} = Max. Rating, V_{GS} = 0V V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	40	60	nC	V_{GS} = 10V, I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	ALL	—	5.5	8.3	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	20	30	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	13	20	ns	V_{DD} = 300V, I_D = 6.2A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	18	27	ns	R_D = 47Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f	Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	160	—	pF	f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.12	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Typical-socket mount

Modified MOSFET symbol showing the internal inductances.



Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifer.
I_{SM}	Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	450	940	ns	T_J = 25°C, I_F = 6.2A, di/dt = 100A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.8	3.8	7.9	μC	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

③ Pulse width ≤ 300μs; Duty Cycle ≤ 2%

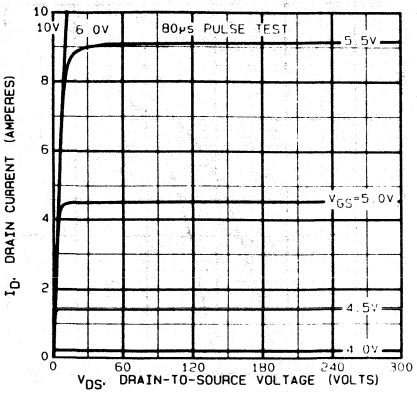


Fig. 1 - Typical Output Characteristics

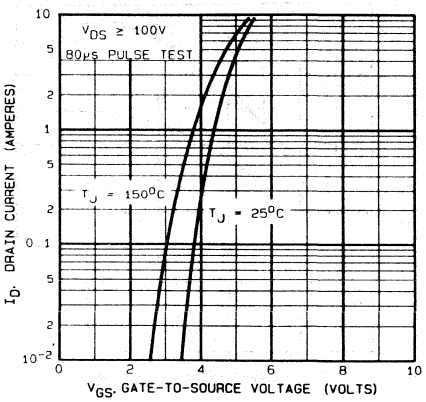


Fig. 2 - Typical Transfer Characteristics

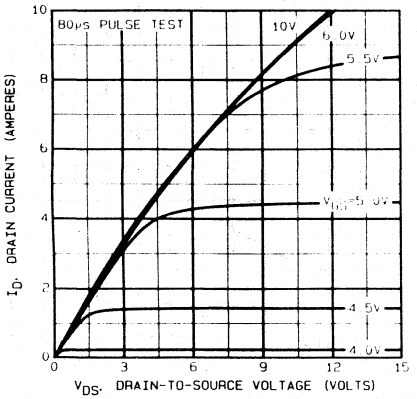


Fig. 3 - Typical Saturation Characteristics

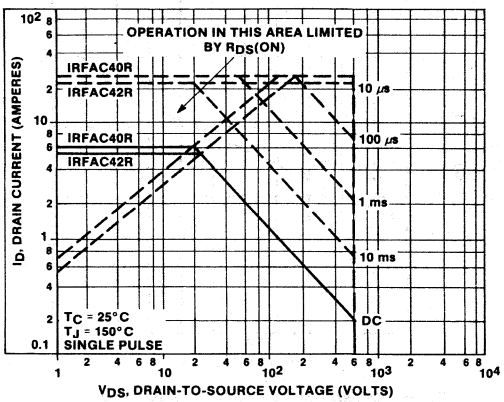


Fig. 4 - Maximum Safe Operating Area

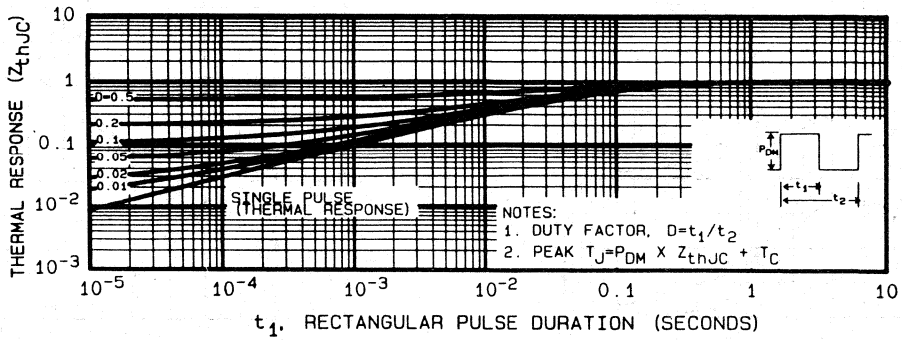


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

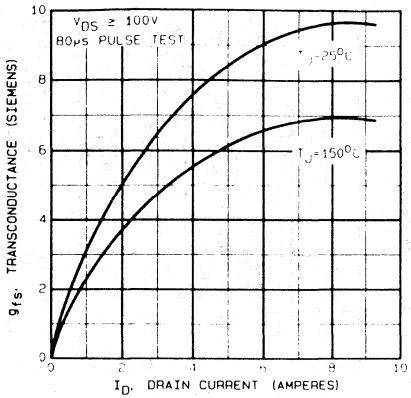


Fig. 6 - Typical Transconductance Vs. Drain Current

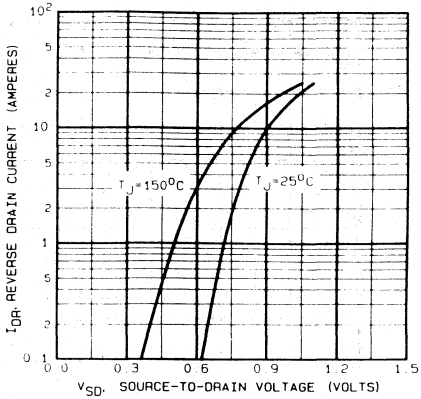


Fig. 7 - Typical Source-Drain Diode Forward Voltage

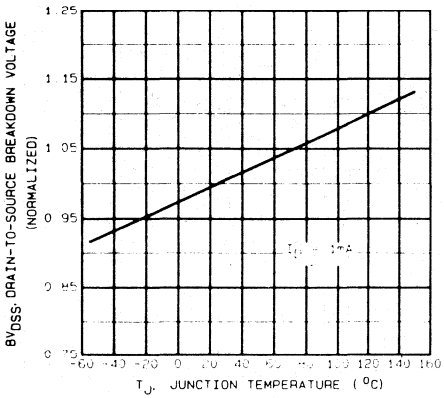


Fig. 8 - Breakdown Voltage Vs. Temperature

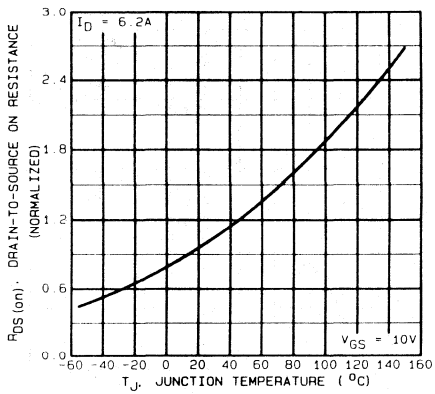


Fig. 9 - Normalized On-Resistance Vs. Temperature

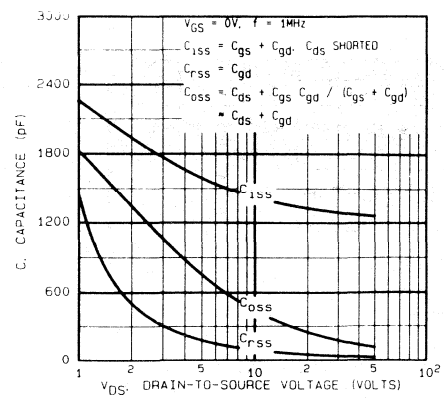


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

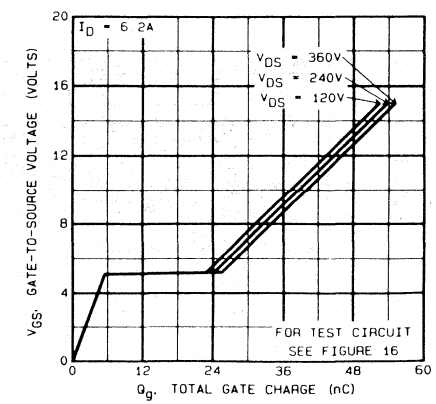


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

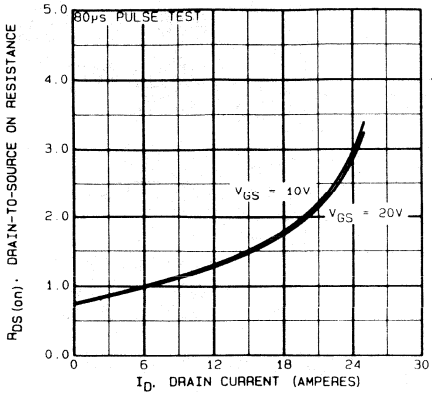


Fig. 12 - Typical On-Resistance Vs. Drain Current

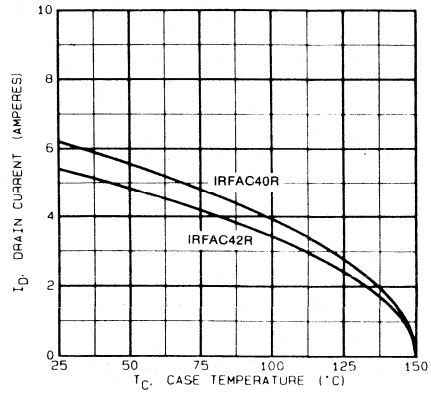


Fig. 13 - Maximum Drain Current Vs. Case Temperature

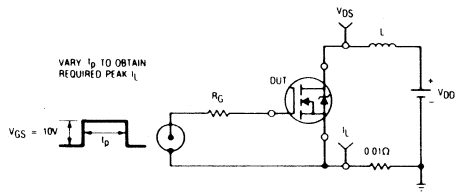


Fig. 14a - Unclamped Inductive Test Circuit

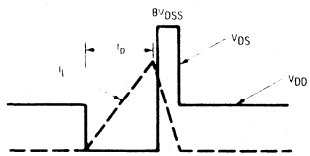


Fig. 14b - Unclamped Inductive Waveforms

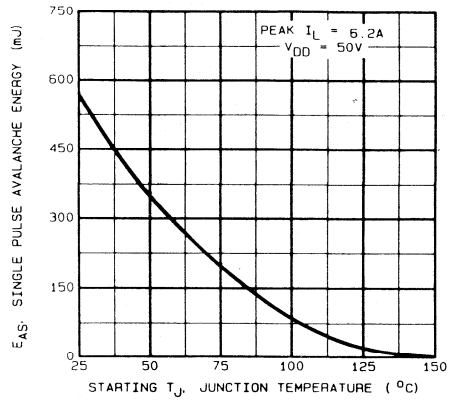


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

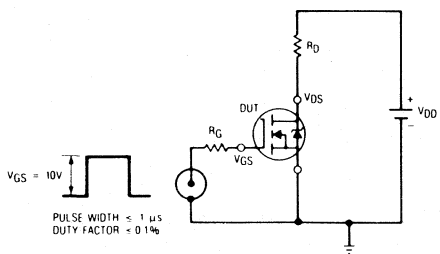


Fig. 15a - Switching Time Test Circuit

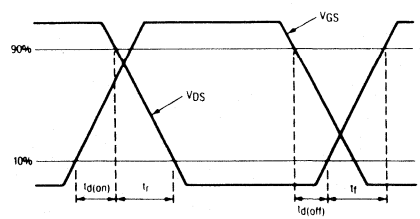


Fig. 15b - Switching Time Waveforms

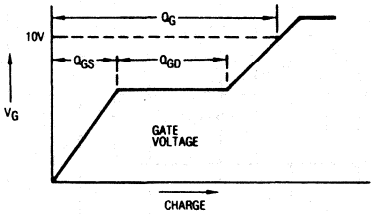
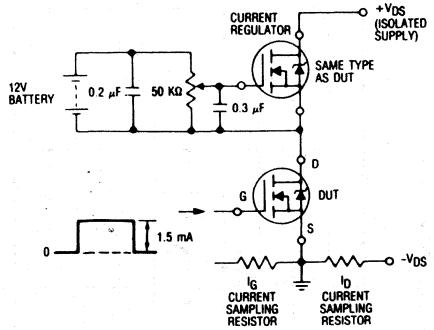


Fig. 16a - Basic Gate Charge Waveform



Fib. 16b - Gate Charge Test Circuit

File Number **2157**

IRFBC40R, IRFBC42R

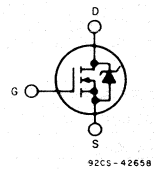
Avalanche-Energy-Rated N-Channel Power MOSFETs

6.2A and 5.4A, 600V
$r_{DS(on)}$ = 1.2Ω and 1.6Ω

Features:

- *Repetitive Avalanche Ratings*
- *Simple Drive Requirements*
- *Ease of Paralleling*

N-CHANNEL ENHANCEMENT MODE

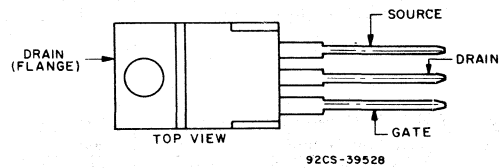


TERMINAL DIAGRAM

The IRFBC40R and IRFBC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFBC-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

Absolute Maximum Ratings

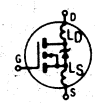
	Parameter	IRFBC40R	IRFBC42R	Units
I_D @ T_C = 25°C	Continuous Drain Current	6.2	5.4	A
I_D @ T_C = 100°C	Continuous Drain Current	3.9	3.4	A
I_{DM}	Pulsed Drain Current ①	25	22	A
P_D @ T_C = 25°C	Max. Power Dissipation	125		W
	Linear Derating Factor	1.0		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	570 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ① (Repetitive or Non-Repetitive)	6.2 (See E_{AR})		A
E_{AR}	Repetitive Avalanche Energy ①	13 (See I_{AR})		mJ
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]		°C

IRFBC40R, IRFBC42R

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFBC40R	600	—	—	V	V_{GS} = 0V, I_D = 250μA
		IRFBC42R					
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFBC40R	—	0.97	1.2	Ω	V_{GS} = 10V, I_D = 3.4A
		IRFBC42R	—	1.2	1.6		
$I_{D(on)}$	On-State Drain Current ③	IRFBC40R	6.2	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
		IRFBC42R	5.4				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	4.7	70	—	S(℧)	$V_{DS} \geq$ 100V, I_{DS} = 3.4A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	40	60	nC	V_{GS} = 10V, I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	ALL	—	5.5	8.3	nC	V_{DS} = 0.7 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	20	30	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	13	20	ns	V_{DD} = 300V, I_D = 6.2A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	18	27	ns	R_D = 47Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f	Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	160	—	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	45	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.50	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Typical-socket mount

Modified MOSFET symbol showing the internal inductances.



Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	450	940	ns	T_J = 25°C, I_F = 6.2A, di/dt = 100A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.8	3.8	8.0	μC	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

③ Pulse width ≤ 300μs; Duty Cycle ≤ 2%

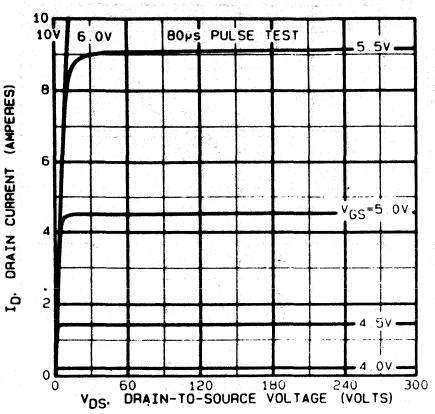


Fig. 1 - Typical Output Characteristics

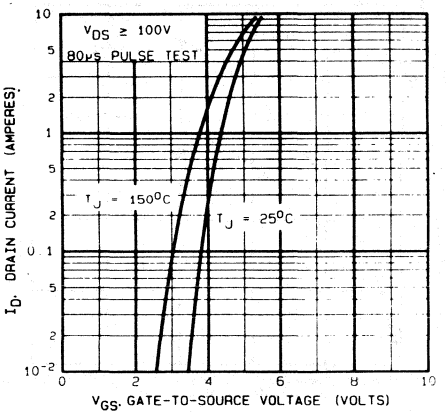


Fig. 2 - Typical Transfer Characteristics

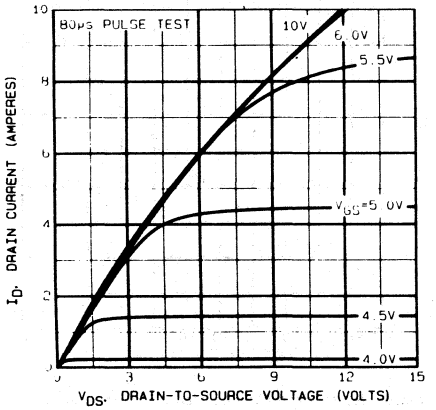


Fig. 3 - Typical Saturation Characteristics

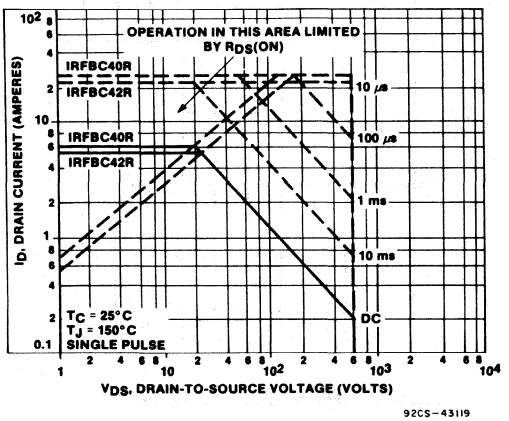


Fig. 4 - Maximum Safe Operating Area

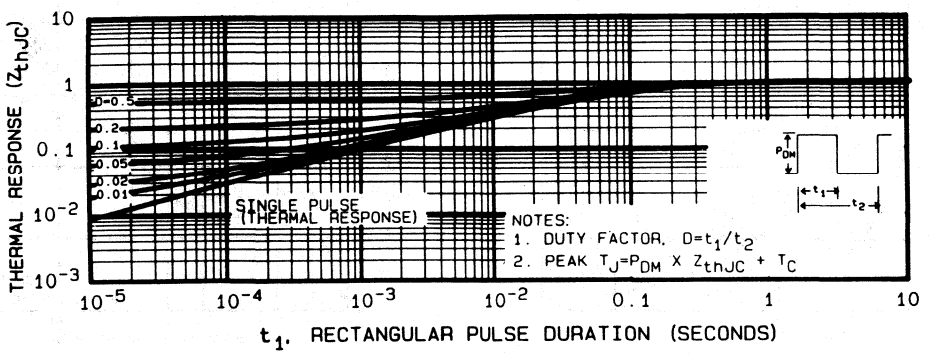


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

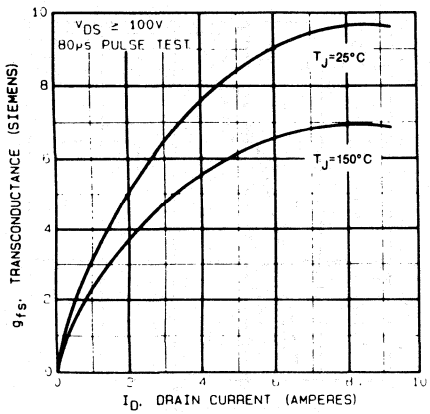


Fig. 6 - Typical Transconductance Vs. Drain Current

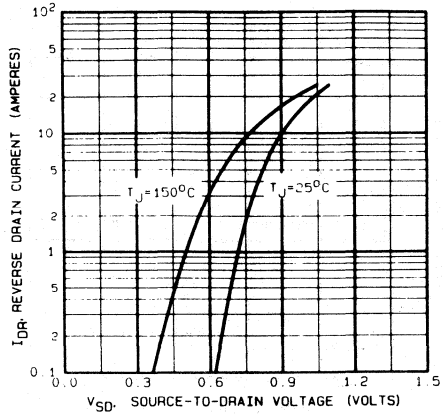


Fig. 7 - Typical Source-Drain Diode Forward Voltage

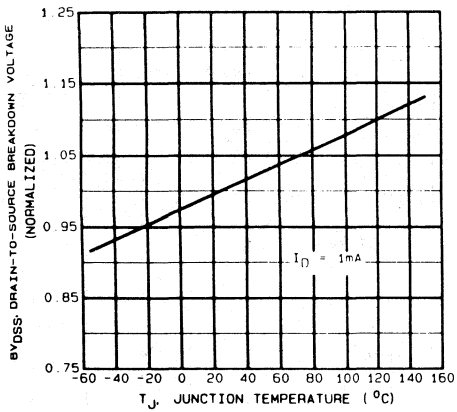


Fig. 8 - Breakdown Voltage Vs. Temperature

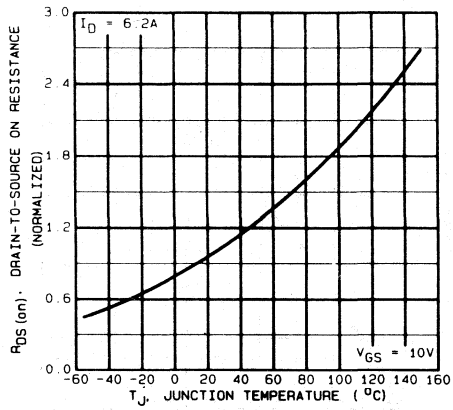


Fig. 9 - Normalized On-Resistance Vs. Temperature

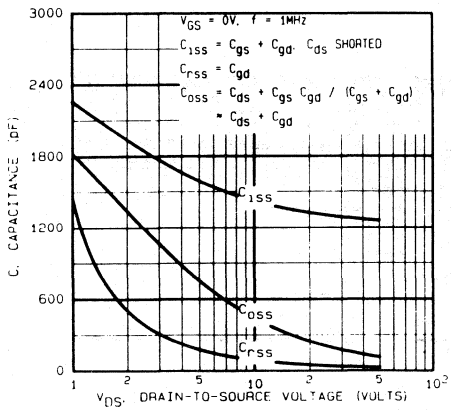


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

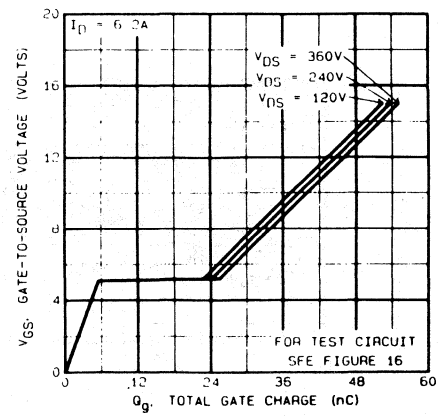


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

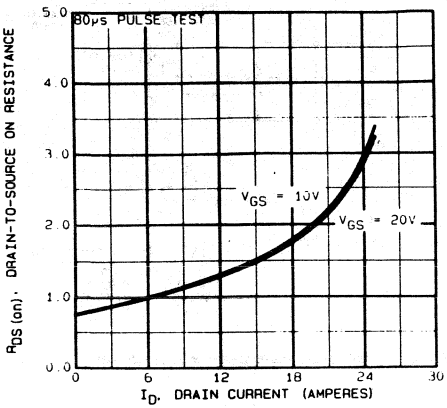


Fig. 12 - Typical On-Resistance Vs. Drain Current

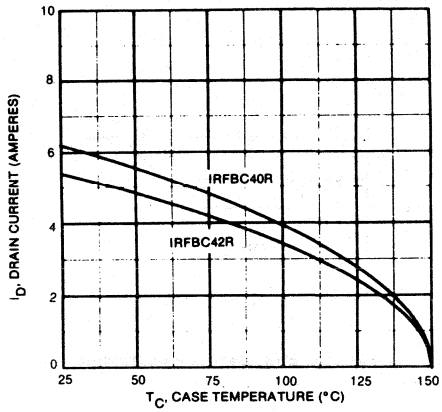


Fig. 13 - Maximum Drain Current Vs. Case Temperature

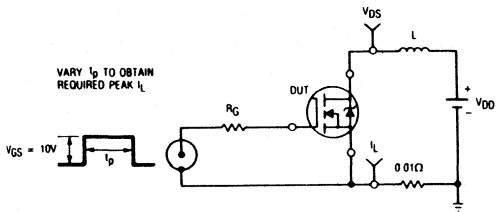


Fig. 14a - Unclamped Inductive Test Circuit

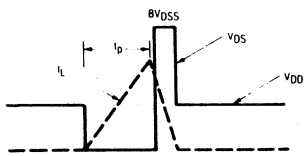


Fig. 14b - Unclamped Inductive Waveforms

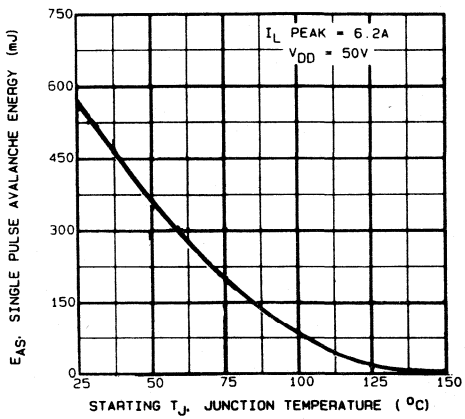


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

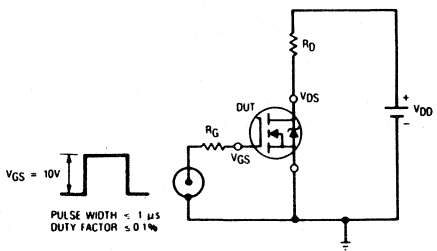


Fig. 15a - Switching Time Test Circuit

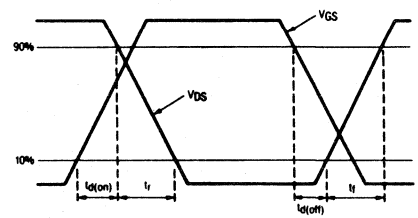


Fig. 15b - Switching Time Waveforms

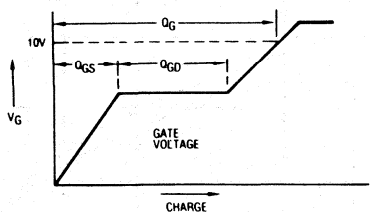


Fig. 16a - Basic Gate Charge Waveform

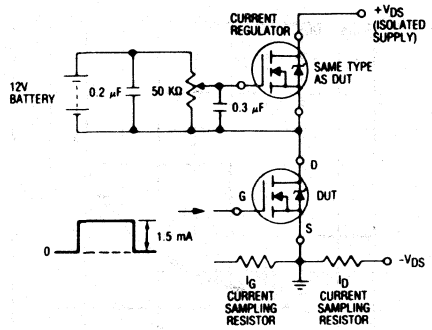


Fig. 16b - Gate Charge Test Circuit

File Number **2035**

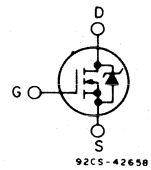
IRFD110R, IRFD111R, IRFD112R, IRFD113R

Avalanche Energy Rated N-Channel Power MOSFETs

1A and 0.8A, 60V-100V
$r_{DS}(on) = 0.6\Omega$ and 0.8Ω

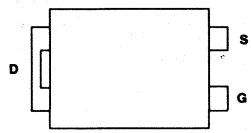
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



TOP VIEW

4-PIN DIP

The IRFD110R, IRFD111R, IRFD112R and IRFD113R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

Absolute Maximum Ratings

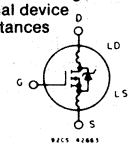
Parameter		IRFD110R	IRFD111R	IRFD112R	IRFD113R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current	8.0	8.0	6.4	6.4	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ③	19				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD110R, IRFD111R, IRFD112R, IRFD113R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD110R IRFD112R	100	—	—	V	V_{GS} = 0V
		IRFD111R IRFD113R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD110R IRFD111R	1.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFD112R IRFD113R	0.8	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD110R IRFD111R	—	0.5	0.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRFD112R IRFD113R	—	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.2	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.8A
C_{iss}	Input Capacitance	ALL	—	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	80	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.8A, Z_0 = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	11	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8V Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD110R IRFD111R	—	—	1.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD112R IRFD113R	—	—	0.8	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD110R IRFD111R	—	—	8.0	A	
		IRFD112R IRFD113R	—	—	6.4	A	
V_{SD}	Diode Forward Voltage ②	IRFD110R IRFD111R	—	—	2.5	V	T_A = 25°C, I_S = 1.0A, V_{GS} = 0V
		IRFD112R IRFD113R	—	—	2.0	V	T_A = 25°C, I_S = 0.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	100	—	ns	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	0.2	—	μC	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ V_{DD} = 25V, starting T_J = 25°C, L = 23.25mH, R_{gs} = 25Ω, I_{peak} = 3.5A. See figs. 15, 16.

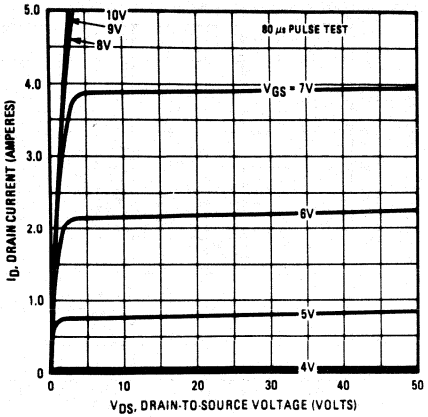


Fig. 1 — Typical Output Characteristics

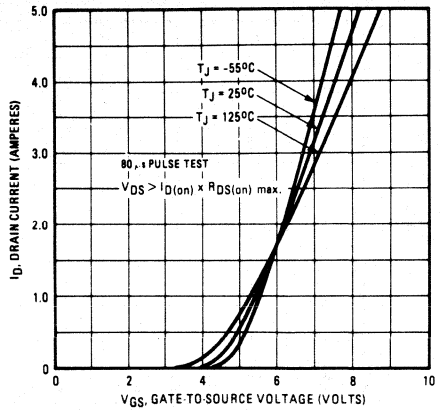


Fig. 2 — Typical Transfer Characteristics

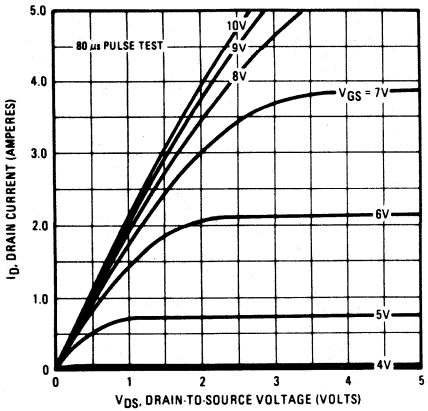


Fig. 3 — Typical Saturation Characteristics

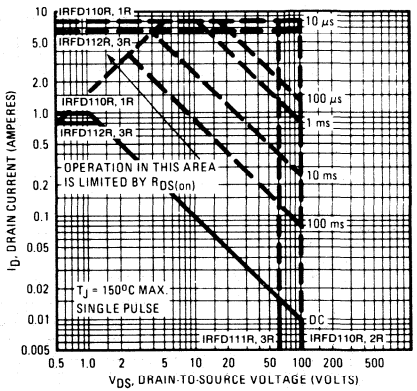


Fig. 4 — Maximum Safe Operating Area

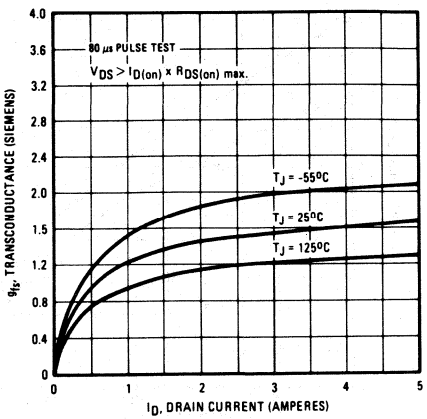


Fig. 5 — Typical Transconductance Vs. Drain Current

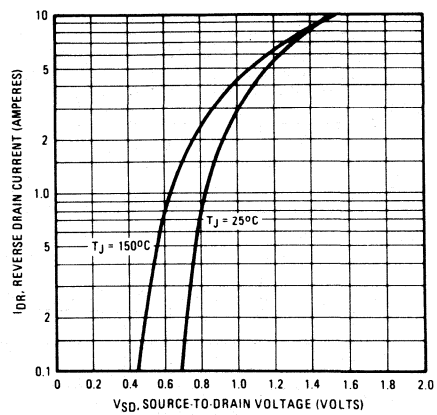


Fig. 6 — Typical Source-Drain Diode Forward Voltage

IRFD110R, IRFD111R, IRFD112R, IRFD113R

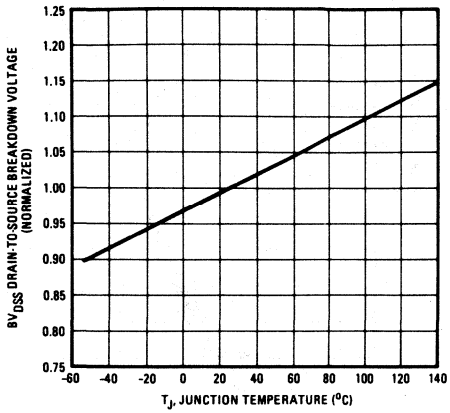


Fig. 7 – Breakdown Voltage Vs. Temperature

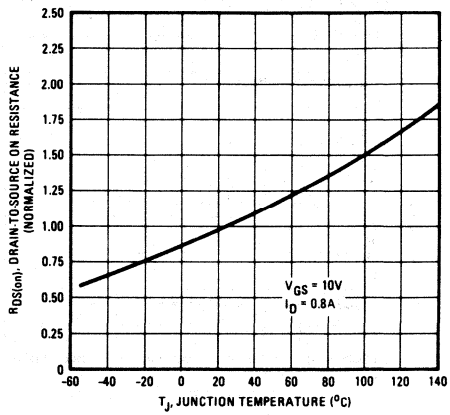


Fig. 8 – Normalized On-Resistance Vs. Temperature

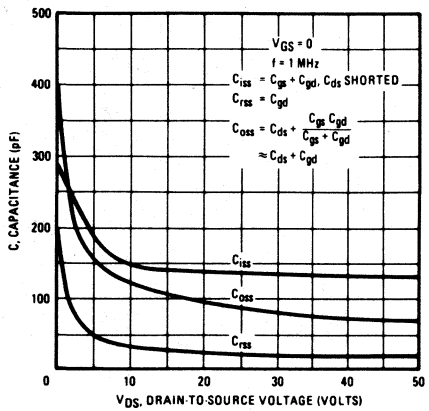


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

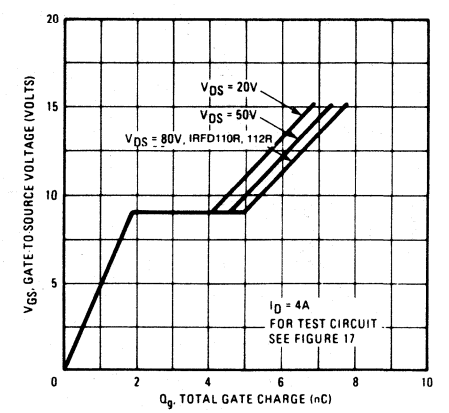


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

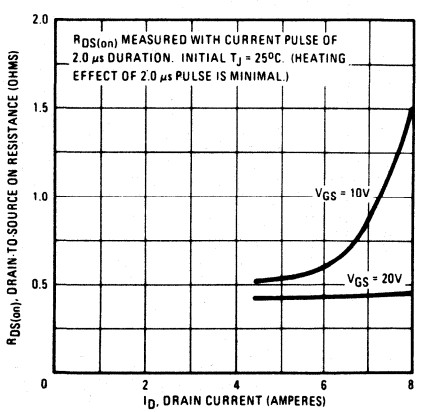


Fig. 11 – Typical On-Resistance Vs. Drain Current

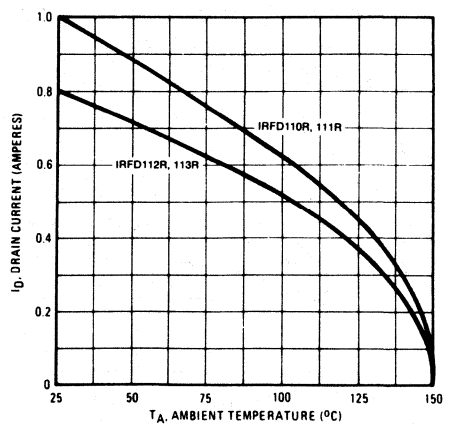


Fig. 12 – Maximum Drain Current Vs. Case Temperature

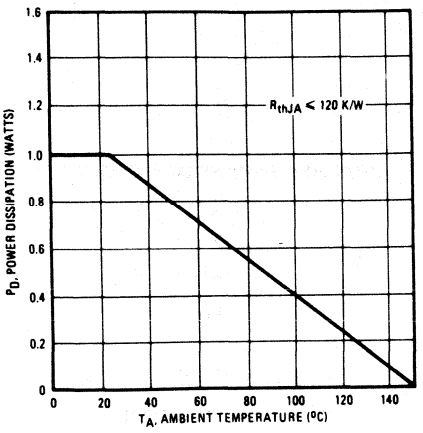


Fig. 13 – Power Vs. Temperature Derating Curve

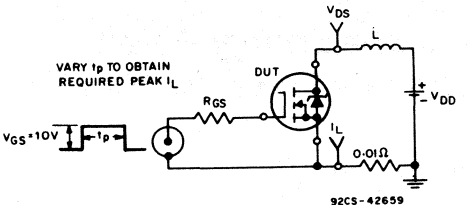


Fig. 14 — Unclamped Energy Test Circuit

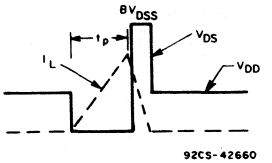


Fig. 15 — Unclamped Energy Waveforms

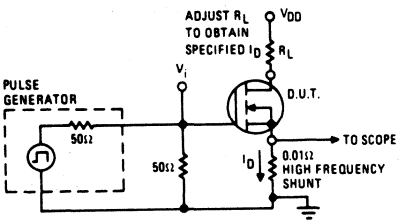


Fig. 16 – Switching Time Test Circuit

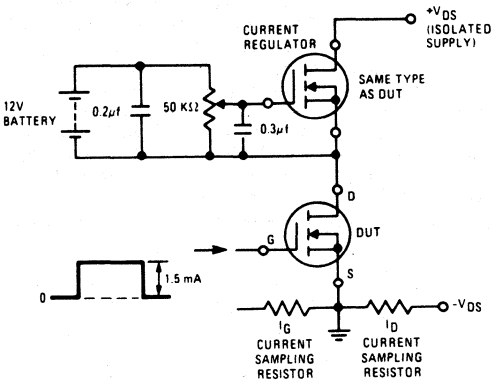


Fig. 17 – Gate Charge Test Circuit

IRFD120R, IRFD121R, IRFD122R, IRFD123R

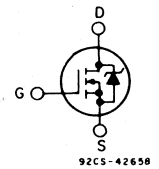
File Number **2036**

Avalanche Energy Rated N-Channel Power MOSFETs

1.3A and 1.1A, 60V-100V
$r_{DS}(on) = 0.30\Omega$ and 0.40Ω

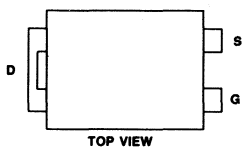
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



4-PIN DIP

The IRFD120R, IRFD121R, IRFD122R and IRFD123R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

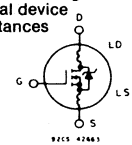
Absolute Maximum Ratings

Parameter		IRFD120R	IRFD121R	IRFD122R	IRFD123R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	1.3	1.3	1.1	1.1	A
I_{DM}	Pulsed Drain Current	5.2	5.2	4.4	4.4	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ③	36				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD120R IRFD122R	100	—	—	V	V_{GS} = 0V
		IRFD121R IRFD123R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD120R IRFD121R	1.3	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFD122R IRFD123R	1.1	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD120R IRFD121R	—	0.25	0.30	Ω	V_{GS} = 10V, I_D = 0.6A
		IRFD122R IRFD123R	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.9	1.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.6A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.6A, Z_0 = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	18	nC	V_{GS} = 10V, I_D = 5.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	5.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD120R IRFD121R	—	—	1.3	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD122R IRFD123R	—	—	1.1	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD120R IRFD121R	—	—	5.2	A	
		IRFD122R IRFD123R	—	—	4.4	A	
V_{SD}	Diode Forward Voltage ②	IRFD120R IRFD121R	—	—	2.5	V	T_C = 25°C, I_S = 1.3A, V_{GS} = 0V
		IRFD122R IRFD123R	—	—	2.3	V	T_C = 25°C, I_S = 1.1A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	280	—	ns	T_J = 150°C, I_F = 1.3A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.6	—	μC	T_J = 150°C, I_F = 1.3A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ V_{DD} = 25V, starting T_J = 25°C, L = 15mH, R_{gs} = 25Ω, I_{peak} = 6A. See figs. 15, 16.

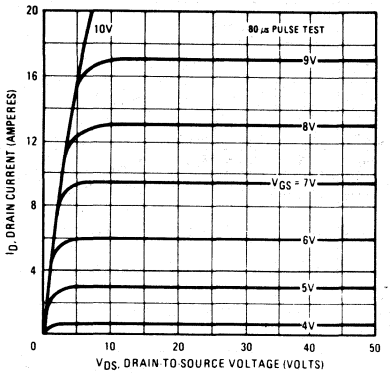


Fig. 1 – Typical Output Characteristics

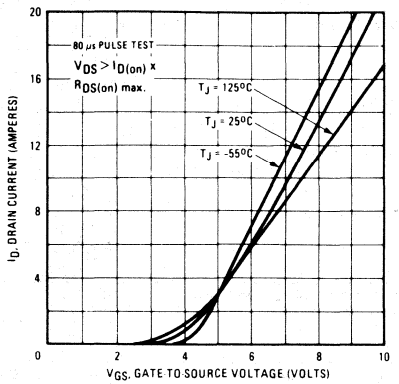


Fig. 2 – Typical Transfer Characteristics

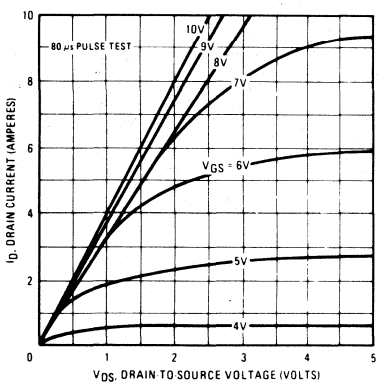


Fig. 3 – Typical Saturation Characteristics

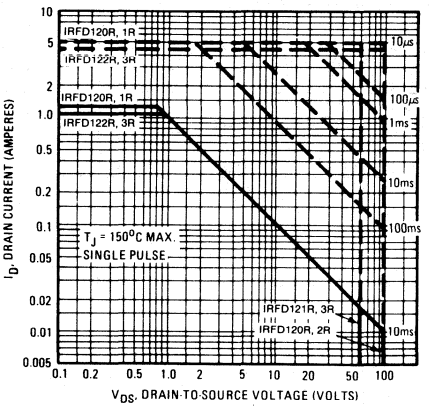


Fig. 4 – Maximum Safe Operating Area

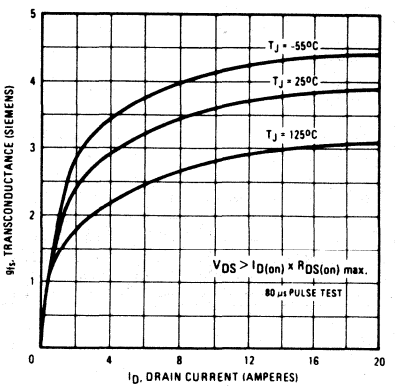


Fig. 5 – Typical Transconductance Vs. Drain Current

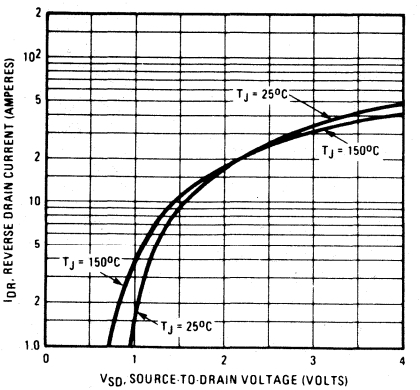


Fig. 6 – Typical Source-Drain Diode Forward Voltage

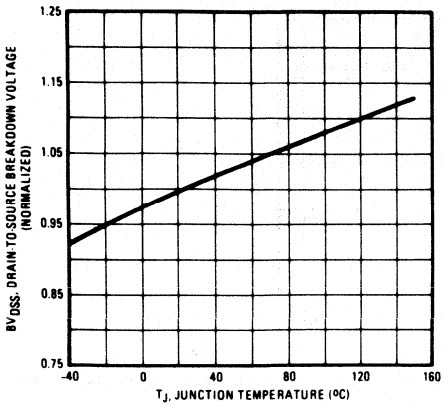


Fig. 7 – Breakdown Voltage Vs. Temperature

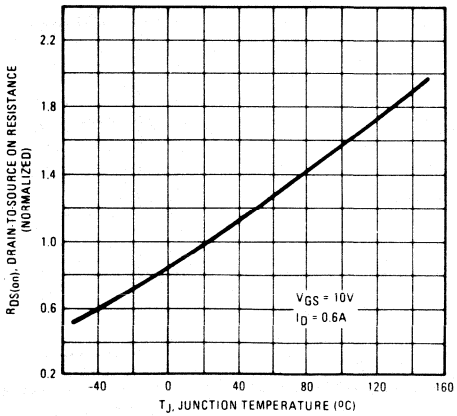


Fig. 8 – Normalized On-Resistance Vs. Temperature

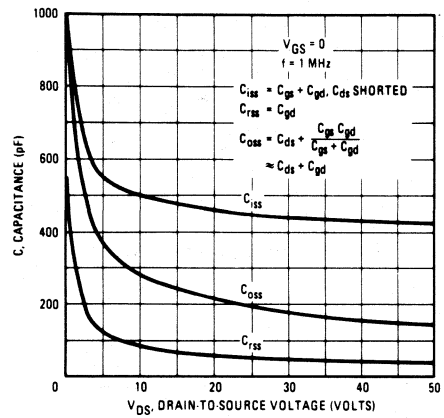


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

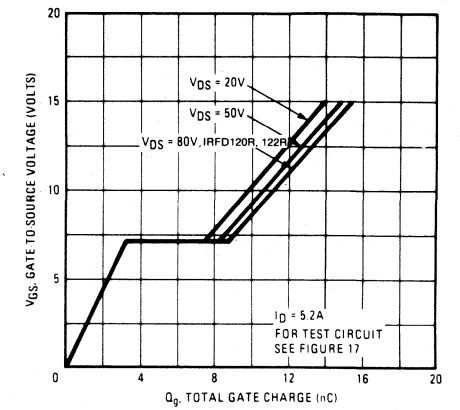


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

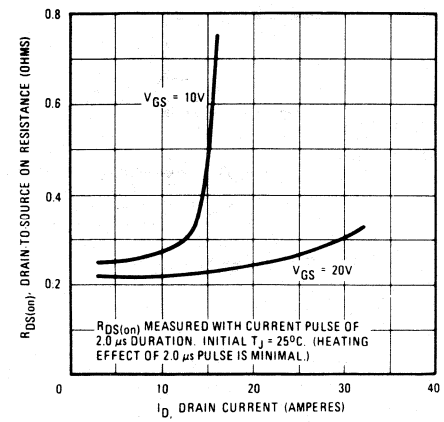


Fig. 11 – Typical On-Resistance Vs. Drain Current

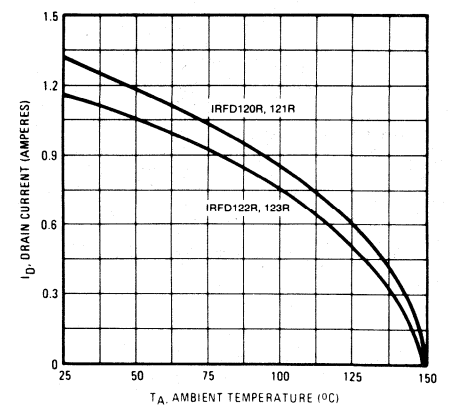


Fig. 12 – Maximum Drain Current Vs. Case Temperature

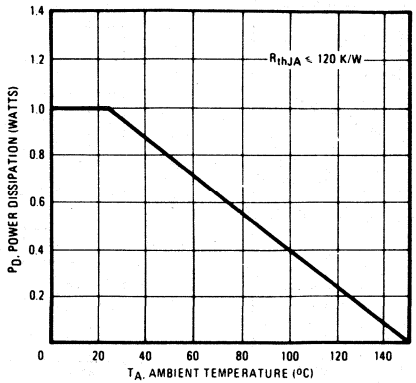


Fig. 13 — Power Vs. Temperature Derating Curve

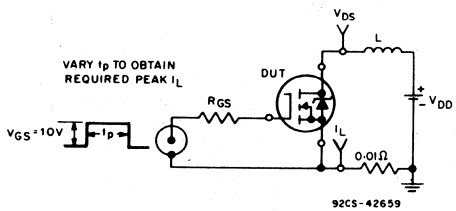


Fig. 14 — Unclamped Energy Test Circuit

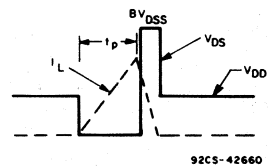


Fig. 15 — Unclamped Energy Waveforms

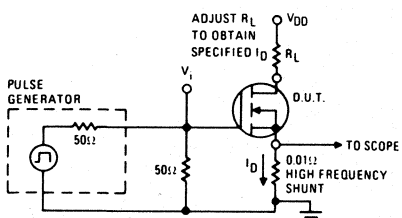


Fig. 16 — Switching Time Test Circuit

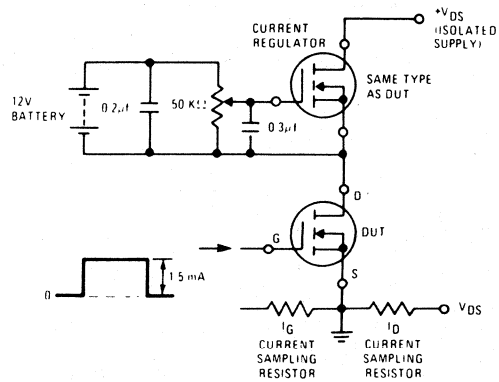


Fig. 17 — Gate Charge Test Circuit

File Number **2037**

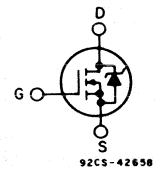
IRFD210R, IRFD211R, IRFD212R, IRFD213R

Avalanche Energy Rated N-Channel Power MOSFETs

0.6A and 0.45A, 150V-200V
$r_{DS}(on) = 1.5\Omega$ and 2.4Ω

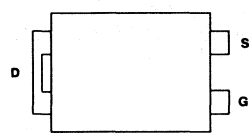
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



4-PIN DIP

The IRFD210R, IRFD211R, IRFD212R and IRFD213R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

Absolute Maximum Ratings

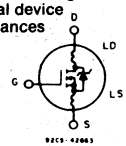
Parameter		IRFD210R	IRFD211R	IRFD212R	IRFD213R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	0.6	0.6	0.45	0.45	A
I_{DM}	Pulsed Drain Current	2.5	2.5	1.8	1.8	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ③	30				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD210R, IRFD211R, IRFD212R, IRFD213R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD210R IRFD212R	200	—	—	V	V_{GS} = 0V
		IRFD211R IRFD213R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD210R IRFD211R	0.6	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRFD212R IRFD213R	0.45	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD210R IRFD211R	—	1.0	1.5	Ω	V_{GS} = 10V, I_D = 0.3A
		IRFD212R IRFD213R	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	0.8	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.3A
C_{iss}	Input Capacitance	ALL	—	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	60	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	16	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.3A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8V Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD210R IRFD211R	—	—	0.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD212R IRFD213R	—	—	0.45	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD210R IRFD211R	—	—	2.5	A	
		IRFD212R IRFD213R	—	—	1.8	A	
V_{SD}	Diode Forward Voltage ②	IRFD210R IRFD211R	—	—	2.0	V	T_C = 25°C, I_S = 0.6A, V_{GS} = 0V
		IRFD212R IRFD213R	—	—	1.8	V	T_C = 25°C, I_S = 0.45A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	T_J = 150°C, I_F = 0.6A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	T_J = 150°C, I_F = 0.6A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ V_{DD} = 20V, starting T_J = 25°C, L = 112.7mH, R_{gs} = 50Ω, I_{peak} = 2.2A. See figs. 15, 16.

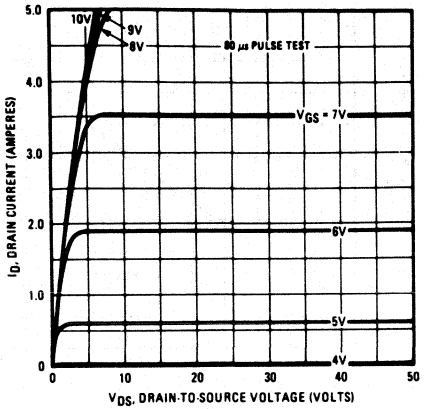


Fig. 1 – Typical Output Characteristics

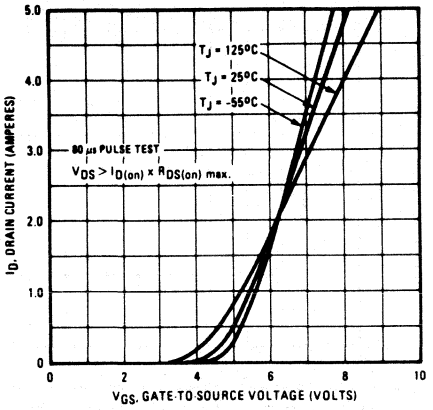


Fig. 2 – Typical Transfer Characteristics

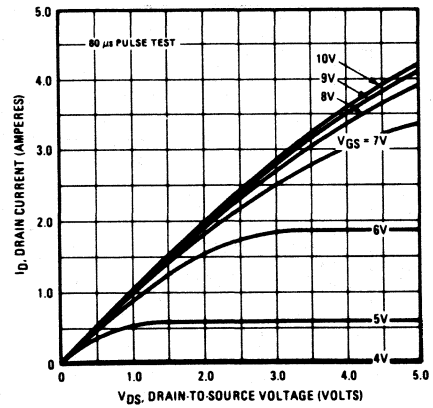


Fig. 3 – Typical Saturation Characteristics

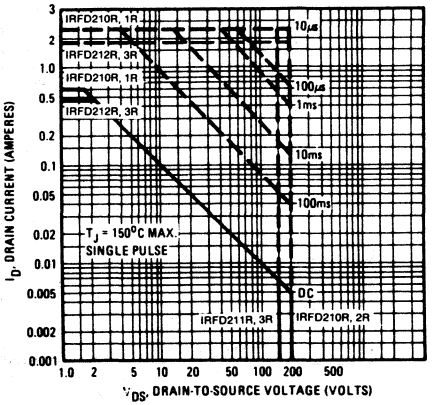


Fig. 4 – Maximum Safe Operating Area

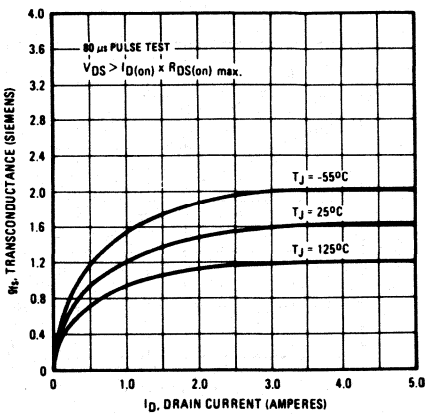


Fig. 5 – Typical Transconductance Vs. Drain Current

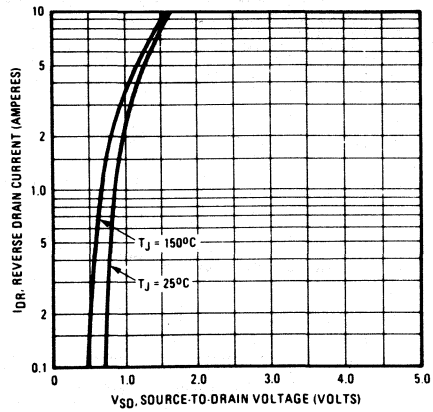


Fig. 6 – Typical Source-Drain Diode Forward Voltage

IRFD210R, IRFD211R, IRFD212R, IRFD213R

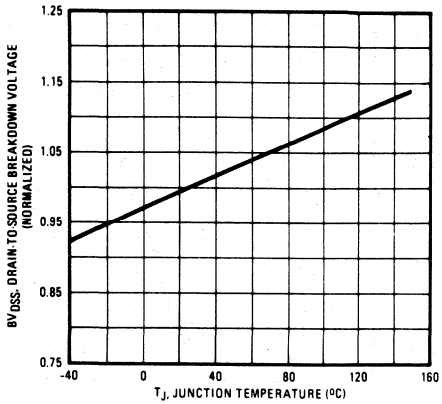


Fig. 7 – Breakdown Voltage Vs. Temperature

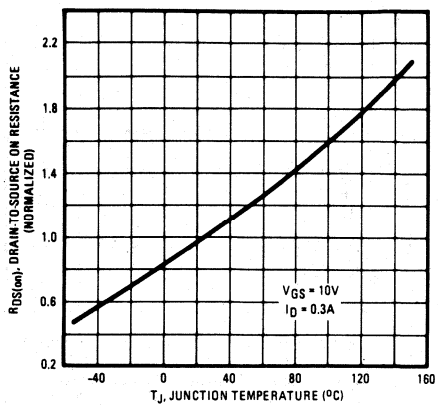


Fig. 8 – Normalized On-Resistance Vs. Temperature

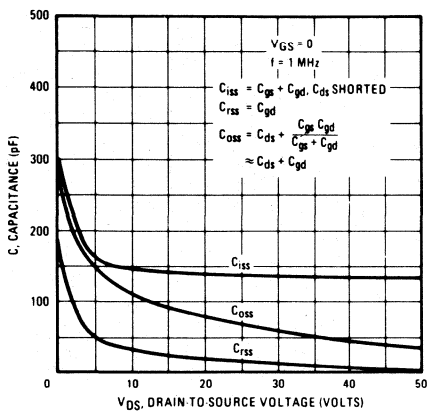


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

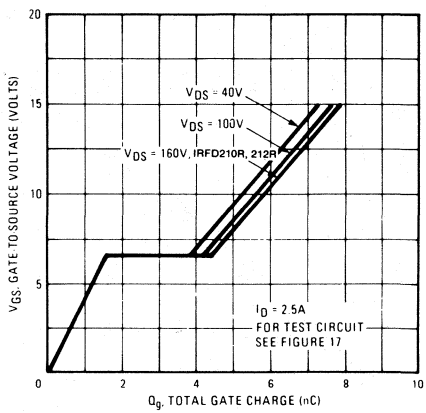


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

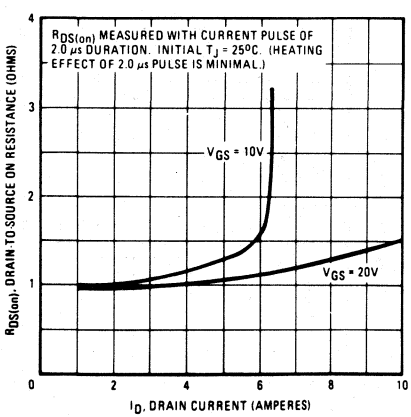


Fig. 11 – Typical On-Resistance Vs. Drain Current

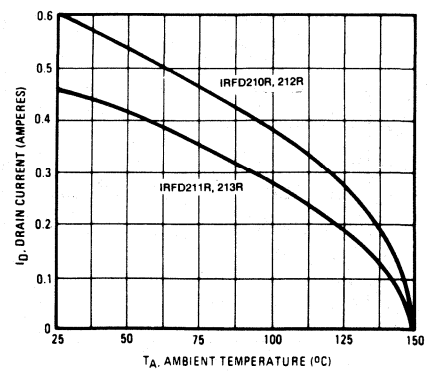


Fig. 12 – Maximum Drain Current Vs. Case Temperature

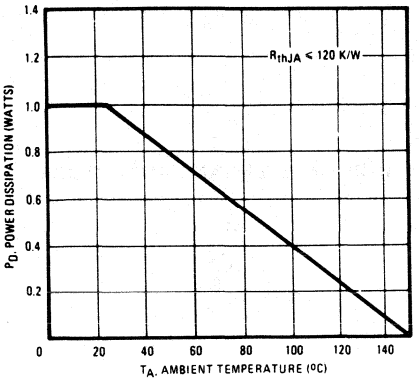


Fig. 13 — Power Vs. Temperature Derating Curve

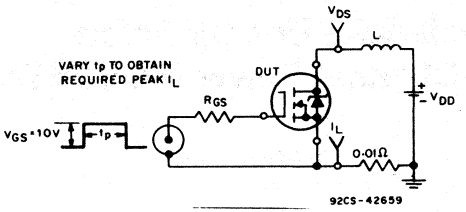


Fig. 14 — Unclamped Energy Test Circuit

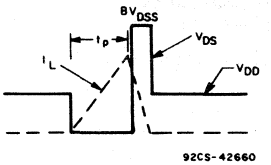


Fig. 15 — Unclamped Energy Waveforms

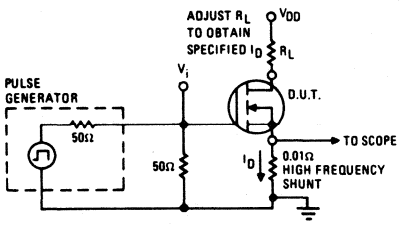


Fig. 16 — Switching Time Test Circuit

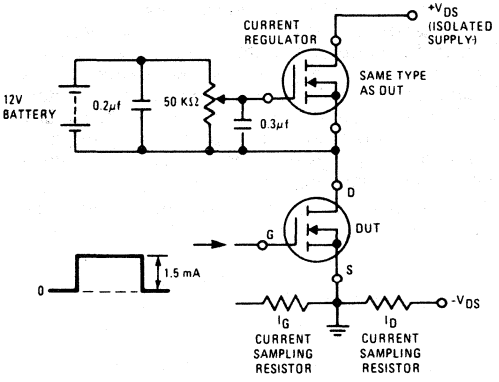


Fig. 17 — Gate Charge Test Circuit

IRFD220R, IRFD221R, IRFD222R, IRFD223R

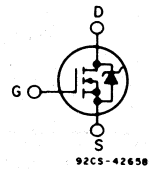
File Number **2038**

Avalanche Energy Rated N-Channel Power MOSFETs

0.8A and 0.7A, 150V-200V
$r_{DS}(on) = 0.8\Omega$ and 1.2Ω

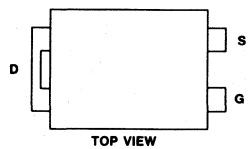
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



4-PIN DIP

The IRFD220R, IRFD221R, IRFD222R and IRFD223R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

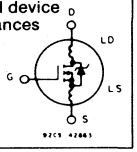
Absolute Maximum Ratings

Parameter		IRFD220R	IRFD221R	IRFD222R	IRFD223R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	0.8	0.8	0.7	0.7	A
I_{DM}	Pulsed Drain Current	6.4	6.4	5.6	5.6	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ③	85				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD220R IRFD222R	200	—	—	V	V_{GS} = 0V
		IRFD221R IRFD223R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD220R IRFD221R	0.8	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFD222R IRFD223R	0.7	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD220R IRFD221R	—	0.5	0.8	Ω	V_{GS} = 10V, I_D = 0.4A
		IRFD222R IRFD223R	—	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.1	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.4A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.4A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8V Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	5.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD220R IRFD221R	—	—	0.8	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD222R IRFD223R	—	—	0.7	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD220R IRFD221R	—	—	6.4	A	
		IRFD222R IRFD223R	—	—	5.6	A	
V_{SD}	Diode Forward Voltage ②	IRFD220R IRFD221R	—	—	2.0	V	T_A = 25°C, I_S = 0.8A, V_{GS} = 0V
		IRFD222R IRFD223R	—	—	1.8	V	T_A = 25°C, I_S = 0.7A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	150	—	ns	T_J = 150°C, I_F = 0.8A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	0.6	—	μC	T_J = 150°C, I_F = 0.8A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ V_{DD} = 25V, starting T_J = 25°C, L = 12.62mH, R_{gs} = 50Ω, I_{peak} = 3.5A. See figs. 15, 16.

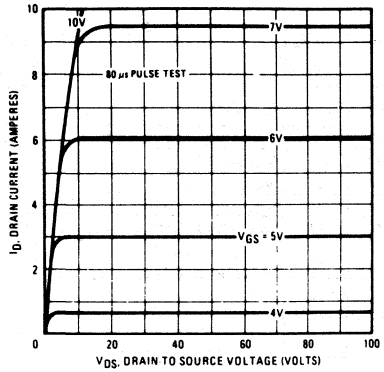


Fig. 1 – Typical Output Characteristics

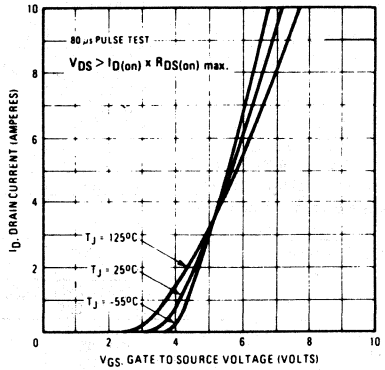


Fig. 2 – Typical Transfer Characteristics

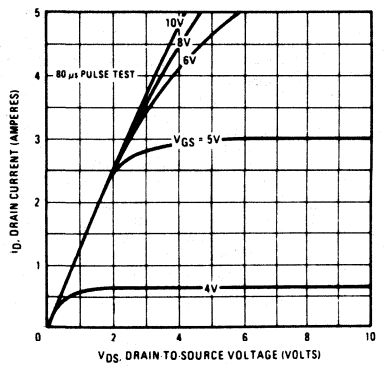


Fig. 3 – Typical Saturation Characteristics

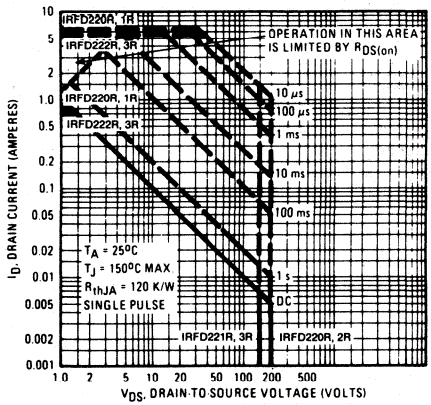


Fig. 4 – Maximum Safe Operating Area

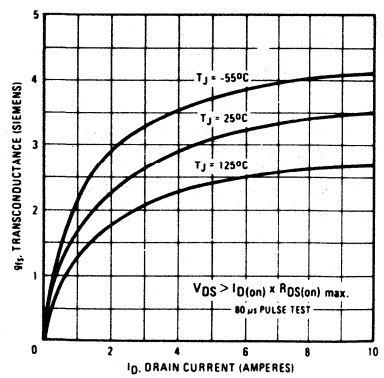


Fig. 5 – Typical Transconductance Vs. Drain Current

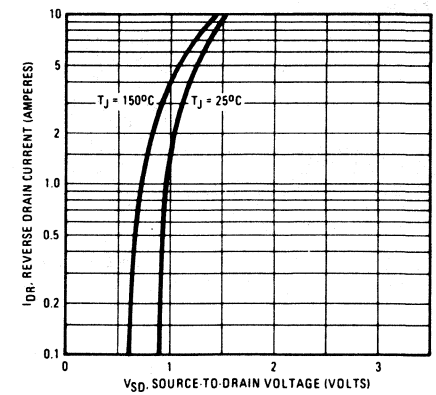


Fig. 6 – Typical Source-Drain Diode Forward Voltage

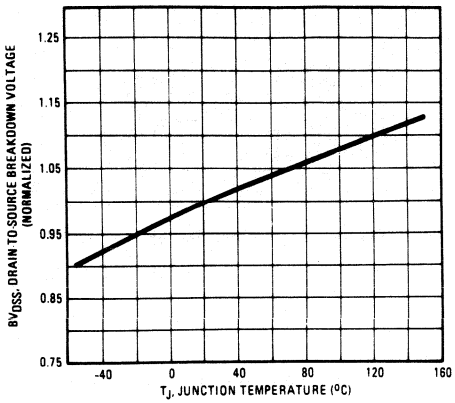


Fig. 7 – Breakdown Voltage Vs. Temperature

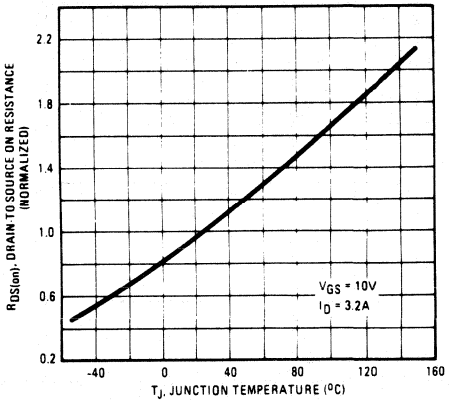


Fig. 8 – Normalized On-Resistance Vs. Temperature

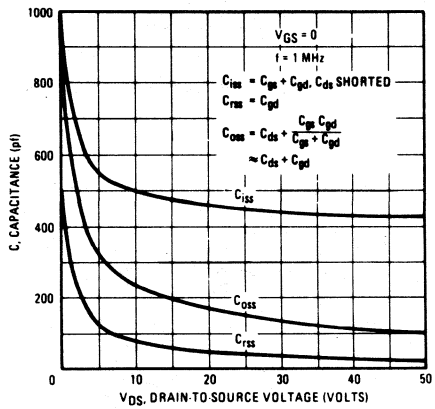


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

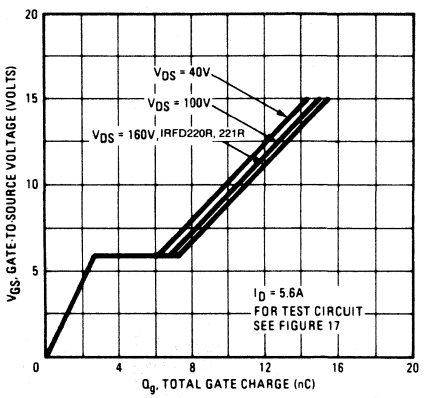


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

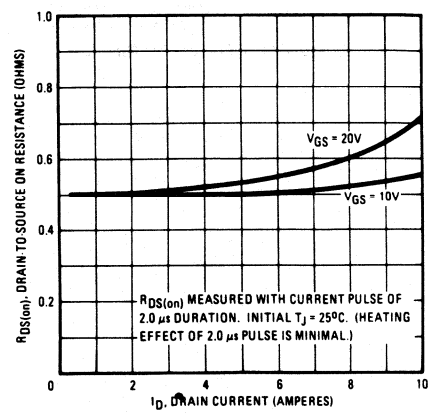


Fig. 11 – Typical On-Resistance Vs. Drain Current

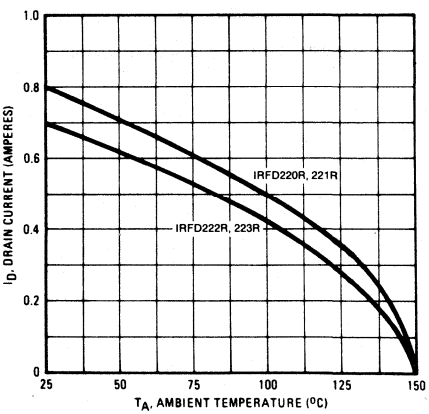


Fig. 12 – Maximum Drain Current Vs. Case Temperature

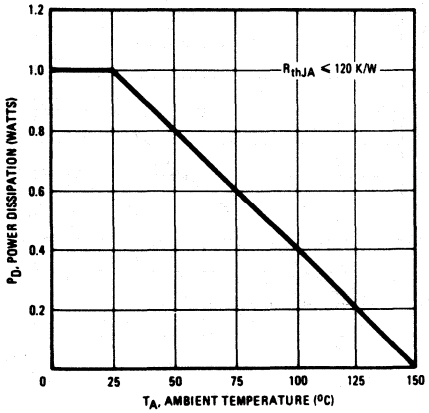


Fig. 13 — Power Vs. Temperature Derating Curve

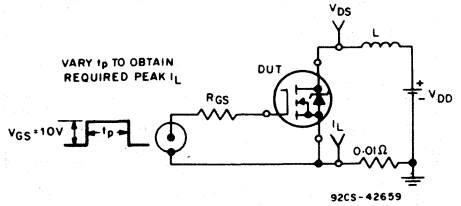


Fig. 14 — Unclamped Energy Test Circuit

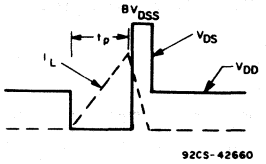


Fig. 15 — Unclamped Energy Waveforms

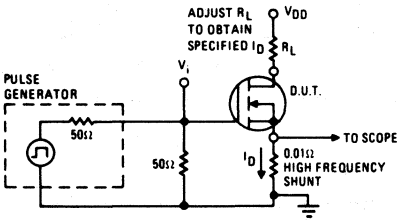


Fig. 16 — Switching Time Test Circuit

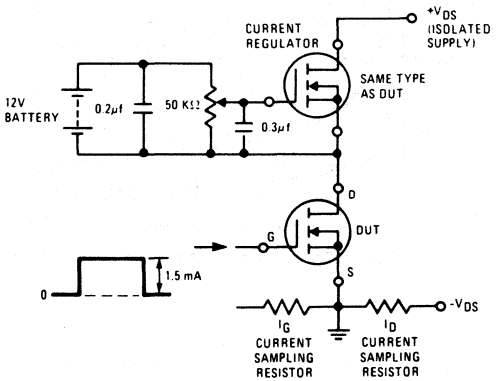


Fig. 17 — Gate Charge Test Circuit

File Number **2039**

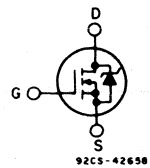
IRFD310R, IRFD311R, IRFD312R, IRFD313R

Avalanche Energy Rated N-Channel Power MOSFETs

0.3A and 0.4A, 350V-400V
$r_{DS}(on) = 3.6\Omega$ and 5.0Ω

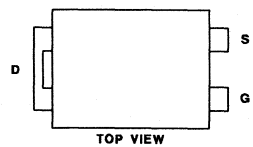
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



4-PIN DIP

The IRFD310R, IRFD311R, IRFD312R and IRFD313R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

Absolute Maximum Ratings

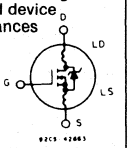
Parameter		IRFD310R	IRFD311R	IRFD312R	IRFD313R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
I_D @ $T_C = 25°C$	Continuous Drain Current	0.4	0.4	0.3	0.3	A
I_{DM}	Pulsed Drain Current ③	1.6	1.6	1.2	1.2	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	1.0 (See Fig. 14)				W
	Linear Derating Factor	0.008 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	45				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD310R, IRFD311R, IRFD312R, IRFD313R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD310R IRFD312R	400	—	—	V	V_{GS} = 0V
		IRFD311R IRFD313R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD310R IRFD311R	0.4	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFD312R IRFD313R	0.3	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD310R IRFD311R	—	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.2A
		IRFD312R IRFD313R	—	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.2A
C_{iss}	Input Capacitance	ALL	—	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	35	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	8.0	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	3.0	10	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.2A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	5.0	10	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	V_{GS} = 10V, I_D = 0.4A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	3.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD310R IRFD311R	—	—	0.4	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD312R IRFD313R	—	—	0.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFD310R IRFD311R	—	—	1.6	A	
		IRFD312R IRFD313R	—	—	1.2	A	
V_{SD}	Diode Forward Voltage ②	IRFD310R IRFD311R	—	—	1.6	V	T_C = 25°C, I_S = 1.6A, V_{GS} = 0V
		IRFD312R IRFD313R	—	—	1.5	V	T_C = 25°C, I_S = 1.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	T_J = 150°C, I_F = 1.6A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.7	—	μC	T_J = 150°C, I_F = 1.6A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 40V, starting T_J = 25°C, L = 44.89mH, R_{gs} = 50Ω, I_{peak} = 1.4A. See figs. 14, 15.

IRFD310R, IRFD311R, IRFD312R, IRFD313R

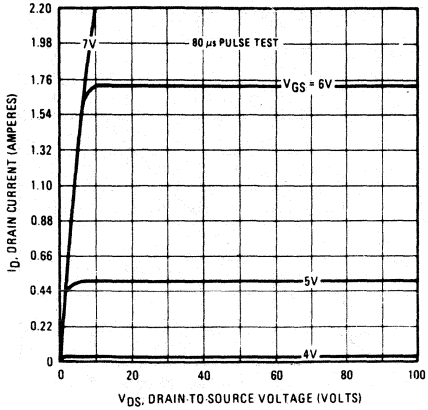


Fig. 1 — Typical Output Characteristics

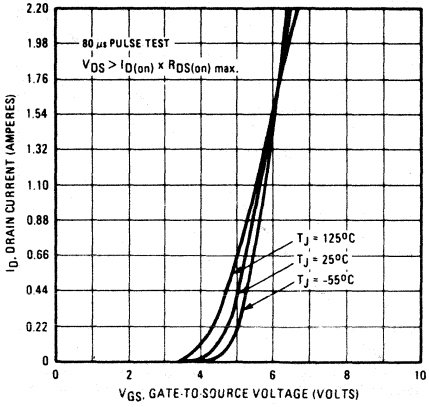


Fig. 2 — Typical Transfer Characteristics

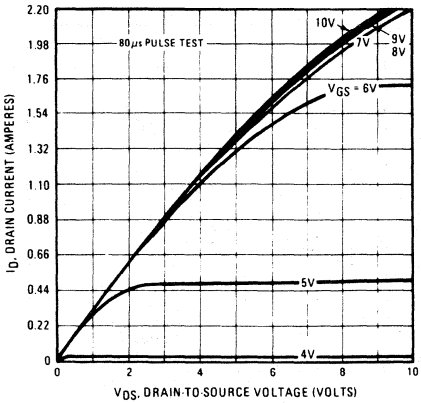


Fig. 3 — Typical Saturation Characteristics

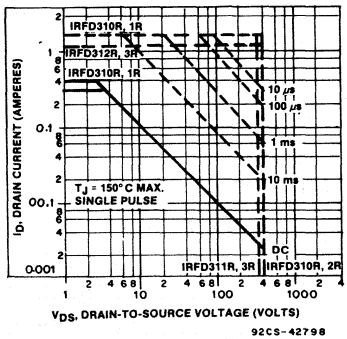


Fig. 4 — Maximum Safe Operating Area

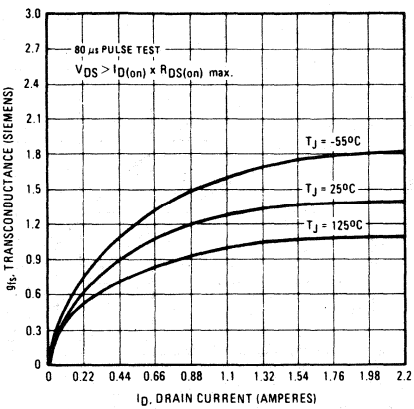


Fig. 5 — Typical Transconductance Vs. Drain Current

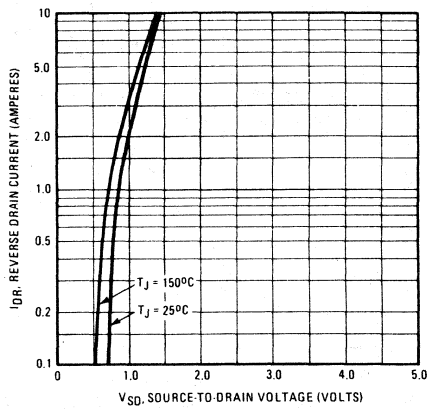


Fig. 6 — Typical Source-Drain Diode Forward Voltage

IRFD310R, IRFD311R, IRFD312R, IRFD313R

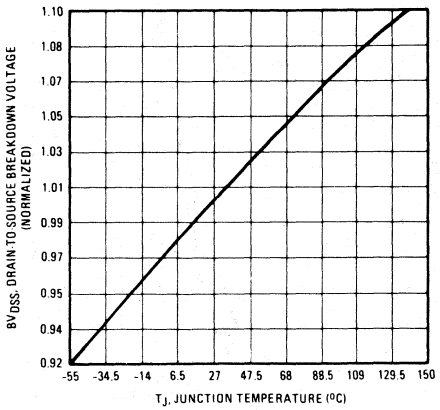


Fig. 7 — Breakdown Voltage Vs. Temperature

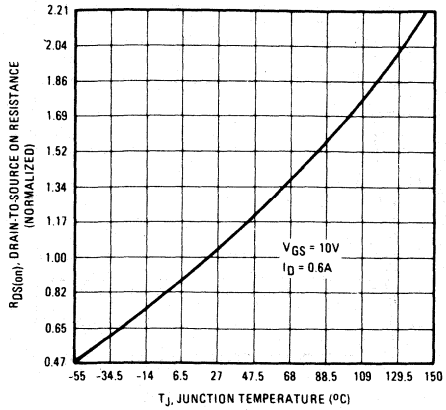


Fig. 8 — Normalized On-Resistance Vs. Temperature

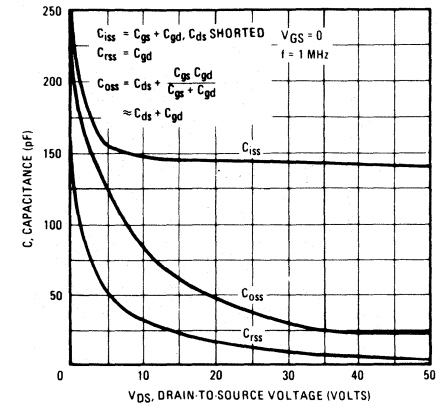


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

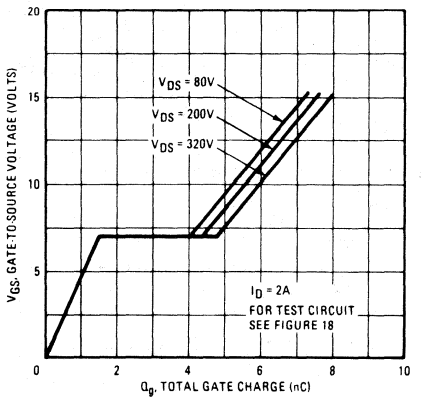


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

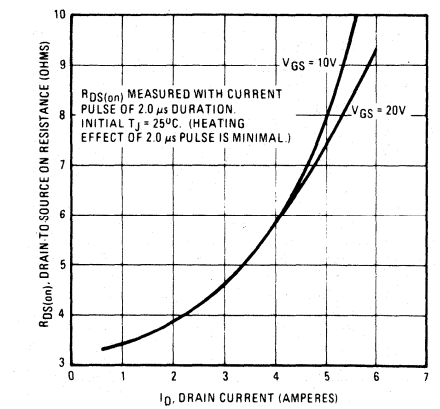


Fig. 11 — Typical On-Resistance Vs. Drain Current

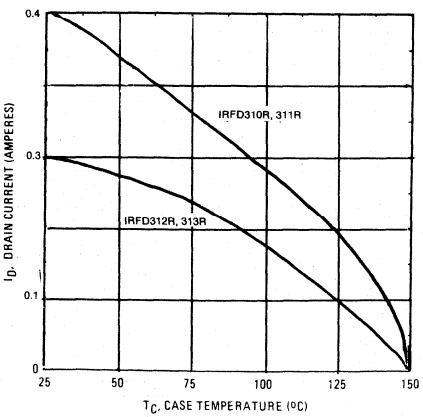


Fig. 12 — Maximum Drain Current Vs. Case Temperature

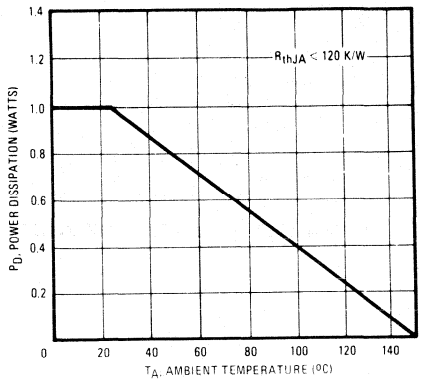


Fig. 13 — Power Vs. Temperature Derating Curve

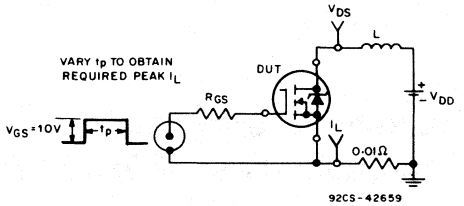


Fig. 14 — Unclamped Energy Test Circuit

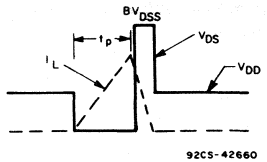


Fig. 15 — Unclamped Energy Waveforms

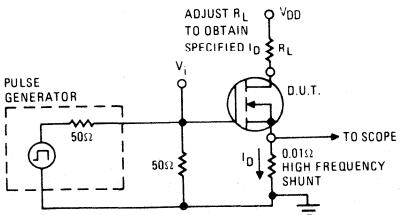


Fig. 16 — Switching Time Test Circuit

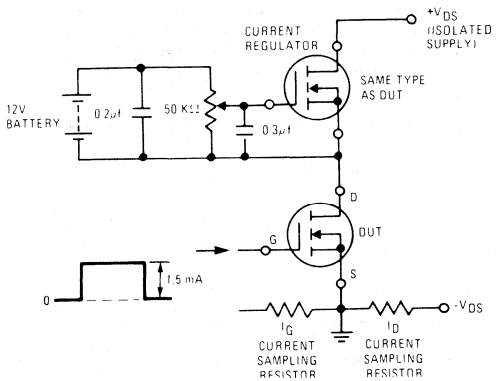


Fig. 17 — Gate Charge Test Circuit

IRFD320R, IRFD321R, IRFD322R, IRFD323R

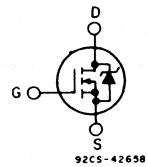
File Number **2040**

Avalanche Energy Rated N-Channel Power MOSFETs

0.5A and 0.4A, 350V-400V
$r_{DS}(on) = 1.8\Omega$ and 2.5Ω

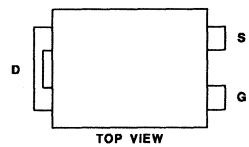
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



4-PIN DIP

The IRFD320R, IRFD321R, IRFD322R and IRFD323R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

The IRFD320R replaces the GF2D05.

Absolute Maximum Ratings

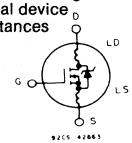
	Parameter	IRFD320R	IRFD321R	IRFD322R	IRFD323R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
I_D @ $T_C = 25°C$	Continuous Drain Current	0.5	0.5	0.4	0.4	A
I_{DM}	Pulsed Drain Current ③	2.0	2.0	1.6	1.6	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	1 (See Fig. 14)				W
	Linear Derating Factor	0.008 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	100				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD320R, IRFD321R, IRFD322R, IRFD323R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD320R IRFD322R	400	—	—	V	V_{GS} = 0V
		IRFD321R IRFD323R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD320R IRFD321R	0.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFD322R IRFD323R	0.4	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD320R IRFD321R	—	1.5	1.8	Ω	V_{GS} = 10V, I_D = 0.25A
		IRFD322R IRFD323R	—	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.25A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V_{GS} = 10V, I_D = 0.5A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

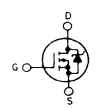


Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD320R IRFD321R	—	—	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD322R IRFD323R	—	—	0.4	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFD320R IRFD321R	—	—	2.0	A	
		IRFD322R IRFD323R	—	—	1.6	A	
V_{SD}	Diode Forward Voltage ②	IRFD320R IRFD321R	—	—	1.6	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
		IRFD322R IRFD323R	—	—	1.5	V	T_C = 25°C, I_S = 1.6A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 40V, starting T_J = 25°C, L = 29.09mH, R_{gs} = 50Ω, I_{peak} = 2.5A. See figs. 14, 15.

IRFD320R, IRFD321R, IRFD322R, IRFD323R

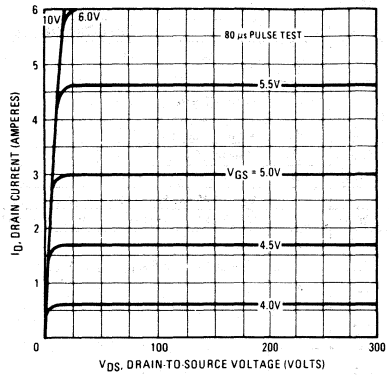


Fig. 1 — Typical Output Characteristics

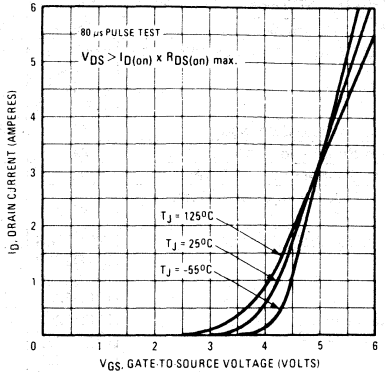


Fig. 2 — Typical Transfer Characteristics

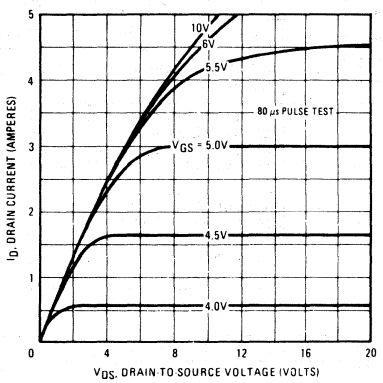


Fig. 3 — Typical Saturation Characteristics

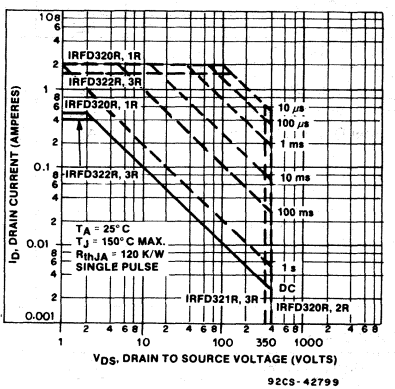


Fig. 4 — Maximum Safe Operating Area

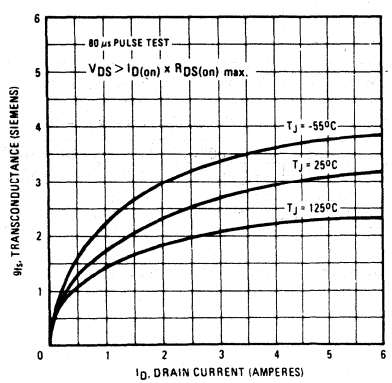


Fig. 5 — Typical Transconductance Vs. Drain Current

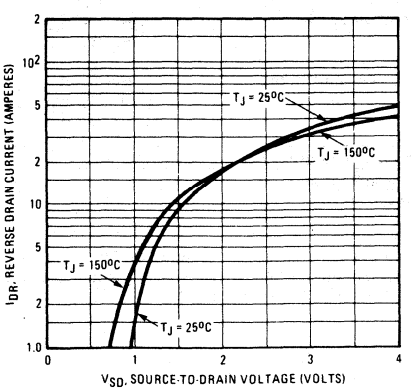


Fig. 6 — Typical Source-Drain Diode Forward Voltage

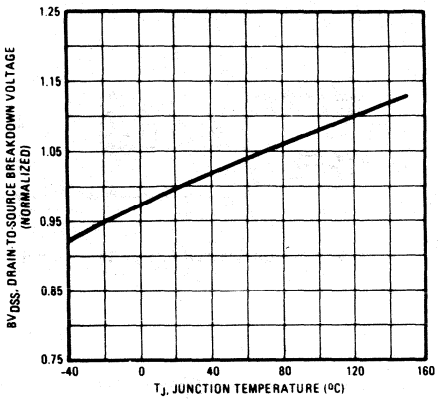


Fig. 7 — Breakdown Voltage Vs. Temperature

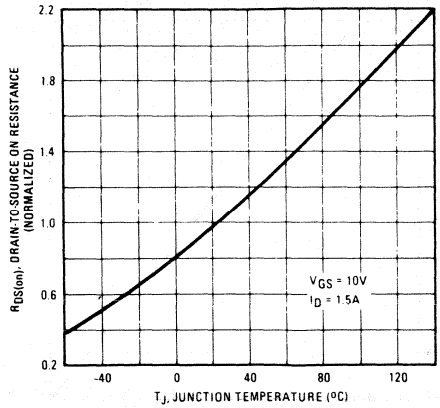


Fig. 8 — Normalized On-Resistance Vs. Temperature

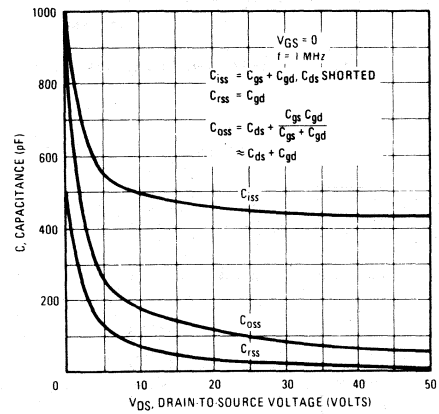


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

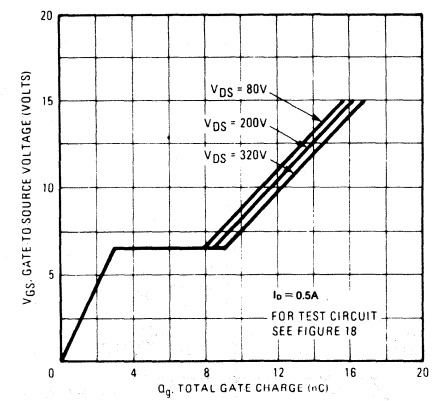


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

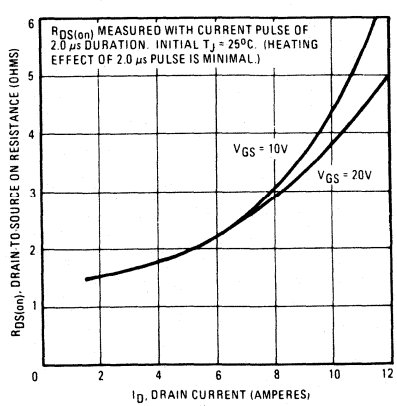


Fig. 11 — Typical On-Resistance Vs. Drain Current

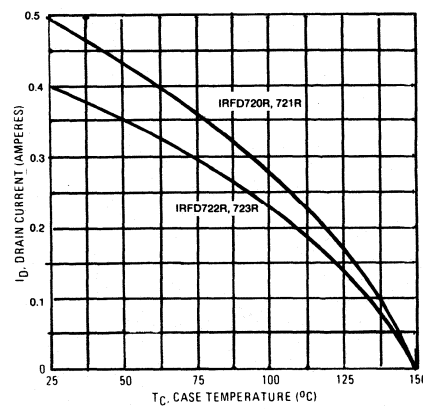


Fig. 12 — Maximum Drain Current Vs. Case Temperature

IRFD320R, IRFD321R, IRFD322R, IRFD323R

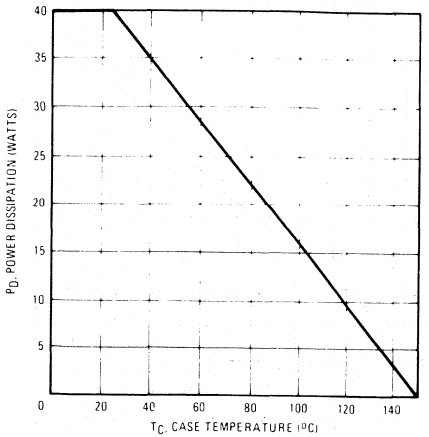


Fig. 13 — Power Vs. Temperature Derating Curve

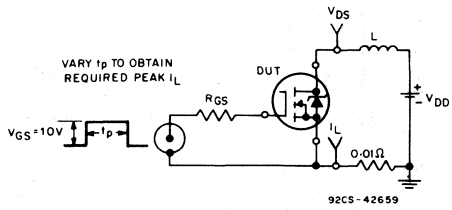


Fig. 14 — Unclamped Energy Test Circuit

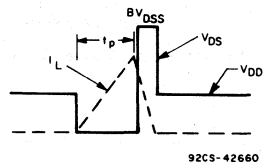


Fig. 15 — Unclamped Energy Waveforms

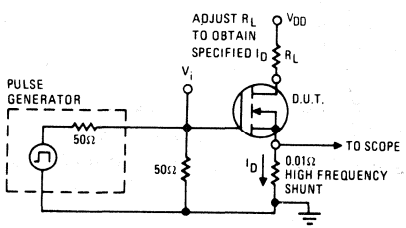


Fig. 16 — Switching Time Test Circuit

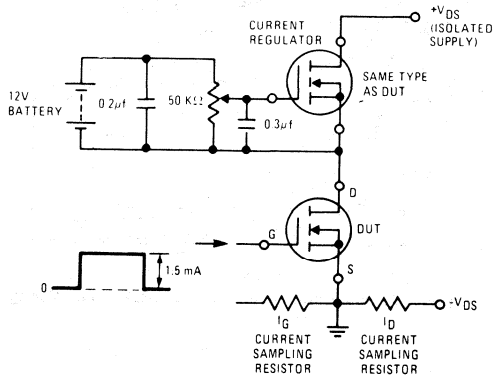


Fig. 17 — Gate Charge Test Circuit

File Number **2022**

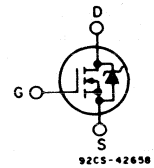
IRFF110R, IRFF111R, IRFF112R, IRFF113R

Avalanche Energy Rated N-Channel Power MOSFETs

3.0A and 3.5A, 60V-100V
$r_{DS}(on) = 0.6\Omega$ and 0.8Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

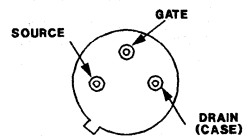


TERMINAL DIAGRAM

The IRFF110R, IRFF111R, IRFF112R and IRFF113R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

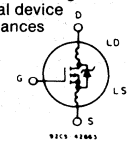
Parameter		IRFF110R	IRFF111R	IRFF112R	IRFF113R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	19				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF110R, IRFF111R, IRFF112R, IRFF113R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF110R, IRFF112R	100	—	—	V	V_{GS} = 0V
		IRFF111R, IRFF113R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF110R, IRFF111R	3.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF112R, IRFF113R	3.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF110R, IRFF111R	—	0.5	0.6	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF112R, IRFF113R	—	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	—	S(Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	80	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.5A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	11	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

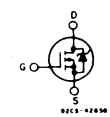


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF110R, IRFF111R	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF112R, IRFF113R	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF110R, IRFF111R	—	—	14	A	
		IRFF112R, IRFF113R	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF110R, IRFF111R	—	—	2.5	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF112R, IRFF113R	—	—	2.0	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	200	—	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.0	—	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 5V, starting T_J = 25°C, L = 2.3mH, R_{gs} = 25Ω, I_{peak} = 3.5A. See figs. 15, 16.

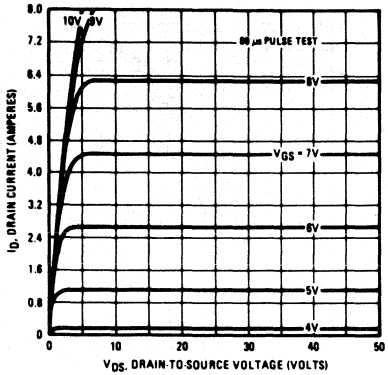


Fig. 1 – Typical Output Characteristics

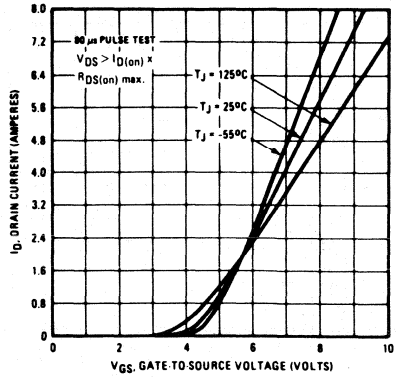


Fig. 2 – Typical Transfer Characteristics

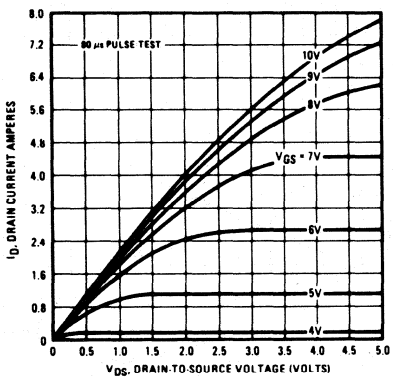


Fig. 3 – Typical Saturation Characteristics

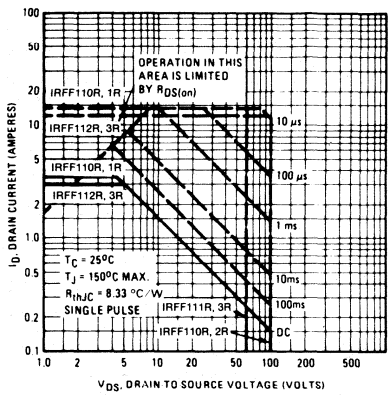


Fig. 4 – Maximum Safe Operating Area

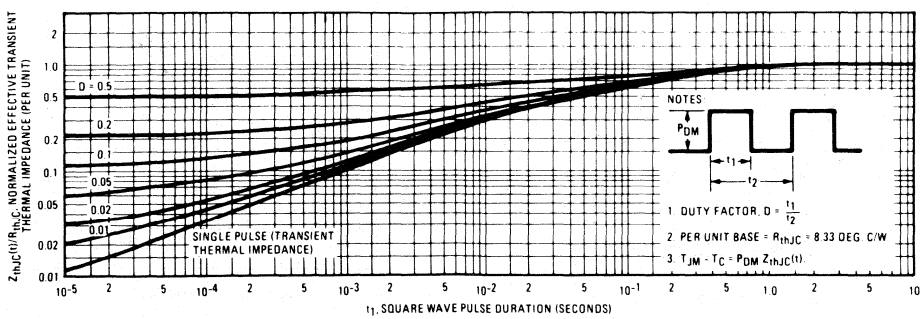


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

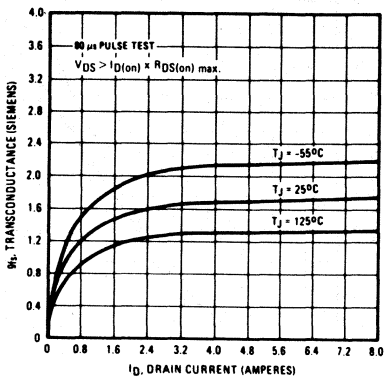


Fig. 6 – Typical Transconductance Vs. Drain Current

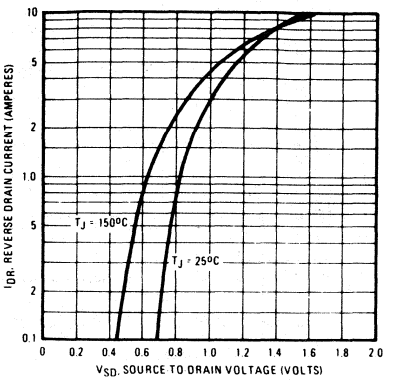


Fig. 7 – Typical Source-Drain Diode Forward Voltage

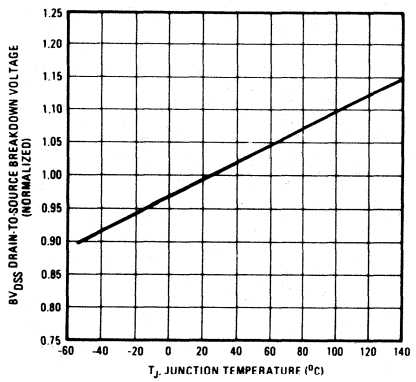


Fig. 8 – Breakdown Voltage Vs. Temperature

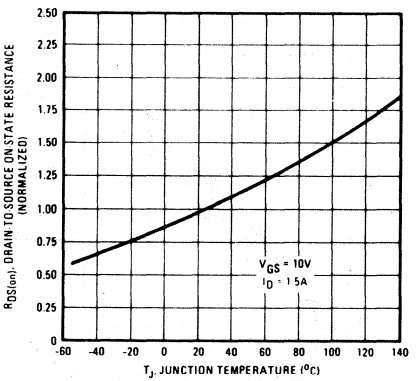


Fig. 9 – Normalized On-Resistance Vs. Temperature

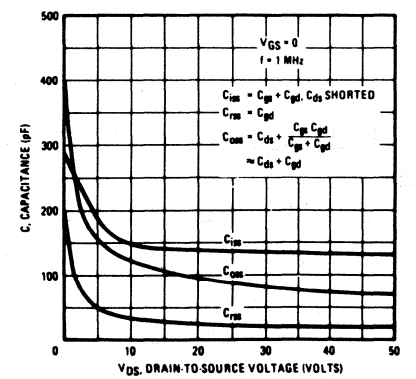


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

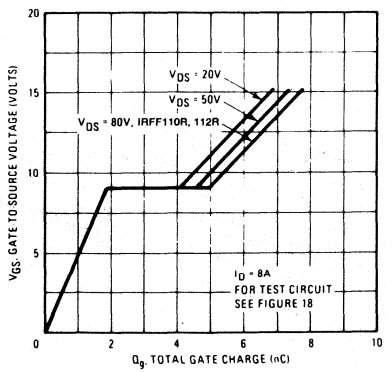


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

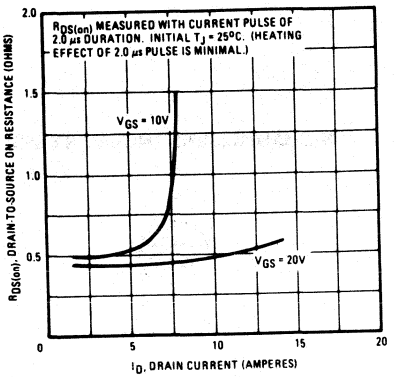


Fig. 12 – Typical On-Resistance Vs. Drain Current

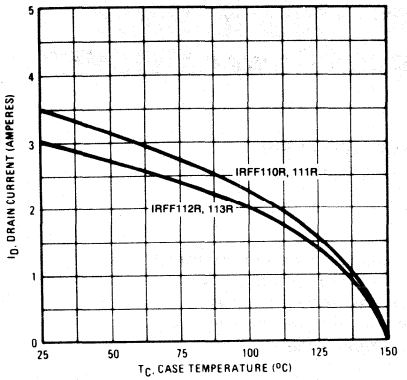


Fig. 13 – Maximum Drain Current Vs. Case Temperature

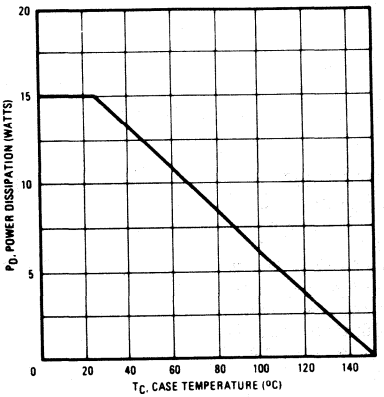


Fig. 14 – Power Vs. Temperature Derating Curve

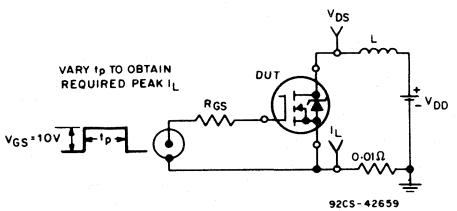


Fig. 15 — Unclamped Energy Test Circuit

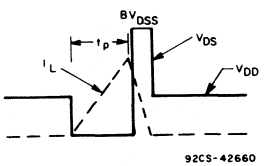


Fig. 16 — Unclamped Energy Waveforms

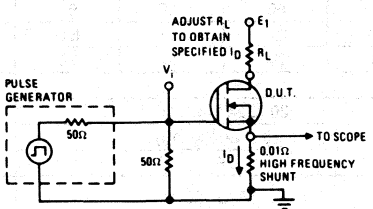


Fig. 17 – Switching Time Test Circuit

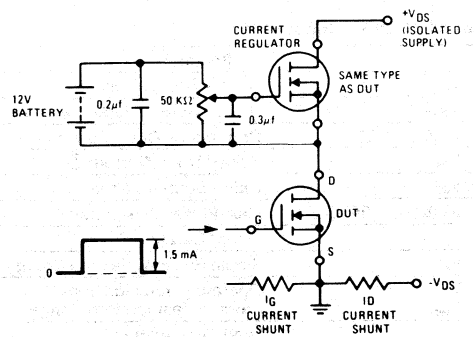


Fig. 18 – Gate Charge Test Circuit

IRFF120R, IRFF121R, IRFF122R, IRFF123R

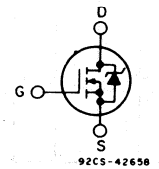
File Number **2023**

Avalanche Energy Rated N-Channel Power MOSFETs

5.0A and 6.0A, 60V-100V
$r_{DS}(on) = 0.30\Omega$ and 0.40Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

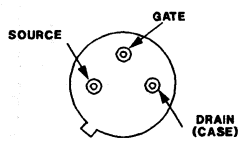


TERMINAL DIAGRAM

The IRFF120R, IRFF121R, IRFF122R and IRFF123R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

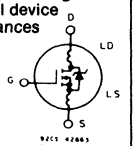
Absolute Maximum Ratings

Parameter		IRFF120R	IRFF121R	IRFF122R	IRFF123R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	24	24	20	20	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	36				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF120R IRFF122R	100	—	—	V	V_{GS} = 0V
		IRFF121R IRFF123R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF120R IRFF121R	6.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF122R IRFF123R	5.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF120R IRFF121R	—	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3.0A
		IRFF122R IRFF123R	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 3.0A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 3.0A, Z_o = 50Ω
t_r	Rise Time	ALL	—	37	70	ns	See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	18	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF120R IRFF121R	—	—	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF122R IRFF123R	—	—	5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF120R IRFF121R	—	—	24	A	
		IRFF122R IRFF123R	—	—	20	A	
V_{SD}	Diode Forward Voltage ②	IRFF120R IRFF121R	—	—	2.5	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
		IRFF122R IRFF123R	—	—	2.3	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	230	—	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.2	—	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_J = 25°C, L = 1.5mH, R_{gs} = 25Ω, I_{peak} = 6A. See figs. 15, 16.

IRFF120R, IRFF121R, IRFF122R, IRFF123R

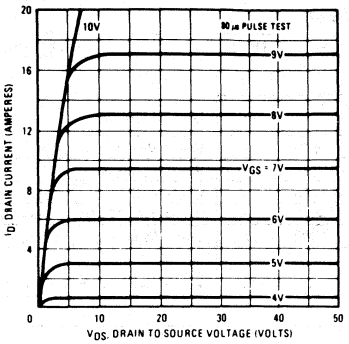


Fig. 1 – Typical Output Characteristics

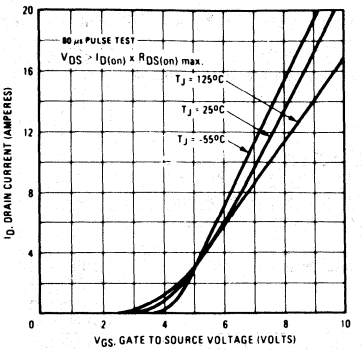


Fig. 2 – Typical Transfer Characteristics

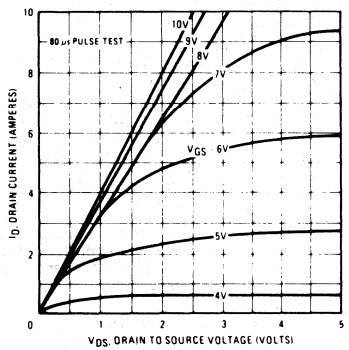


Fig. 3 – Typical Saturation Characteristics

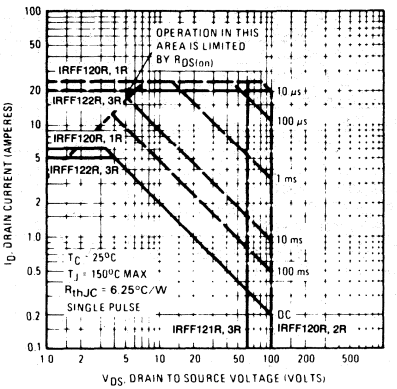


Fig. 4 – Maximum Safe Operating Area

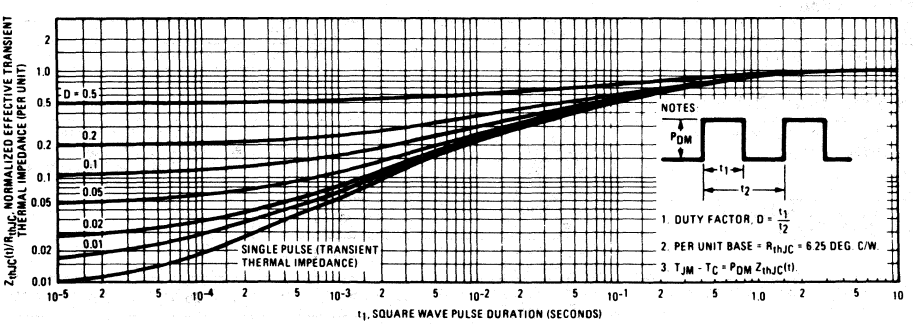


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

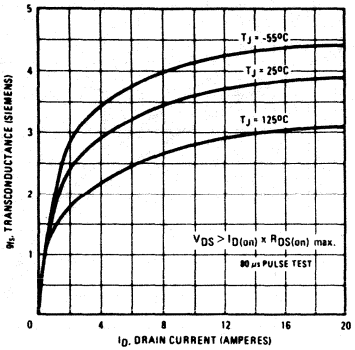


Fig. 6 – Typical Transconductance Vs. Drain Current

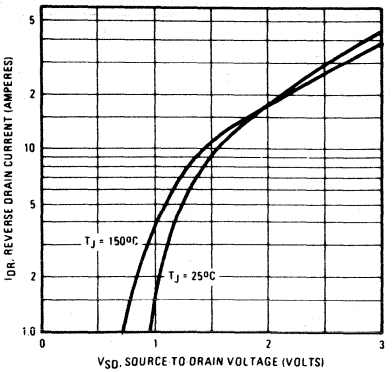


Fig. 7 – Typical Source-Drain Diode Forward Voltage

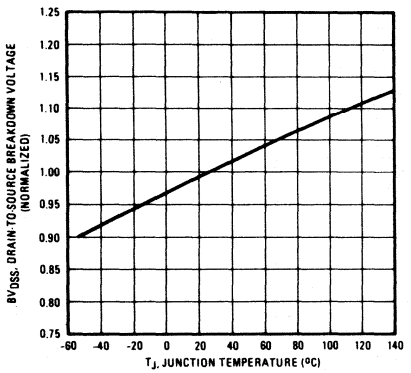


Fig. 8 – Breakdown Voltage Vs. Temperature

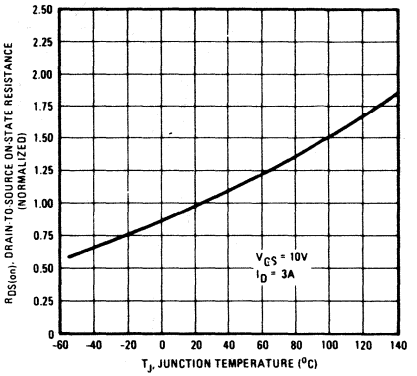


Fig. 9 – Normalized On-Resistance Vs. Temperature

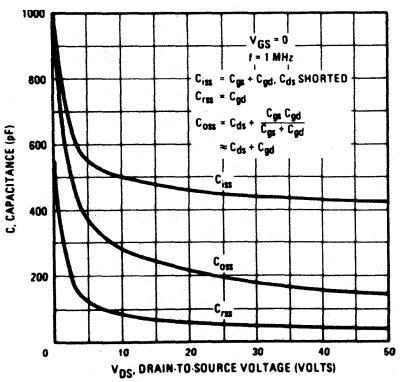


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

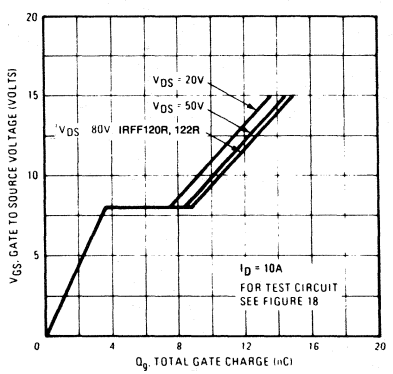


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRFF120R, IRFF121R, IRFF122R, IRFF123R

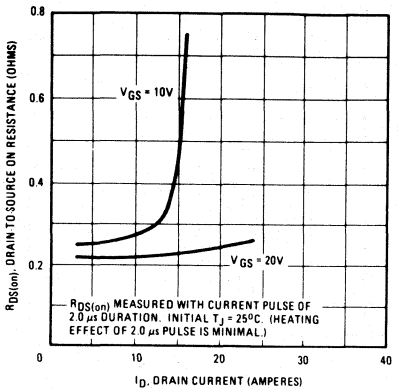


Fig. 12 – Typical On-Resistance Vs. Drain Current

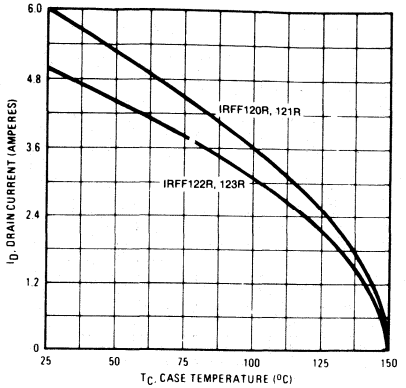


Fig. 13 – Maximum Drain Current Vs. Case Temperature

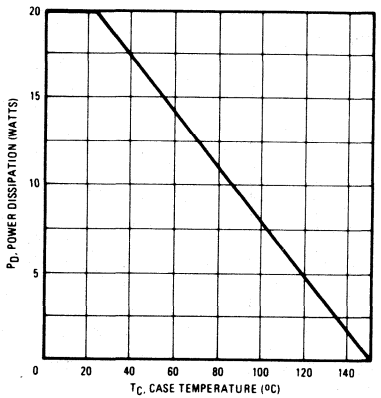


Fig. 14 – Power Vs. Temperature Derating Curve

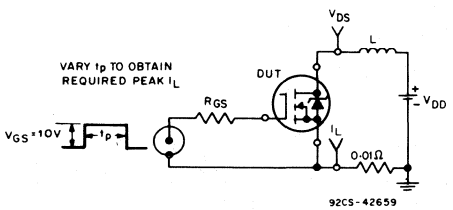


Fig. 15 – Unclamped Energy Test Circuit

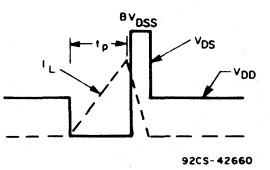


Fig. 16 – Unclamped Energy Waveforms

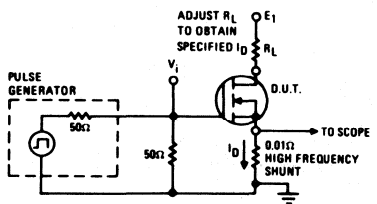


Fig. 17 – Switching Time Test Circuit

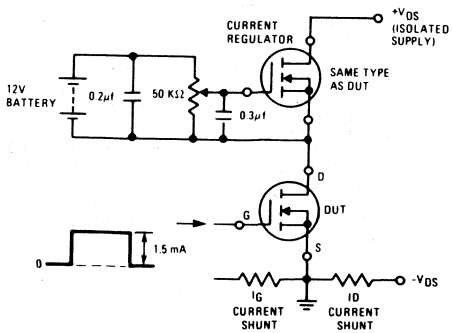


Fig. 18 – Gate Charge Test Circuit

File Number **2024**

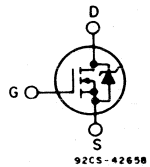
IRFF130R, IRFF131R, IRFF132R, IRFF133R

Avalanche Energy Rated N-Channel Power MOSFETs

7.0A and 8.0A, 60V-100V
$r_{DS}(on) = 0.18\Omega$ and 0.25Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

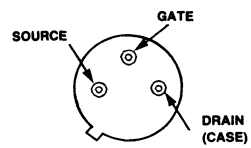


TERMINAL DIAGRAM

The IRFF130R, IRFF131R, IRFF132R and IRFF133R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

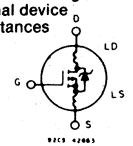
Parameter		IRFF130R	IRFF131R	IRFF132R	IRFF133R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	69				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF130R, IRFF131R, IRFF132R, IRFF133R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF130R IRFF132R	100	—	—	V	V_{GS} = 0V
		IRFF131R IRFF133R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF130R IRFF131R	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF132R IRFF133R	7.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF130R IRFF131R	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 4.0A
		IRFF132R IRFF133R	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 4.0A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	50	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	80	150	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	80	150	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

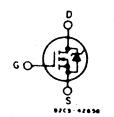


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF130R IRFF131R	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF132R IRFF133R	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF130R IRFF131R	—	—	32	A	
		IRFF132R IRFF133R	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	IRFF130R IRFF131R	—	—	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRFF132R IRFF133R	—	—	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.5	—	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_J = 25°C, L = 1.62mH, R_{gs} = 25Ω, I_{peak} = 8A.

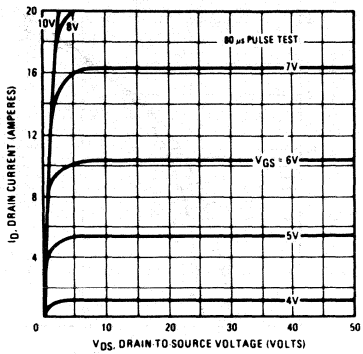


Fig. 1 – Typical Output Characteristics

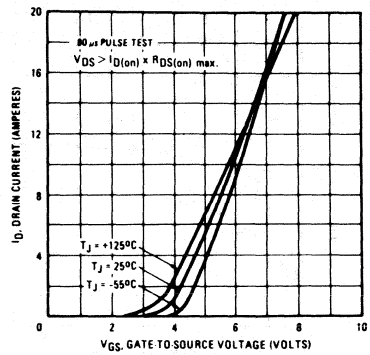


Fig. 2 – Typical Transfer Characteristics

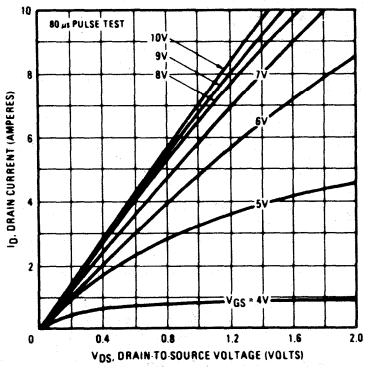


Fig. 3 – Typical Saturation Characteristics

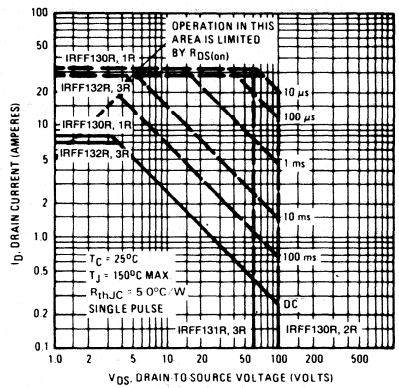


Fig. 4 – Maximum Safe Operating Area

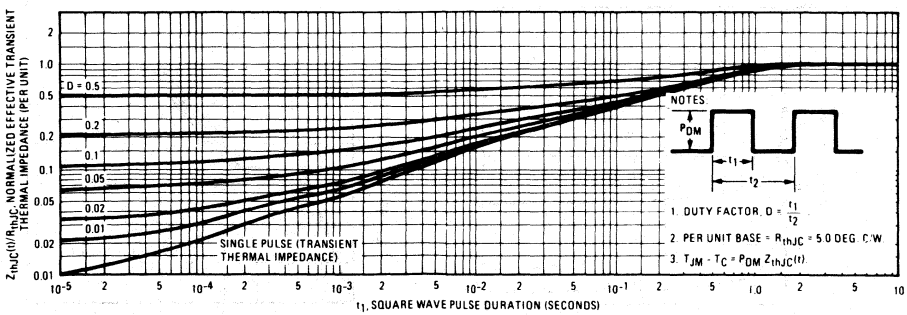


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

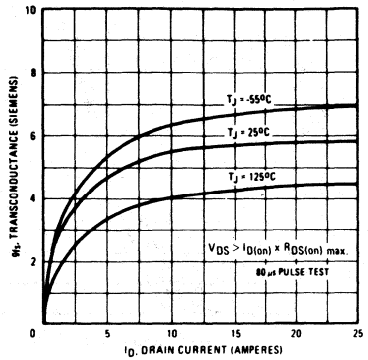


Fig. 6 – Typical Transconductance Vs. Drain Current

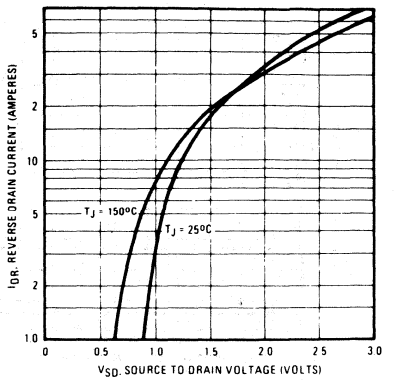


Fig. 7 – Typical Source-Drain Diode Forward Voltage

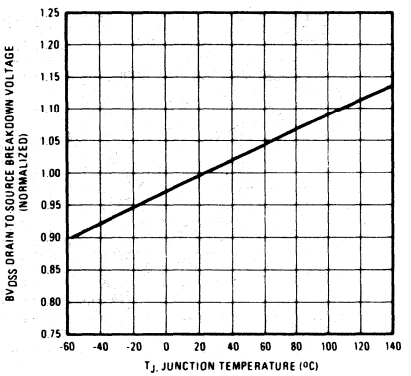


Fig. 8 – Breakdown Voltage Vs. Temperature

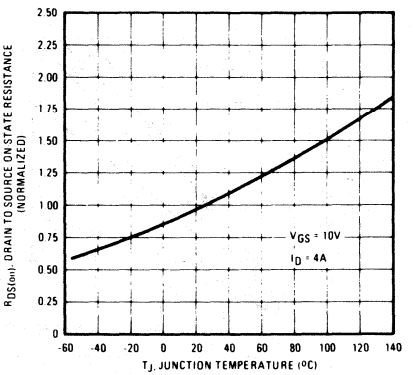


Fig. 9 – Normalized On-Resistance Vs. Temperature

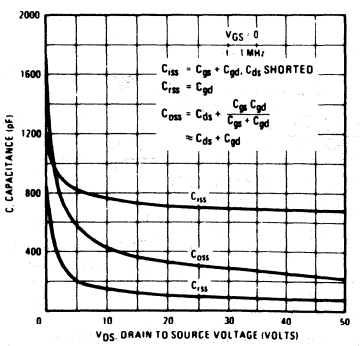


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

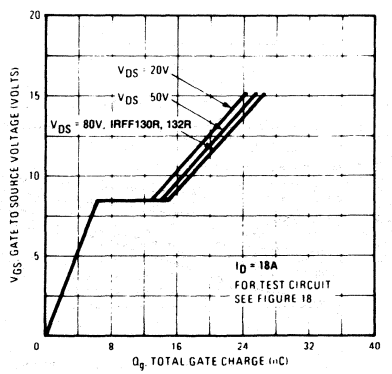


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

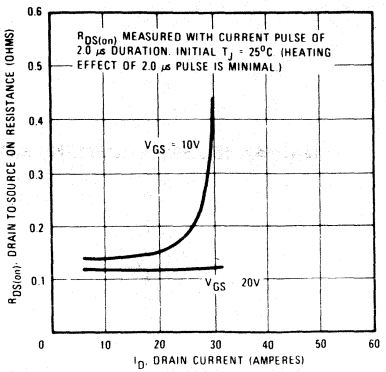


Fig. 12 – Typical On-Resistance Vs. Drain Current

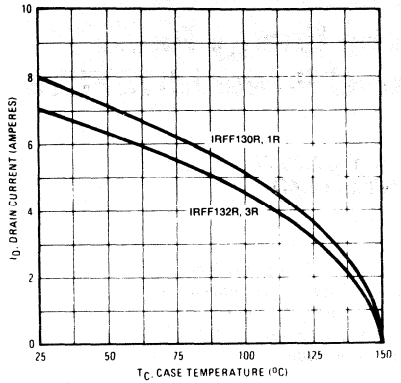


Fig. 13 – Maximum Drain Current Vs. Case Temperature

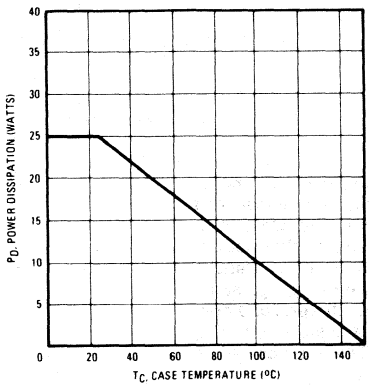


Fig. 14 – Power Vs. Temperature Derating Curve

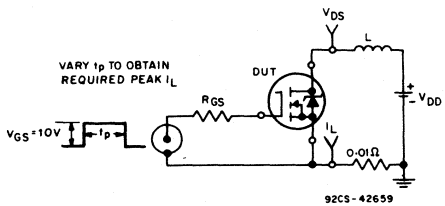


Fig. 15 — Unclamped Energy Test Circuit

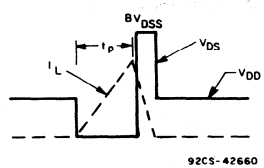


Fig. 16 — Unclamped Energy Waveforms

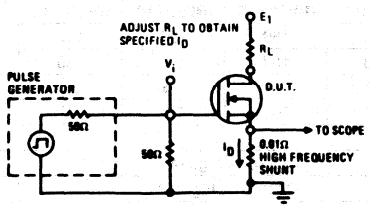


Fig. 17 – Switching Time Test Circuit

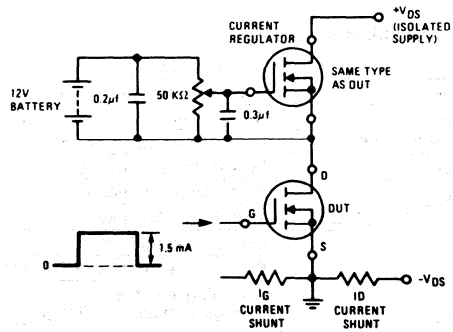


Fig. 18 – Gate Charge Test Circuit

IRFF210R, IRFF211R, IRFF212R, IRFF213R

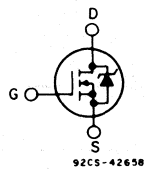
File Number **2025**

Avalanche Energy Rated N-Channel Power MOSFETs

1.8A and 2.2A, 150V-200V
$r_{DS}(on) = 1.5\Omega$ and 2.4Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

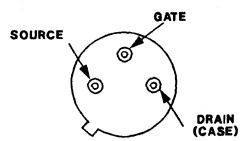


TERMINAL DIAGRAM

The IRFF210R, IRFF211R, IRFF212R and IRFF213R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

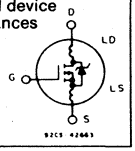
Absolute Maximum Ratings

Parameter		IRFF210R	IRFF211R	IRFF212R	IRFF213R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.2	2.2	1.8	1.8	A
I_{DM}	Pulsed Drain Current ③	9.0	9.0	7.5	7.5	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	30				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF210R IRFF212R	200	—	—	V	V_{GS} = 0V
		IRFF211R IRFF213R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF210R IRFF211R	2.2	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRFF212R IRFF213R	1.8	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF210R IRFF211R	—	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		IRFF212R IRFF213R	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 1.25A
C_{iss}	Input Capacitance	ALL	—	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	60	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	16	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V_{GS} = 10V, I_D = 4.5A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

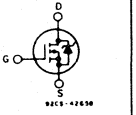


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF210R IRFF211R	—	—	2.2	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF212R IRFF213R	—	—	1.8	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF210R IRFF211R	—	—	9.0	A	
		IRFF212R IRFF213R	—	—	7.5	A	
V_{SD}	Diode Forward Voltage ②	IRFF210R IRFF211R	—	—	2.0	V	T_C = 25°C, I_S = 2.2A, V_{GS} = 0V
		IRFF212R IRFF213R	—	—	1.8	V	T_C = 25°C, I_S = 1.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	290	—	ns	T_J = 150°C, I_F = 2.2A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	T_J = 150°C, I_F = 2.2A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 20V, starting T_J = 25°C, L = 11.16mH, R_{gs} = 50Ω, I_{peak} = 2.2A.

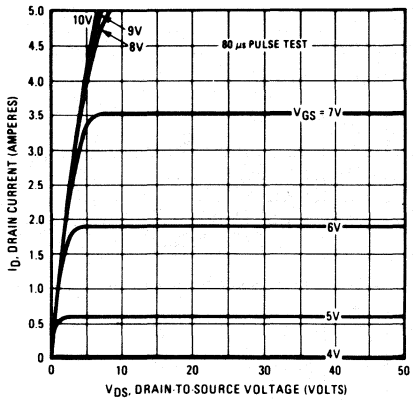


Fig. 1 - Typical output characteristics.

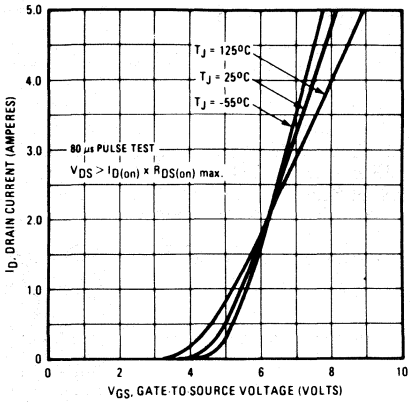


Fig. 2 - Typical transfer characteristics.

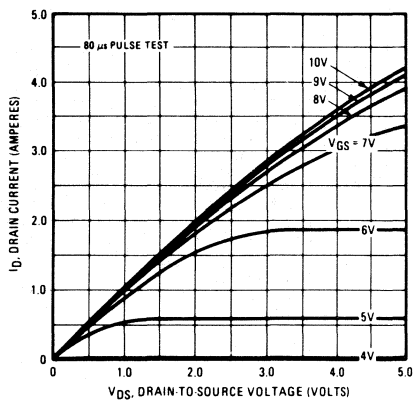


Fig. 3 - Typical saturation characteristics.

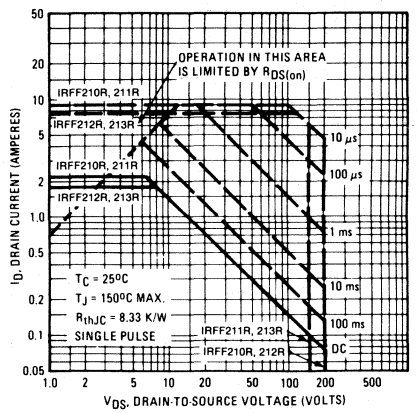


Fig. 4 - Maximum safe operating area.

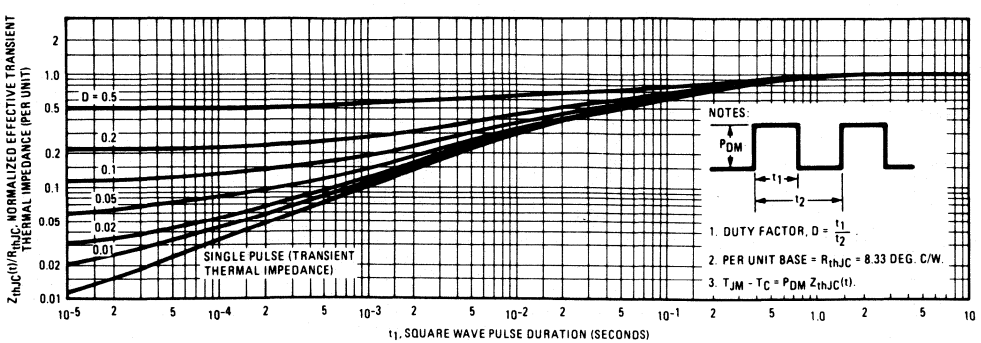


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

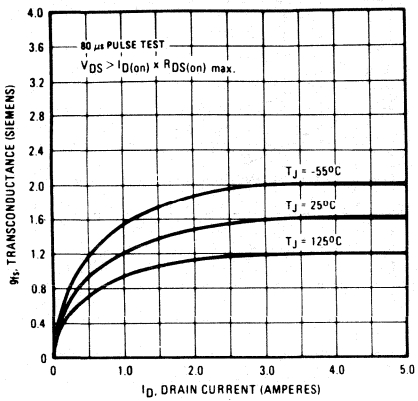


Fig. 6 - Typical transconductance vs. drain current.

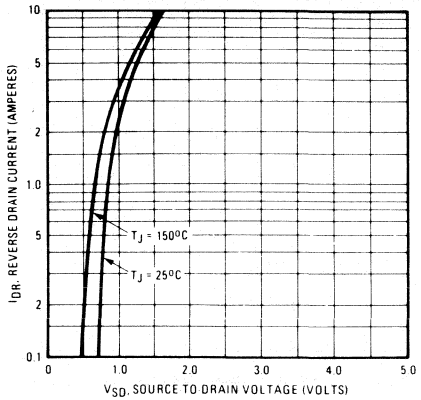


Fig. 7 - Typical source-drain diode forward voltage.

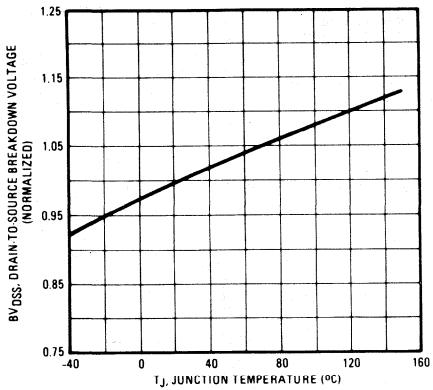


Fig. 8 - Breakdown voltage vs. temperature.

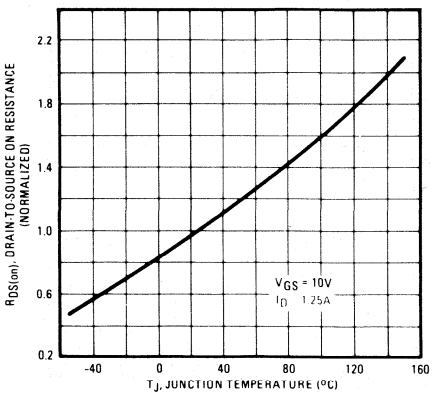


Fig. 9 - Normalized on-resistance vs. temperature.

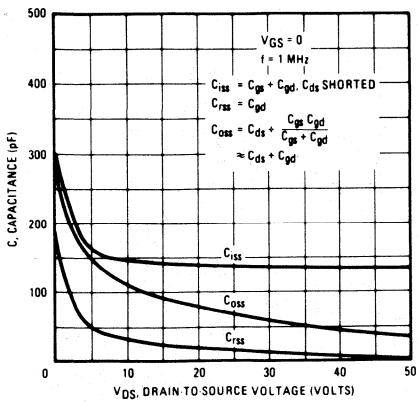


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

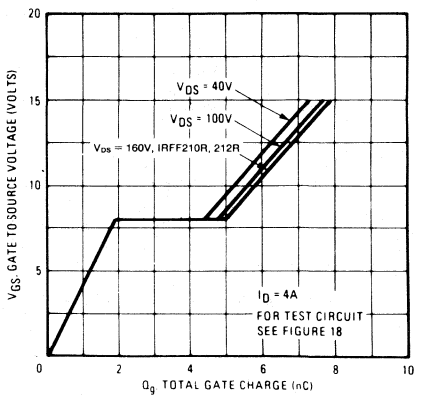


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF210R, IRFF211R, IRFF212R, IRFF213R

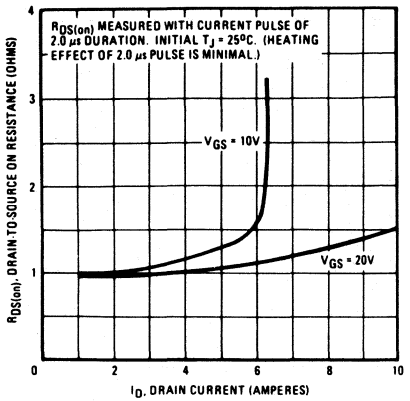


Fig. 12 - Typical on-resistance vs. drain current.

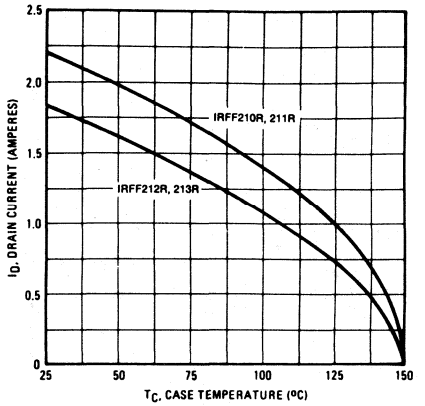


Fig. 13 - Maximum drain current vs. case temperature.

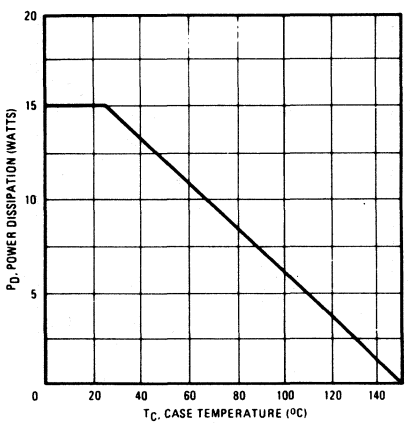


Fig. 14 - Power vs. temperature derating curve.

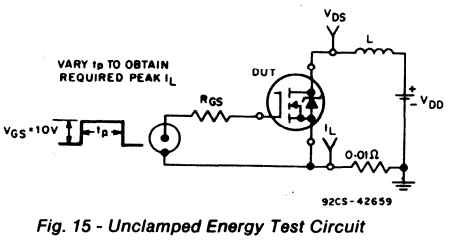


Fig. 15 - Unclamped Energy Test Circuit

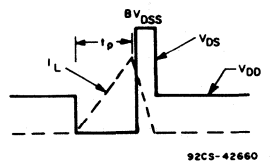


Fig. 16 - Unclamped Energy Waveforms

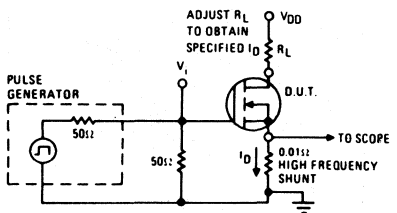


Fig. 17 - Switching time test circuit.

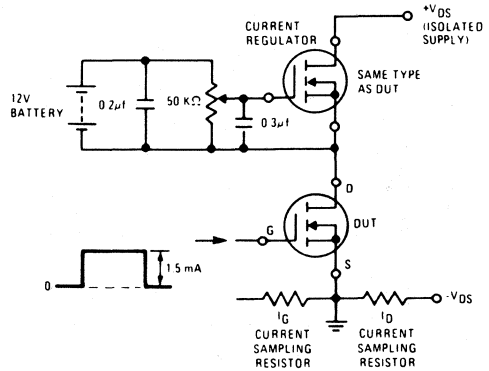


Fig. 18 - Gate charge test circuit.

File Number **2026**

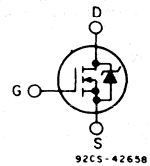
IRFF220R, IRFF221R, IRFF222R, IRFF223R

Avalanche Energy Rated N-Channel Power MOSFETs

3.0A and 3.5A, 150V-200V
$r_{DS}(on) = 0.8\Omega$ and 1.2Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

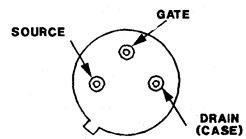


TERMINAL DIAGRAM

The IRFF220R, IRFF221R, IRFF222R and IRFF223R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

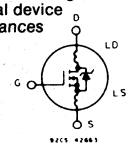
Parameter		IRFF220R	IRFF221R	IRFF222R	IRFF223R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	85				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF220R, IRFF221R, IRFF222R, IRFF223R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF220R IRFF222R	200	—	—	V	V_{GS} = 0V
		IRFF221R IRFF223R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF220R IRFF221R	3.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF222R IRFF223R	3.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF220R IRFF221R	—	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.0A
		IRFF222R IRFF223R	—	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.25	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 2.0A
C_{iss}	Input Capacitance	ALL	—	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 2.0A, Z_o = 50Ω
t_r	Rise Time	ALL	—	30	60	ns	See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF220R IRFF221R	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF222R IRFF223R	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF220R IRFF221R	—	—	14	A	
		IRFF222R IRFF223R	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF220R IRFF221R	—	—	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF222R IRFF223R	—	—	1.8	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 20V, starting T_J = 25°C, L = 12.5mH, R_{gs} = 50Ω, I_{peak} = 3.5A.

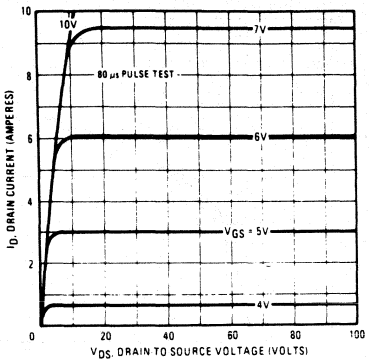


Fig. 1 - Typical output characteristics.

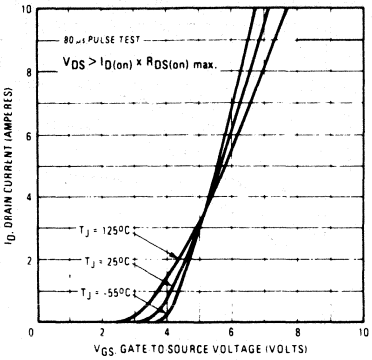


Fig. 2 - Typical transfer characteristics.

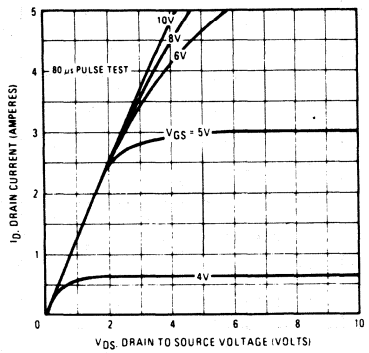
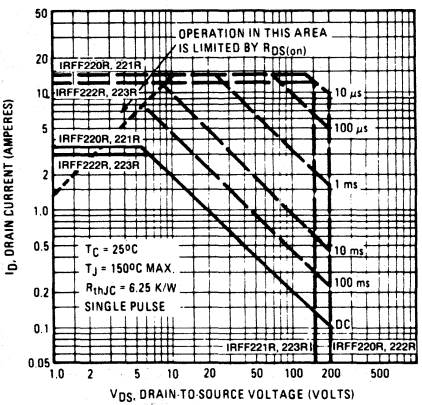


Fig. 3 - Typical saturation characteristics.



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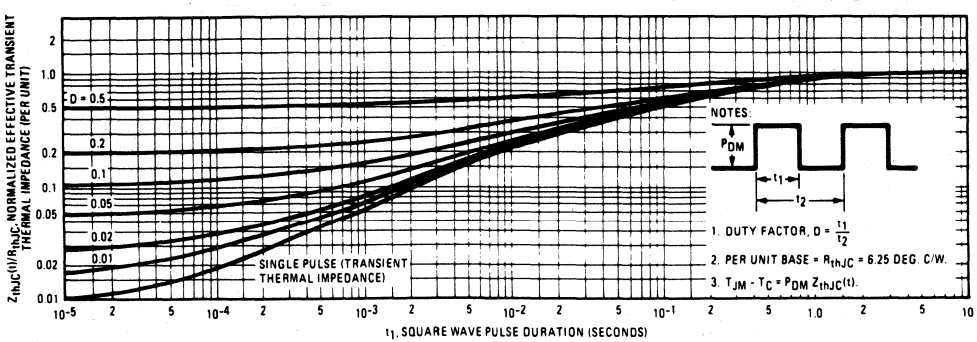

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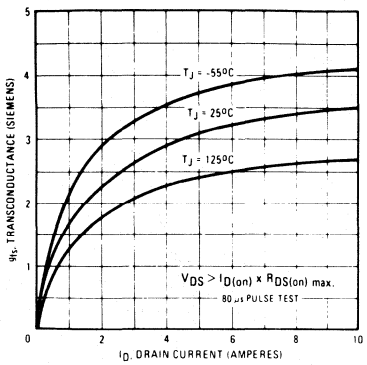

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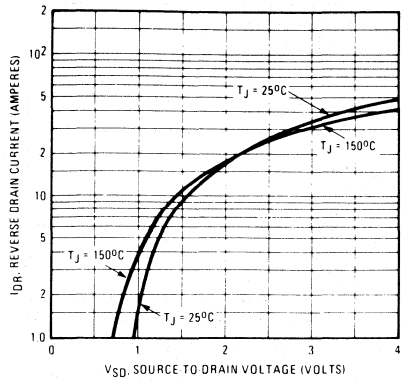
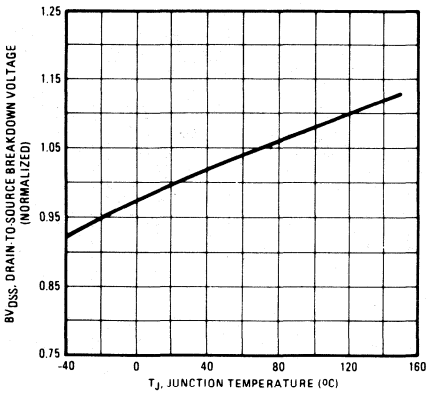


Fig. 7 - Typical source-drain diode forward voltage.



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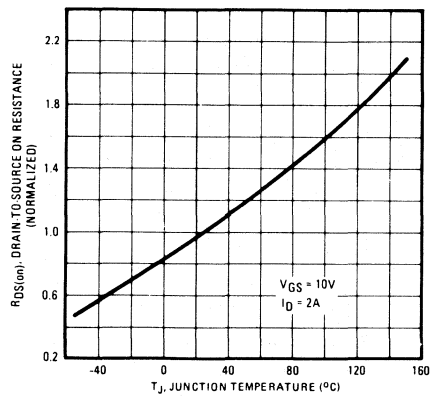


Fig. 9 - Normalized on-resistance vs. temperature.

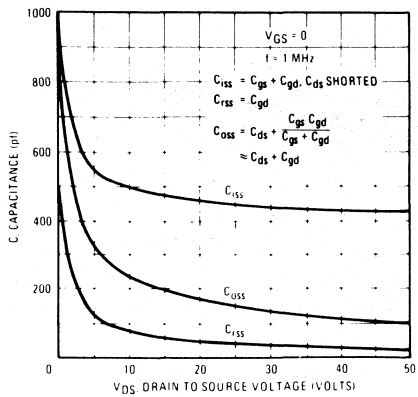


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

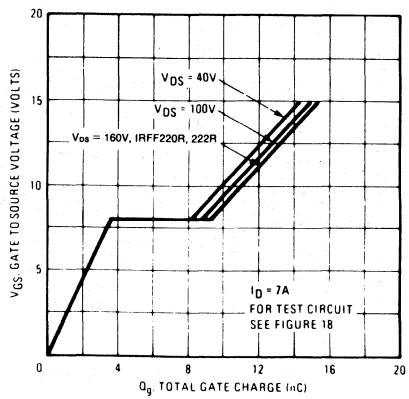
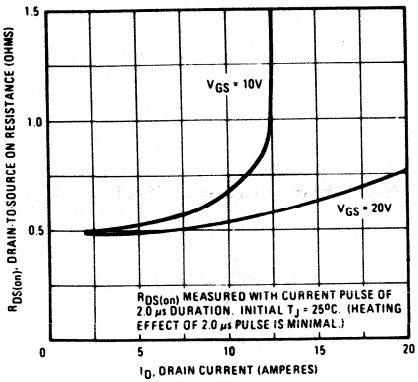


Fig. 11 - Typical gate charge vs. gate-to-source voltage.



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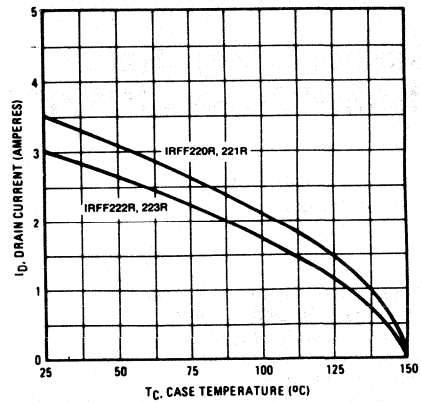


Fig. 13 - Maximum drain current vs. case temperature.

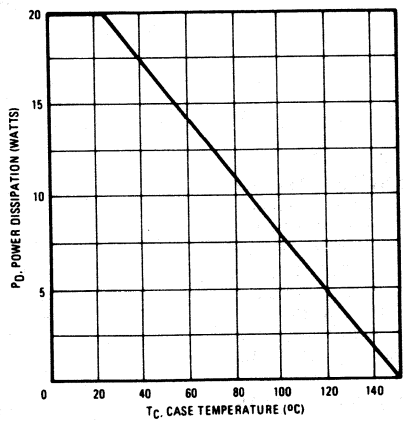


Fig. 14 - Power vs. temperature derating curve.

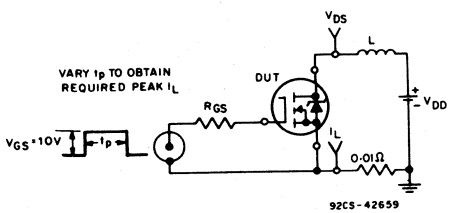


Fig. 15 - Unclamped Energy Test Circuit

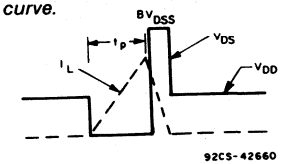


Fig. 16 - Unclamped Energy Waveforms

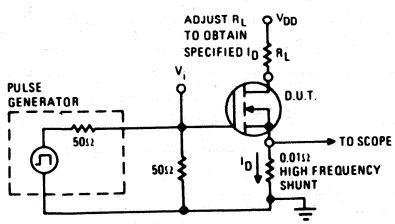


Fig. 17 - Switching time test circuit.

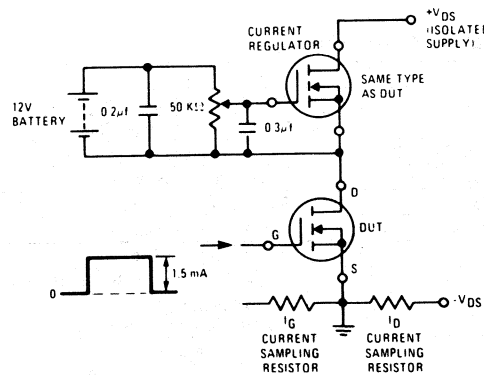


Fig. 18 - Gate charge test circuit.

IRFF230R, IRFF231R, IRFF232R, IRFF233R

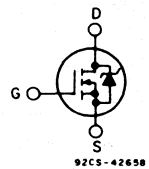
File Number **2027**

Avalanche Energy Rated N-Channel Power MOSFETs

4.5A and 5.5A, 150V-200V
$r_{DS}(on) = 0.4\Omega$ and 0.6Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

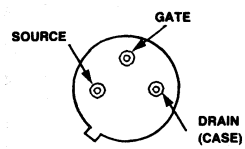


TERMINAL DIAGRAM

The IRFF230R, IRFF231R, IRFF232R and IRFF233R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

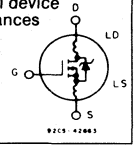
Absolute Maximum Ratings

Parameter		IRFF230R	IRFF231R	IRFF232R	IRFF233R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	85				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF230R IRFF232R	200	—	—	V	V_{GS} = 0V
		IRFF231R IRFF233R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF230R IRFF231R	5.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF232R IRFF233R	4.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF230R IRFF231R	—	0.25	0.4	Ω	V_{GS} = 10V, I_D = 3.0A
		IRFF232R IRFF233R	—	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	4.5	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 3.0A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	250	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 90V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	50	ns	
t_f	Fall Time	ALL	—	—	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	19	30	nC	V_{GS} = 10V, I_D = 11A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	10	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

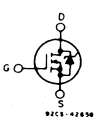


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF230R IRFF231R	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF232R IRFF233R	—	—	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF230R IRFF231R	—	—	22	A	
		IRFF232R IRFF233R	—	—	18	A	
V_{SD}	Diode Forward Voltage ②	IRFF230R IRFF231R	—	—	2.0	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRFF232R IRFF233R	—	—	1.8	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 20V, starting T_J = 25°C, L = 8.9mH, R_{gs} = 50Ω, I_{peak} = 5.5A.

IRFF230R, IRFF231R, IRFF232R, IRFF233R

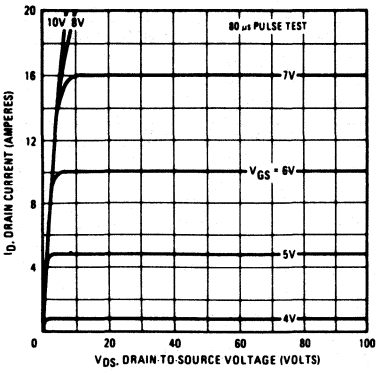


Fig. 1 - Typical output characteristics.

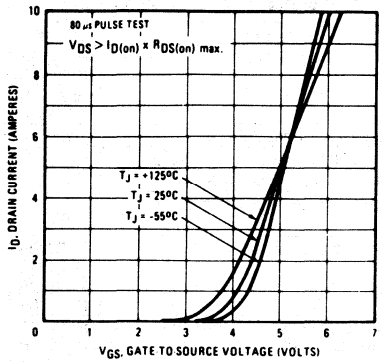


Fig. 2 - Typical transfer characteristics.

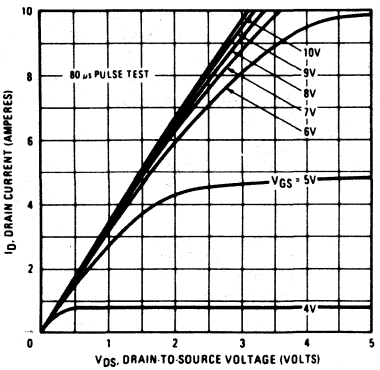


Fig. 3 - Typical saturation characteristics.

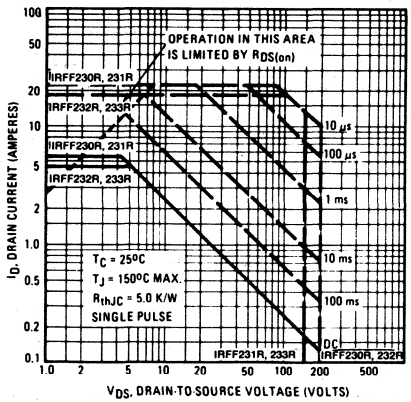


Fig. 4 - Maximum safe operating area.

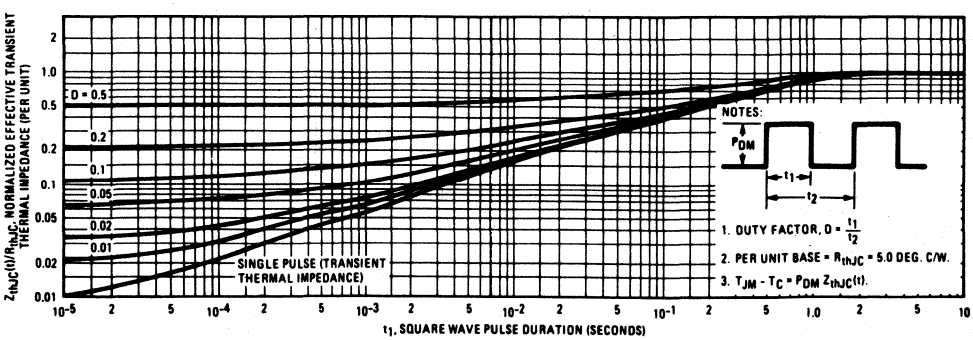


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

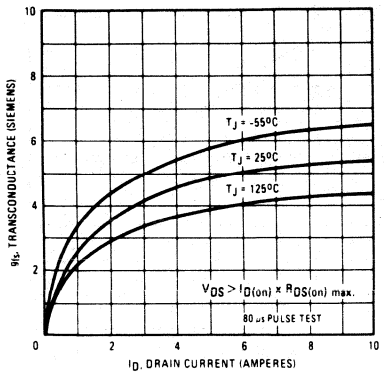


Fig. 6 - Typical transconductance vs. drain current.

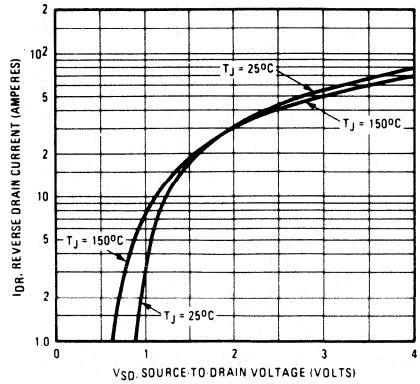


Fig. 7 - Typical source-drain diode forward voltage.

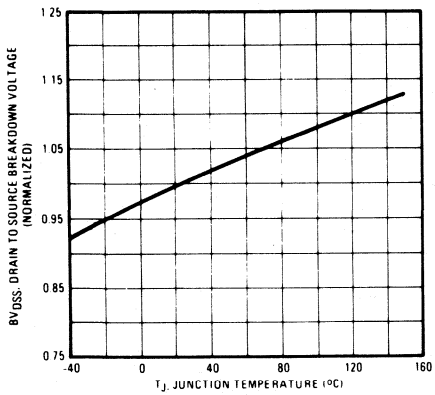


Fig. 8 - Breakdown voltage vs. temperature.

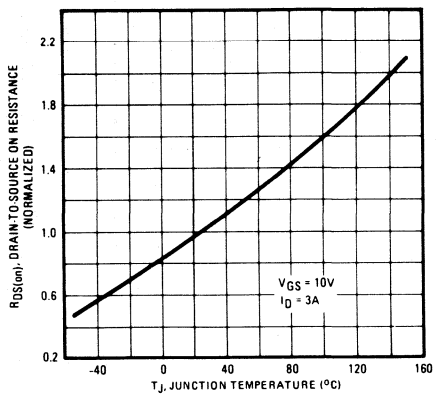


Fig. 9 - Normalized on-resistance vs. temperature.

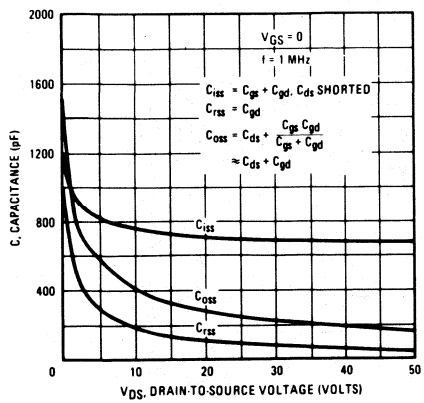


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

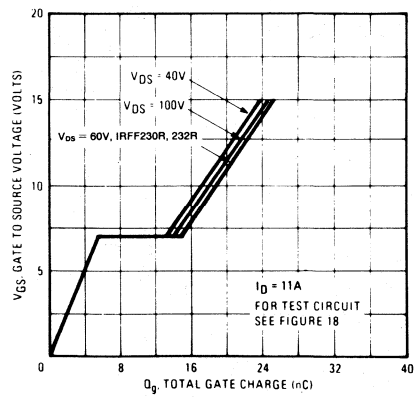


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF230R, IRFF231R, IRFF232R, IRFF233R

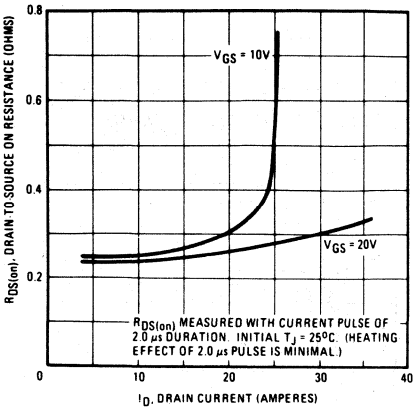


Fig. 12 - Typical on-resistance vs. drain current.

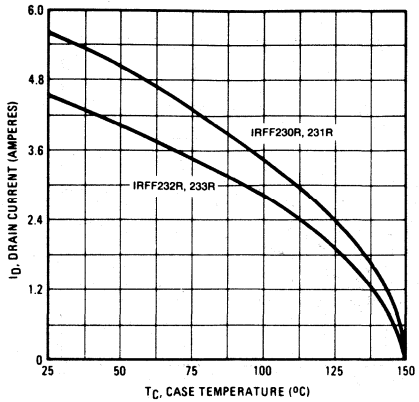


Fig. 13 - Maximum drain current vs. case temperature.

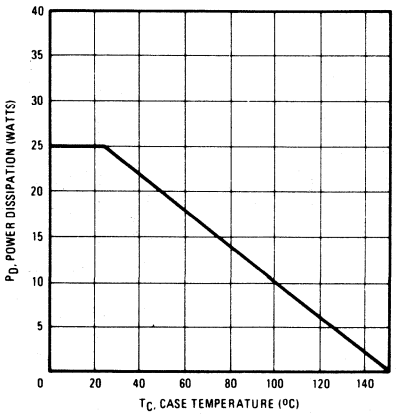


Fig. 14 - Power vs. temperature derating curve.

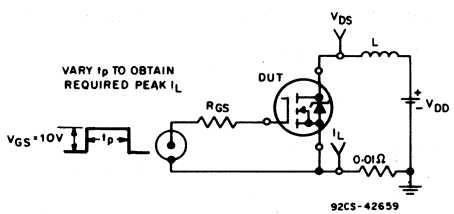


Fig. 15 - Unclamped Energy Test Circuit

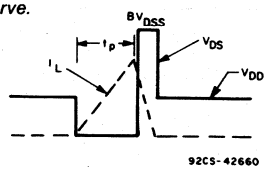


Fig. 16 - Unclamped Energy Waveforms

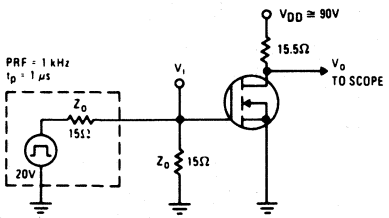


Fig. 17 - Switching time test circuit.

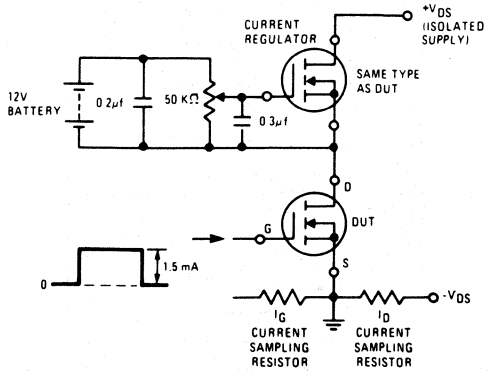


Fig. 18 - Gate charge test circuit.

File Number **2032**

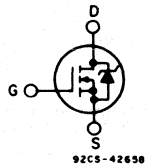
IRFF310R, IRFF311R, IRFF312R, IRFF313R

Avalanche Energy Rated N-Channel Power MOSFETs

1.35A and 1.15A, 350V-400V
$r_{DS}(on) = 3.6\Omega$ and 5.0Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

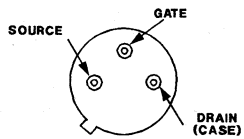


TERMINAL DIAGRAM

The IRFF310R, IRFF311R, IRFF312R and IRFF313R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

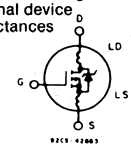
Parameter		IRFF310R	IRFF311R	IRFF312R	IRFF313R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
I_D @ $T_C = 25°C$	Continuous Drain Current	1.35	1.35	1.15	1.15	A
I_{DM}	Pulsed Drain Current ③	5.5	5.5	4.5	4.5	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/K
E_{as}	Single Pulse Avalanche Energy Rating ④	150				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF310R, IRFF311R, IRFF312R, IRFF313R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF310R IRFF312R	400	—	—	V	V_{GS} = 0V
		IRFF311R IRFF313R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF310R IRFF311R	1.35	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF312R IRFF313R	1.15	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF310R IRFF311R	—	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRFF312R IRFF313R	—	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	—	S(Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 0.8A
C_{iss}	Input Capacitance	ALL	—	135	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	35	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	8.0	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	3.0	10	ns	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.8A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	5.0	10	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	3.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

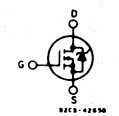


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF310R IRFF311R	—	—	1.35	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF312R IRFF313R	—	—	1.15	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF310R IRFF311R	—	—	5.5	A	
		IRFF312R IRFF313R	—	—	4.5	A	
V_{SD}	Diode Forward Voltage ②	IRFF310R IRFF311R	—	—	1.6	V	T_C = 25°C, I_S = 1.35A, V_{GS} = 0V
		IRFF312R IRFF313R	—	—	1.5	V	T_C = 25°C, I_S = 1.15A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	380	—	ns	T_J = 150°C, I_F = 1.35A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.7	—	μC	T_J = 150°C, I_F = 1.35A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 40V, starting T_J = 25°C, L = 44.89mH, R_{gs} = 50Ω, I_{peak} = 1.35A.

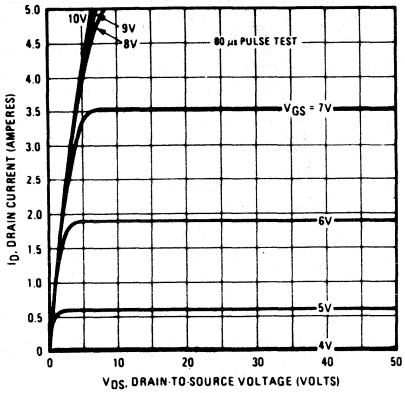


Fig. 1 - Typical output characteristics.

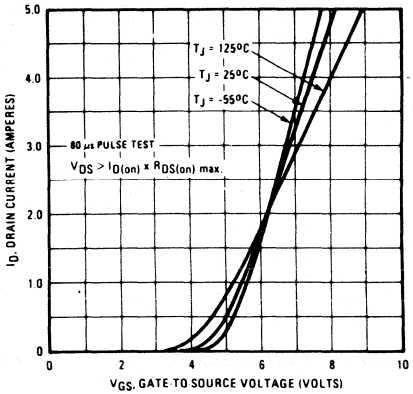


Fig. 2 - Typical transfer characteristics.

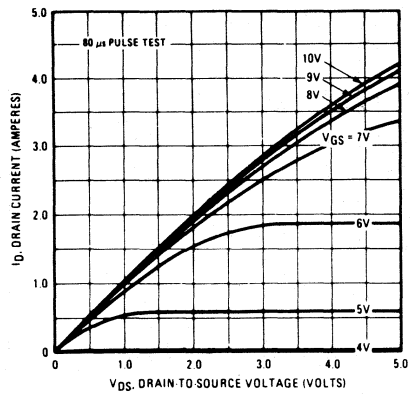


Fig. 3 - Typical saturation characteristics.

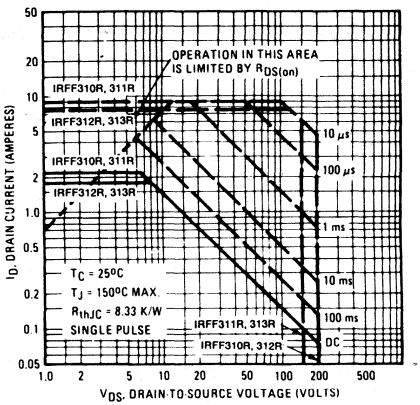


Fig. 4 - Maximum safe operating area.

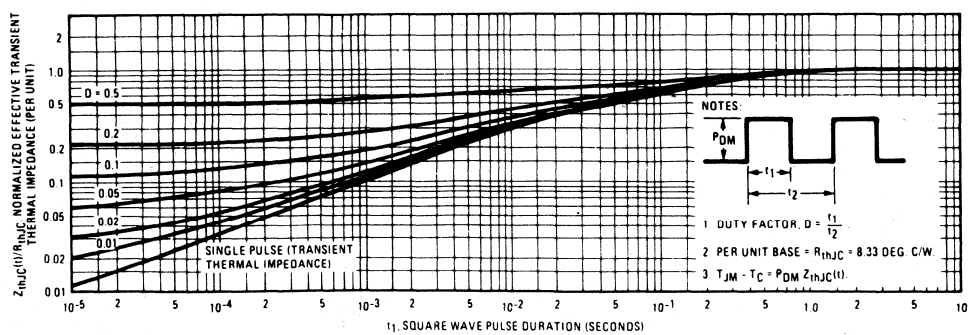


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFF310R, IRFF311R, IRFF312R, IRFF313R

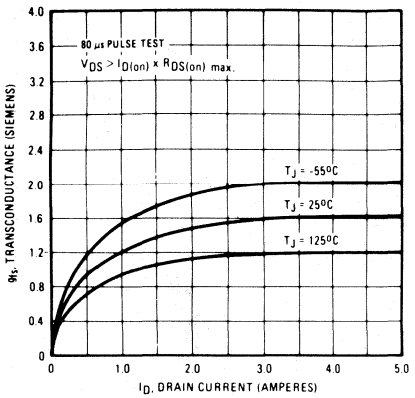


Fig. 6 - Typical transconductance vs. drain current.

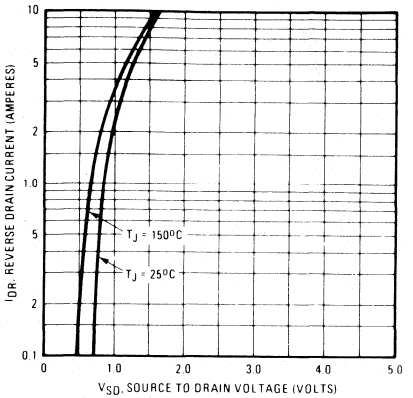


Fig. 7 - Typical source-drain diode forward voltage.

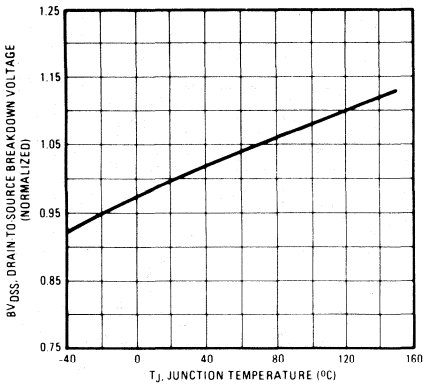


Fig. 8 - Breakdown voltage vs. temperature.

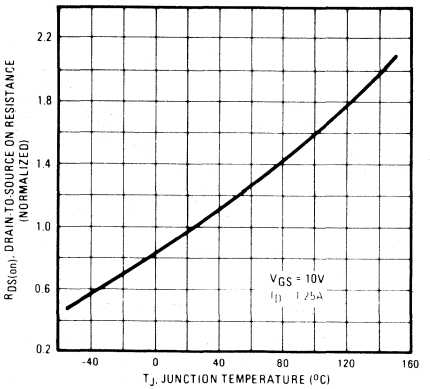


Fig. 9 - Normalized on-resistance vs. temperature.

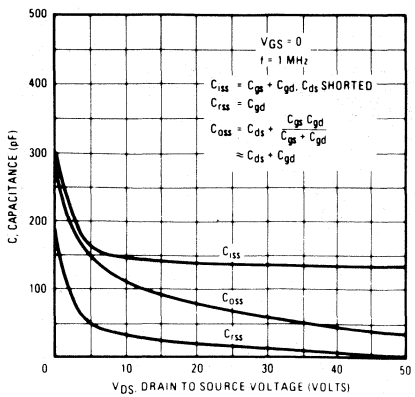


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

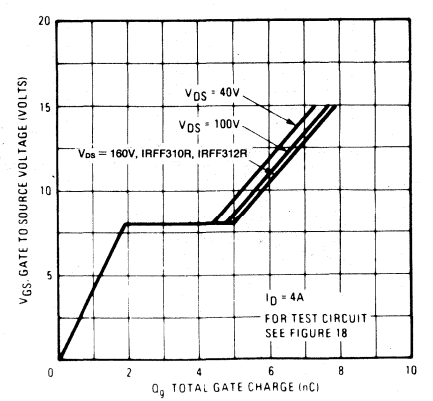


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

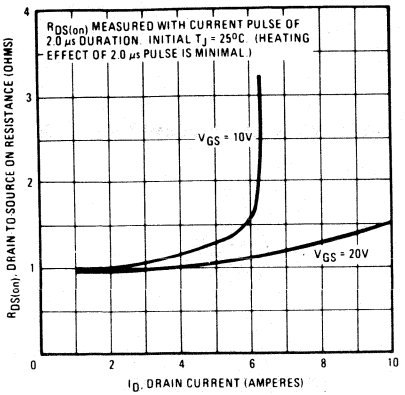


Fig. 12 - Typical on-resistance vs. drain current.

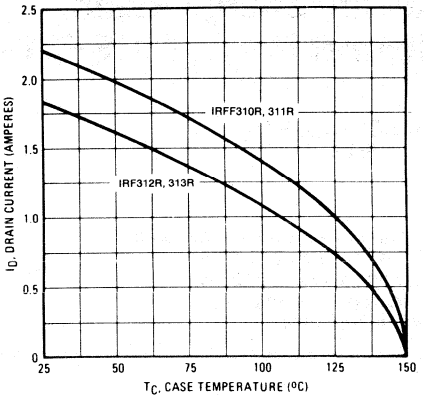


Fig. 13 - Maximum drain current vs. case temperature.

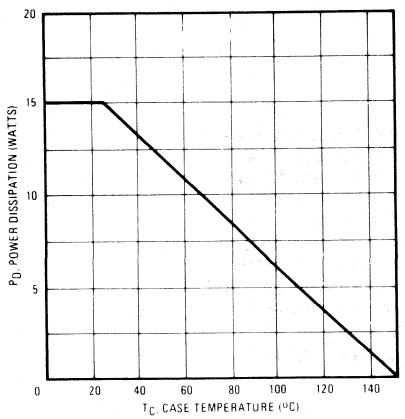


Fig. 14 - Power vs. temperature derating curve.

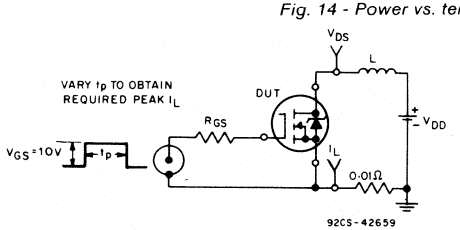


Fig. 15 - Unclamped Energy Test Circuit

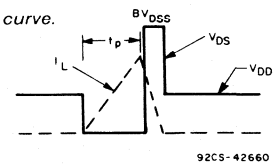


Fig. 16 - Unclamped Energy Waveforms

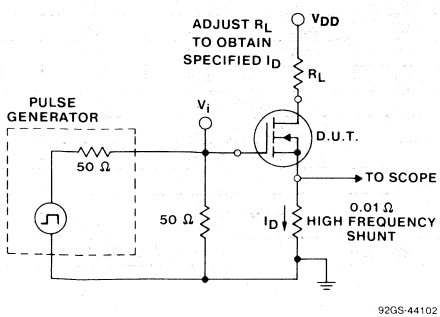


Fig. 17 - Switching time test circuit.

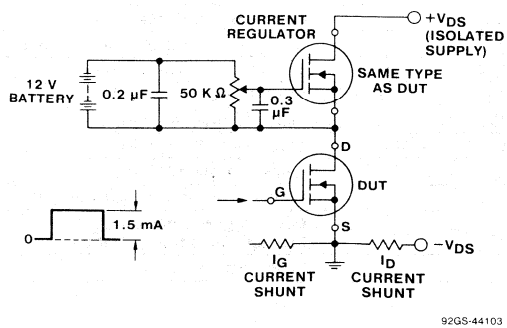


Fig. 18 - Gate charge test circuit.

IRFF320R, IRFF321R, IRFF322R, IRFF323R

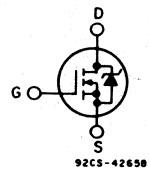
File Number **2028**

Avalanche Energy Rated N-Channel Power MOSFETs

2.0A and 2.5A, 350V-400V
$r_{DS}(on) = 1.8\Omega$ and 2.5Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

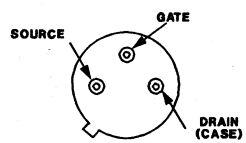


TERMINAL DIAGRAM

The IRFF320R, IRFF321R, IRFF322R and IRFF323R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

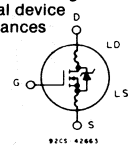
Absolute Maximum Ratings

Parameter		IRFF320R	IRFF321R	IRFF322R	IRFF323R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	100				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF320R IRFF322R	400	—	—	V	$V_{GS} = 0V$
		IRFF321R IRFF323R	350	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRFF320R IRFF321R	2.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRFF322R IRFF323R	2.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF320R IRFF321R	—	1.5	1.8	Ω	$V_{GS} = 10V$, $I_D = 1.25A$
		IRFF322R IRFF323R	—	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 1.25A$
C_{iss}	Input Capacitance	ALL	—	450	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \simeq 0.5BV_{DSS}$, $I_D = 2.0A$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	$V_{GS} = 10V$, $I_D = 5.0A$, $V_{DS} = 0.8V$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances

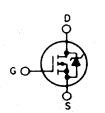


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF320R IRFF321R	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF322R IRFF323R	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF320R IRFF321R	—	—	10	A	
		IRFF322R IRFF323R	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRFF320R IRFF321R	—	—	1.6	V	$T_C = 25°C$, $I_S = 2.5A$, $V_{GS} = 0V$
		IRFF322R IRFF323R	—	—	1.5	V	$T_C = 25°C$, $I_S = 2.0A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150°C$, $I_F = 2.5A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	$T_J = 150°C$, $I_F = 2.5A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 40V$, starting $T_J = 25°C$, L = 29.09mH, $R_{gs} = 50\Omega$, $I_{peak} = 2.5A$.

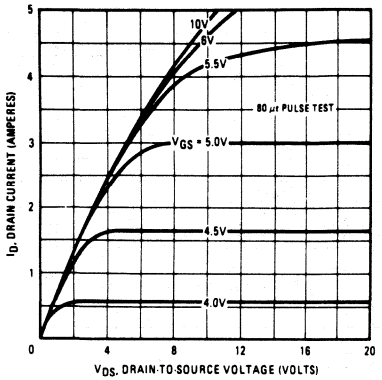


Fig. 1 - Typical output characteristics.

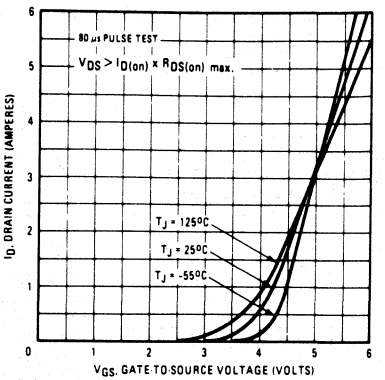


Fig. 2 - Typical transfer characteristics.

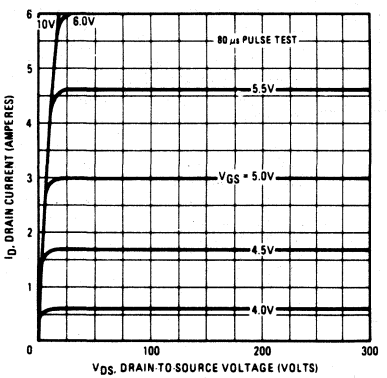


Fig. 3 - Typical saturation characteristics.

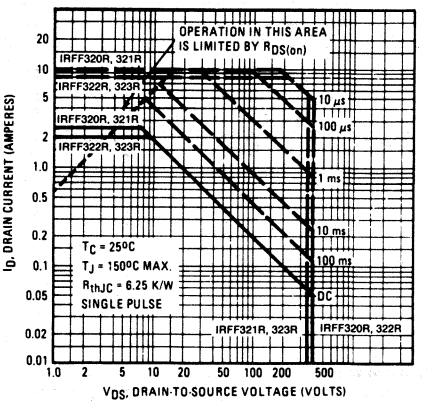


Fig. 4 - Maximum safe operating area.

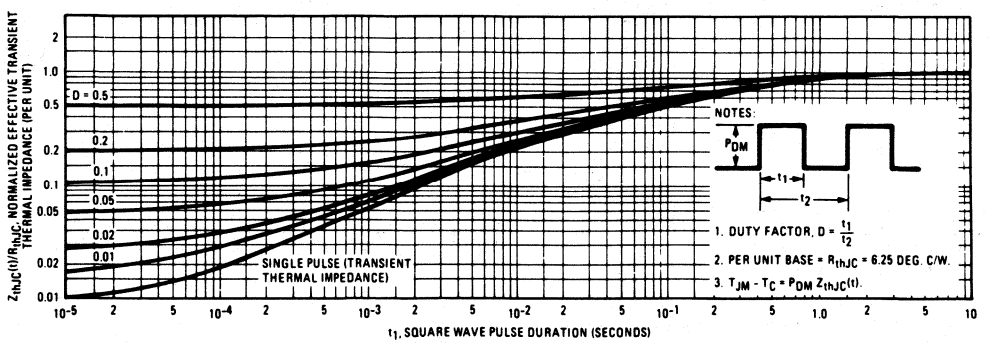


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

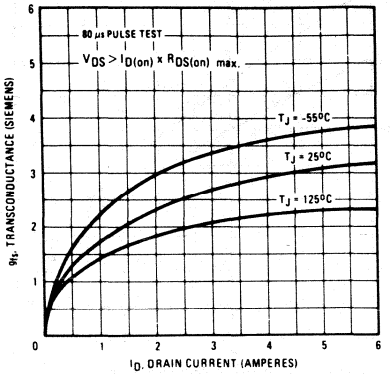


Fig. 6 - Typical transconductance vs. drain current.

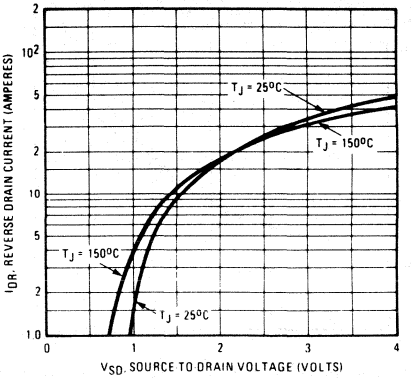


Fig. 7 - Typical source-drain diode forward voltage.

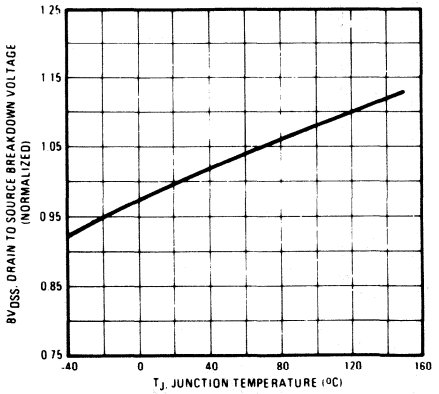


Fig. 8 - Breakdown voltage vs. temperature.

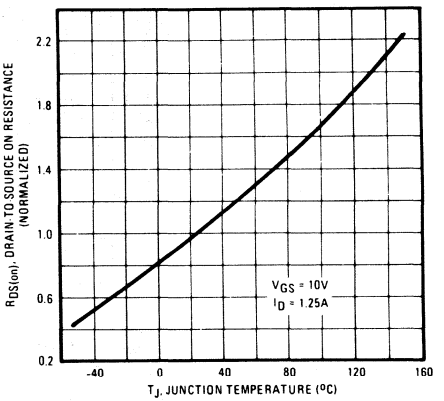


Fig. 9 - Normalized on-resistance vs. temperature.

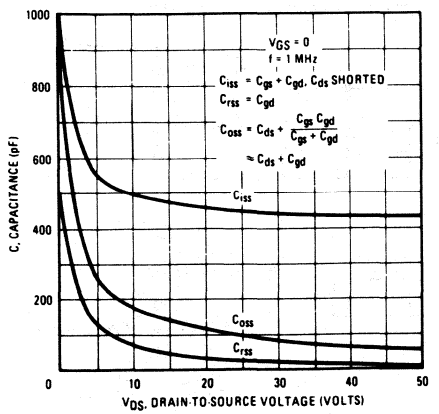


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

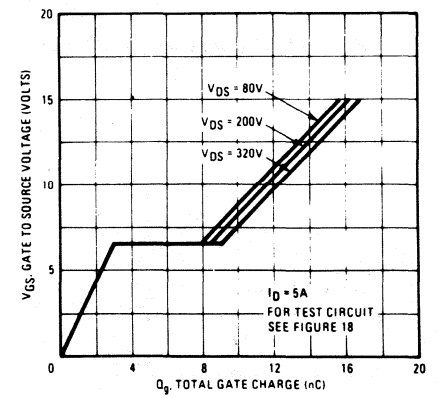


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF320R, IRFF321R, IRFF322R, IRFF323R

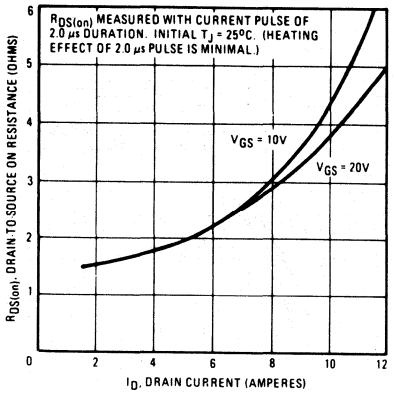


Fig. 12 - Typical on-resistance vs. drain current.

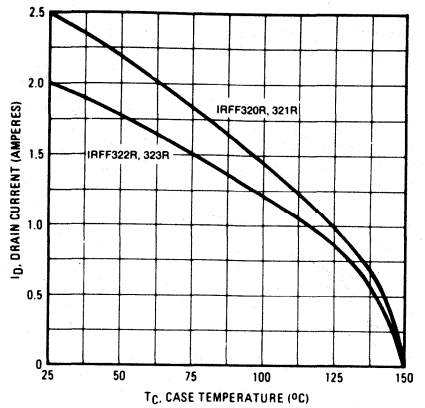


Fig. 13 - Maximum drain current vs. case temperature.

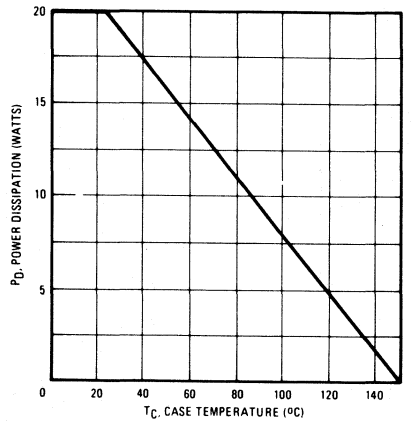


Fig. 14 - Power vs. temperature derating curve.

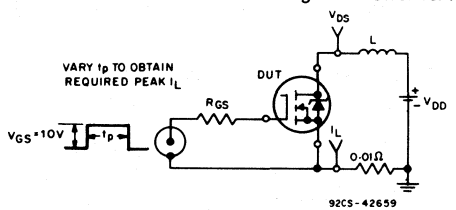


Fig. 15 - Unclamped Energy Test Circuit

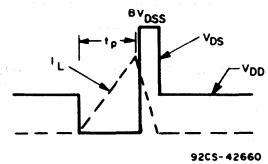


Fig. 16 - Unclamped Energy Waveforms

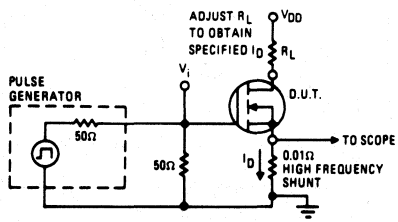


Fig. 17 - Switching time test circuit.

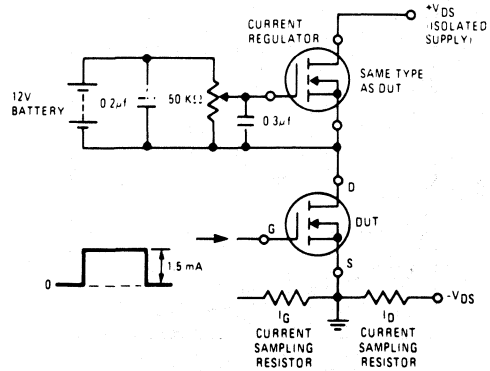


Fig. 18 - Gate charge test circuit.

File Number **2029**

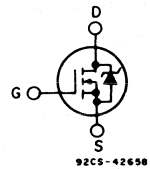
IRFF330R, IRFF331R, IRFF332R, IRFF333R

Avalanche Energy Rated N-Channel Power MOSFETs

3.0A and 3.5A, 350V-400V
$r_{DS}(on) = 1.0\Omega$ and 1.5Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

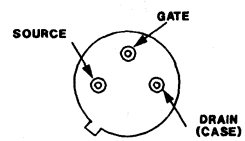


TERMINAL DIAGRAM

The IRFF330R, IRFF331R, IRFF332R and IRFF333R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

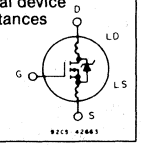
Parameter		IRFF330R	IRFF331R	IRFF332R	IRFF333R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
I_D @ $T_C = 25°C$	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	300				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF330R, IRFF331R, IRFF332R, IRFF333R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF330R IRFF332R	400	—	—	V	V_{GS} = 0V
		IRFF331R IRFF333R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF330R IRFF331R	3.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF332R IRFF333R	3.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF330R IRFF331R	—	0.8	1.0	Ω	V_{GS} = 10V, I_D = 2.0A
		IRFF332R IRFF333R	—	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.0	3.5	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 2.0A
C_{iss}	Input Capacitance	ALL	—	700	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 175V, I_D = 2.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	39	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF330R IRFF331R	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF332R IRFF333R	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF330R IRFF331R	—	—	14	A	
		IRFF332R IRFF333R	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF330R IRFF331R	—	—	1.6	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF332R IRFF333R	—	—	1.5	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 42.85mH, R_{gs} = 25Ω, I_{peak} = 3.5A.

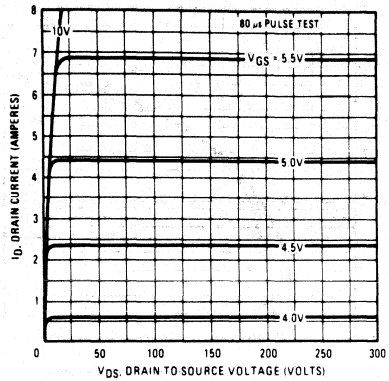


Fig. 1 - Typical output characteristics.

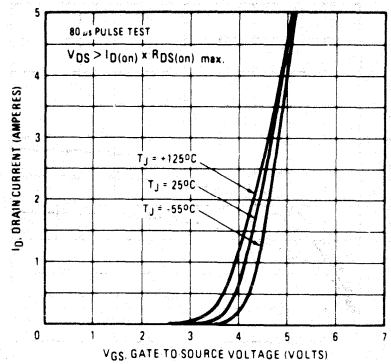


Fig. 2 - Typical transfer characteristics.

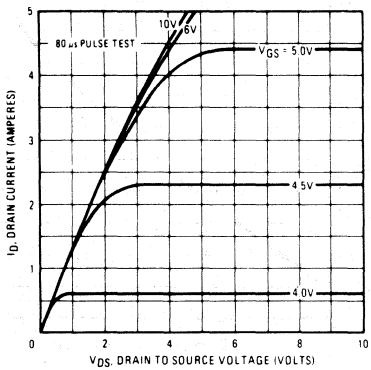


Fig. 3 - Typical saturation characteristics.

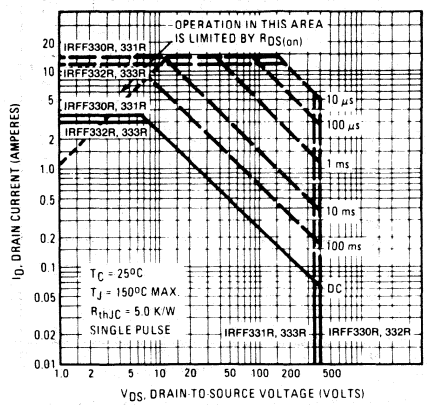


Fig. 4 - Maximum safe operating area.

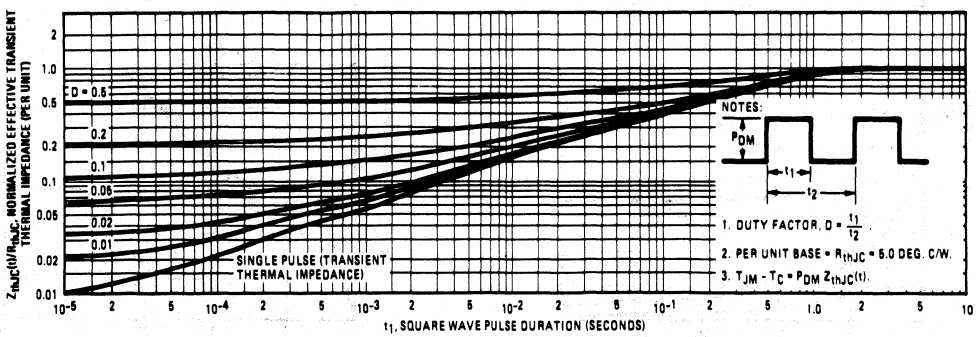


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFF330R, IRFF331R, IRFF332R, IRFF333R

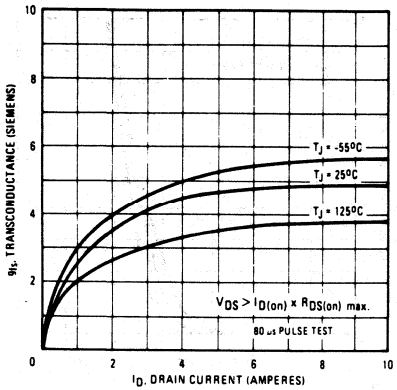


Fig. 6 - Typical transconductance vs. drain current.

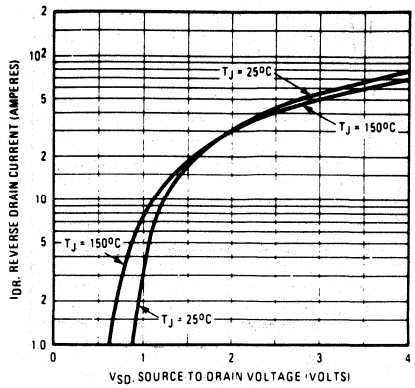


Fig. 7 - Typical source-drain diode forward voltage.

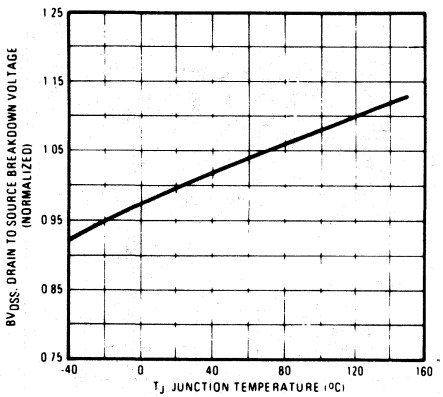


Fig. 8 - Breakdown voltage vs. temperature.

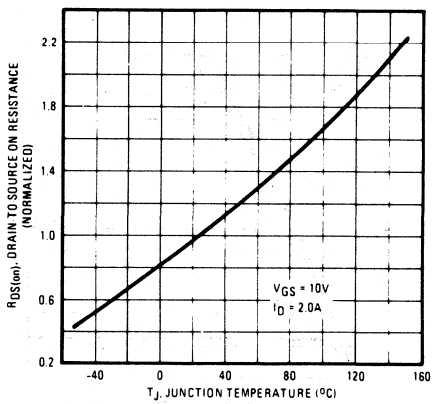


Fig. 9 - Normalized on-resistance vs. temperature.

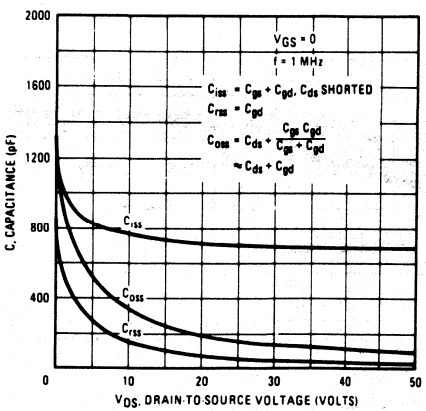


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

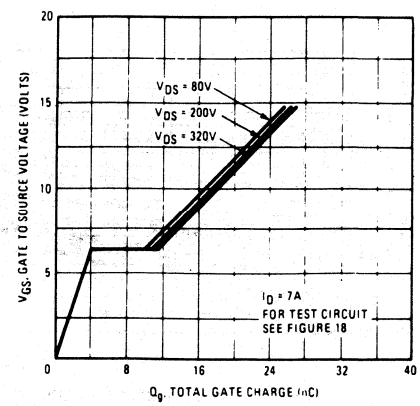
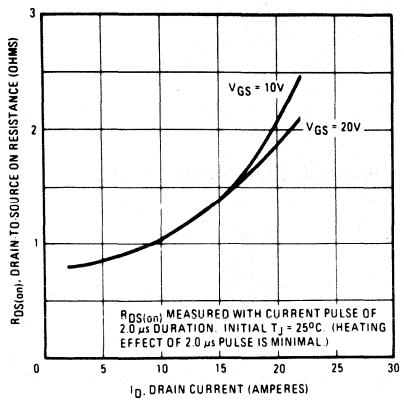


Fig. 11 - Typical gate charge vs. gate-to-source voltage.



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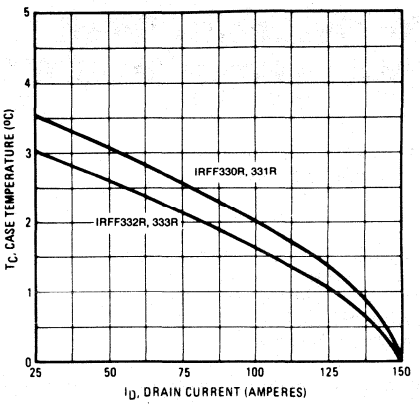


Fig. 13 - Maximum drain current vs. case temperature.

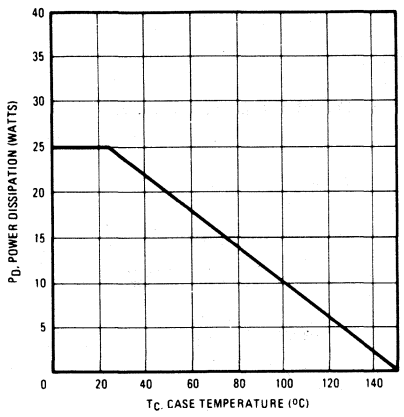


Fig. 14 - Power vs. temperature derating curve.

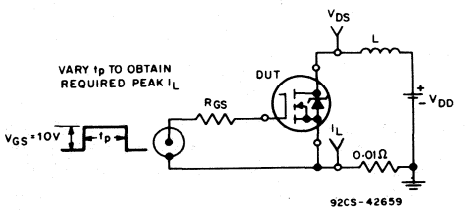


Fig. 15 - Unclamped Energy Test Circuit

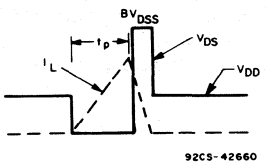


Fig. 16 - Unclamped Energy Waveforms

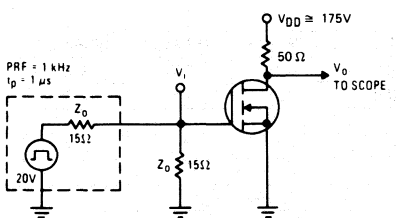


Fig. 17 - Switching time test circuit.

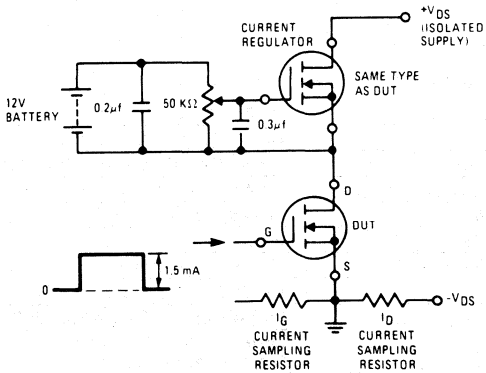


Fig. 18 - Gate charge test circuit.

IRFF420R, IRFF421R, IRFF422R, IRFF423R

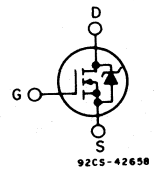
File Number **2030**

Avalanche Energy Rated N-Channel Power MOSFETs

1.4A and 1.6A, 450V-500V
$r_{DS}(on) = 3.0\Omega$ and 4.0Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

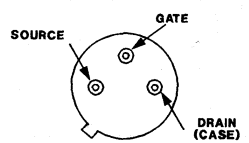


TERMINAL DIAGRAM

The IRFF420R, IRFF421R, IRFF422R and IRFF423R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

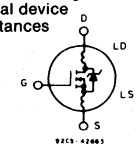
Absolute Maximum Ratings

Parameter		IRFF420R	IRFF421R	IRFF422R	IRFF423R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	1.6	1.6	1.4	1.4	A
I_{DM}	Pulsed Drain Current ③	6.5	6.5	5.5	5.5	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	210				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF420R IRFF422R	500	—	—	V	$V_{GS} = 0V$
		IRFF421R IRFF423R	450	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRFF420R IRFF421R	1.6	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRFF422R IRFF423R	1.4	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF420R IRFF421R	—	2.5	3.0	Ω	$V_{GS} = 10V$, $I_D = 1.0A$
		IRFF422R IRFF423R	—	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 1.0A$
C_{iss}	Input Capacitance	ALL	—	300	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	75	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	$V_{DD} \simeq 0.5BV_{DSS}$, $I_D = 1.0A$, $Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	30	60	ns	
t_f	Fall Time	ALL	—	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	26	nC	$V_{GS} = 10V$, $I_D = 3.0A$, $V_{DS} = 0.8V$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF420R IRFF421R	—	—	1.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF422R IRFF423R	—	—	1.4	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF420R IRFF421R	—	—	6.5	A	
		IRFF422R IRFF423R	—	—	5.5	A	
V_{SD}	Diode Forward Voltage ②	IRFF420R IRFF421R	—	—	1.4	V	$T_C = 25°C$, $I_S = 1.6A$, $V_{GS} = 0V$
		IRFF422R IRFF423R	—	—	1.3	V	$T_C = 25°C$, $I_S = 1.4A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150°C$, $I_F = 1.6A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.5	—	μC	$T_J = 150°C$, $I_F = 1.6A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 50V$, starting $T_J = 25°C$, L = 143.5mH, $R_{gs} = 25\Omega$, $I_{peak} = 1.6A$.

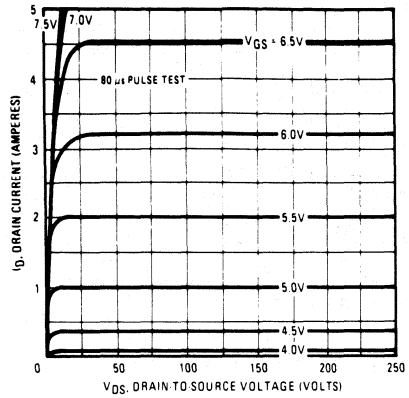


Fig. 1 - Typical output characteristics.

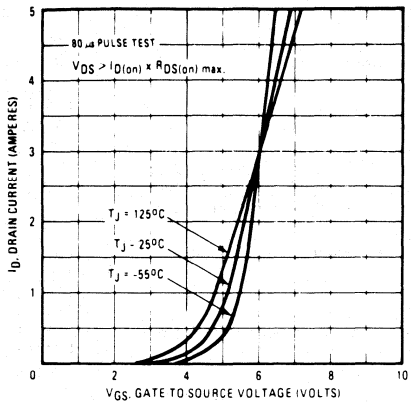


Fig. 2 - Typical transfer characteristics.

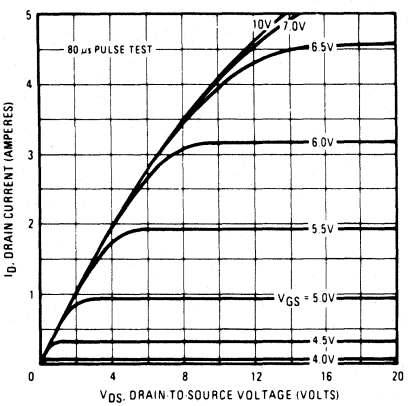


Fig. 3 - Typical saturation characteristics.

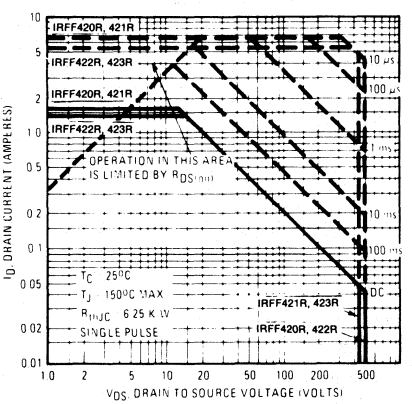


Fig. 4 - Maximum safe operating area.

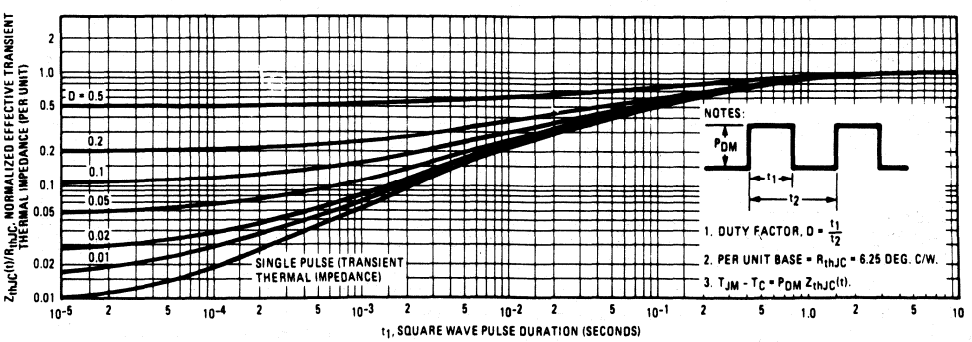


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

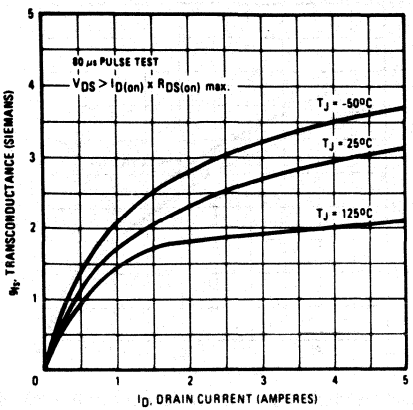


Fig. 6 - Typical transconductance vs. drain current.

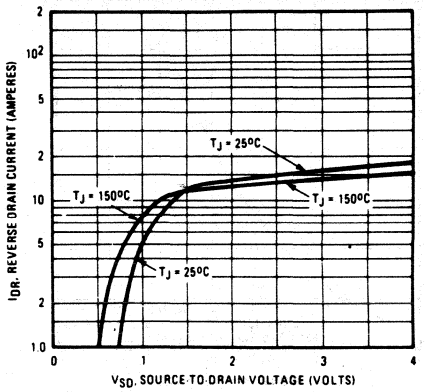


Fig. 7 - Typical source-drain diode forward voltage.

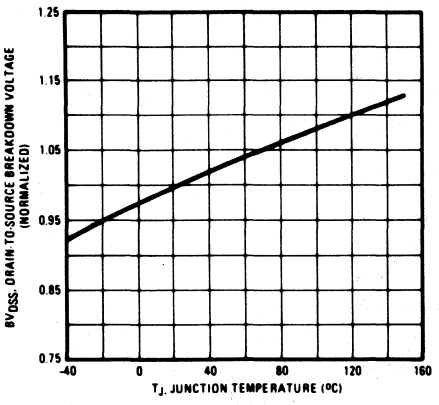


Fig. 8 - Breakdown voltage vs. temperature.

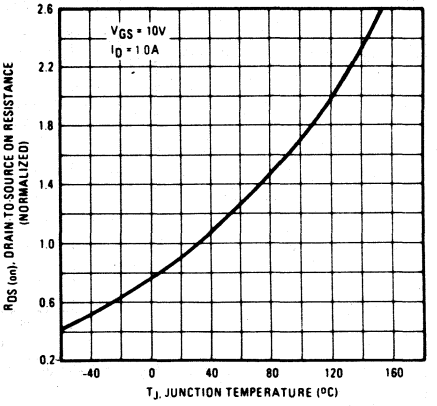


Fig. 9 - Normalized on-resistance vs. temperature.

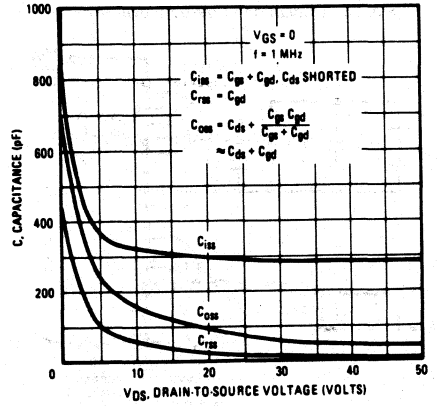


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

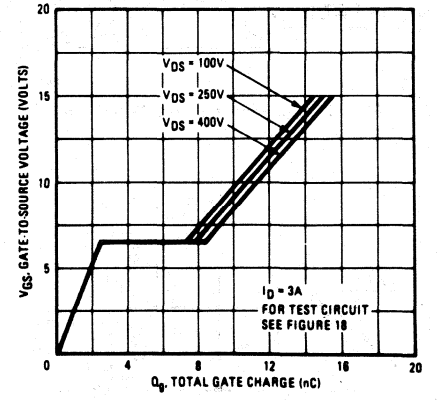


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFF420R, IRFF421R, IRFF422R, IRFF423R

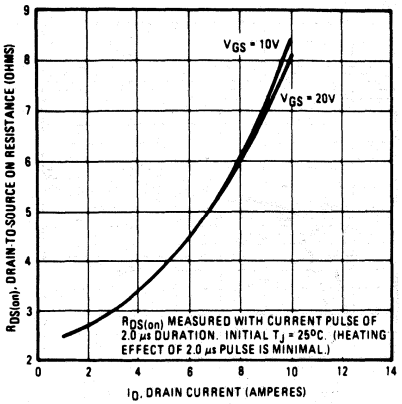


Fig. 12 - Typical on-resistance vs. drain current.

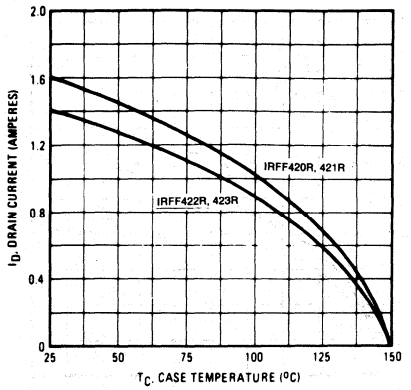


Fig. 13 - Maximum drain current vs. case temperature.

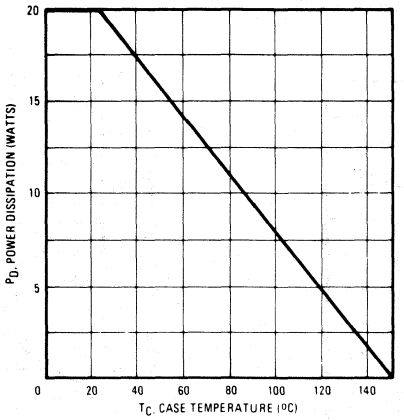


Fig. 14 - Power vs. temperature derating curve.

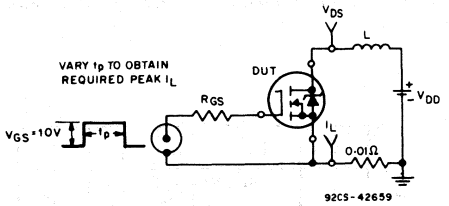


Fig. 15 - Unclamped Energy Test Circuit

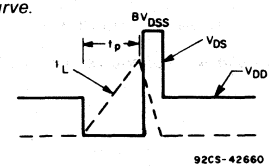


Fig. 16 - Unclamped Energy Waveforms

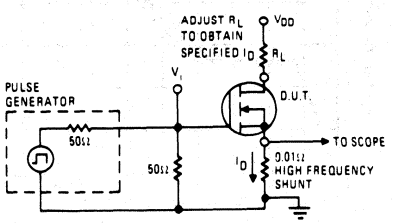


Fig. 17 - Switching time test circuit.

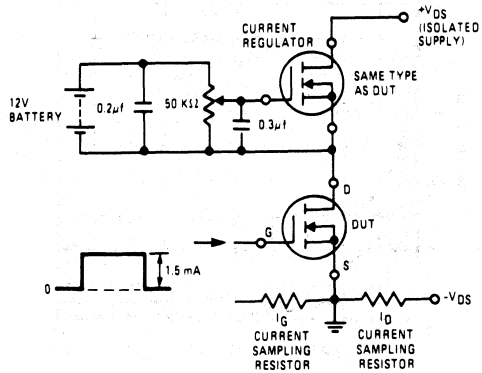


Fig. 18 - Gate charge test circuit.

File Number **2031**

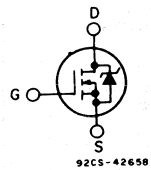
IRFF430R, IRFF431R, IRFF432R, IRFF433R

Avalanche Energy Rated N-Channel Power MOSFETs

2.25A and 2.75A, 450V-500V
$r_{DS}(on) = 1.5\Omega$ and 2.0Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

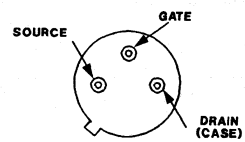


TERMINAL DIAGRAM

The IRFF430R, IRFF431R, IRFF432R and IRFF433R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

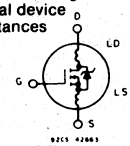
Parameter		IRFF430R	IRFF431R	IRFF432R	IRFF433R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	2.75	2.75	2.25	2.25	A
I_{DM}	Pulsed Drain Current ③	11	11	9.0	9.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	300				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF430R, IRFF431R, IRFF432R, IRFF433R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF430R IRFF432R	500	—	—	V	V_{GS} = 0V
		IRFF431R IRFF433R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF430R IRFF431R	2.75	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFF432R IRFF433R	2.25	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF430R IRFF431R	—	1.3	1.5	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF432R IRFF433R	—	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.5	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 225V, I_D = 1.5A, Z_0 = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	39	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	11	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF430R IRFF431R	—	—	2.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF432R IRFF433R	—	—	2.25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF430R IRFF431R	—	—	11	A	
		IRFF432R IRFF433R	—	—	9.0	A	
V_{SD}	Diode Forward Voltage ②	IRFF430R IRFF431R	—	—	1.4	V	T_C = 25°C, I_S = 2.75A, V_{GS} = 0V
		IRFF432R IRFF433R	—	—	1.3	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 69.42mH, R_{gs} = 50Ω, I_{peak} = 2.75A.

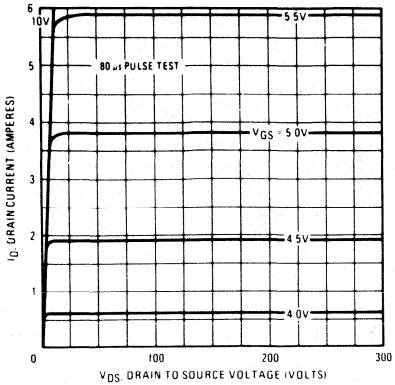


Fig. 1 - Typical output characteristics.

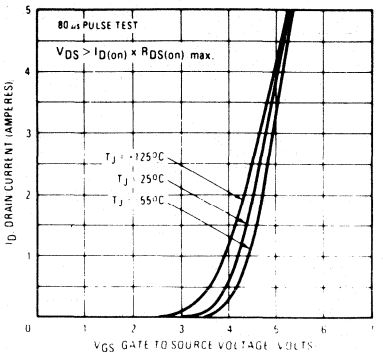


Fig. 2 - Typical transfer characteristics.

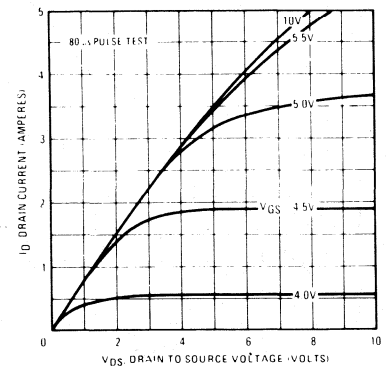


Fig. 3 - Typical saturation characteristics.

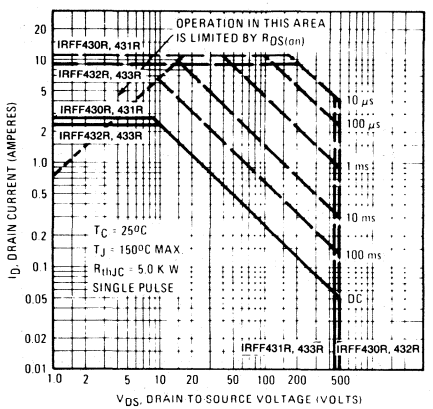


Fig. 4 - Maximum safe operating area.

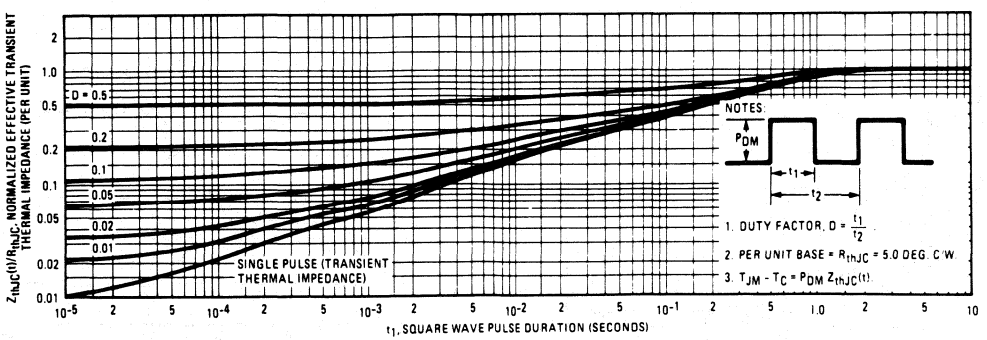


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFF430R, IRFF431R, IRFF432R, IRFF433R

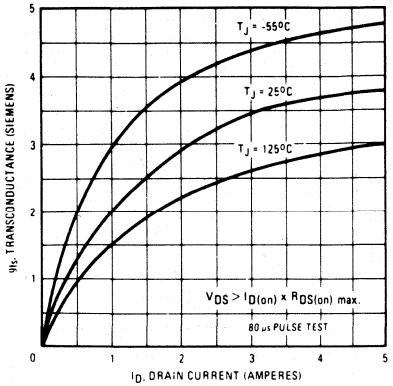


Fig. 6 - Typical transconductance vs. drain current.

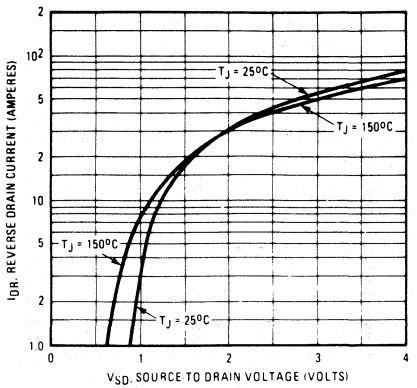


Fig. 7 - Typical source-drain diode forward voltage.

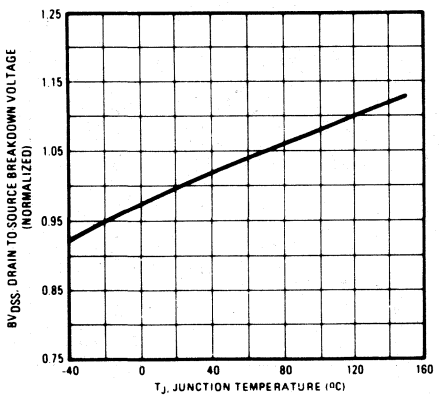


Fig. 8 - Breakdown voltage vs. temperature.

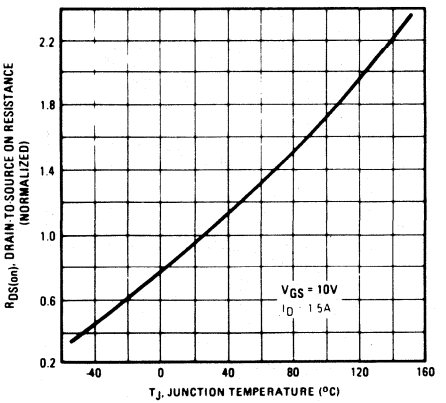


Fig. 9 - Normalized on-resistance vs. temperature.

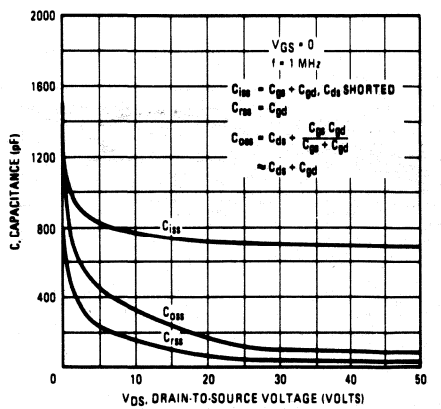


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

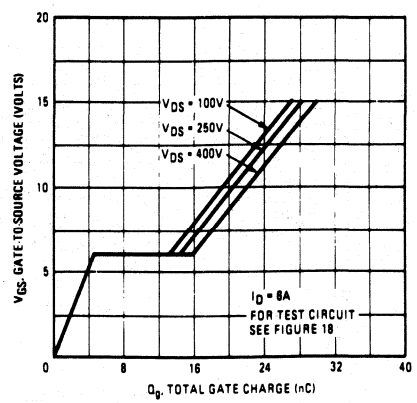


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

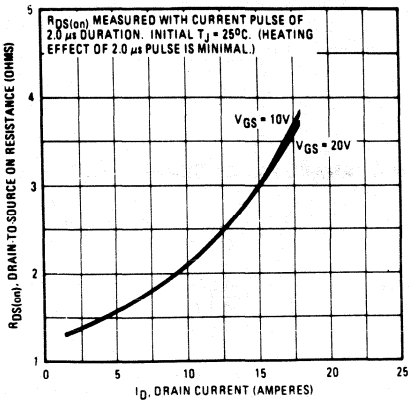


Fig. 12 - Typical on-resistance vs. drain current.

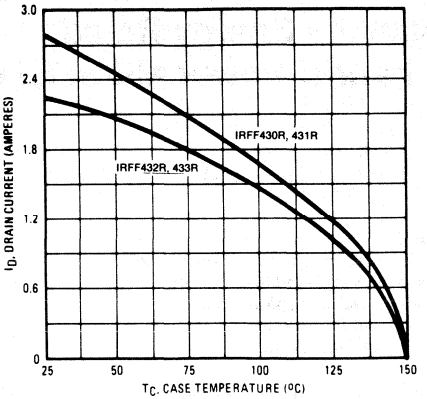


Fig. 13 - Maximum drain current vs. case temperature.

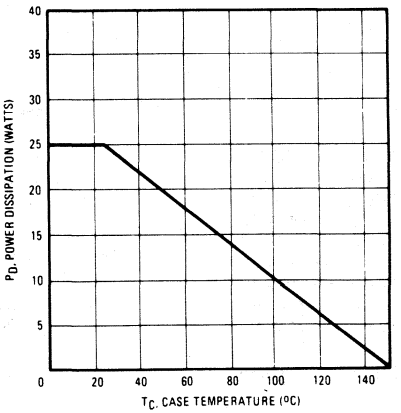


Fig. 14 - Power vs. temperature derating curve.

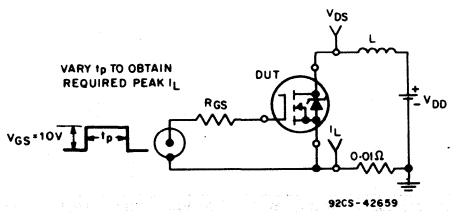


Fig. 15 - Unclamped Energy Test Circuit

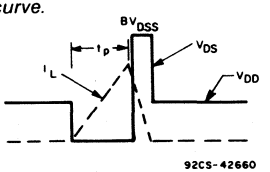


Fig. 16 - Unclamped Energy Waveforms

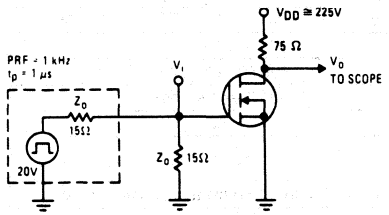


Fig. 17 - Switching time test circuit.

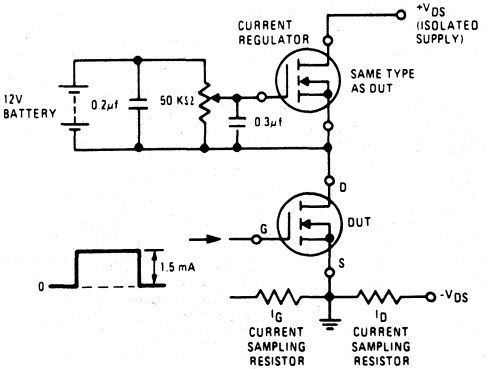


Fig. 18 - Gate charge test circuit.

IRFP140R, IRFP141R, IRFP142R, IRFP143R

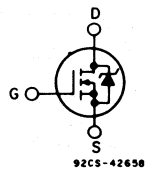
File Number **2086**

Avalanche Energy Rated N-Channel Power MOSFETs

27A and 24A, 60V-100V
$r_{DS}(on) = 0.085\Omega$ and 0.11Ω

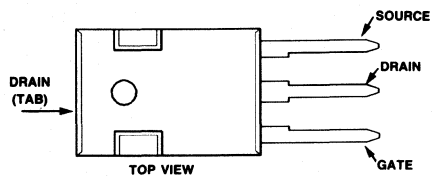
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-247

The IRFP140R, IRFP141R, IRFP142R and IRFP143R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

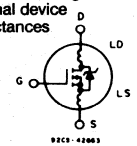
Absolute Maximum Ratings

Parameter		IRFP140R	IRFP141R	IRFP142R	IRFP143R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	27	27	24	24	A
I_D @ $T_C = 100°C$	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	100				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP140R IRFP142R	100	—	—	V	$V_{GS} = 0V$
		IRFP141R IRFP143R	60	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRFP140R IRFP141R	27	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, $V_{GS} = 10V$
		IRFP142R IRFP143R	24	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP140R IRFP141R	—	0.07	0.085	Ω	$V_{GS} = 10V$, $I_D = 15A$
		IRFP142R IRFP143R	—	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 15A$
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	550	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} \simeq 30V$, $I_D = 15A$, $Z_o = 4.7\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	38	80	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	$V_{GS} = 10V$, $I_D = 34A$, $V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	17	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	21	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

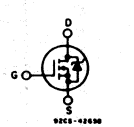


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP140R IRFP141R	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP142R IRFP143R	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP140R IRFP141R	—	—	108	A	
		IRFP142R IRFP143R	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	IRFP140R IRFP141R	—	—	2.5	V	$T_C = 25°C$, $I_S = 27A$, $V_{GS} = 0V$
		IRFP142R IRFP143R	—	—	2.3	V	$T_C = 25°C$, $I_S = 24A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	$T_J = 150°C$, $I_F = 27A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	$T_J = 150°C$, $I_F = 27A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 10V$, starting $T_J = 25°C$, $L = 250\mu H$, $R_{gs} = 50\Omega$, $I_{peak} = 27A$. See figures 15, 16.

IRFP140R, IRFP141R, IRFP142R, IRFP143R

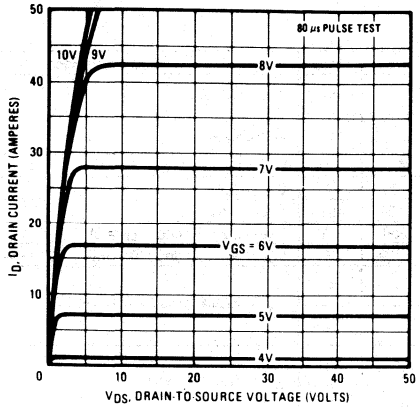


Fig. 1 - Typical output characteristics.

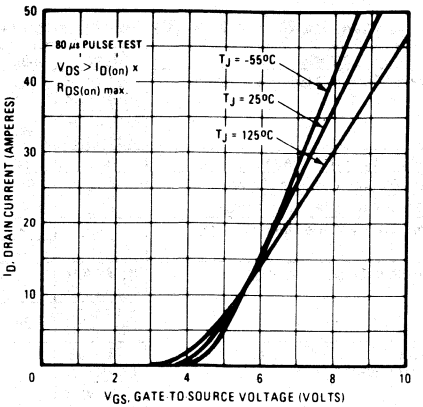


Fig. 2 - Typical transfer characteristics.

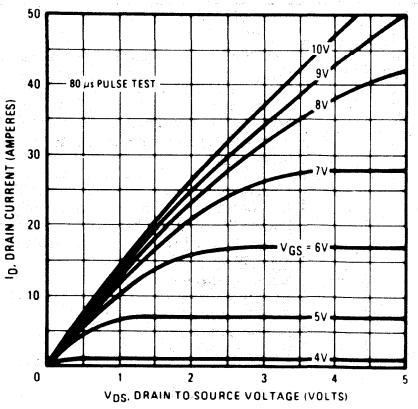


Fig. 3 - Typical saturation characteristics.

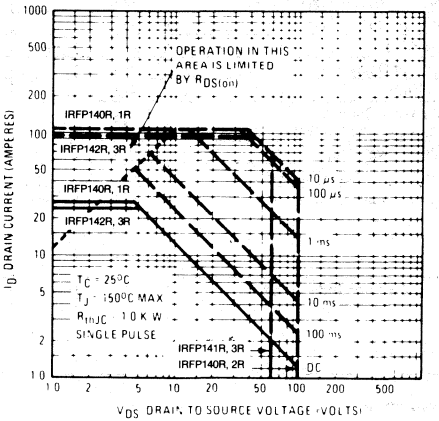


Fig. 4 - Maximum safe operating area.

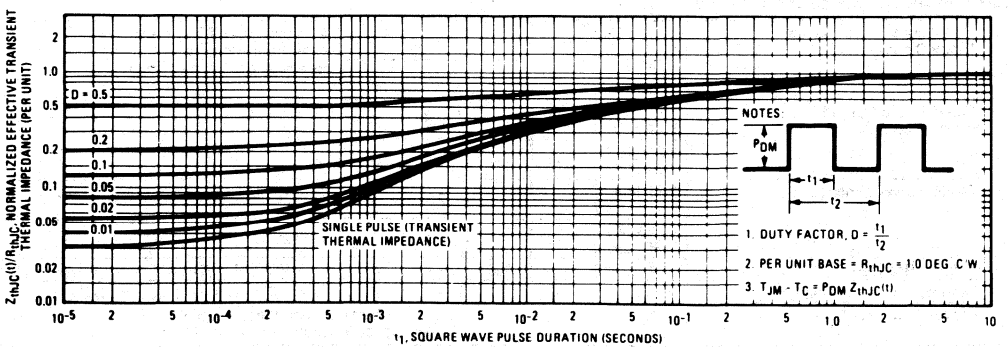


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

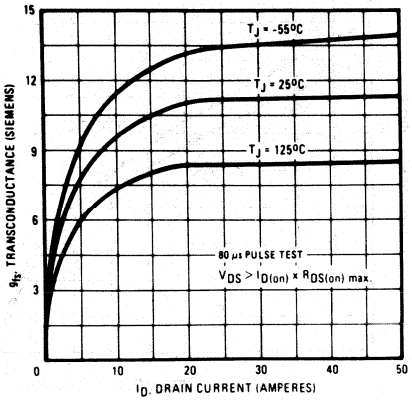


Fig. 6 - Typical transconductance vs. drain current.

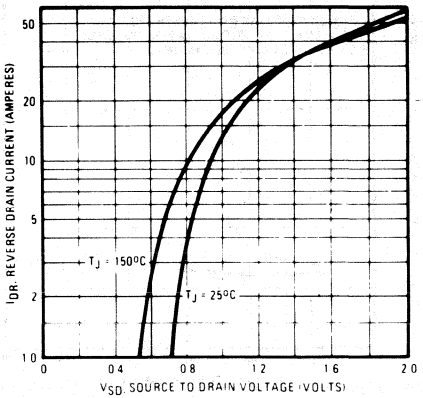


Fig. 7 - Typical source-drain diode forward voltage.

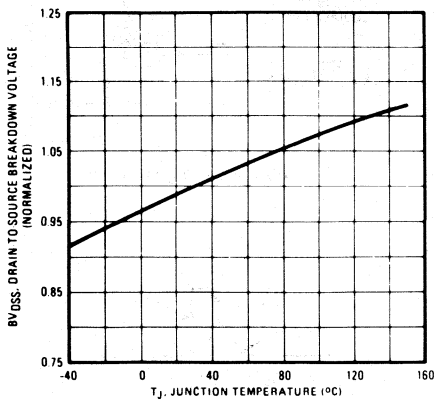


Fig. 8 - Breakdown voltage vs. temperature.

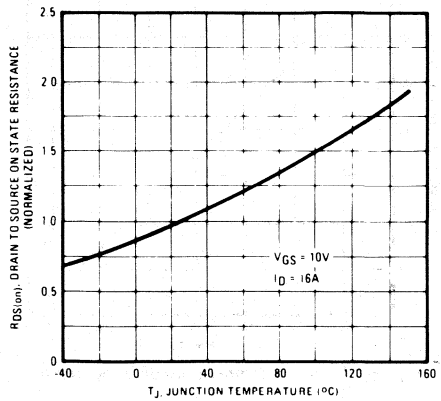


Fig. 9 - Normalized on-resistance vs. temperature.

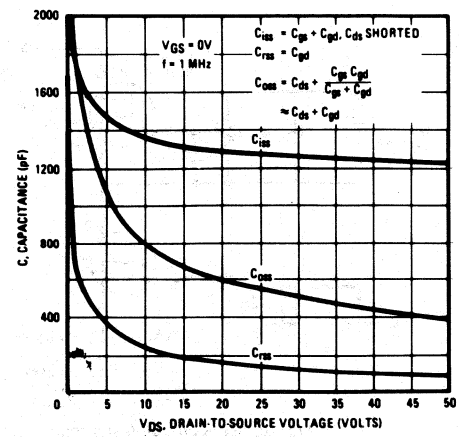


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

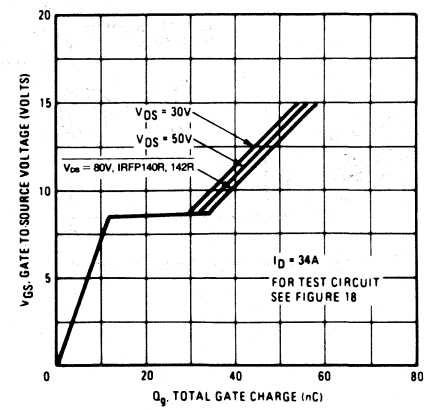


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFP140R, IRFP141R, IRFP142R, IRFP143R

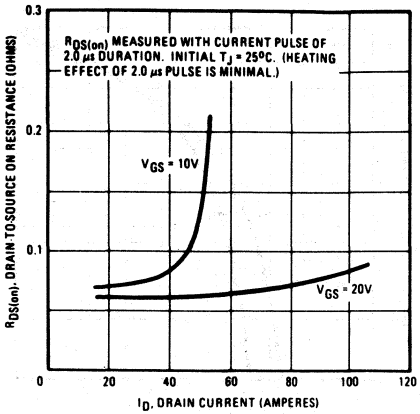


Fig. 12 - Typical on-resistance vs. drain current.

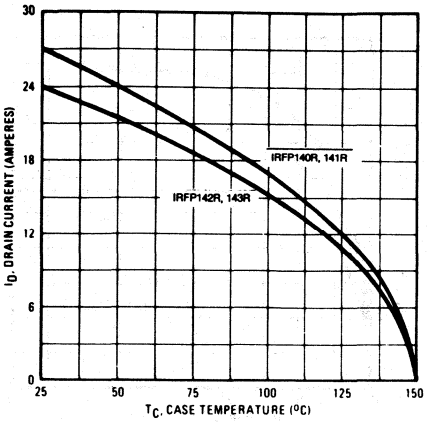


Fig. 13 - Maximum drain current vs. case temperature.

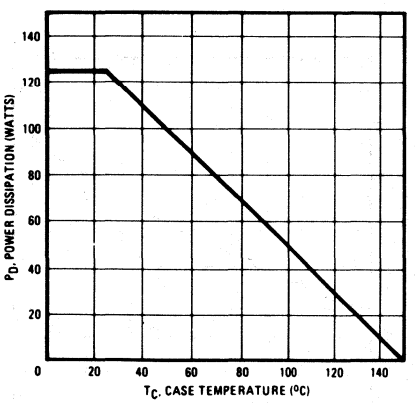


Fig. 14 - Power vs. temperature derating curve.

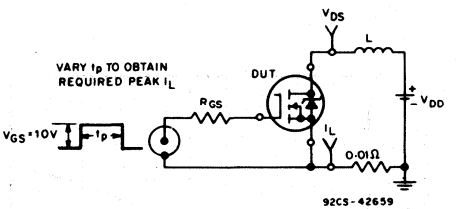


Fig. 15 - Unclamped energy test circuit.

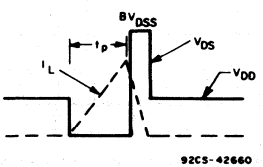


Fig. 16 - Unclamped energy waveforms.

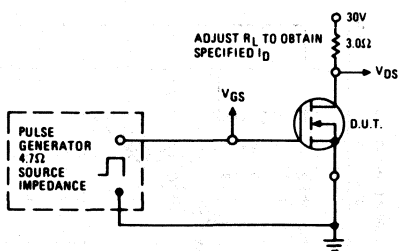


Fig. 17 - Switching time test circuit.

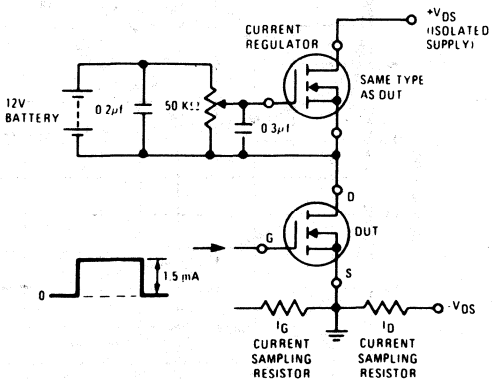


Fig. 18 - Gate charge test circuit.

File Number **2015**

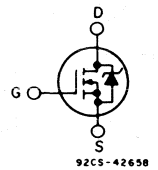
IRFP150R, IRFP151R, IRFP152R, IRFP153R

Avalanche Energy Rated N-Channel Power MOSFETs

33A and 40A, 60V-100V
$r_{DS}(on)$ = 0.055Ω and 0.08Ω

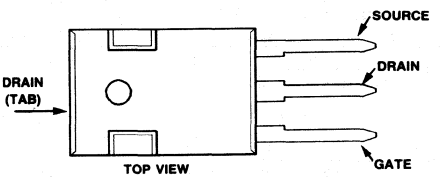
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-247

The IRFP150R, IRFP151R, IRFP152R and IRFP153R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

Absolute Maximum Ratings

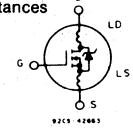
Parameter		IRFP150R	IRFP151R	IRFP152R	IRFP153R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	40	40	33	33	A
I_D @ T_C = 100°C	Continuous Drain Current	25	25	20	20	A
I_{DM}	Pulsed Drain Current ③	160	160	132	132	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	150				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP150R, IRFP151R, IRFP152R, IRFP153R

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP150R IRFP152R	100	—	—	V	$V_{GS} = 0V$
		IRFP151R IRFP153R	60	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRFP150R IRFP151R	40	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRFP152R IRFP153R	33	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP150R IRFP151R	—	0.045	0.055	Ω	$V_{GS} = 10V$, $I_D = 20A$
		IRFP152R IRFP153R	—	0.06	0.08	Ω	
g_{fs}	Forward Transconductance ②	ALL	9.0	11	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 20A$
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	1000	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	350	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq 24V$, $I_D = 20A$, $Z_o = 4.7\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	125	ns	
t_f	Fall Time	ALL	—	—	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	63	120	nC	$V_{GS} = 10V$, $I_D = 50A$, $V_{DS} = 0.8V$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	27	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	36	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

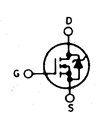


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP150R IRFP151R	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP152R IRFP153R	—	—	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP150R IRFP151R	—	—	160	A	
		IRFP152R IRFP153R	—	—	132	A	
V_{SD}	Diode Forward Voltage ②	IRFP150R IRFP151R	—	—	2.5	V	$T_C = 25°C$, $I_S = 40A$, $V_{GS} = 0V$
		IRFP152R IRFP153R	—	—	2.3	V	$T_C = 25°C$, $I_S = 33A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	$T_J = 150°C$, $I_F = 40A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	3.3	—	μC	$T_J = 150°C$, $I_F = 40A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 10V$, starting $T_J = 25°C$, L = 170μH, $R_{gs} = 50\Omega$, $I_{peak} = 40A$. See figures 15, 16.

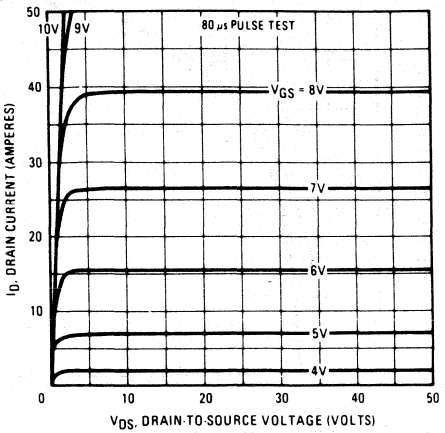


Fig. 1 — Typical Output Characteristics

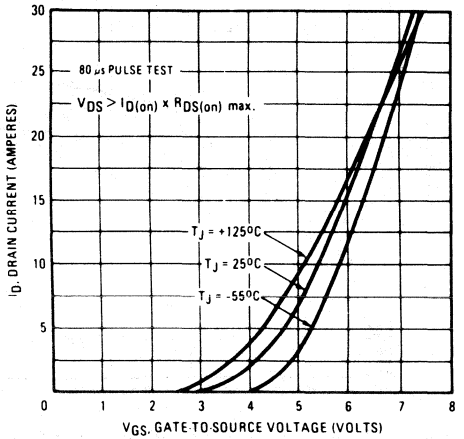


Fig. 2 — Typical Transfer Characteristics

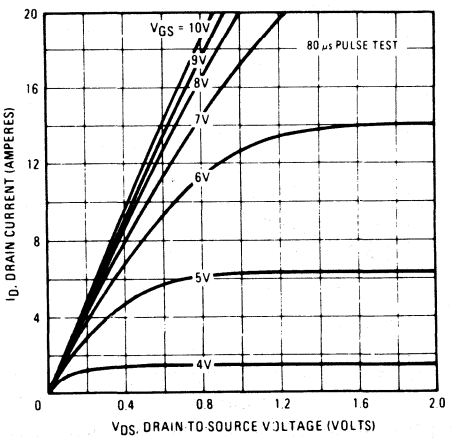


Fig. 3 — Typical Saturation Characteristics

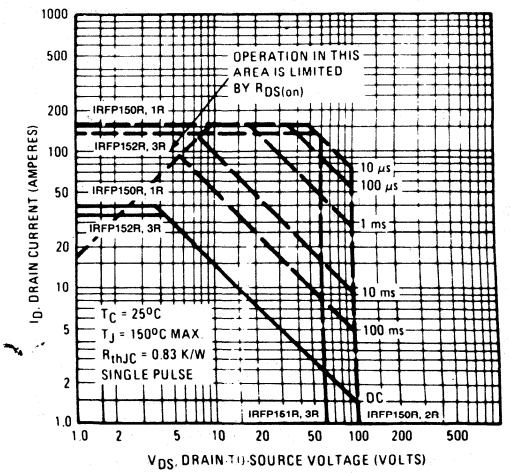


Fig. 4 — Maximum Safe Operating Area

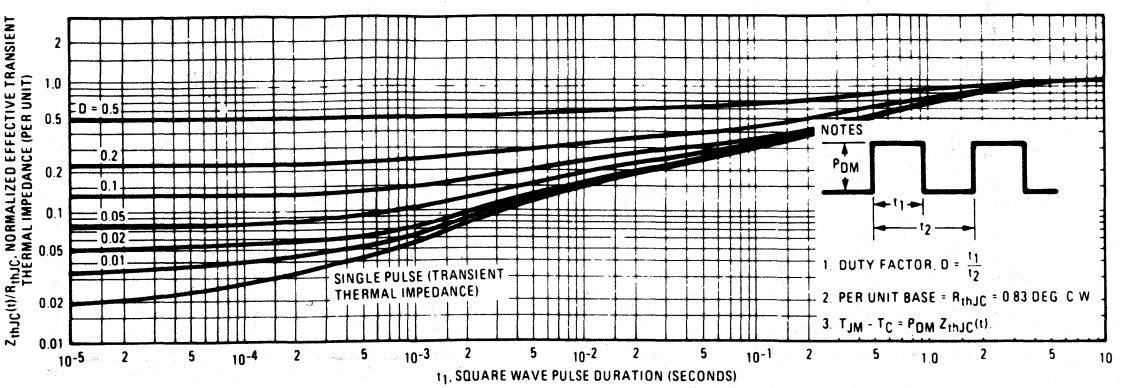


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

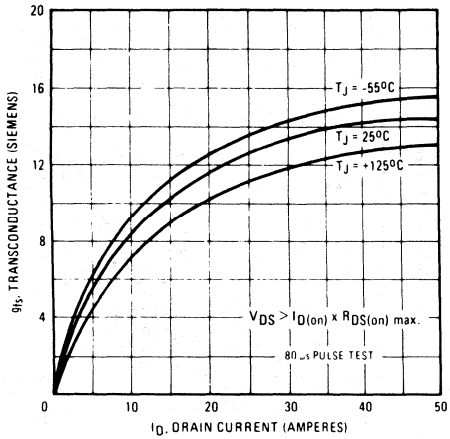


Fig. 6 – Typical Transconductance Vs. Drain Current

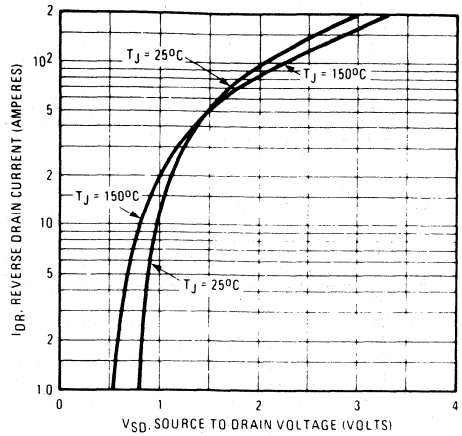


Fig. 7 – Typical Source-Drain Diode Forward Voltage

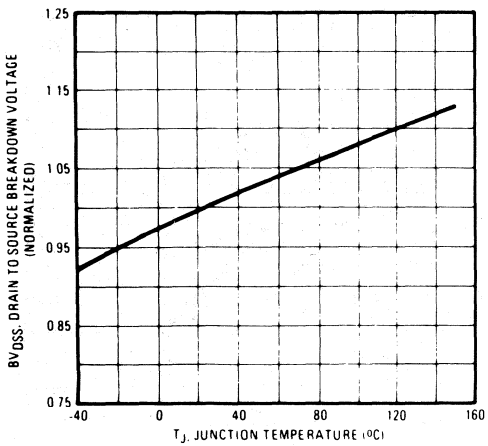


Fig. 8 – Breakdown Voltage Vs. Temperature

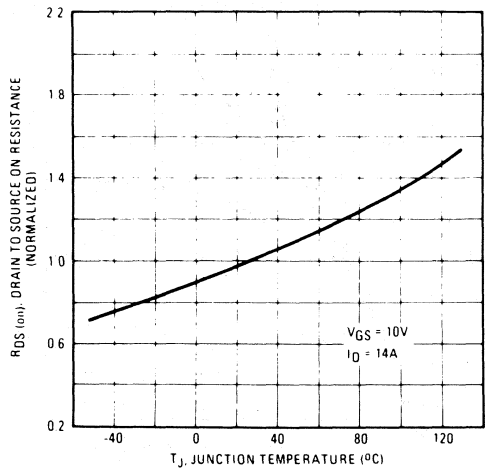


Fig. 9 – Normalized On-Resistance Vs. Temperature

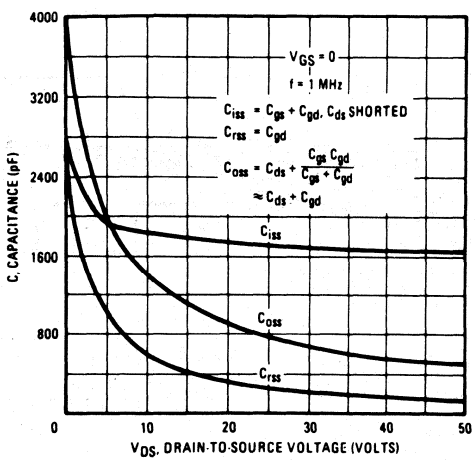


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

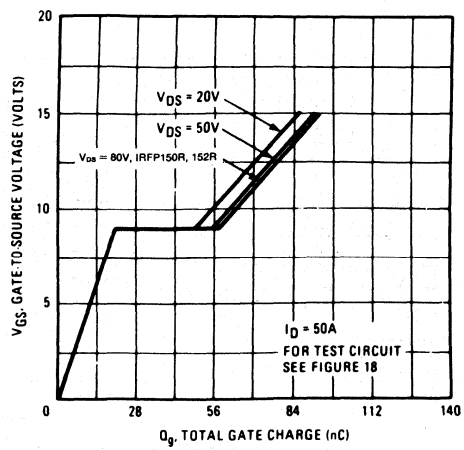


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

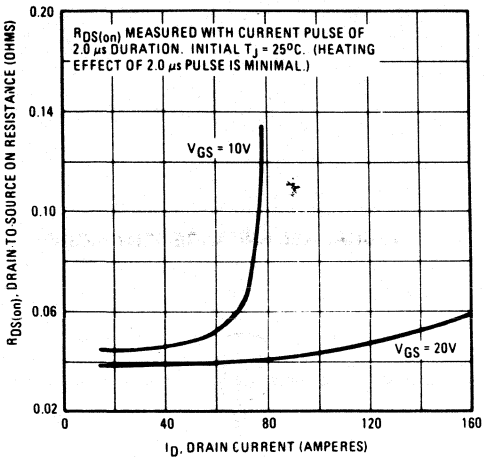


Fig. 12 – Typical On-Resistance Vs. Drain Current

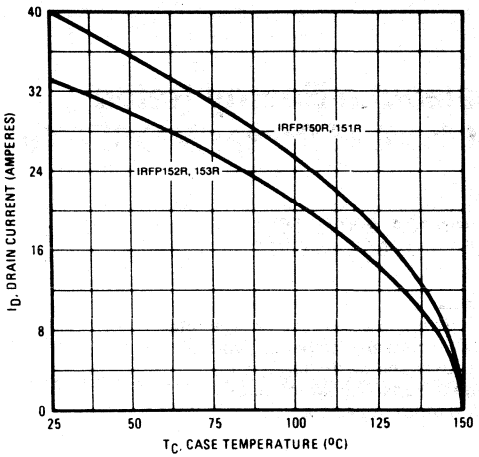


Fig. 13 – Maximum Drain Current Vs. Case Temperature

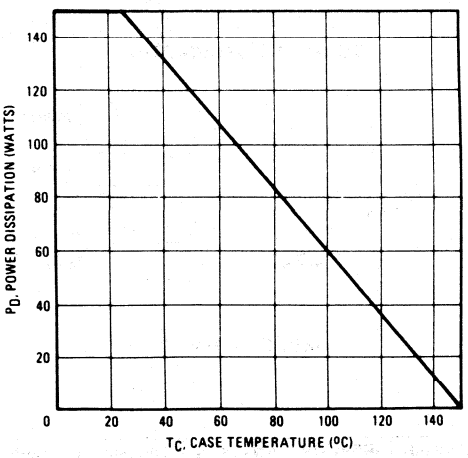


Fig. 14 – Power Vs. Temperature Derating Curve

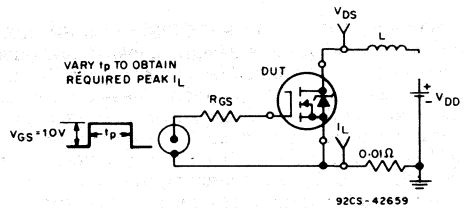


Fig. 15 — Unclamped Energy Test Circuit

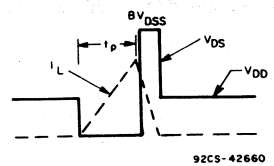


Fig. 16 — Unclamped Energy Waveforms

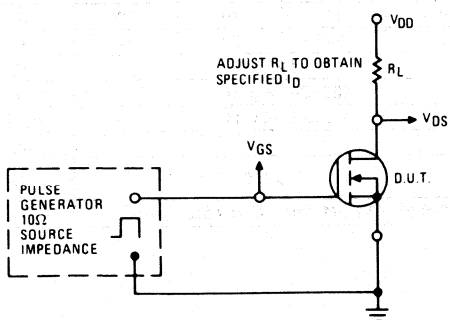


Fig. 17 – Switching Time Test Circuit

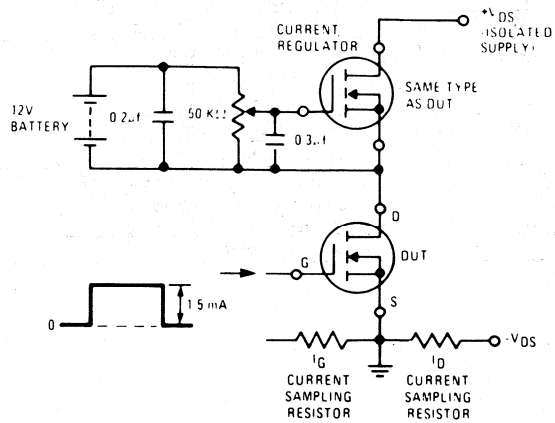


Fig. 18 – Gate Charge Test Circuit

IRFP240R, IRFP241R
IRFP242R, IRFP243R

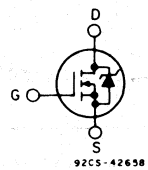
File Number **2087**

Avalanche Energy Rated N-Channel Power MOSFETs

16A and 18A, 200V, 150V
$r_{DS}(on) = 0.18\Omega$ and 0.22Ω

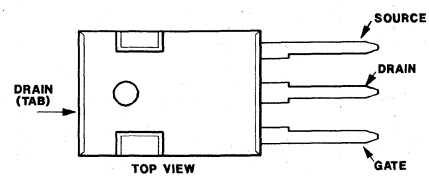
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-247

The IRFP240R, IRFP241R, IRFP242R and IRFP243R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

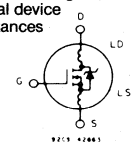
Absolute Maximum Ratings

Parameter		IRFP240R	IRFP241R	IRFP242R	IRFP243R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	510				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP240R IRFP242R	200	—	—	V	V_{GS} = 0V
		IRFP241R IRFP243R	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP240R IRFP241R	18	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFP242R IRFP243R	16	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP240R IRFP241R	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRFP242R IRFP243R	—	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	9.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 10A
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	—	500	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} \simeq$ 75V, I_D = 10A, Z_0 = 4.7Ω
t_r	Rise Time	ALL	—	27	60	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	40	80	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	—	31	60	ns	independent of operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	16	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	27	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

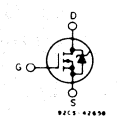


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP240R IRFP241R	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP242R IRFP243R	—	—	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP240R IRFP241R	—	—	72	A	
		IRFP242R IRFP243R	—	—	64	A	
V_{SD}	Diode Forward Voltage ②	IRFP240R IRFP241R	—	—	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRFP242R IRFP243R	—	—	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.1	—	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 1.9 mH, R_{gs} = 50Ω, I_{peak} = 20A. See figures 15, 16.

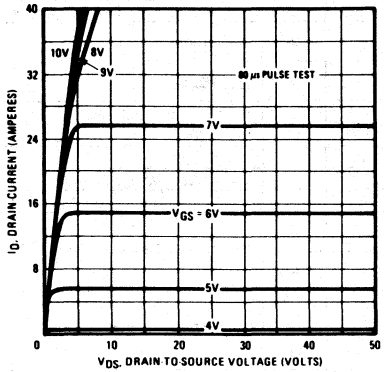


Fig. 1 - Typical output characteristics.

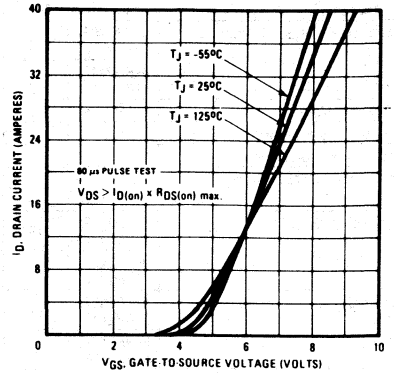


Fig. 2 - Typical transfer characteristics.

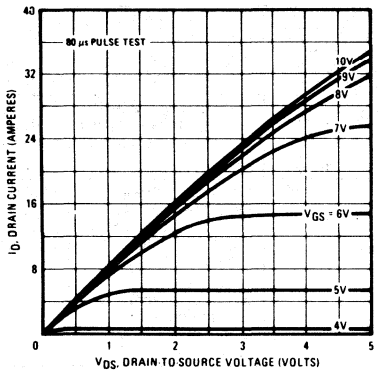


Fig. 3 - Typical saturation characteristics.

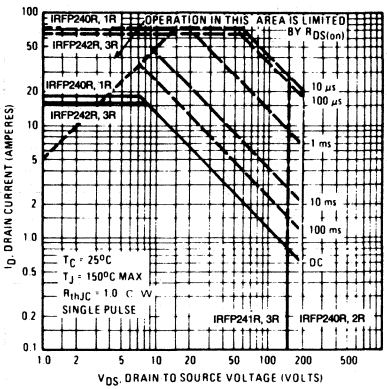


Fig. 4 - Maximum safe operating area.

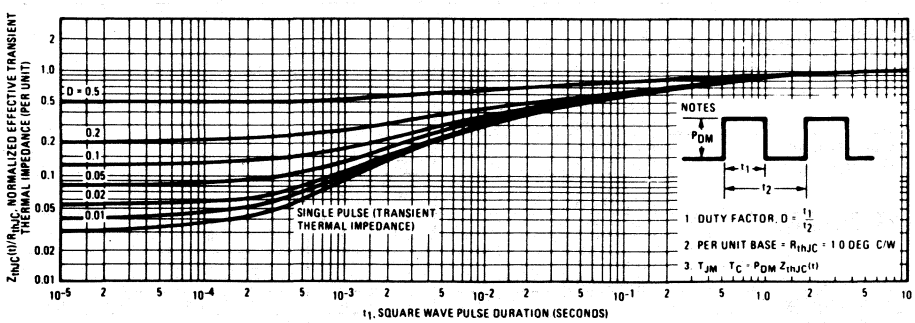


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

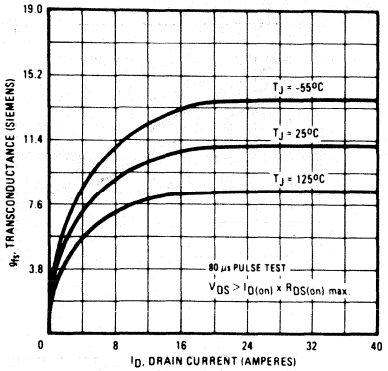


Fig. 6 - Typical transconductance vs. drain current.

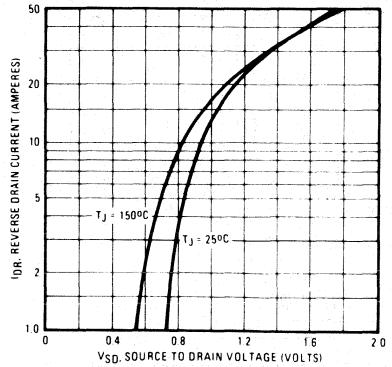


Fig. 7 - Typical source-drain diode forward voltage.

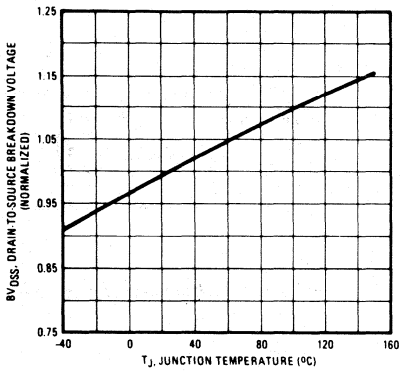


Fig. 8 - Breakdown voltage vs. temperature.

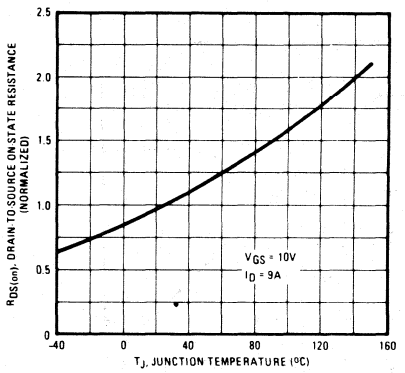


Fig. 9 - Normalized on-resistance vs. temperature.

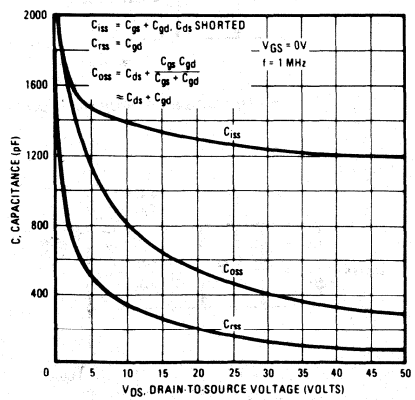


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

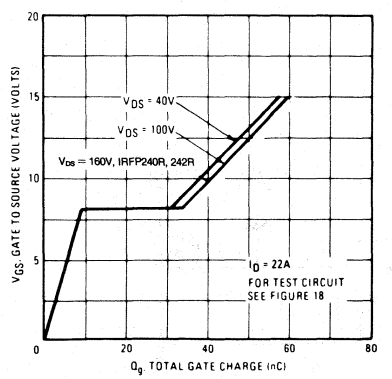


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

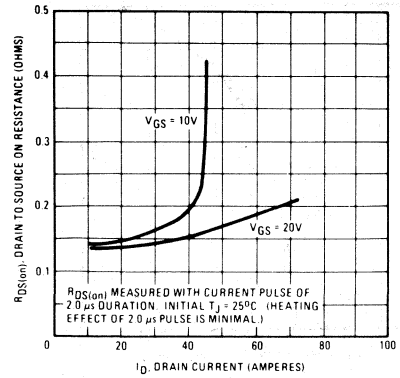


Fig. 12 - Typical on-resistance vs. drain current.

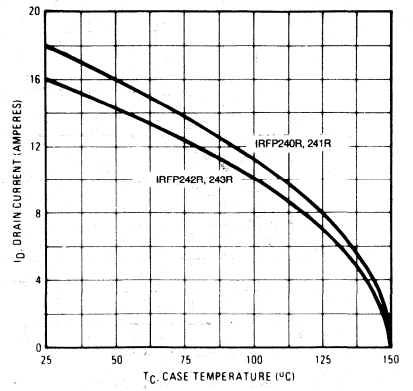


Fig. 13 - Maximum drain current vs. case temperature.

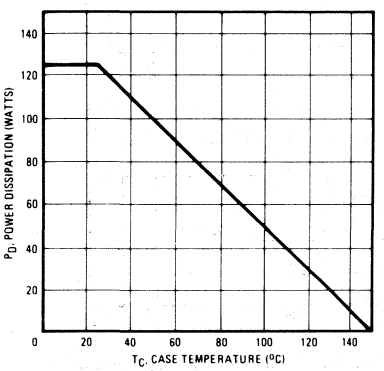


Fig. 14 - Power vs. temperature derating curve.

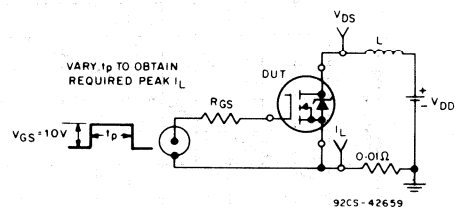


Fig. 15 - Unclamped energy test circuit.

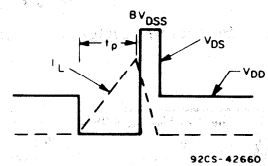


Fig. 16 - Unclamped energy waveforms.

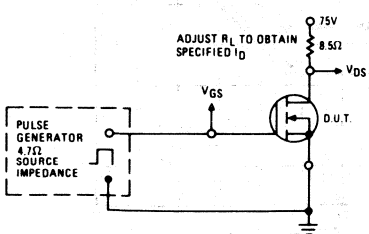


Fig. 17 - Switching time test circuit.

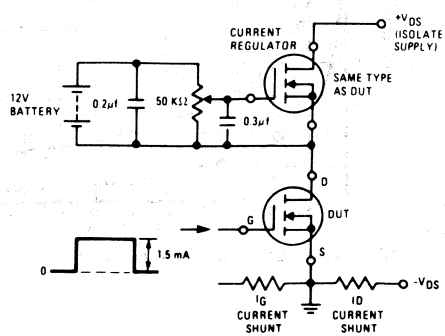


Fig. 18 - Gate charge test circuit.

File Number **2211**

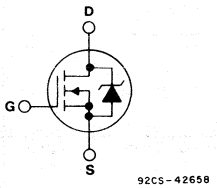
IRFP244, IRFP245, IRFP246, IRFP247

Avalanche-Energy-Rated N-Channel Power MOSFETs

14 A and 13 A, 275 V and 250 V
$r_{DS}(on)$ = 0.28 Ω and 0.34 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250V dc rated - 120V ac line system operation*

N-CHANNEL ENHANCEMENT MODE

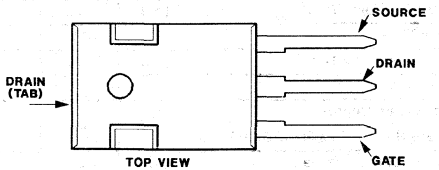


TERMINAL DIAGRAM

The IRFP244, IRFP245, IRFP246 and IRFP247 are advanced power MOSFETS designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

ABSOLUTE-MAXIMUM RATINGS

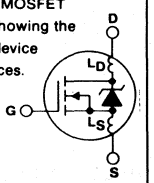
CHARACTERISTIC		IRFP244	IRFP245	IRFP246	IRFP247	UNITS
Drain-Source Voltage ①	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	250	250	275	275	V
Continuous Drain Current	I_D @ T_C = 25°C	14	13	14	13	A
Continuous Drain Current	I_D @ T_C = 100°C	8.8	8.0	8.8	8.0	A
Pulsed Drain Current ③	I_{DM}	56	52	56	52	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	125				W
Linear Derating Factor		1.0				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	550				mj
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. (1.6 mm) from case for 10s)				°C

IRFP244, IRFP245, IRFP246, IRFP247

ELECTRICAL CHARACTERISTICS, At T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFP246 IRFP247	275	—	—	V	V_{GS} = 0 V
		IRFP244 IRFP245	250	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS}(th)$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_D(on)$	IRFP244 IRFP246	14	—	—	A	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., V_{GS} = 10 V
		IRFP245 IRFP247	13	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS}(on)$	IRFP244 IRFP246	—	0.20	0.28	Ω	V_{GS} = 10 V, I_D = 10 A
		IRFP245 IRFP247	—	0.24	0.34	Ω	
Forward Transconductance ②	g_{fs}	ALL	6.7	10	—	S (℧)	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., I_D = 10 A
Input Capacitance	C_{iss}	ALL	—	1300	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	320	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	69	—	pF	
Turn-On Delay Time	$t_d(on)$	ALL	—	16	24	ns	V_{DD} = 90 V, I_D = 10 A, Z_O = 4.7 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	67	100	ns	
Turn-Off Delay Time	$t_d(off)$	ALL	—	53	80	ns	
Fall Time	t_f	ALL	—	49	74	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	39	59	nC	V_{GS} = 10 V, I_D = 22 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	6.6	9.9	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	20	30	nC	
Internal Drain Inductance	L_D	ALL	—	4.5	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

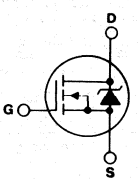


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1.0	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Free air operation.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFP244 IRFP246	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP245 IRFP247	—	—	13	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFP244 IRFP246	—	—	56	A	
		IRFP245 IRFP247	—	—	52	A	
Diode Forward Voltage ②	V_{SD}	ALL	—	—	1.8	V	T_C = 25°C, I_S = 14 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	150	300	640	ns	T_J = 150°C, I_F = 14 A, di_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	1.6	3.4	7.2	μC	T_J = 150°C, I_F = 14 A, di_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs. Duty Cycle ≤ 2%

③ Repetitive Rating: Pulse width limited by max. junction temperature See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50 V, Starting T_J = 25°C, L = 4.5 mH, R_G = 25 Ω, Peak I_L = 14 A (See Figs. 14 & 15).

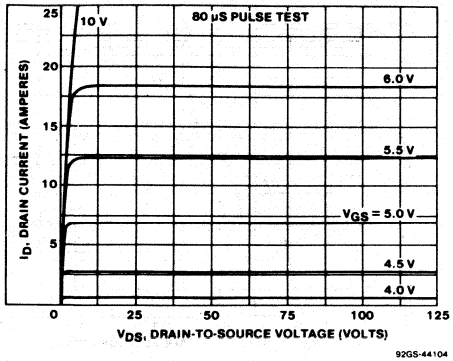


Fig. 1 - Typical output characteristics.

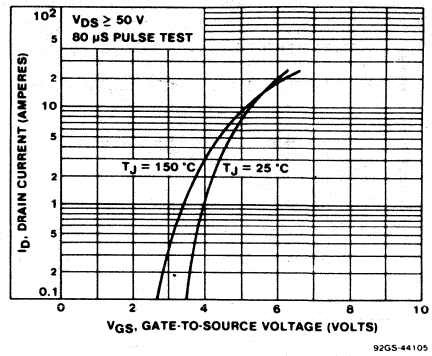


Fig. 2 - Typical transfer characteristics.

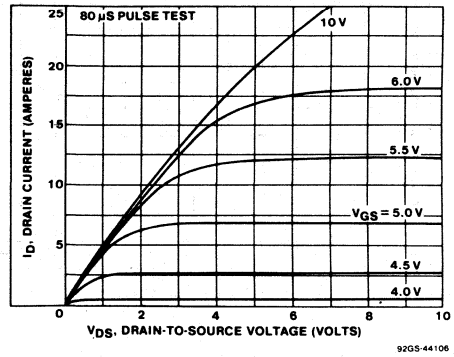


Fig. 3 - Typical saturation characteristics.

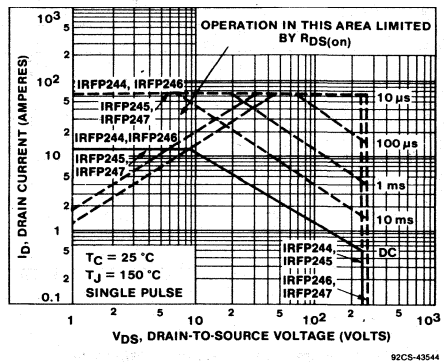


Fig. 4 - Maximum safe operating area.

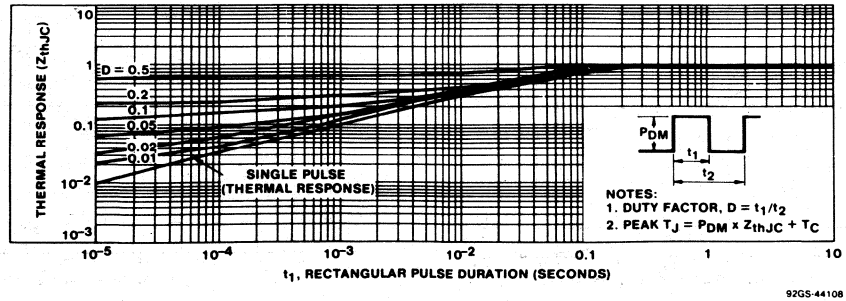


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFP244, IRFP245, IRFP246, IRFP247

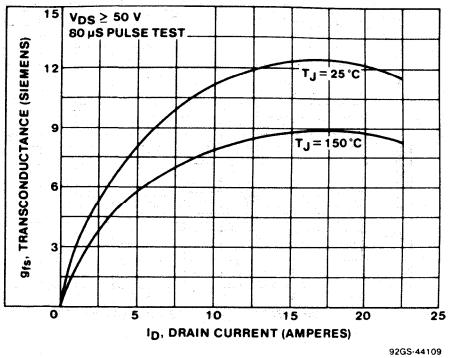


Fig. 6 - Typical transconductance vs. drain current.

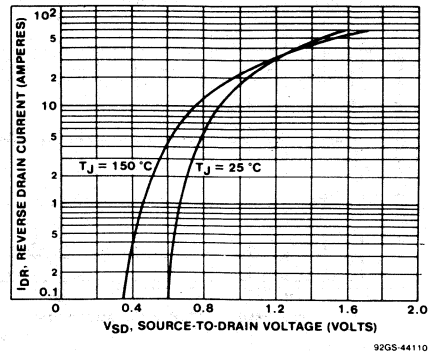


Fig. 7 - Typical source-drain diode forward voltage.

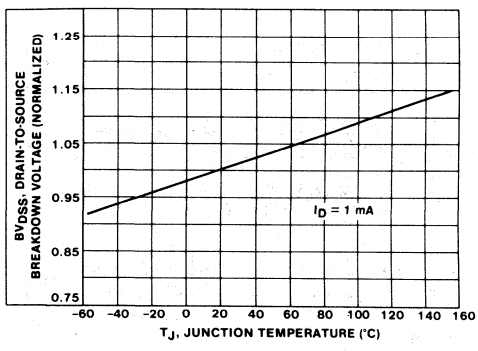


Fig. 8 - Breakdown voltage vs. temperature.

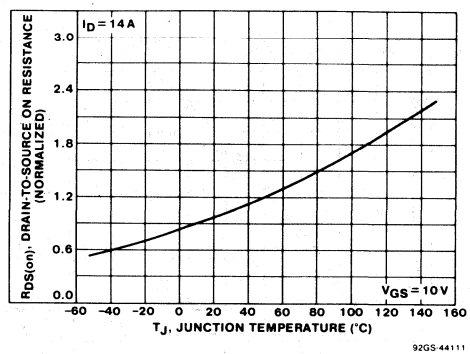


Fig. 9 - Normalized on-resistance vs. temperature.

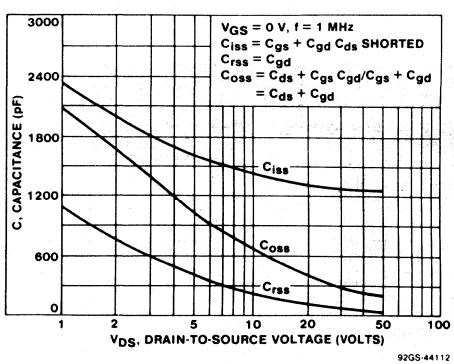


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

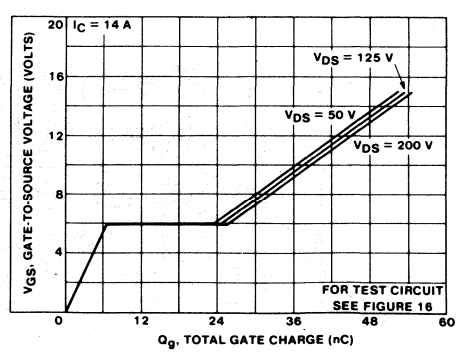


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

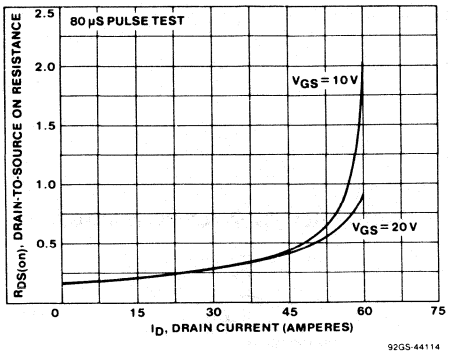


Fig. 12 - Typical on-resistance vs. drain current.

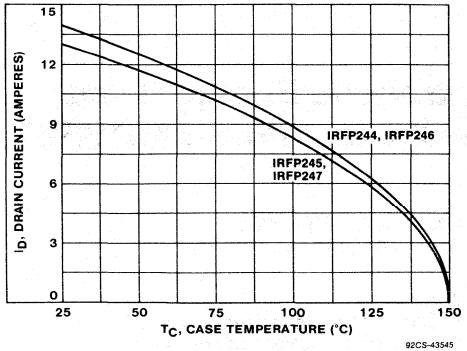


Fig. 13 - Maximum drain current vs. case temperature.

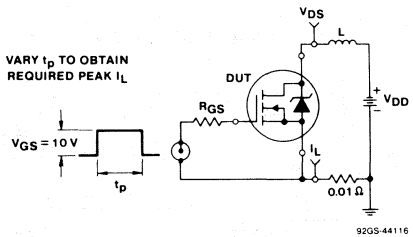


Fig. 14 - Unclamped energy test circuit.

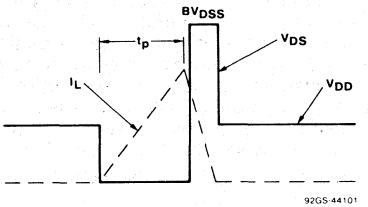


Fig. 15 - Unclamped energy waveforms.

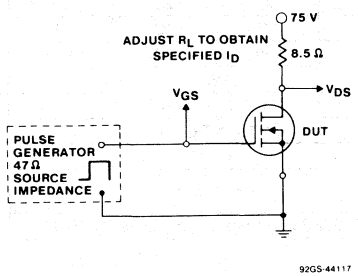


Fig. 16 - Switching time test circuit.

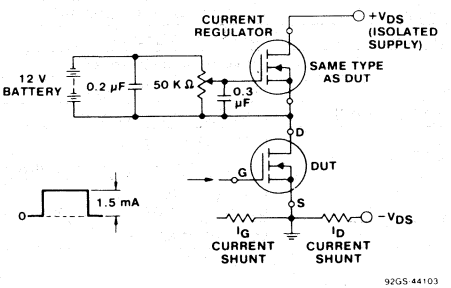


Fig. 17 - Gate charge test circuit.

IRFP250R, IRFP251R, IRFP252R, IRFP253R

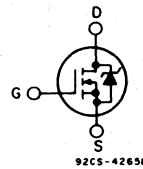
File Number **2016**

Avalanche Energy Rated N-Channel Power MOSFETs

25A and 30A, 150V-200V
$r_{DS}(on) = 0.085\Omega$ and 0.120Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

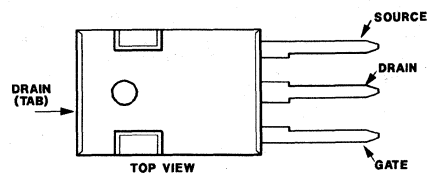


TERMINAL DIAGRAM

The IRFP250R, IRFP251R, IRFP252R and IRFP253R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

Absolute Maximum Ratings

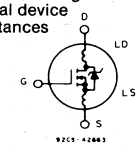
Parameter		IRFP250R	IRFP251R	IRFP252R	IRFP253R	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	200	150	200	150	V
I_D @ $T_C = 25°C$	Continuous Drain Current	30	30	25	25	A
I_D @ $T_C = 100°C$	Continuous Drain Current	19	19	16	16	A
I_{DM}	Pulsed Drain Current ③	120	120	100	100	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	810				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP250R, IRFP251R, IRFP252R, IRFP253R

Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP250R IRFP252R	200	—	—	V	$V_{GS} = 0V$
		IRFP251R IRFP253R	150	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu$ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current ②	IRFP250R IRFP251R	30	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, $V_{GS} = 10V$
		IRFP252R IRFP253R	25	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP250R IRFP251R	—	0.07	0.085	Ω	$V_{GS} = 10V$, $I_D = 16A$
		IRFP252R IRFP253R	—	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, $I_D = 16A$
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	800	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	300	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq 95V$, $I_D = 16A$, $Z_o = 4.7\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	125	ns	
t_f	Fall Time	ALL	—	—	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	$V_{GS} = 10V$, $I_D = 38A$, $V_{DS} = 0.8V$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	37	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	42	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP250R IRFP251R	—	—	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP252R IRFP253R	—	—	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP250R IRFP251R	—	—	120	A	
		IRFP252R IRFP253R	—	—	100	A	
V_{SD}	Diode Forward Voltage ②	IRFP250R IRFP251R	—	—	2.0	V	$T_C = 25°C$, $I_S = 30A$, $V_{GS} = 0V$
		IRFP252R IRFP253R	—	—	1.8	V	$T_C = 25°C$, $I_S = 25A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	750	—	ns	$T_J = 150°C$, $I_F = 30A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	4.7	—	μC	$T_J = 150°C$, $I_F = 30A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ $V_{DD} = 50V$, starting $T_J = 25°C$, L = 1.1 mH, $R_{gs} = 50\Omega$, $I_{peak} = 33A$. See figures 15, 16.

IRFP250R, IRFP251R, IRFP252R, IRFP253R

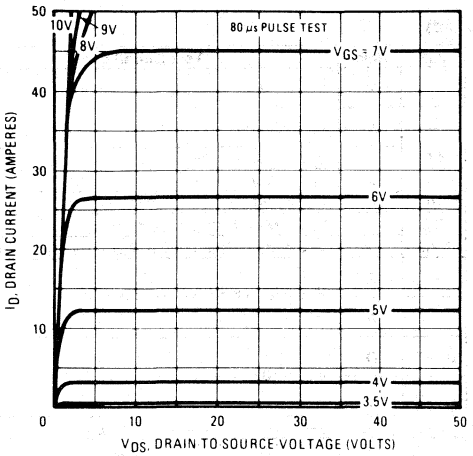


Fig. 1 — Typical Output Characteristics

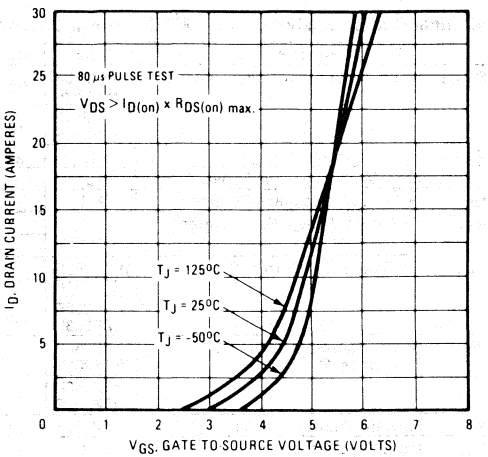


Fig. 2 — Typical Transfer Characteristics

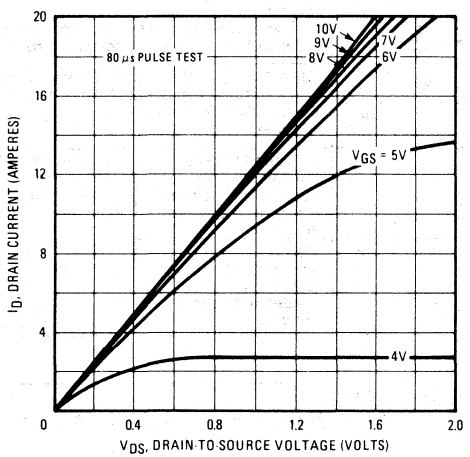


Fig. 3 — Typical Saturation Characteristics

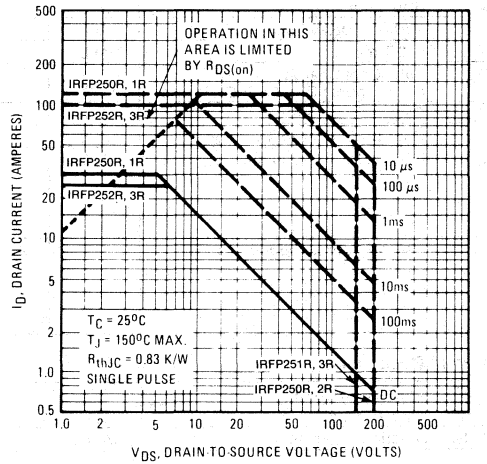


Fig. 4 — Maximum Safe Operating Area

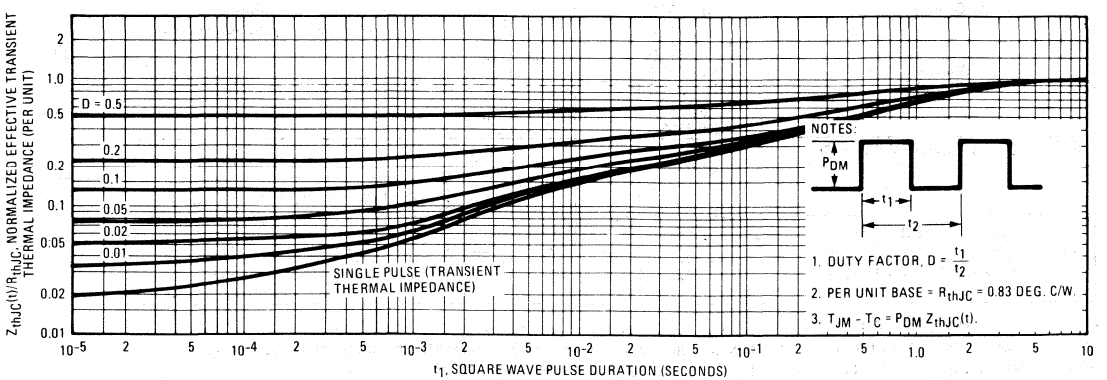


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

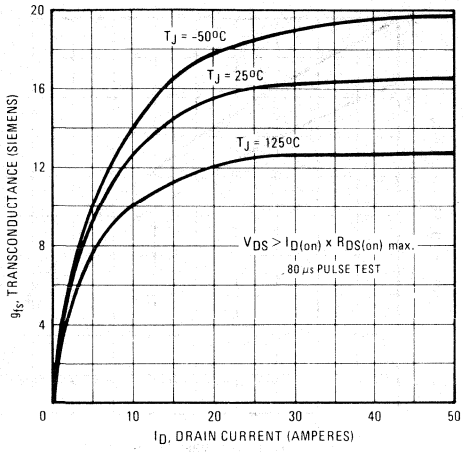


Fig. 6 — Typical Transconductance Vs. Drain Current

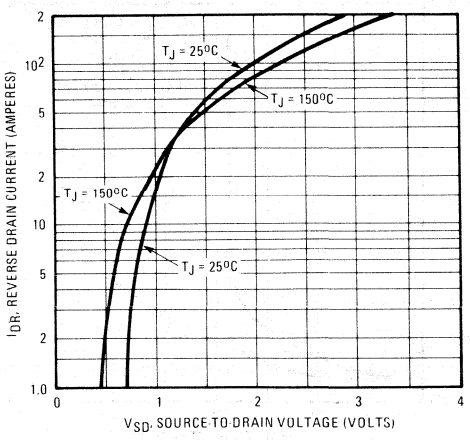


Fig. 7 — Typical Source-Drain Diode Forward Voltage

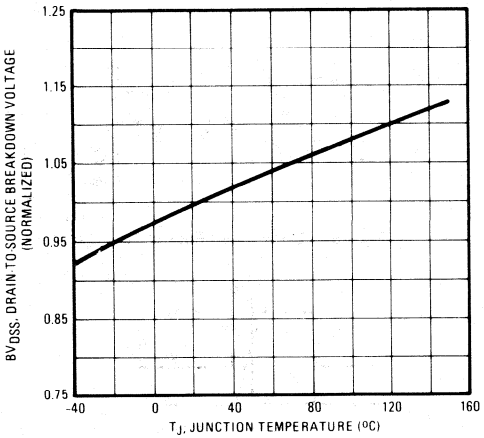


Fig. 8 — Breakdown Voltage Vs. Temperature

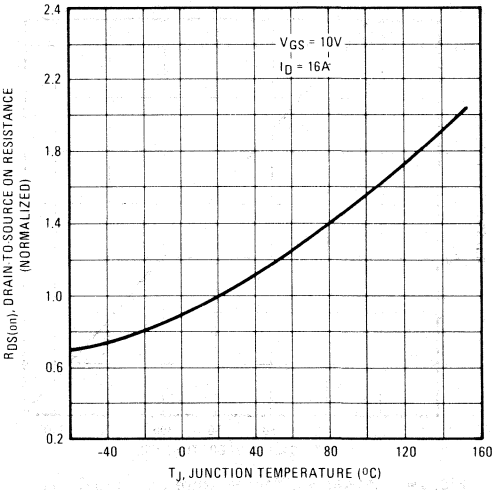


Fig. 9 — Normalized On-Resistance Vs. Temperature

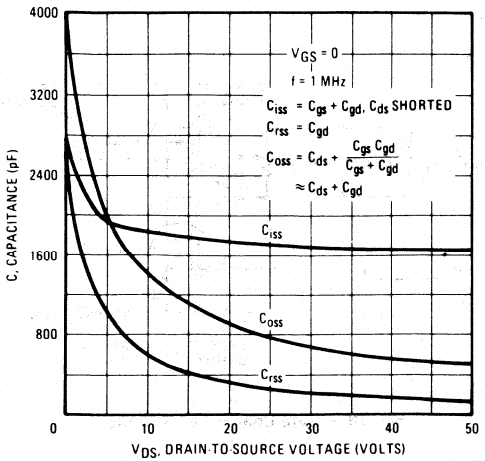


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

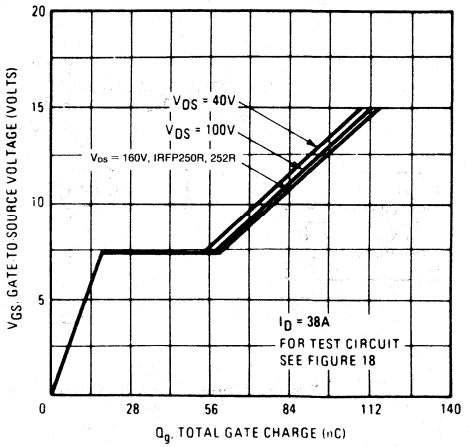


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRFP250R, IRFP251R, IRFP252R, IRFP253R

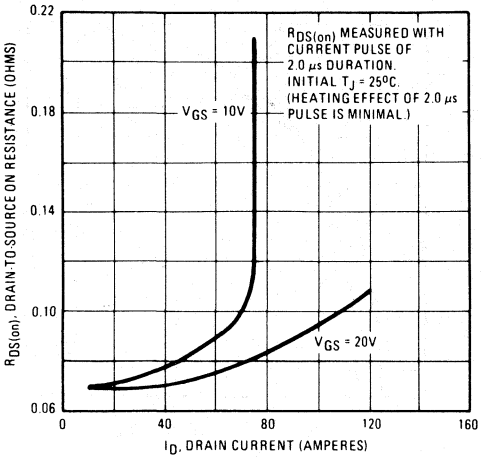


Fig. 12 — Typical On-Resistance Vs. Drain Current

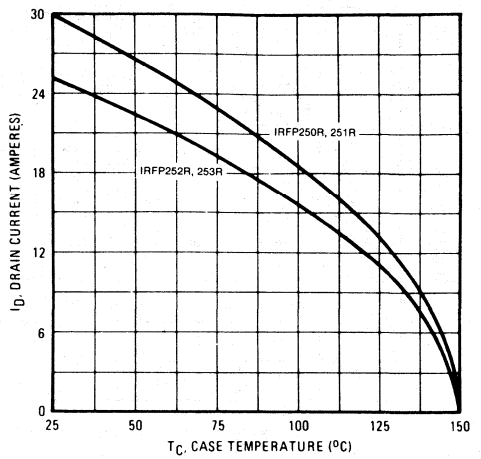


Fig. 13 — Maximum Drain Current Vs. Case Temperature

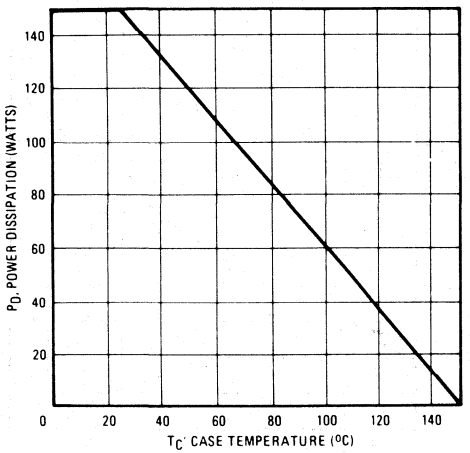


Fig. 14 — Power Vs. Temperature Derating Curve

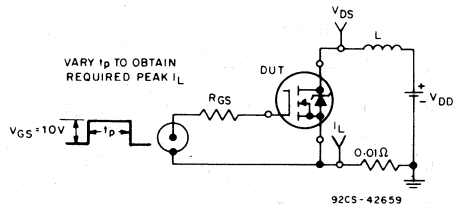


Fig. 15 — Unclamped Energy Test Circuit

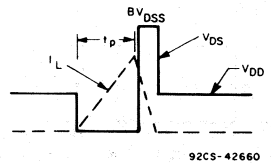


Fig. 16 — Unclamped Energy Waveforms

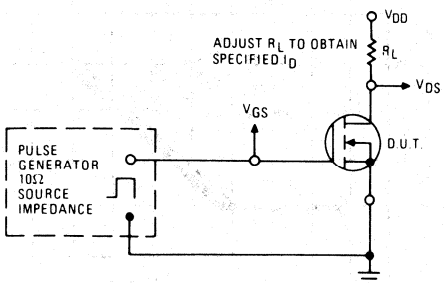


Fig. 17 — Switching Time Test Circuit

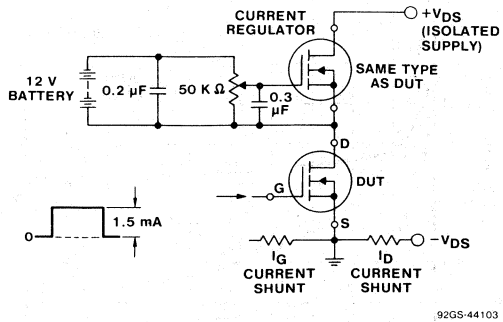


Fig. 18 — Gate Charge Test Circuit

File Number **2289**

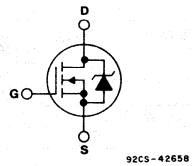
IRFP254, IRFP255
IRFP256, IRFP257

Avalanche-Energy-Rated N-Channel Power MOSFETs

22 A and 20 A, 275 V and 250 V
$r_{DS(on)}$ = 0.14 Ω and 0.17 Ω

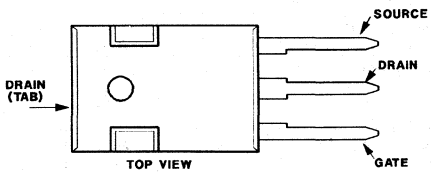
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250 V dc rated - 120 V ac line system operation*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-247

The IRFP254, IRFP255, IRFP256 and IRFP257 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

ABSOLUTE-MAXIMUM RATINGS

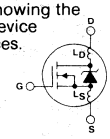
CHARACTERISTIC		IRFP254	IRFP255	IRFP256	IRFP257	UNITS
Drain-Source Voltage ①	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	250	250	275	275	V
Continuous Drain Current	I_D @ T_C = 25°C	22	20	22	20	A
Continuous Drain Current	I_D @ T_C = 100°C	14	12	14	12	A
Pulsed Drain Current ③	I_{DM}	88	80	88	80	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	150				W
Linear Derating Factor		1.2				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	1000				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

IRFP254, IRFP255, IRFP256, IRFP257

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFP256 IRFP257	275	—	—	V	V_{GS} = 0 V
		IRFP254 IRFP255	250	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFP254 IRFP256	22	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = 10 V
		IRFP255 IRFP257	20	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFP254 IRFP256	—	0.11	0.14	Ω	V_{GS} = 10 V, I_D = 12 A
		IRFP255 IRFP257	—	0.14	0.17	Ω	
Forward Transconductance ②	g_{fs}	ALL	11	17	—	S(Ω)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = 12 A
Input Capacitance	C_{iss}	ALL	—	2700	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	580	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	130	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	19	29	ns	V_{DD} = 125 V, I_D = 22 A, Z_o = 6.2 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	84	130	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	75	110	ns	
Fall Time	t_f	ALL	—	65	98	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	87	130	nC	V_{GS} = 10 V, I_D = 22 A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	14	20	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	73	110	nC	
Internal Drain Inductance	L_D	ALL	—	5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

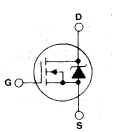


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	0.83	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.12	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	30	°C/W	Free air operation.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFP254 IRFP256	—	—	22	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP255 IRFP257	—	—	22	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFP254 IRFP256	—	—	88	A	
		IRFP255 IRFP257	—	—	88	A	
Diode Forward Voltage ②	V_{SD}	ALL	—	—	1.8	V	T_C = 25°C, I_S = 22 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	150	310	650	ns	T_J = 150°C, I_F = 22 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	1.9	4	8.4	μC	T_J = 150°C, I_F = 22 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_J = 25°C, L = 3.3 mH, R_G = 25 Ω, Peak I_L = 22 A (See Figs. 14 & 15).

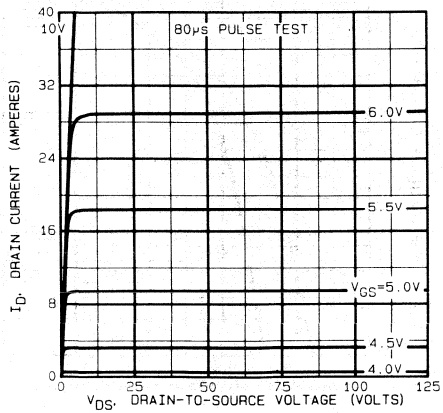


Fig. 1 - Typical output characteristics.

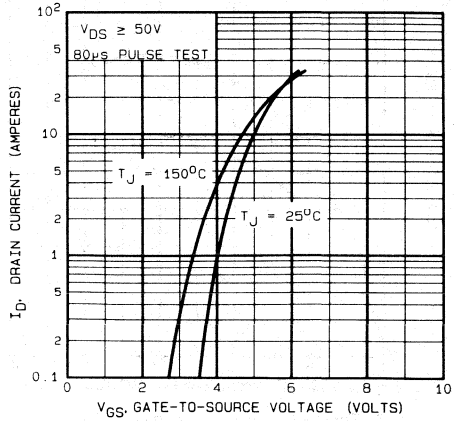


Fig. 2 - Typical transfer characteristics.

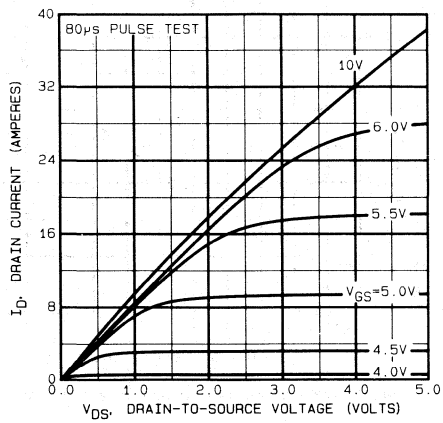


Fig. 3 - Typical saturation characteristics.

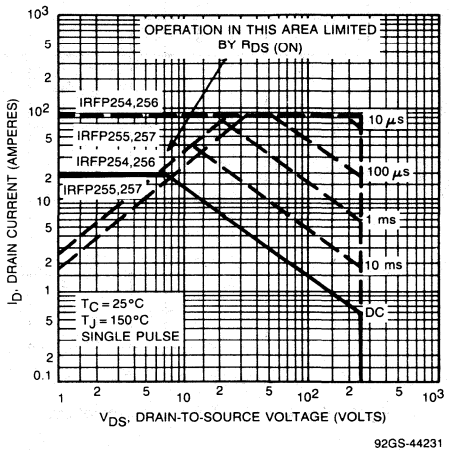


Fig. 4 - Maximum safe operating area.

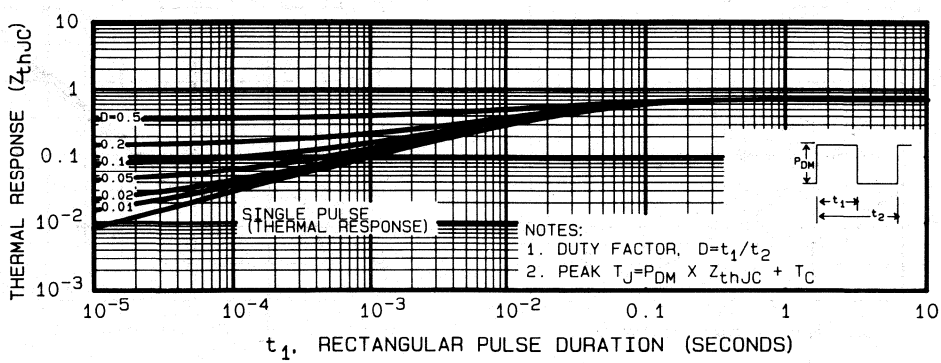


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFP254, IRFP255, IRFP256, IRFP257

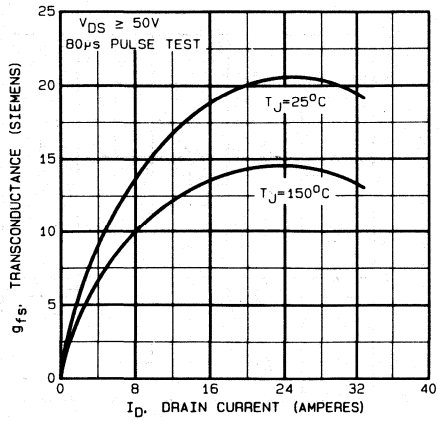


Fig. 6 - Typical transconductance vs. drain current.

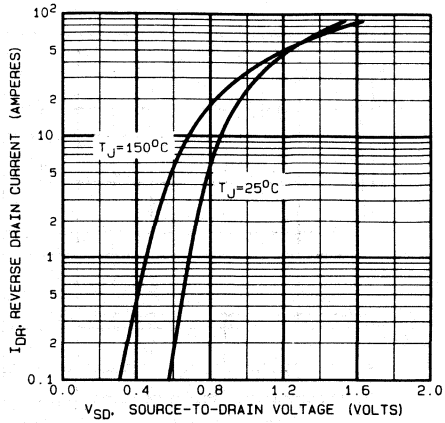


Fig. 7 - Typical source-drain diode forward voltage.

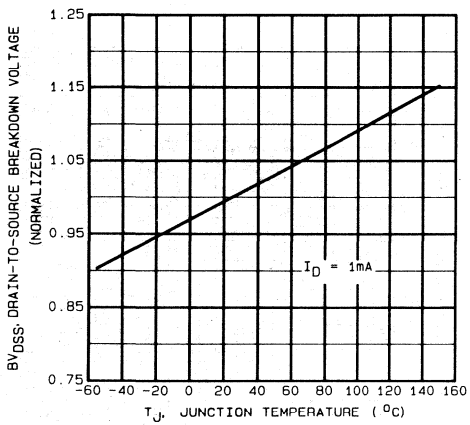


Fig. 8 - Breakdown voltage vs. temperature.

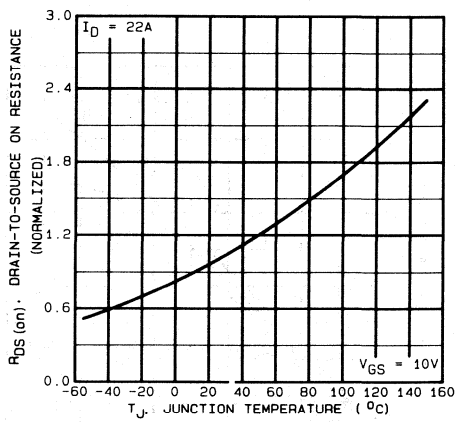


Fig. 9 - Normalized on-resistance vs. temperature.

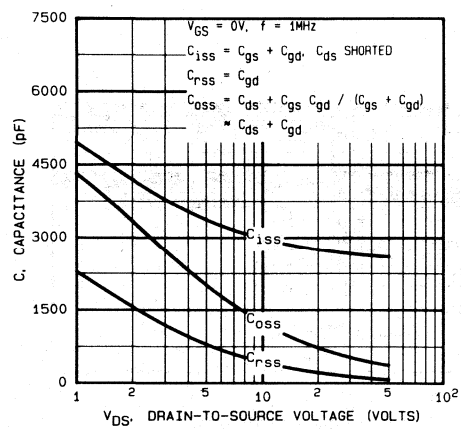


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

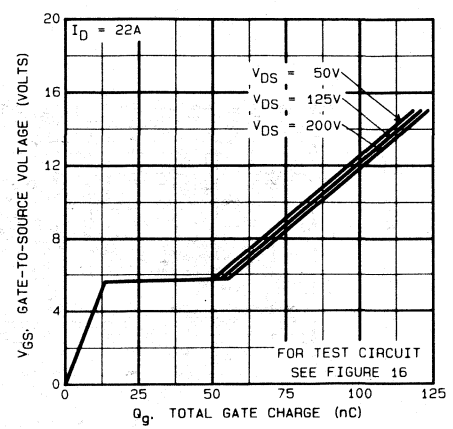


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

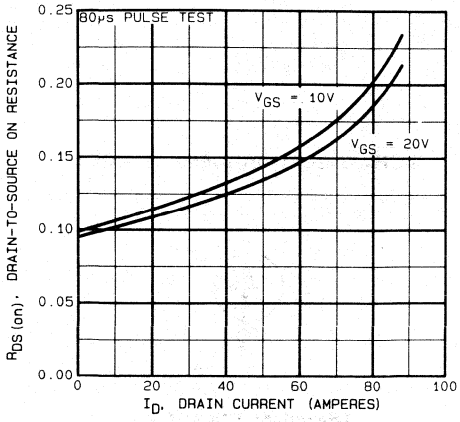


Fig. 12 - Typical on-resistance vs. drain current.

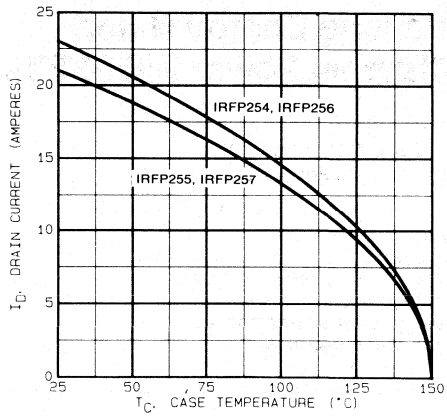


Fig. 13 - Maximum drain current vs. case temperature.

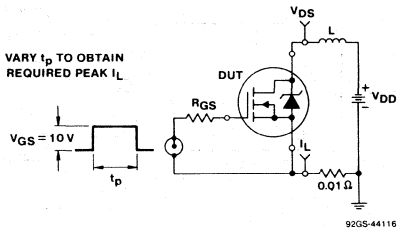


Fig. 14 - Unclamped energy test circuit.

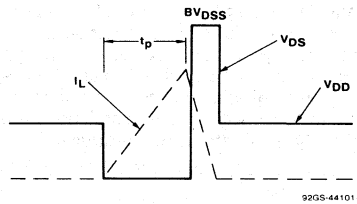


Fig. 15 - Unclamped energy waveforms.

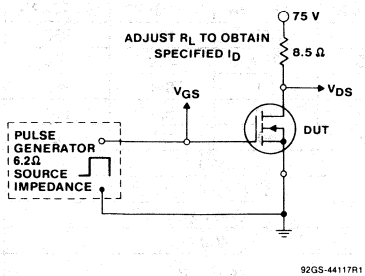


Fig. 16 - Switching time test circuit.

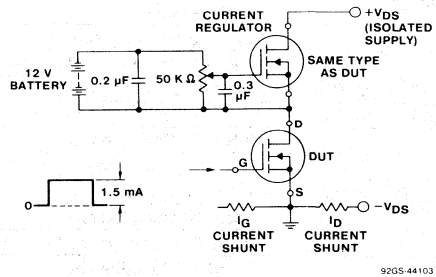


Fig. 17 - Gate charge test circuit.

IRFP340R, IRFP341R, IRFP342R, IRFP343R

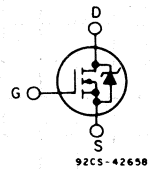
File Number **2088**

Avalanche Energy Rated N-Channel Power MOSFETs

10A and 8A, 400V and 350V
$r_{DS}(on)$ = 0.55Ω and 0.80Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

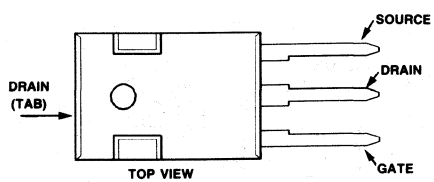


TERMINAL DIAGRAM

The IRFP340R, IRFP341R, IRFP342R and IRFP343R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

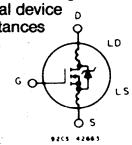
Absolute Maximum Ratings

Parameter		IRFP340R	IRFP341R	IRFP342R	IRFP343R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	400				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP340R IRFP342R	400	—	—	V	V_{GS} = 0V
		IRFP341R IRFP343R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP340R IRFP341R	10	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFP342R IRFP343R	8.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP340R IRFP341R	—	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A
		IRFP342R IRFP343R	—	0.68	0.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 5.0A
C_{iss}	Input Capacitance	ALL	—	1250	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	17	35	ns	$V_{DD} \simeq$ 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5.0	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	45	90	ns	
t_f	Fall Time	ALL	—	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	18	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	23	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



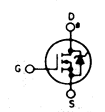
92CS-42663

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP340R IRFP341R	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP342R IRFP343R	—	—	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP340R IRFP341R	—	—	40	A	
		IRFP342R IRFP343R	—	—	32	A	
V_{SD}	Diode Forward Voltage ②	IRFP340R IRFP341R	—	—	2.0	V	T_C = 25°C, I_S = 10A, V_{GS} = 0V
		IRFP342R IRFP343R	—	—	1.9	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	5.7	—	μC	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



92CS-42650

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 40V, starting T_J = 25°C, L = 7.27mH, R_{gs} = 50Ω, I_{peak} = 10A. See figures 15, 16.

IRFP340R, IRFP341R, IRFP342R, IRFP343R

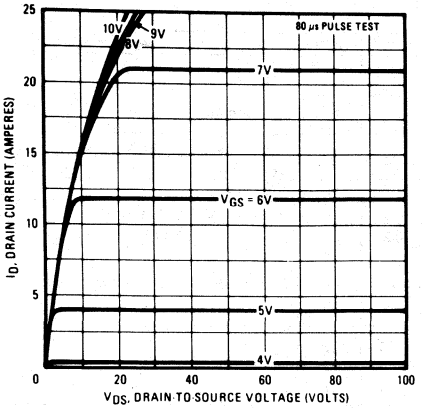


Fig. 1 - Typical output characteristics.

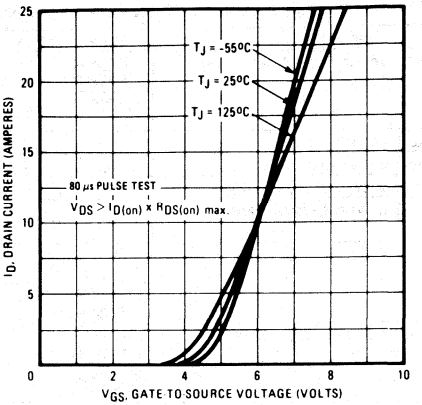


Fig. 2 - Typical transfer characteristics.

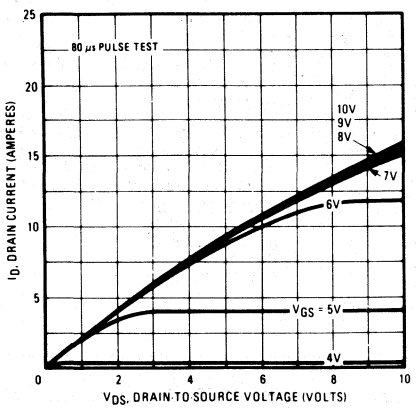


Fig. 3 - Typical saturation characteristics.

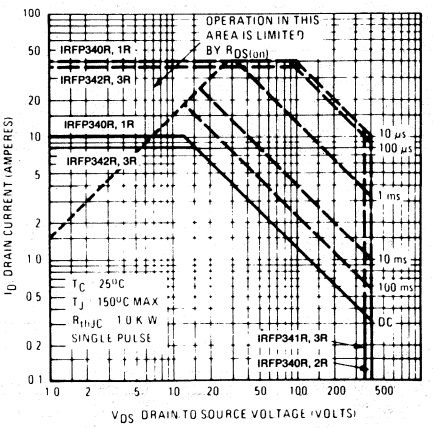


Fig. 4 - Maximum safe operating area.

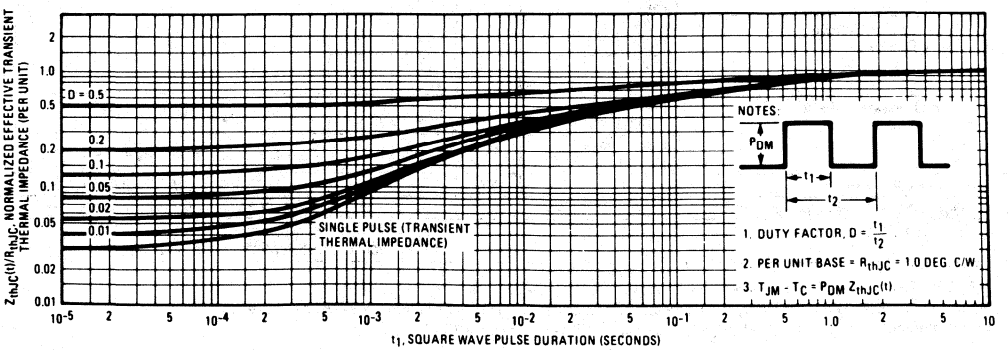


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

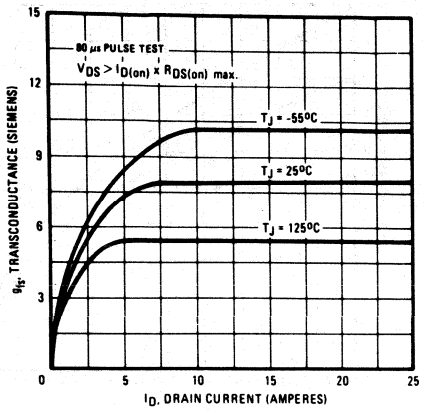


Fig. 6 - Typical transconductance vs. drain current.

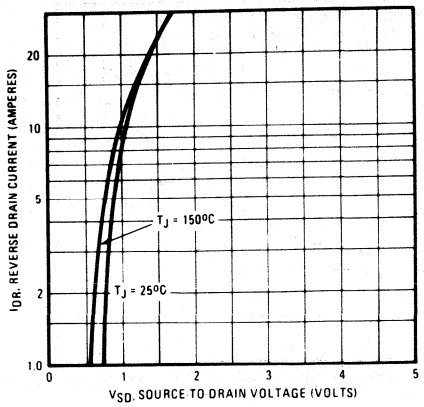


Fig. 7 - Typical source-drain diode forward voltage.

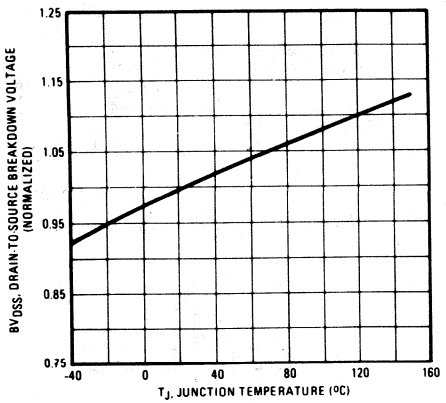


Fig. 8 - Breakdown voltage vs. temperature.

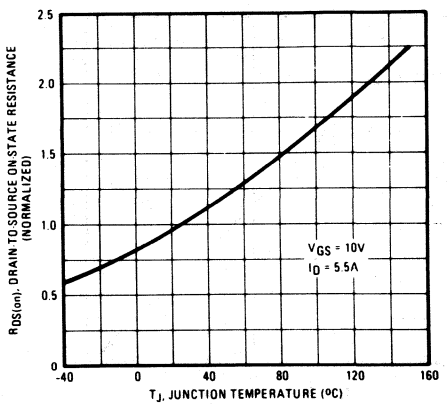


Fig. 9 - Normalized on-resistance vs. temperature.

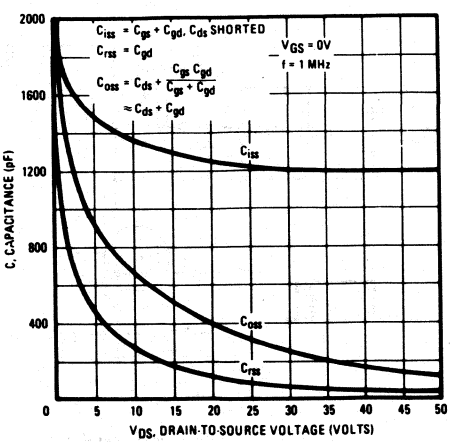


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

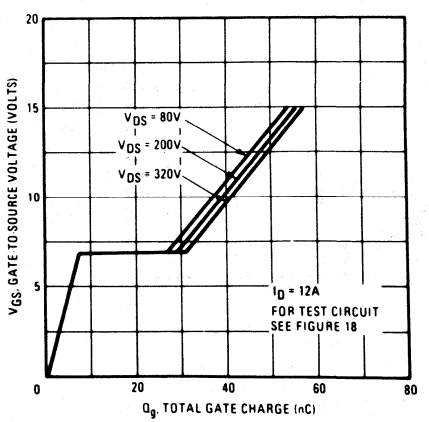


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFP340R, IRFP341R, IRFP342R, IRFP343R

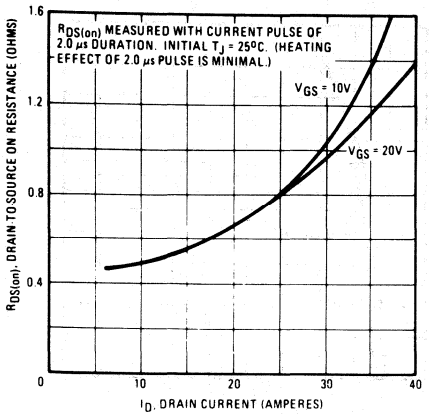


Fig. 12 - Typical on-resistance vs. drain current.

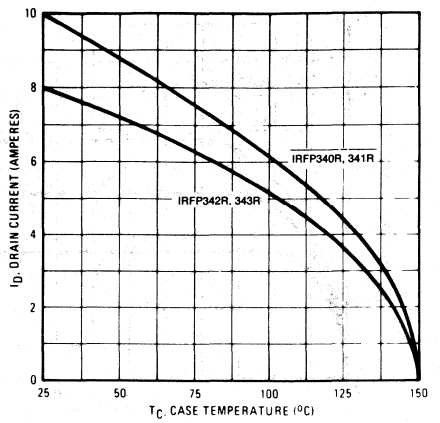


Fig. 13 - Maximum drain current vs. case temperature.

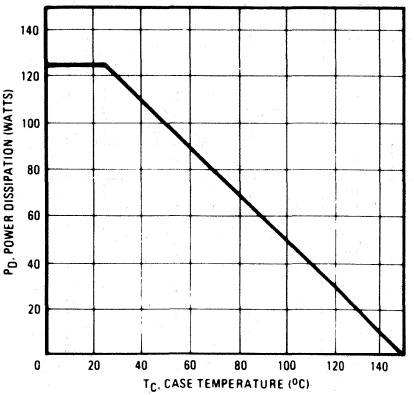


Fig. 14 - Power vs. temperature derating curve.

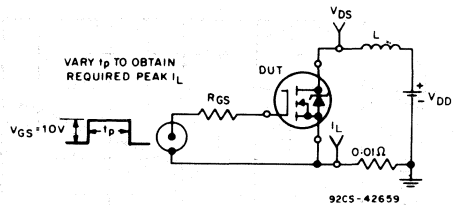


Fig. 15 - Unclamped energy test circuit.

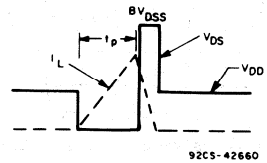


Fig. 16 - Unclamped energy waveforms.

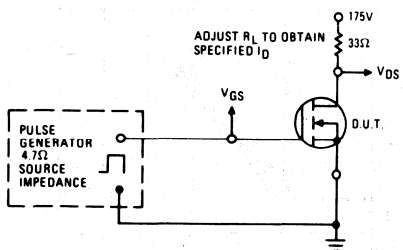


Fig. 17 - Switching time test circuit.

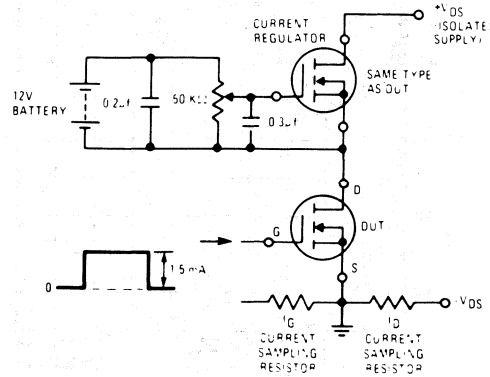


Fig. 18 - Gate charge test circuit.

File Number **2017**

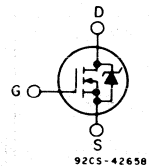
IRFP350R, IRFP351R, IRFP352R, IRFP353R

Avalanche Energy Rated N-Channel Power MOSFETs

13A and 15A, 350V-400V
$r_{DS}(on) = 0.3\Omega$ and 0.4Ω

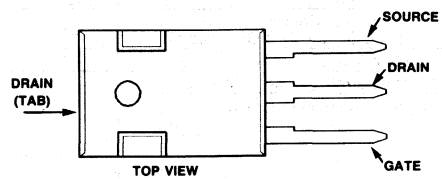
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-247

The IRFP350R, IRFP351R, IRFP352R and IRFP353R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

Absolute Maximum Ratings

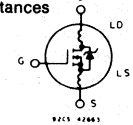
Parameter		IRFP350R	IRFP351R	IRFP352R	IRFP353R	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	15	15	13	13	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	60	60	52	52	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	700				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP350R, IRFP351R, IRFP352R, IRFP353R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP350R IRFP352R	400	—	—	V	V_{GS} = 0V
		IRFP351R IRFP353R	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP350R IRFP351R	15	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRFP352R IRFP353R	13	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP350R IRFP351R	—	0.25	0.3	Ω	V_{GS} = 10V, I_D = 8.0A
		IRFP352R IRFP353R	—	0.3	0.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	10	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 8.0A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 180V, I_D = 8.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	65	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	150	ns	
t_f	Fall Time	ALL	—	—	75	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	38	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	41	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

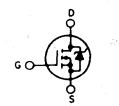


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP350R IRFP351R	—	—	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP352R IRFP353R	—	—	13	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP350R IRFP351R	—	—	60	A	
		IRFP352R IRFP353R	—	—	52	A	
V_{SD}	Diode Forward Voltage ②	IRFP350R IRFP351R	—	—	1.6	V	T_C = 25°C, I_S = 15A, V_{GS} = 0V
		IRFP352R IRFP353R	—	—	1.5	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1000	—	ns	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.6	—	μC	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 40V, starting T_J = 25°C, L = 5.66mH, R_{gs} = 50Ω, I_{peak} = 15A. See figures 15, 16.

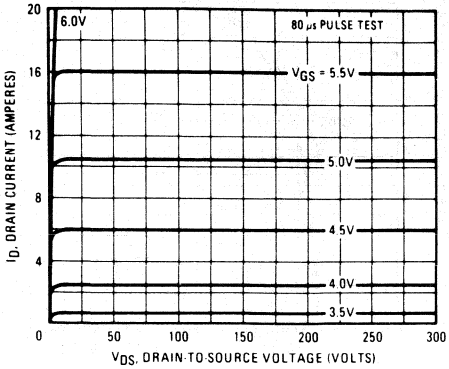


Fig. 1 – Typical Output Characteristics

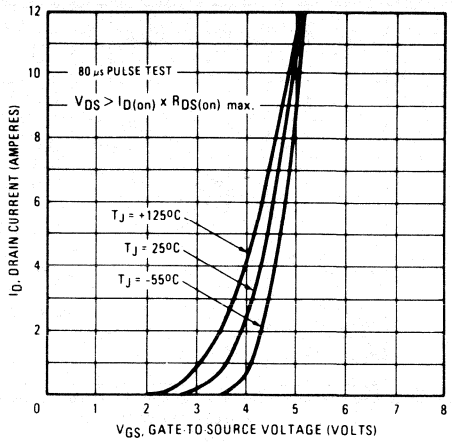


Fig. 2 – Typical Transfer Characteristics

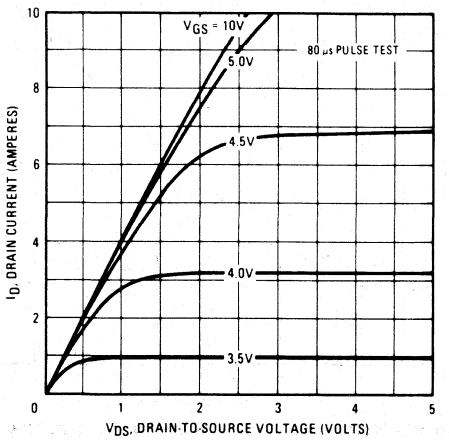


Fig. 3 – Typical Saturation Characteristics

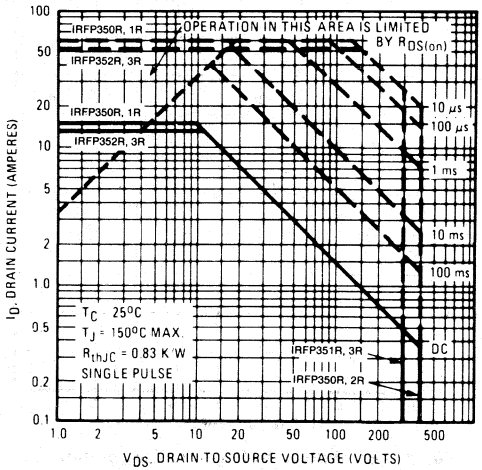


Fig. 4 – Maximum Safe Operating Area

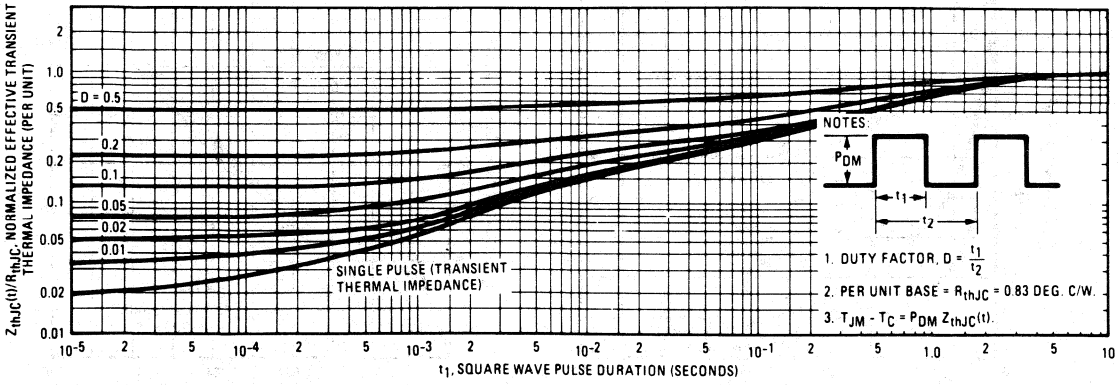


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

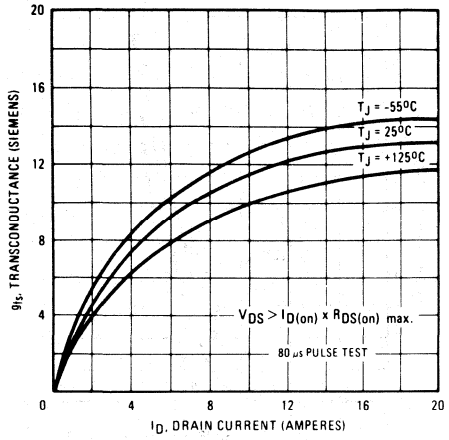


Fig. 6 — Typical Transconductance Vs. Drain Current

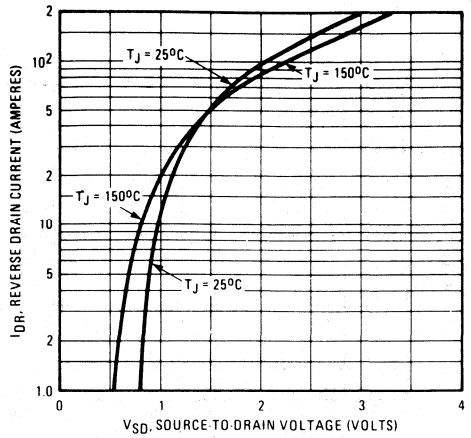


Fig. 7 — Typical Source-Drain Diode Forward Voltage

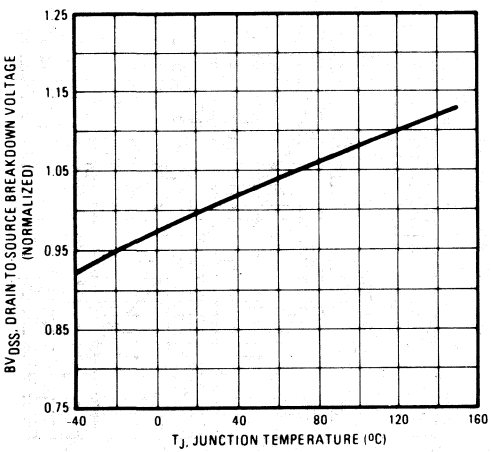


Fig. 8 — Breakdown Voltage Vs. Temperature

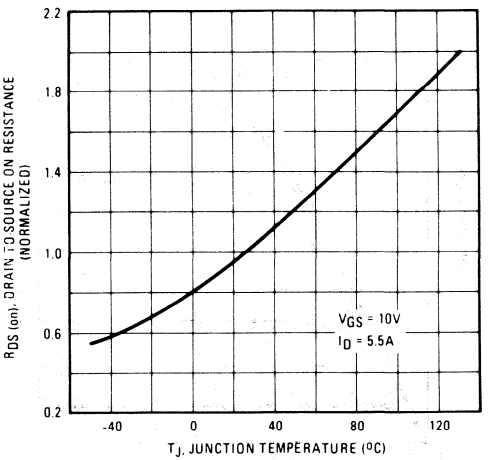


Fig. 9 — Normalized On-Resistance Vs. Temperature

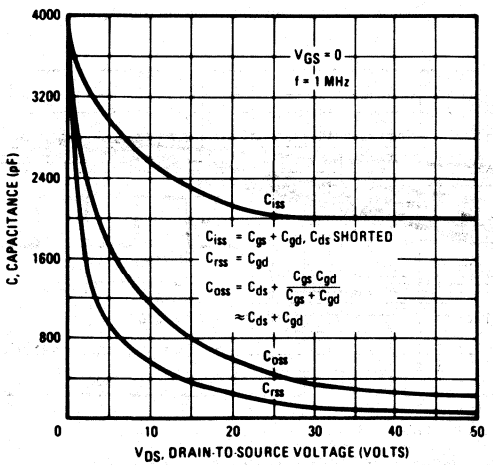


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

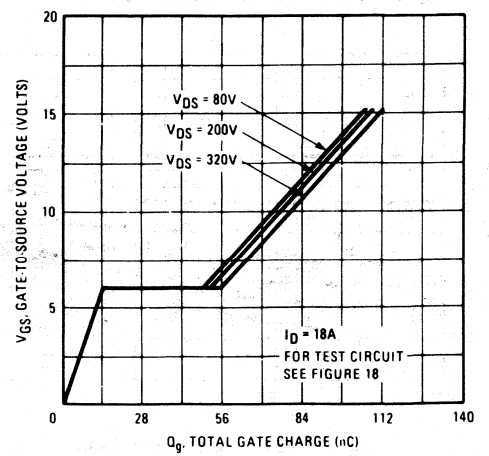


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

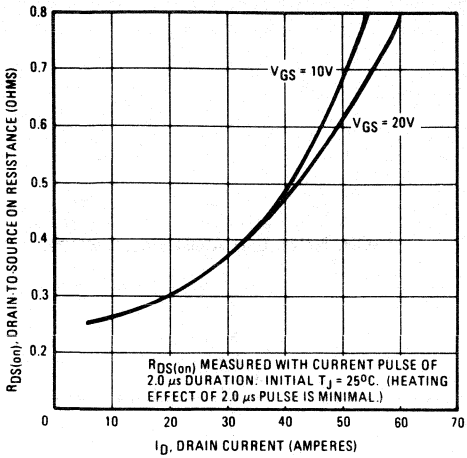


Fig. 12 – Typical On-Resistance Vs. Drain Current

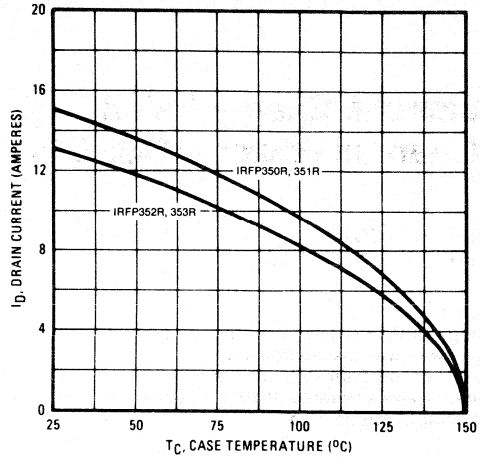


Fig. 13 – Maximum Drain Current Vs. Case Temperature

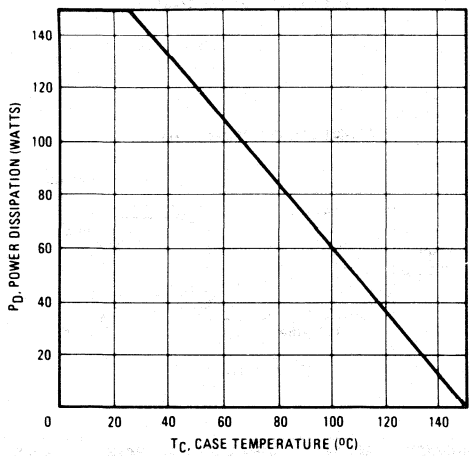


Fig. 14 – Power Vs. Temperature Derating Curve

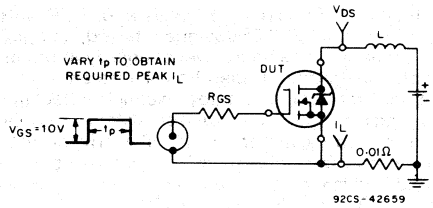


Fig. 15 — Unclamped Energy Test Circuit

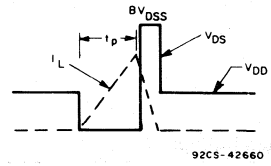


Fig. 16 — Unclamped Energy Waveforms

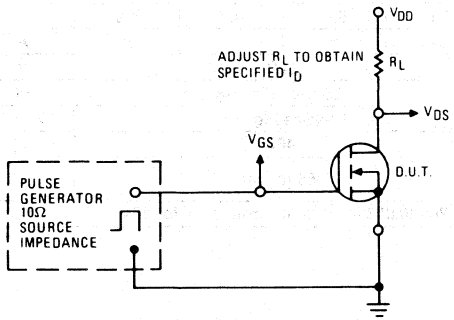


Fig. 17 – Switching Time Test Circuit

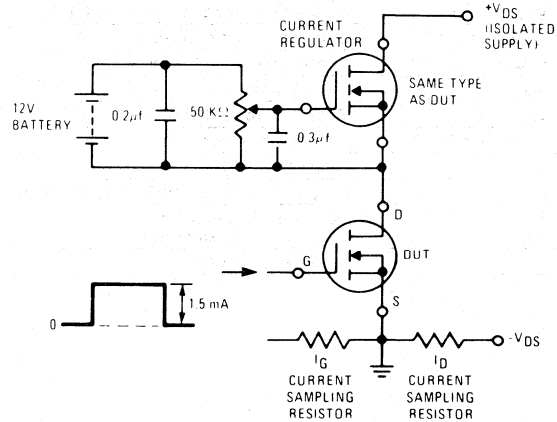


Fig. 18 – Gate Charge Test Circuit

IRFP440R, IRFP441R, IRFP442R, IRFP443R

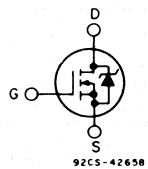
File Number **2089**

Avalanche Energy Rated N-Channel Power MOSFETs

8A and 7A, 500V-400V
$r_{DS}(on) = 0.85\Omega$ and 1.1Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

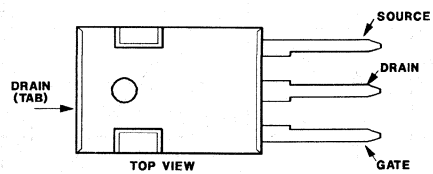


TERMINAL DIAGRAM

The IRFP440R, IRFP441R, IRFP442R and IRFP443R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic. package.

TERMINAL DESIGNATION



JEDEC TO-247

Absolute Maximum Ratings

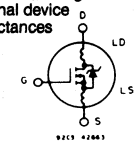
Parameter		IRFP440R	IRFP441R	IRFP442R	IRFP443R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	480				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP440R, IRFP441R, IRFP442R, IRFP443R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP440R IRFP442R	500	—	—	V	V_{GS} = 0V
		IRFP441R IRFP443R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP440R IRFP441R	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFP442R IRFP443R	7.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP440R IRFP441R	—	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		IRFP442R IRFP443R	—	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 4.0A
C_{iss}	Input Capacitance	ALL	—	1225	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	85	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	17	35	ns	$V_{DD} \simeq$ 200V, I_D = 4.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	42	90	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	20	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	22	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances

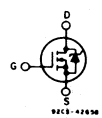


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP440R IRFP441R	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP442R IRFP443R	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP440R IRFP441R	—	—	32	A	
		IRFP442R IRFP443R	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	IRFP440R IRFP441R	—	—	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRFP442R IRFP443R	—	—	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1100	—	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.4	—	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 11 mH, R_{gs} = 50Ω, I_{peak} = 8.8A. See figures 15, 16.

IRFP440R, IRFP441R, IRFP442R, IRFP443R

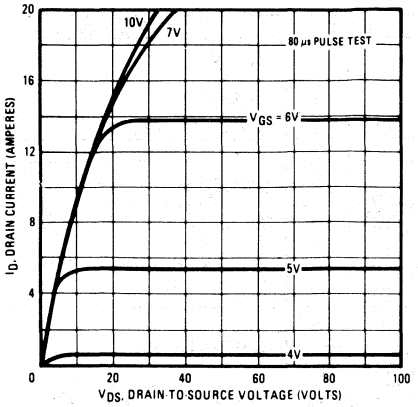


Fig. 1 - Typical output characteristics.

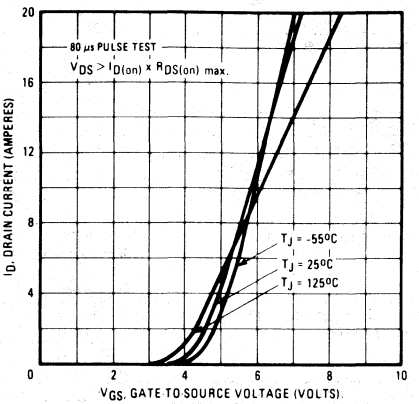


Fig. 2 - Typical transfer characteristics.

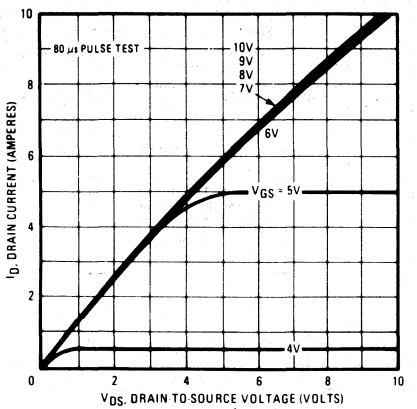


Fig. 3 - Typical saturation characteristics.

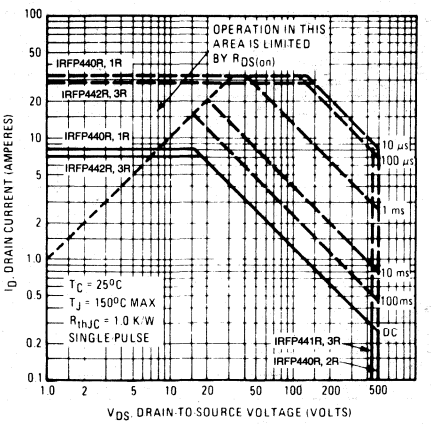


Fig. 4 - Maximum safe operating area.

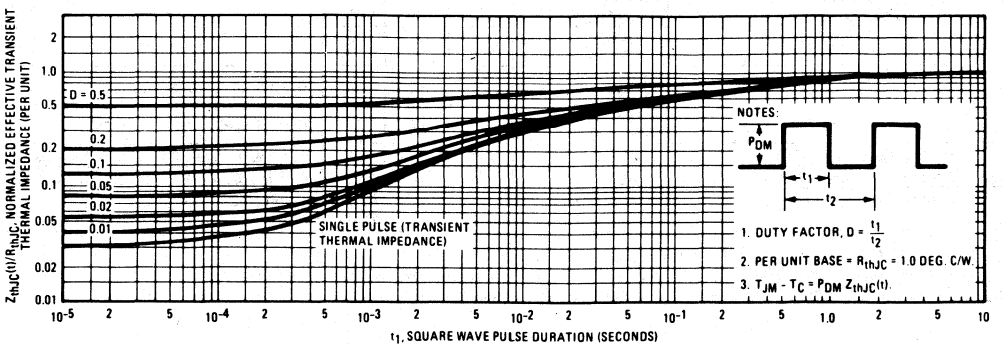


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

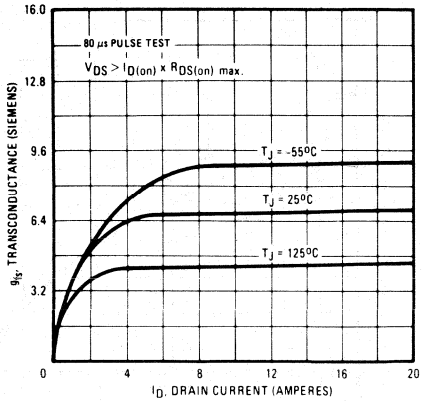


Fig. 6 - Typical transconductance vs. drain current.

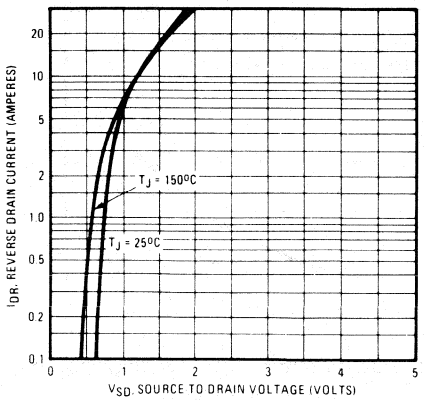


Fig. 7 - Typical source-drain diode forward voltage.

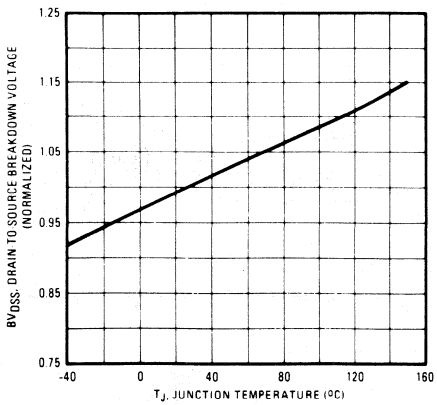


Fig. 8 - Breakdown voltage vs. temperature.

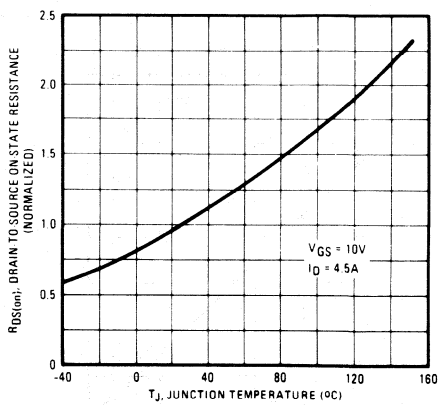


Fig. 9 - Normalized on-resistance vs. temperature.

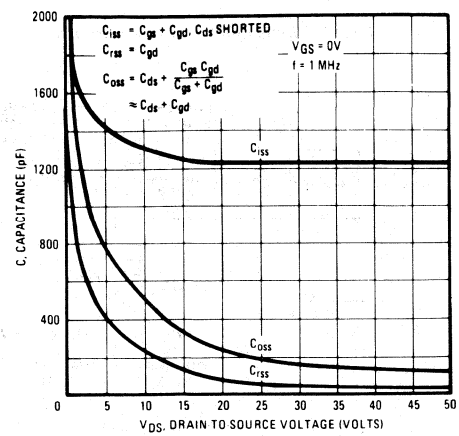


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

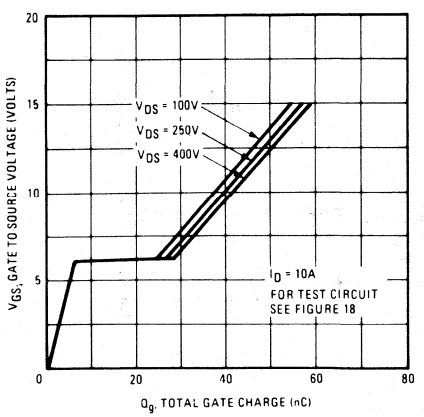


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFP440R, IRFP441R, IRFP442R, IRFP443R

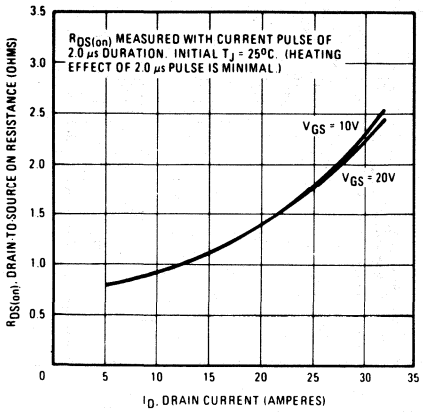


Fig. 12 - Typical on-resistance vs. drain current.

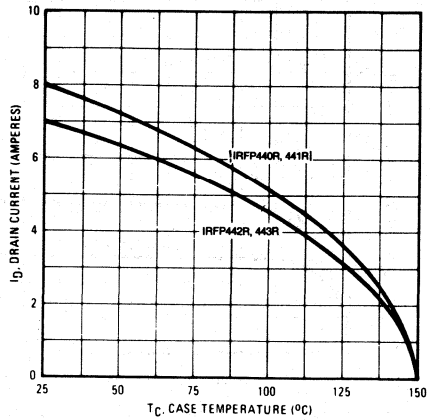


Fig. 13 - Maximum drain current vs. case temperature.

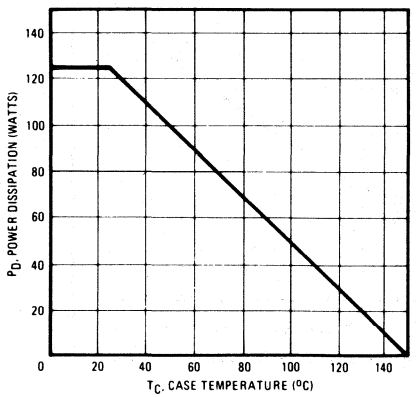


Fig. 14 - Power vs. temperature derating curve.

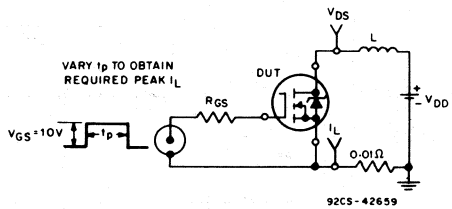


Fig. 15 - Unclamped energy test circuit.

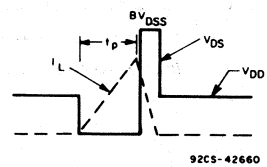


Fig. 16 - Unclamped energy waveforms.

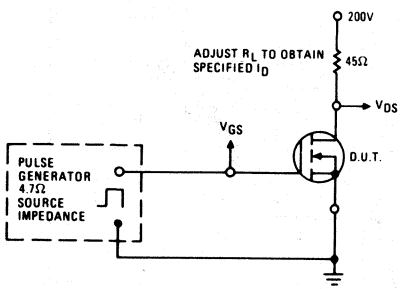


Fig. 17 - Switching time test circuit.

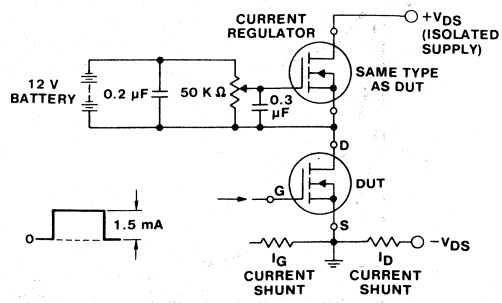


Fig. 18 - Gate charge test circuit.

File Number **2018**

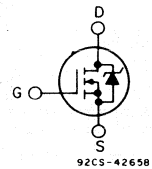
IRFP450R, IRFP451R
IRFP452R, IRFP453R

Avalanche Energy Rated N-Channel Power MOSFETs

12A and 13A, 450V-500V
$r_{DS}(on) = 0.4\Omega$ and 0.5Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

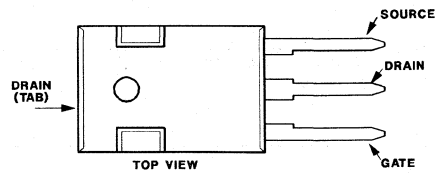


TERMINAL DIAGRAM

The IRFP450R, IRFP451R, IRFP452R and IRFP453R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

Absolute Maximum Ratings

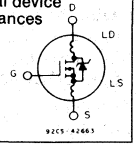
Parameter		IRFP450R	IRFP451R	IRFP452R	IRFP453R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	13	13	12	12	A
I_D @ $T_C = 100°C$	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	860				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP450R, IRFP451R, IRFP452R, IRFP453R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP450R IRFP452R	500	—	—	V	V_{GS} = 0V
		IRFP451R IRFP453R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP450R IRFP451R	13	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRFP452R IRFP453R	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP450R IRFP451R	—	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		IRFP452R IRFP453R	—	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 7.0A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} \simeq$ 210V, I_D = 7.0A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	150	ns	
t_f	Fall Time	ALL	—	—	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	82	140	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	40	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	42	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP450R IRFP451R	—	—	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP452R IRFP453R	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP450R IRFP451R	—	—	52	A	
		IRFP452R IRFP453R	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	IRFP450R IRFP451R	—	—	1.4	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
		IRFP452R IRFP453R	—	—	1.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	1300	—	ns	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	7.4	—	μC	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25V, starting T_J = 25°C, L = 9.2mH, R_{gs} = 25Ω, I_{peak} = 13A. See figures 15, 16.

IRFP450R, IRFP451R, IRFP452R, IRFP453R

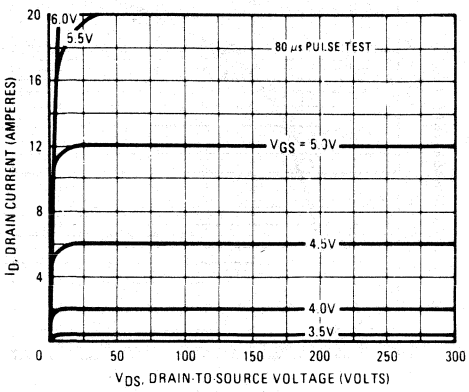


Fig. 1 — Typical Output Characteristics

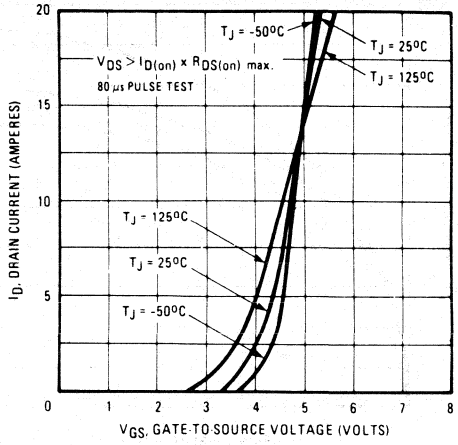


Fig. 2 — Typical Transfer Characteristics

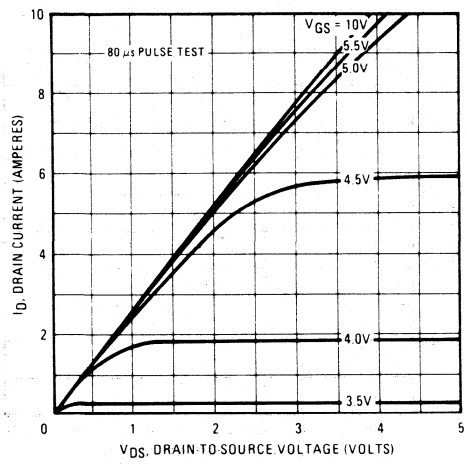


Fig. 3 — Typical Saturation Characteristics

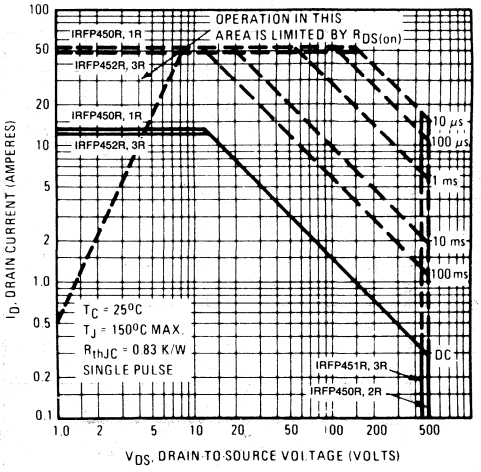


Fig. 4 — Maximum Safe Operating Area

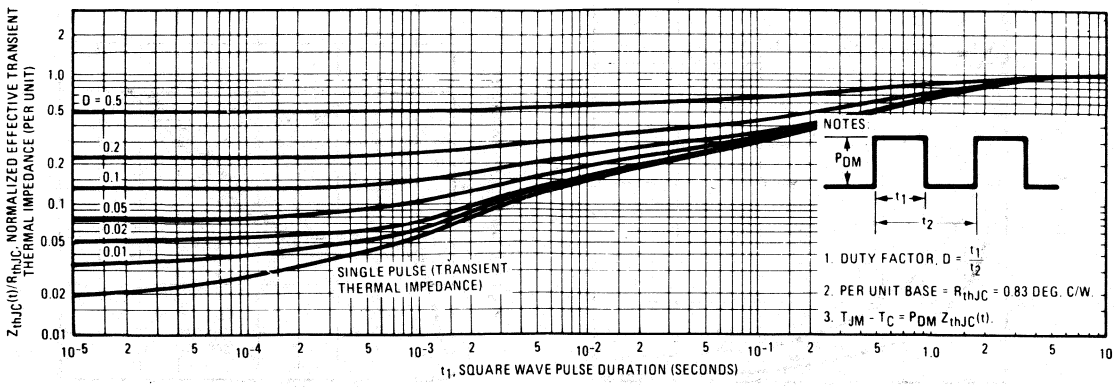


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFP450R, IRFP451R, IRFP452R, IRFP453R

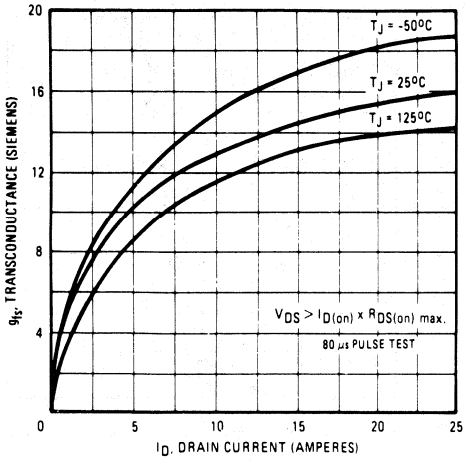


Fig. 6 — Typical Transconductance Vs. Drain Current

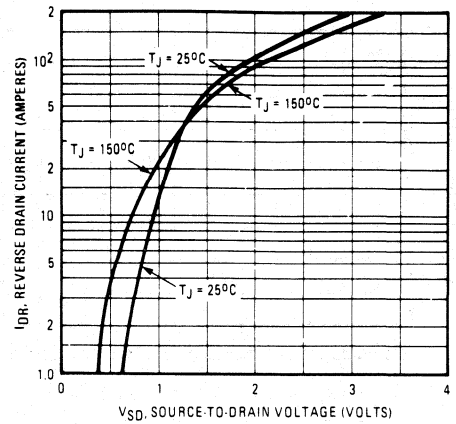


Fig. 7 — Typical Source-Drain Diode Forward Voltage

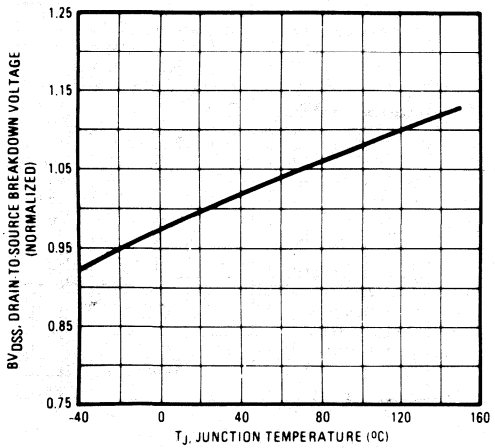


Fig. 8 — Breakdown Voltage Vs. Temperature

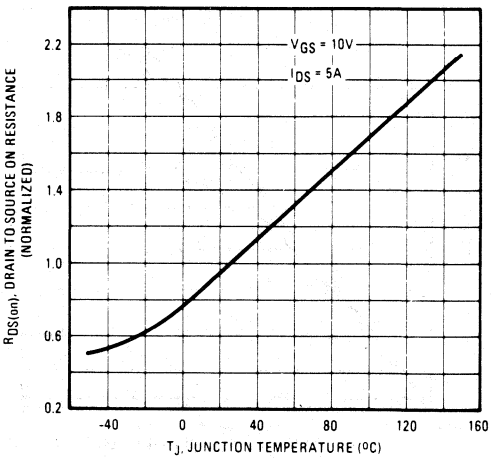


Fig. 9 — Normalized On-Resistance Vs. Temperature

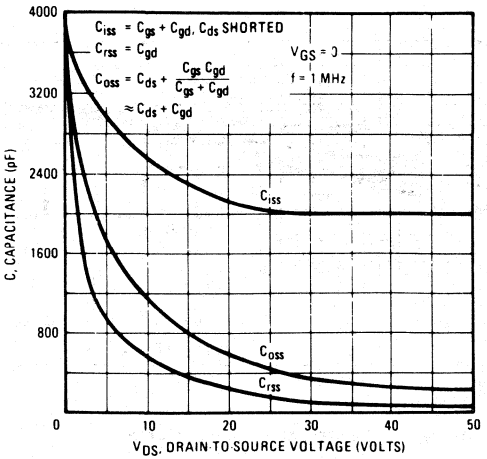


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

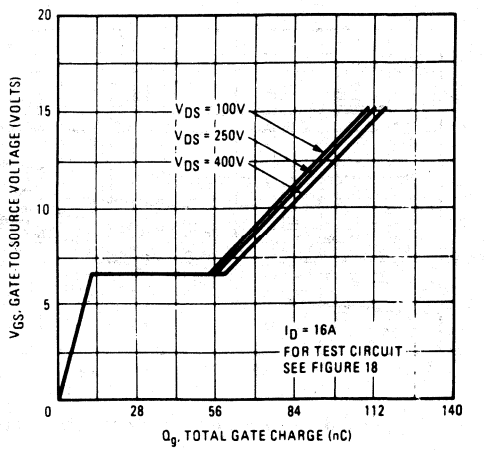


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

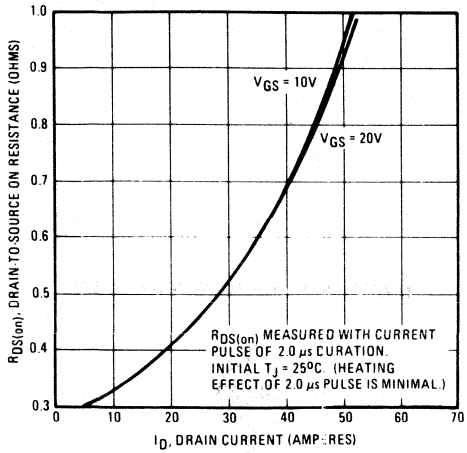


Fig. 12 — Typical On-Resistance Vs. Drain Current

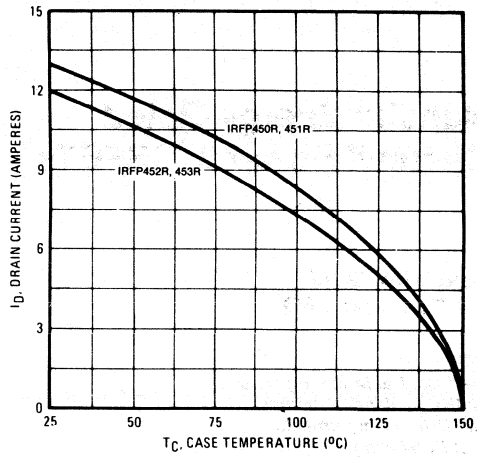


Fig. 13 — Maximum Drain Current Vs. Case Temperature

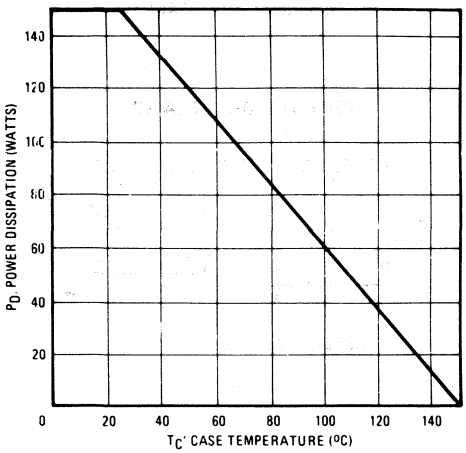


Fig. 14 — Power Vs. Temperature Derating Curve

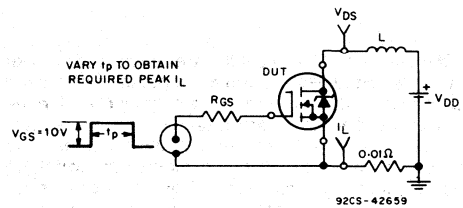


Fig. 15 — Unclamped Energy Test Circuit

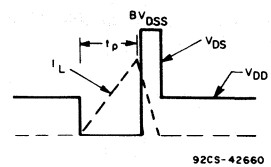


Fig. 16 — Unclamped Energy Waveforms

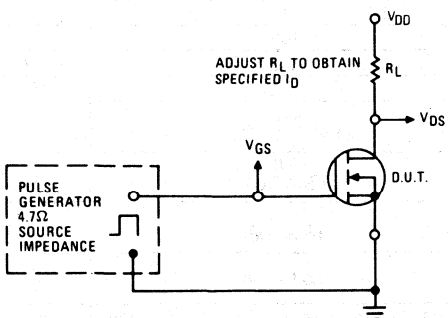


Fig. 17 — Switching Time Test Circuit

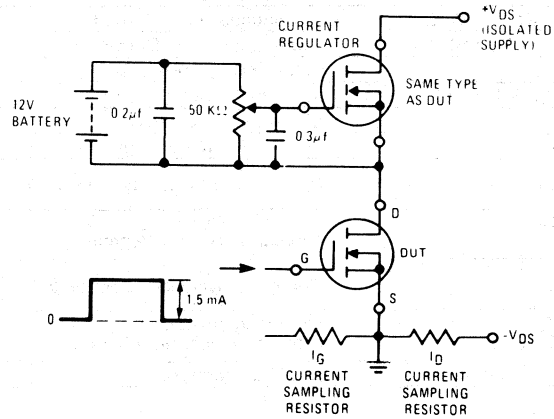


Fig. 18 — Gate Charge Test Circuit

IRFPC40R, IRFPC42R

File Number **2158**

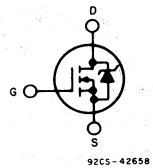
Avalanche-Energy-Rated N-Channel Power MOSFETs

6.8A and 5.9A, 600V
$r_{DS(on)}$ = 1.2Ω and 1.6Ω

Features:

- *Isolated Central Mounting Hole*
- *Repetitive Avalanche Ratings*
- *Simple Drive Requirements*
- *Ease of Paralleling*

N-CHANNEL ENHANCEMENT MODE

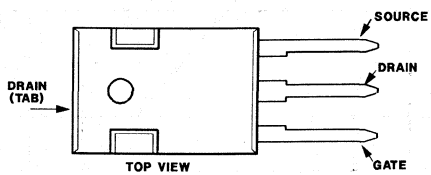


TERMINAL DIAGRAM

The IRFPC40R and IRFPC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFPC-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

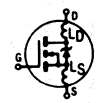
Absolute Maximum Ratings

Parameter		IRFPC40R	IRFPC42R	Units
I_D @ T_C = 25°C	Continuous Drain Current	6.8	5.9	A
I_D @ T_C = 100°C	Continuous Drain Current	4.3	3.7	A
I_{DM}	Pulsed Drain Current ①	27	24	A
P_D @ T_C = 25°C	Max. Power Dissipation	150		W
	Linear Derating Factor	1.2		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	410 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ① (Repetitive or Non-Repetitive)	6.8 (See E_{AR})		A
E_{AR}	Repetitive Avalanche Energy ①	15 (See I_{AR})		mJ
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]		°C

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	600	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFPC40R	—	0.97	1.2	Ω	V_{GS} = 10V, I_D = 3.7A
		IRFPC42R	—	1.2	1.6		
$I_{D(on)}$	On-State Drain Current ③	IRFPC40R	6.8	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
		IRFPC42R	5.9				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	4.9	7.3	—	S(℧)	$V_{DS} \geq 100V$, I_{DS} = 3.7A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	40	60	nC	V_{GS} = 10V, I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	ALL	—	5.5	8.3	nC	V_{DS} = 0.6 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	20	30	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	13	20	ns	V_{DD} = 200V, I_D = 6.2A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	18	27	ns	R_D = 47Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f	Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal inductances.



C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	160	—	pF	f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	45	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	0.83	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.24	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	40	°C/W	Typical-socket mount
	Mounting Torque	ALL	—	—	10	in.•lbs.	Standard 6-32 screw

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.8	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ①	ALL	—	—	27	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	450	940	ns	T_J = 25°C, I_F = 6.2A, di/dt = 100A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.8	3.8	7.9	μC	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

③ Pulse width ≤ 300μs; Duty Cycle ≤ 2%

IRFPC40R, IRFPC42R

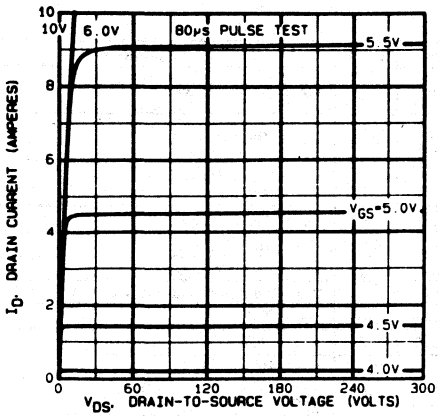


Fig. 1 - Typical Output Characteristics

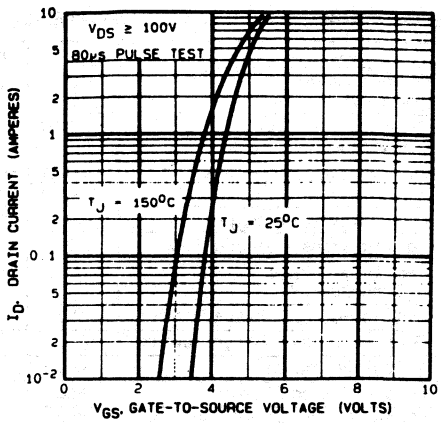


Fig. 2 - Typical Transfer Characteristics

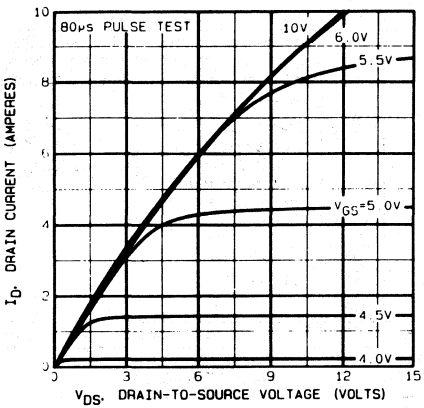


Fig. 3 - Typical Saturation Characteristics

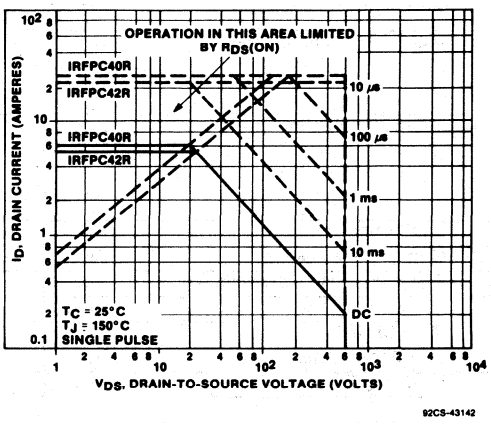


Fig. 4 - Maximum Safe Operating Area

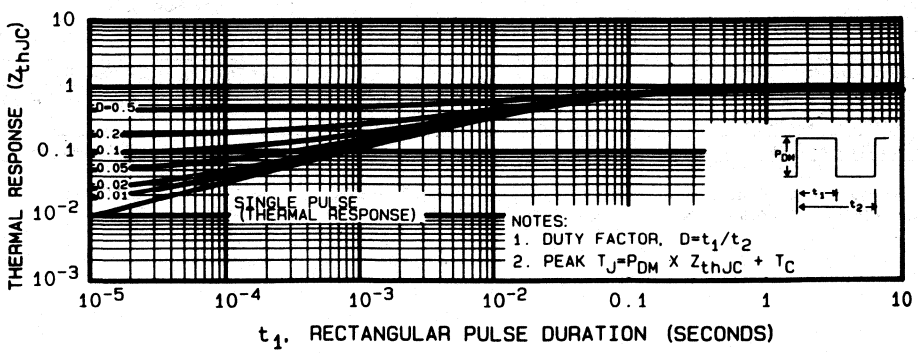


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

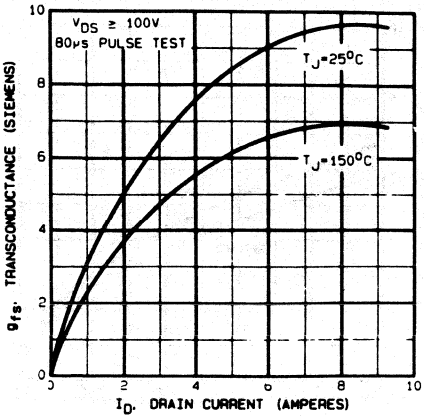


Fig. 6 - Typical Transconductance Vs. Drain Current

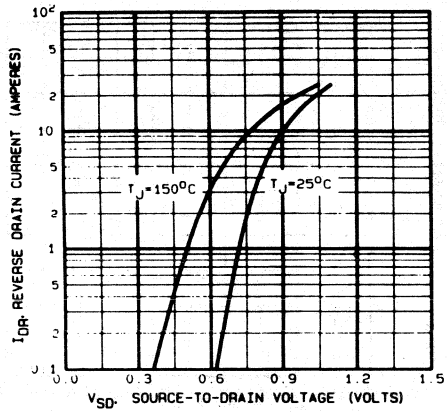


Fig. 7 - Typical Source-Drain Diode Forward Voltage

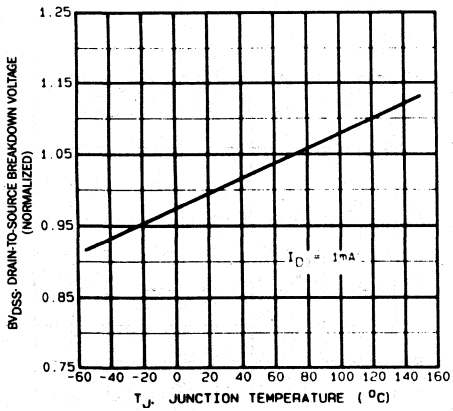


Fig. 8 - Breakdown Voltage Vs. Temperature

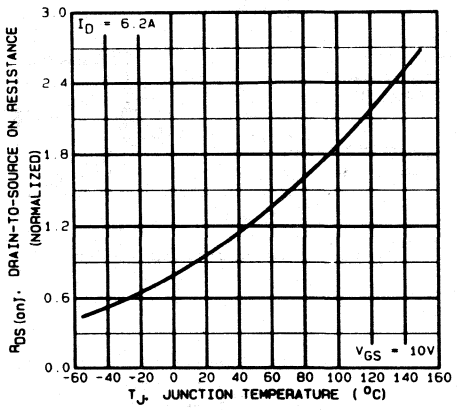


Fig. 9 - Normalized On-Resistance Vs. Temperature

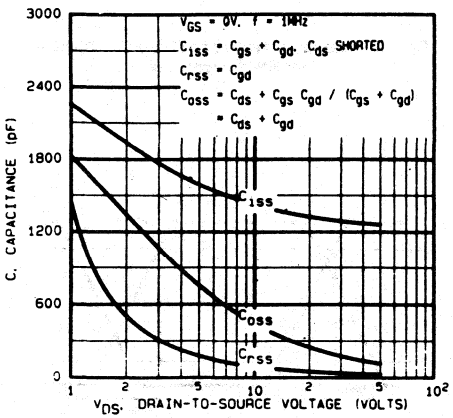


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

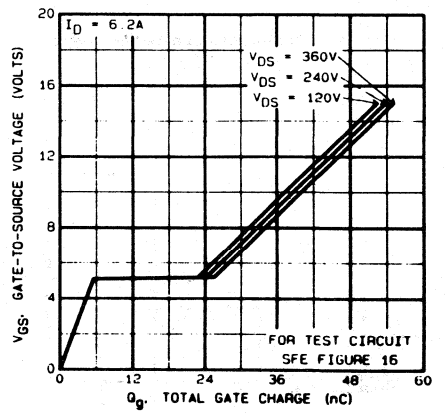


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRFPC40R, IRFPC42R

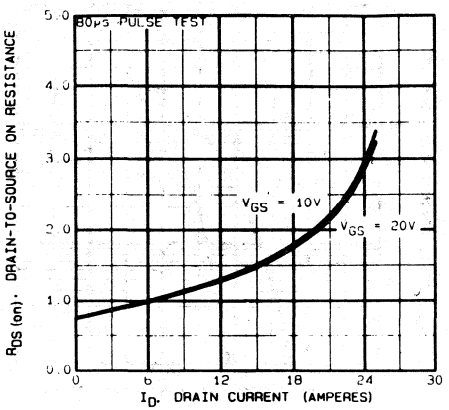


Fig. 12 - Typical On-Resistance Vs. Drain Current

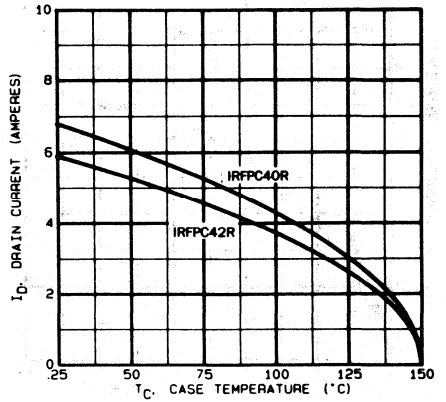


Fig. 13 - Maximum Drain Current Vs. Case Temperature

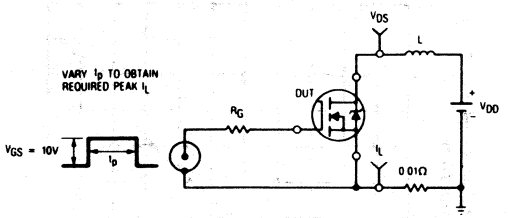


Fig. 14a - Unclamped Inductive Test Circuit

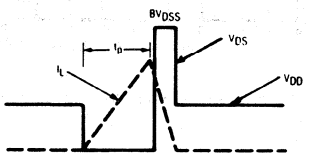


Fig. 14b - Unclamped Inductive Waveforms

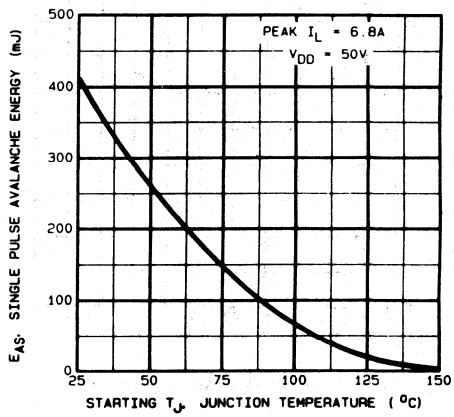


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

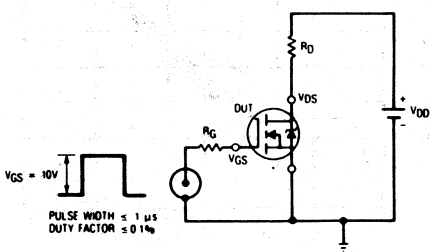


Fig. 15a - Switching Time Test Circuit

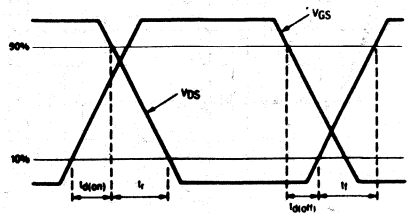


Fig. 15b - Switching Time Waveforms

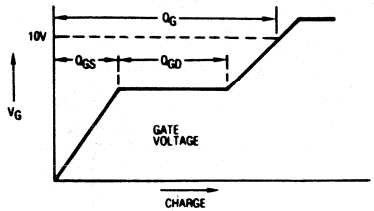
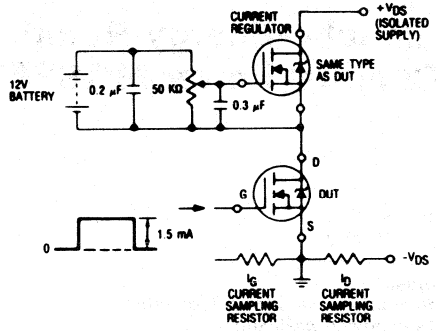


Fig. 16a - Basic Gate Charge Waveform



Fib. 16b - Gate Charge Test Circuit

2N6804

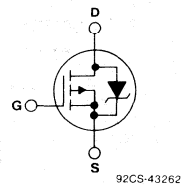
File Number **2217**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-11A, -100V
$r_{DS(on)}$ = 0.30Ω

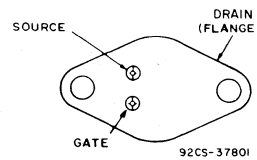
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA

The 2N6804 is an advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits

The 2N6804 is supplied in the JEDEC TO-204AA steel package.

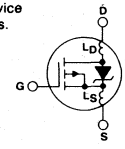
Absolute Maximum Ratings

Parameter		2N6804	Units
V_{DS}	Drain-Source Voltage	-100*	V
V_{DG}	Drain-Gate Voltage (R_{GS} = 20kΩ)	-100*	V
I_D @ T_C = 25°C	Continuous Drain Current	-11*	A
I_D @ T_C = 100°C	Continuous Drain Current	-7.0*	A
I_{DM}	Pulsed Drain Current ②	-50*	A
V_{GS}	Gate-Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 14)	W
	Linear Derating Factor	0.6* (See Fig. 14)	W/°C
E_{AS}	Single Pulse Avalanche Energy ③	500	mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Current ①	−11*	—	—	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ max., V_{GS} = −10V
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30	Ω	V_{GS} = −10V, I_D = −6.5A
g_{fs}	Forward Transconductance ①	2.0	3.7	—	S(℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = −6.5A
C_{iss}	Input Capacitance	400	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} ≅ −35V, I_D = −7.0A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

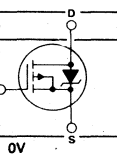


Thermal Resistance

$R_{\theta JC}$	Junction-to-Case	—	—	1.67*	°C/W	
$R_{\theta CS}$	Case-to-Sink	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{\theta JA}$	Junction-to-Ambient	—	—	30	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−50	A	
V_{SD}	Diode Forward Voltage ①	—	—	−1.5	V	T_C = 25°C, I_S = −11A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, Starting T_J = 25°C, L = 6.2 mH,
R_g = 25Ω, Peak I_L = 11 A, (See Fig. 15 and 16).

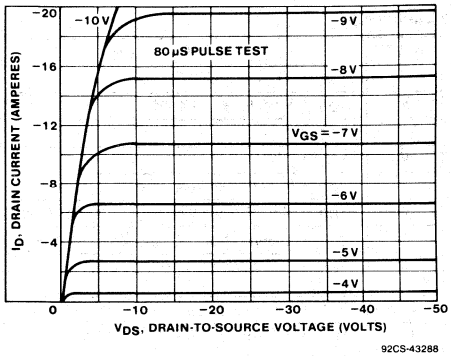


Fig. 1 - Typical Output Characteristics

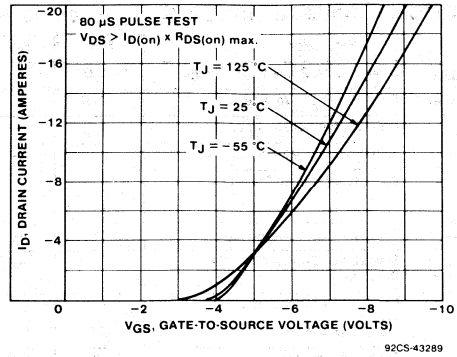


Fig. 2 - Typical Transfer Characteristics

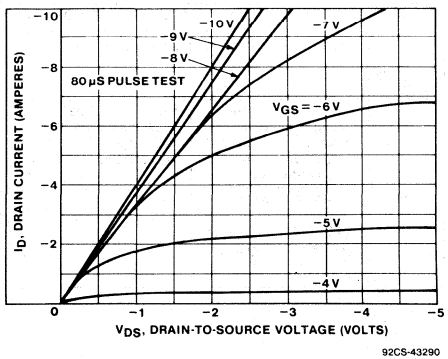


Fig. 3 - Typical saturation characteristic.

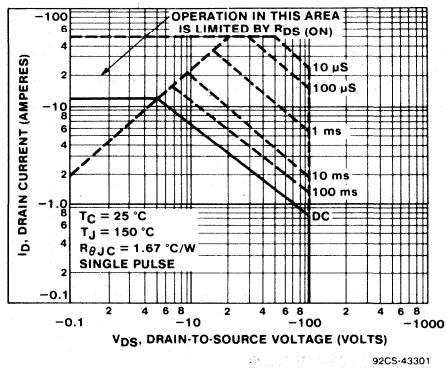


Fig. 4 - Maximum safe operating area.

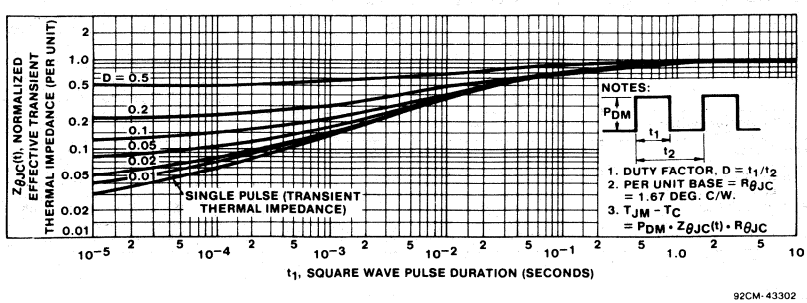


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

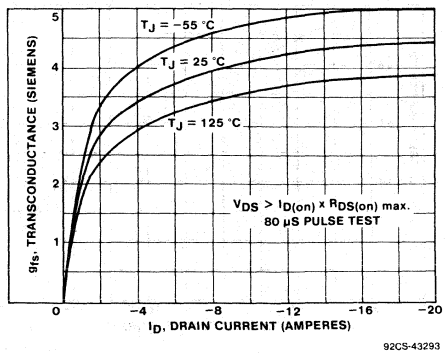


Fig. 6 - Typical transconductance vs. drain current.

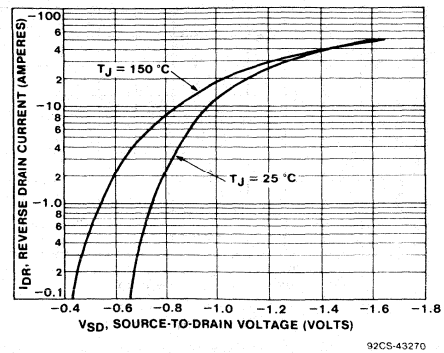


Fig. 7 - Typical source-drain diode forward voltage.

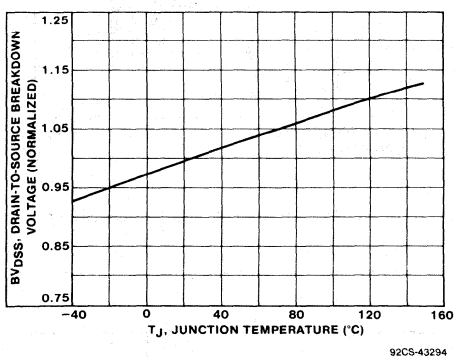


Fig. 8 - Breakdown voltage vs. temperature.

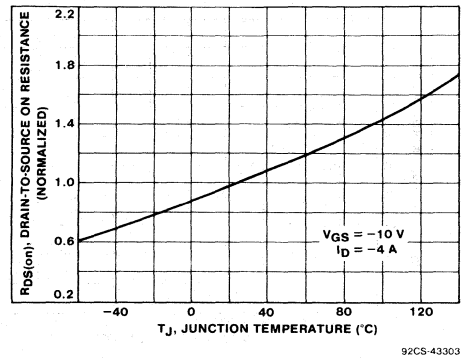


Fig. 9 - Normalized on-resistance vs. temperature.

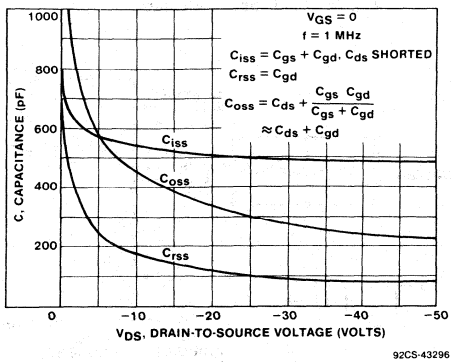


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

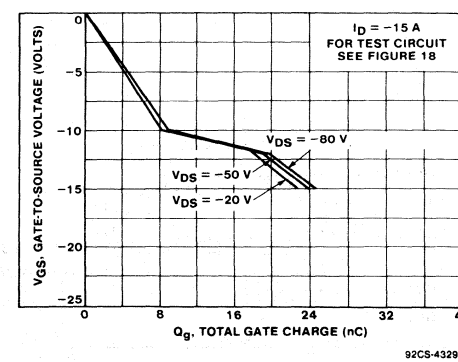


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

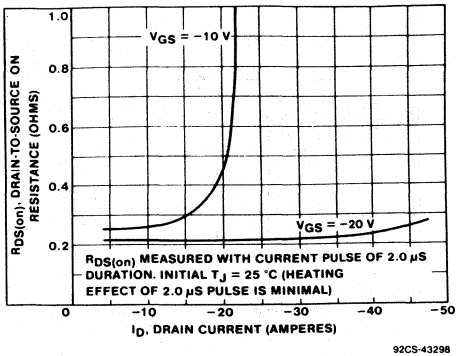


Fig. 12 - Typical on-resistance vs. drain current.

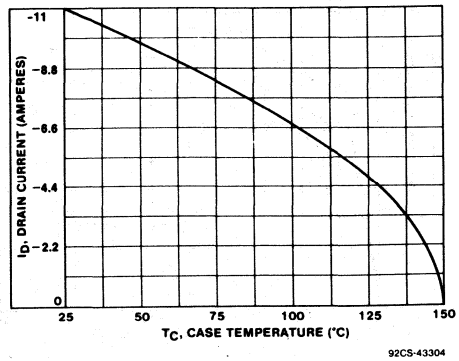


Fig. 13 - Maximum drain current vs. case temperature.

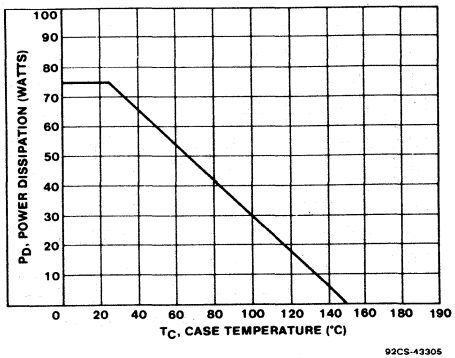


Fig. 14 - Power vs. temperature derating curve.

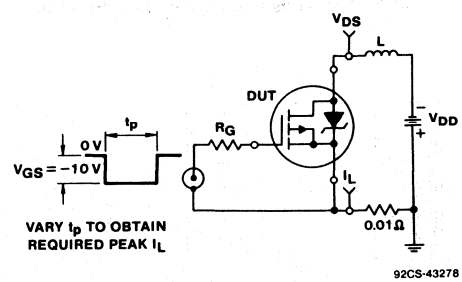


Fig. 15 - Unclamped inductive test circuit.

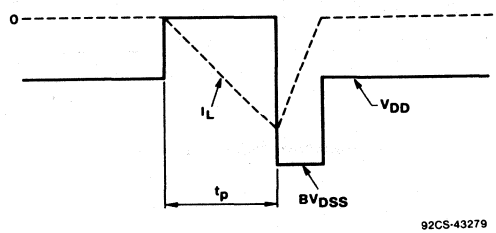


Fig. 16 - Unclamped inductive waveforms.

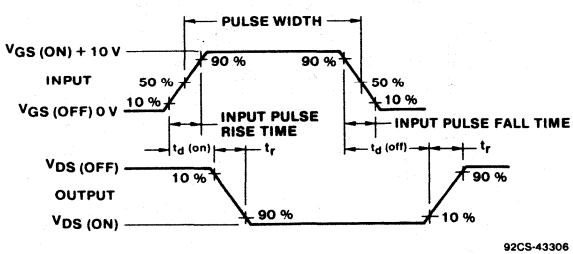


Fig. 17 - Switching time test circuit.

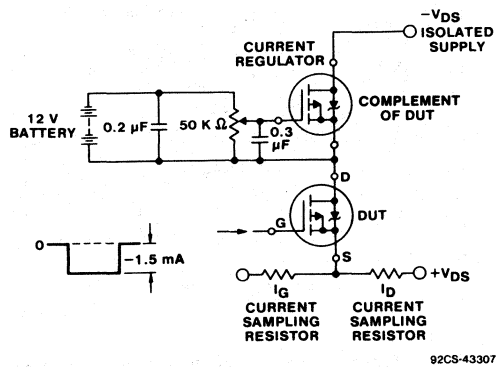


Fig. 18 - Gate charge test circuit.

File Number **2219**

2N6849

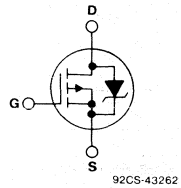
Avalanche-Energy-Rated P-Channel Power MOSFETs

-6.5A, and -100V
r_{DS} (on) = 0.30Ω

Features:

- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

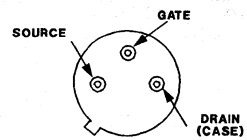


P-CHANNEL ENHANCEMENT MODE

The 2N6849 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6849 is supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

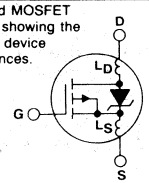
Parameter		2N6849	Units
V_{DS}	Drain-Source Voltage	-100*	V
V_{DG}	Drain-Gate Voltage (R_{GS} = 20kΩ)	-100*	V
I_D @ T_C = 25°C	Continuous Drain Current	-6.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	-4.1*	A
I_{DM}	Pulsed Drain Current ②	-25*	A
V_{GS}	Gate-Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	25* (See Fig. 14)	W
	Linear Derating Factor	0.2* (See Fig. 14)	W/°C
E_{AS}	Single Pulse Avalanche Energy ③	500	mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150*	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	°C

2N6849

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−2.1	V	V_{DS} > $I_{D(on)}R_{DS(on)}$max., V_{GS} = −10V, I_D = 6.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30*	Ω	V_{GS} = −10V, I_D = −4.1A
g_{fs}	Forward Transconductance ①	2.5	3.5	7.5	S(℧)	V_{DS} = −5V, $I_{D(on)}$ × $R_{DS(on)}$ max., I_D = −4.1A
C_{iss}	Input Capacitance	—	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	—	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} ≅ −42V, I_D = −4.1A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

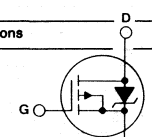


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−6.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−25	A	
V_{SD}	Diode Forward Voltage ①	—	—	-1.5	V	T_C = 25°C, I_S = −6.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, starting T_J = 25°C, L = 17.25 mH, R_G = 25Ω, Peak I_L = 6.5A. (See Fig. 15 and 16)

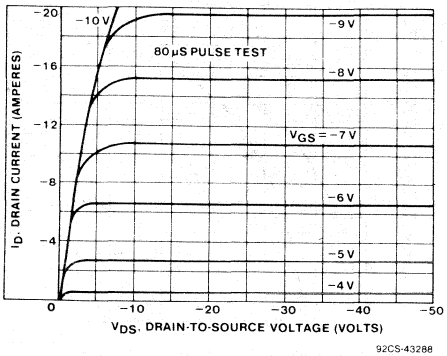


Fig. 1 - Typical Output Characteristics

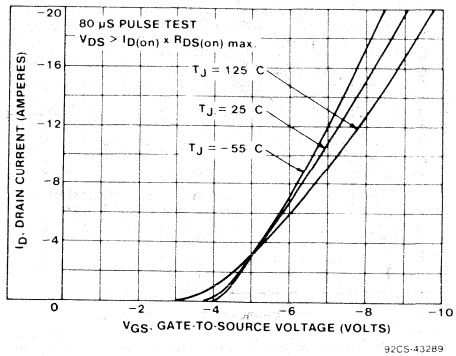


Fig. 2 - Typical Transfer Characteristics

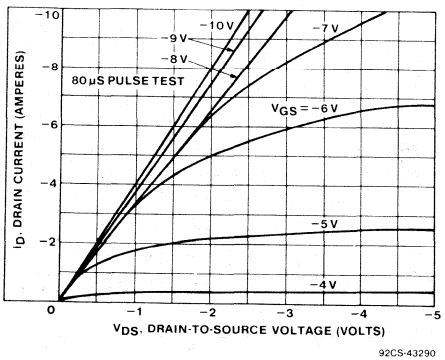


Fig. 3 - Typical Saturation Characteristics

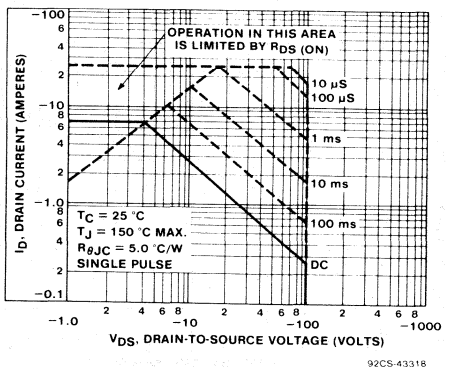


Fig. 4 - Maximum Safe Operating Area

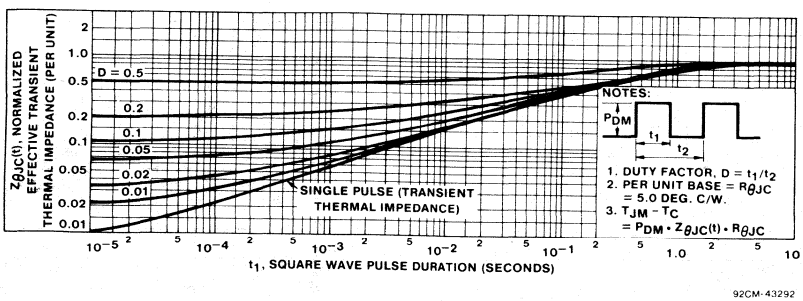


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

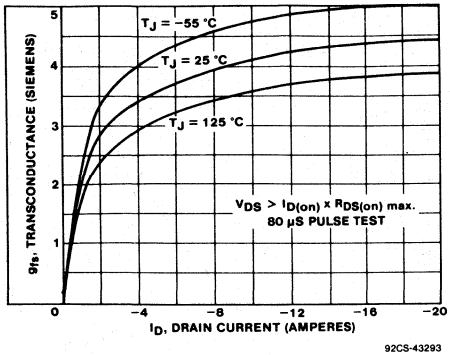


Fig. 6 - Typical Transconductance Vs. Drain Current

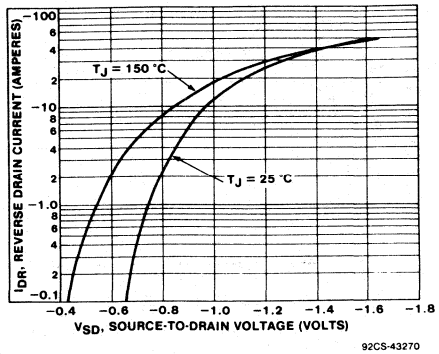


Fig. 7 - Typical Source-Drain Diode Forward Voltage

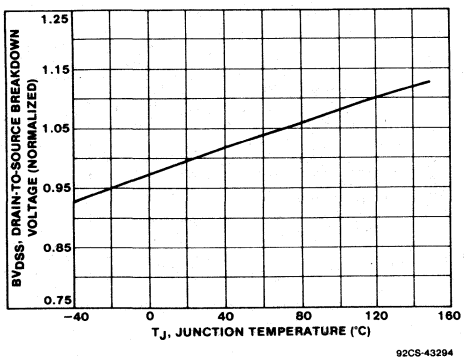


Fig. 8 - Breakdown Voltage Vs. Temperature

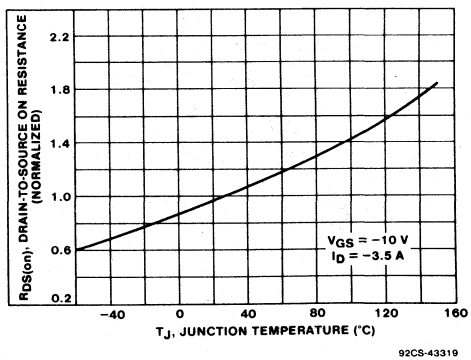


Fig. 9 - Normalized On-Resistance Vs. Temperature

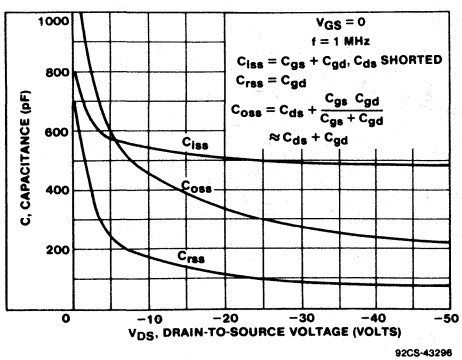


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

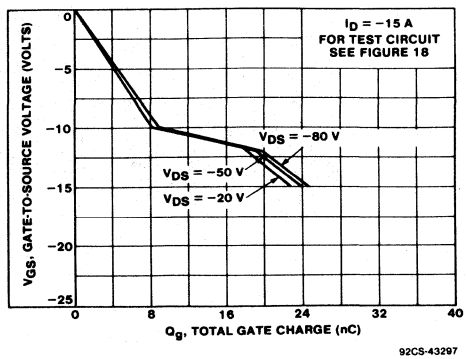


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

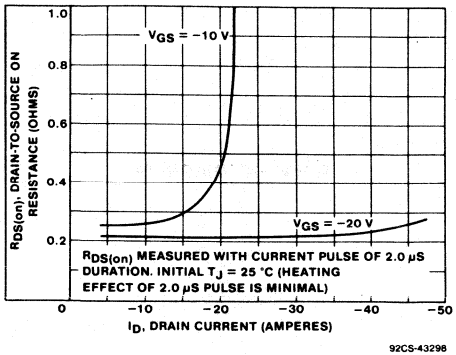


Fig. 12 - Typical On-Resistance Vs. Drain Current

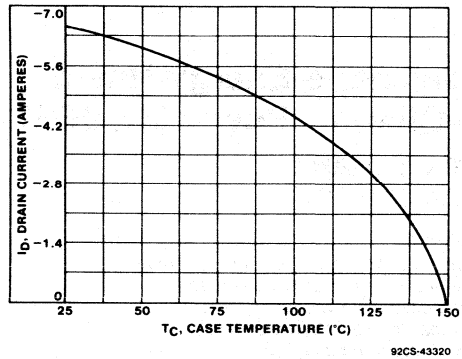


Fig. 13 - Maximum Drain Current Vs. Case Temperature

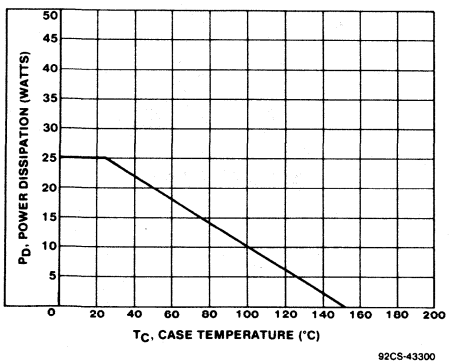


Fig. 14 - Power Vs. Temperature Derating Curve

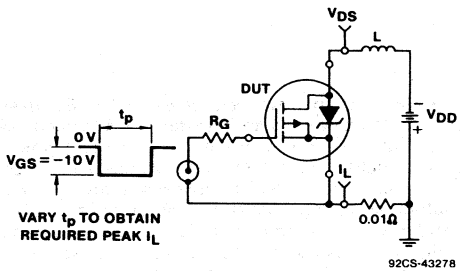


Fig. 15 - Unclamped Inductive Test Circuit

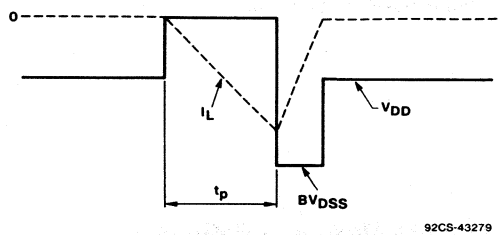


Fig. 16 - Unclamped Inductive Waveforms

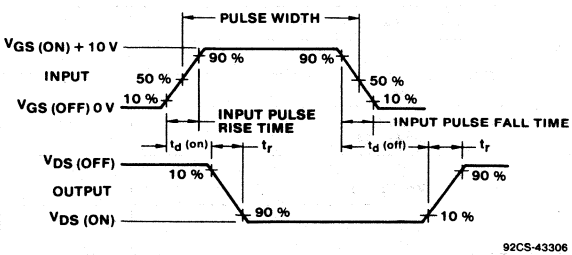


Fig. 17 - Switching Time Test Circuit

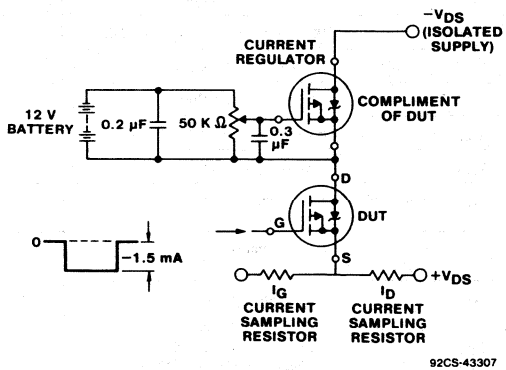


Fig. 18 - Gate Charge Test Circuit

2N6851 File Number **2218**

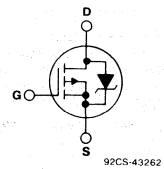
Avalanche-Energy-Rated P-Channel Power MOSFETs

-4.0A, and -200V
r_{DS} (on) = 0.80Ω

Features:

- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

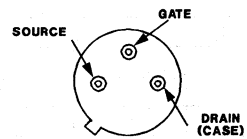


P-CHANNEL ENHANCEMENT MODE

The 2N6851 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6851 is supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

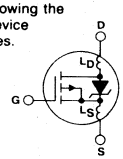
Absolute Maximum Ratings

Parameter		2N6851	Units
V_{DS}	Drain-Source Voltage	-200*	V
V_{DG}	Drain-Gate Voltage (R_{GS} = 20kΩ)	-200*	V
I_D @ T_C = 25°C	Continuous Drain Current	-4.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	-2.4*	A
I_{DM}	Pulsed Drain Current ②	-20*	A
V_{GS}	Gate-Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	25* (See Fig. 14)	W
	Linear Derating Factor	0.2* (See Fig. 14)	W/°C
E_{AS}	Single Pulse Avalanche Energy ③	500	mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−200*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−3.3	V	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ max., V_{GS} = −10V, I_D = −4.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.80*	Ω	V_{GS} = −10V, I_D = −2.4A
g_{fs}	Forward Transconductance ①	2.2	3.5	−6.6	S(℧)	V_{DS} = −5V × $R_{DS(on)max.}$, I_D = −2.4A
C_{iss}	Input Capacitance	400	550	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	50	170	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	40	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	50	ns	V_{DD} ≈ −95V, I_D = −2.4A, Z_o = 50Ω
t_r	Rise Time	—	50	100	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	50	80	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	40	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	31	45	nC	V_{GS} = −15V, I_D = −8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	18	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	13	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

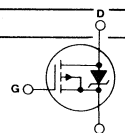


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−20	A	
V_{SD}	Diode Forward Voltage ①	—	—	-1.5	V	T_C = 25°C, I_S = −4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	400	ns	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	2.6	—	μC	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 50V, starting T_J = 25°C, L = 46.9 mH, R_G = 25Ω, Peak I_L = 4.0A. (See Fig. 15 and 16)

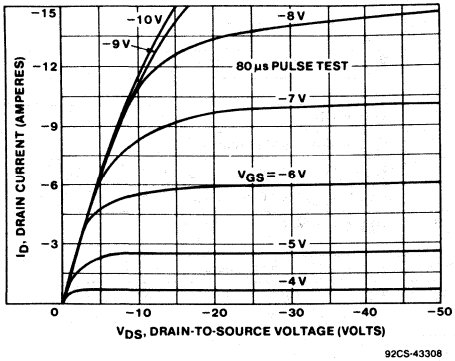


Fig. 1 - Typical Output Characteristics

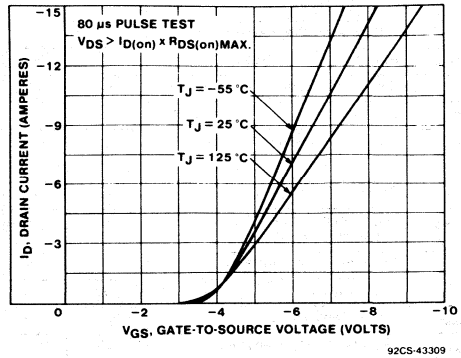


Fig. 2 - Typical Transfer Characteristics

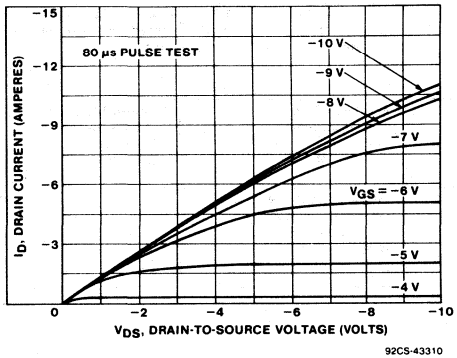


Fig. 3 - Typical Saturation Characteristics

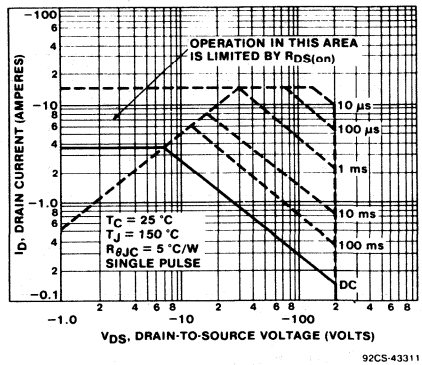


Fig. 4 - Maximum Safe Operating Area

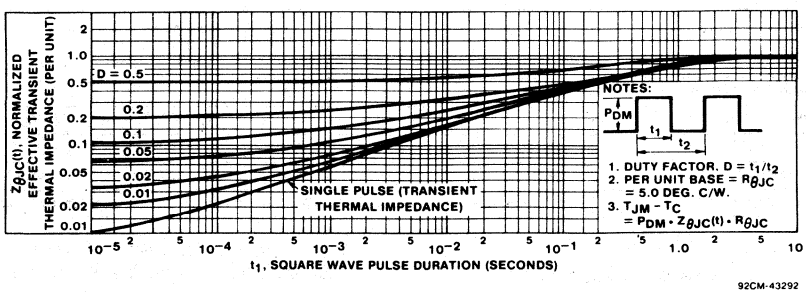


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

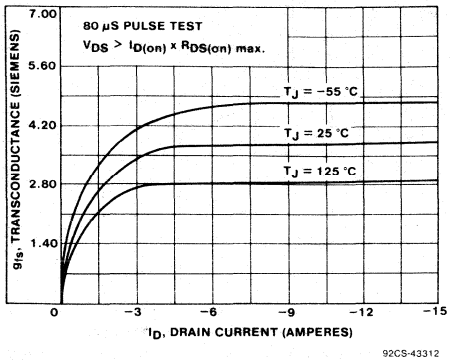


Fig. 6 - Typical Transconductance Vs. Drain Current

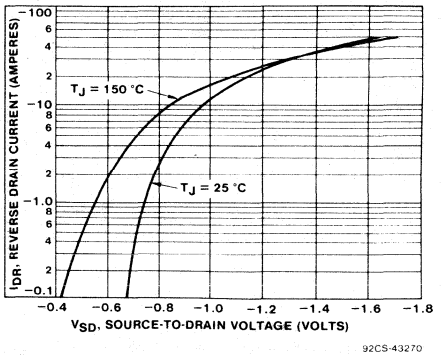


Fig. 7 - Typical Source-Drain Diode Forward Voltage

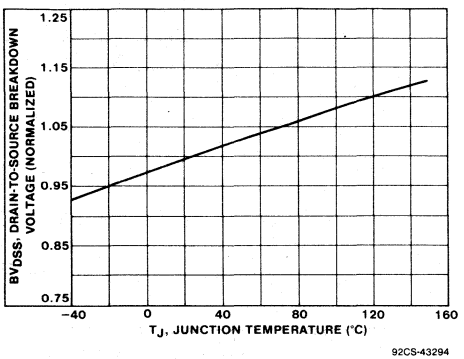


Fig. 8 - Breakdown Voltage Vs. Temperature

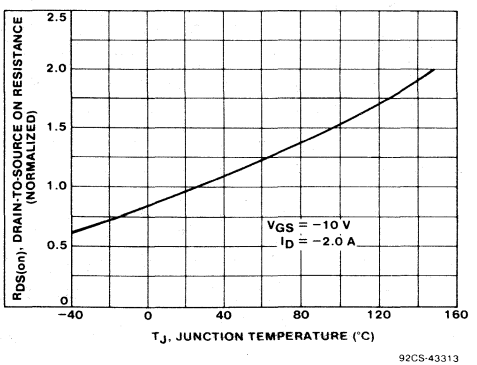


Fig. 9 - Normalized On-Resistance Vs. Temperature

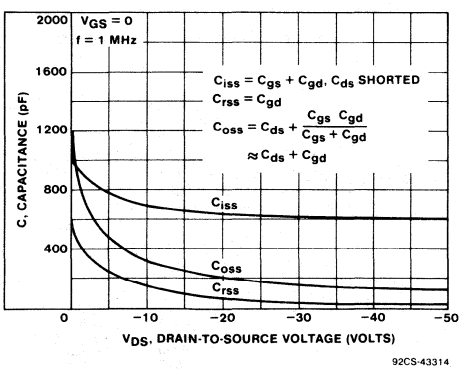


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

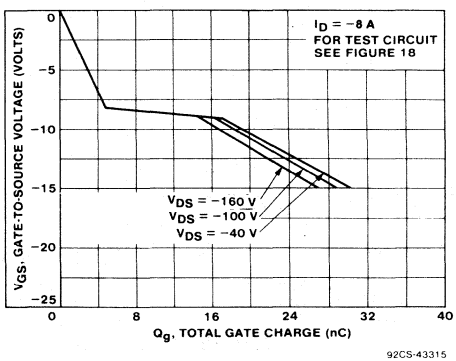


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

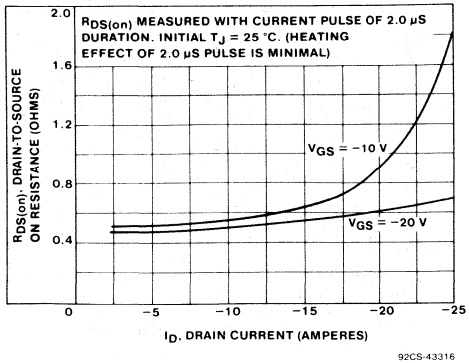


Fig. 12 - Typical On-Resistance Vs. Drain Current

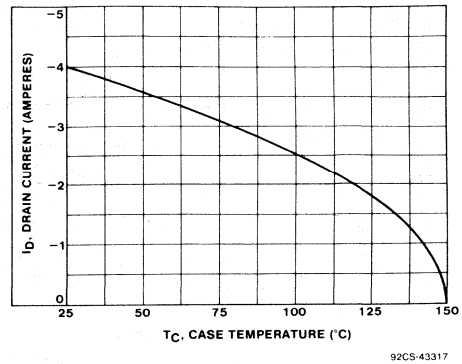


Fig. 13 - Maximum Drain Current Vs. Case Temperature

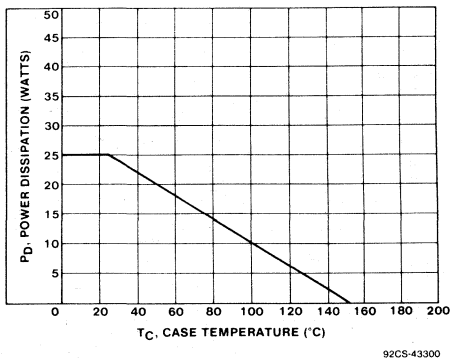


Fig. 14 - Power Vs. Temperature Derating Curve

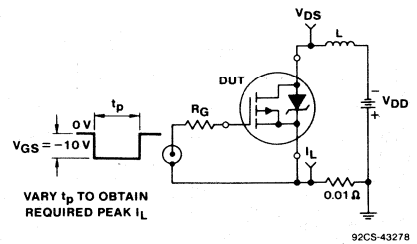


Fig. 15 - Unclamped Inductive Test Circuit

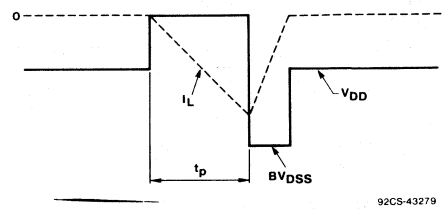


Fig. 16 - Unclamped Inductive Waveforms

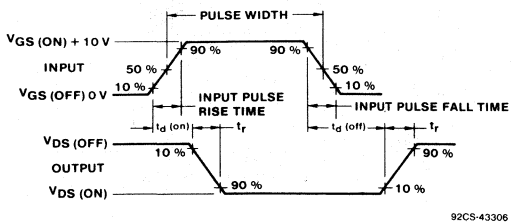


Fig. 17 - Switching Time Test Circuit

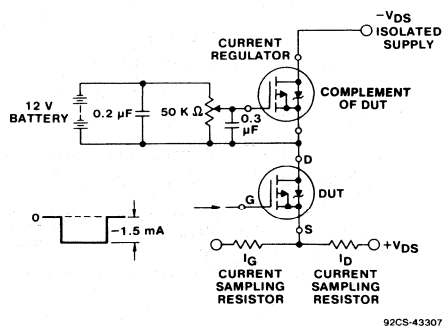


Fig. 18 - Gate Charge Test Circuit

File Number **2220**

IRF9130, IRF9131
IRF9132, IRF9133

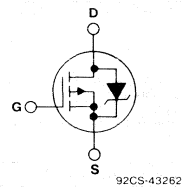
Avalanche-Energy-Rated P-Channel Power MOSFETs

-10A and -12A, -60V and -100V
r_{DS} (on) = 0.30Ω and 0.40Ω

Features:

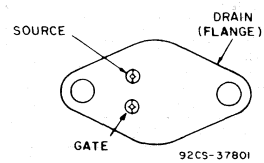
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA

The IRF9130, IRF9131, IRF9132 and IRF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

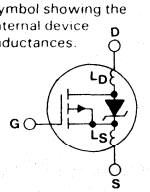
Parameter		IRF9130	IRF9131	IRF9132	IRF9133	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-12	-12	-10	-10	A
I_D @ T_C = 100°C	Continuous Drain Current	-7.5	-7.5	-6.5	-6.5	A
I_{DM}	Pulsed Drain Current ③	-48	-48	-40	-40	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{AS}	Single Pulse Avalanche Energy ④	500				mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF9130, IRF9131, IRF9132, IRF9133

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9130 IRF9132	-100	—	—	V	V_{GS} = 0V
		IRF9131 IRF9133	-60	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9130 IRF9131	-12	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = -10V
		IRF9132 IRF9133	-10	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9130 IRF9131	—	0.25	0.30	Ω	V_{GS} = -10V, I_D = -6.5A
		IRF9132 IRF9133	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.0	3.7	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = -6.5A
C_{iss}	Input Capacitance	ALL	—	500	—	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -6.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	70	140	ns	
t_f	Fall Time	ALL	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	25	45	nC	V_{GS} = -15V, I_D = -15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	12	22	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

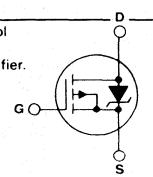


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	ALL	—	—	1.67	°C/W	
$R\theta_{CS}$	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
$R\theta_{JA}$	Junction-to-Ambient	ALL	—	—	30	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9130 IRF9131	—	—	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9132 IRF9133	—	—	-10	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9130 IRF9131	—	—	-48	A	
		IRF9132 IRF9133	—	—	-40	A	
V_{SD}	Diode Forward Voltage ②	IRF9130 IRF9131	—	—	-1.5	V	T_C = 25°C, I_S = -12A, V_{GS} = 0V
		IRF9132 IRF9133	—	—	-1.5	V	T_C = 25°C, I_S = -10A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, I_F = -12A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.8	—	μC	T_J = 150°C, I_F = -12A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 25V, starting T_J = 25°C, L = 5.2 mH, R_G = 25Ω, Peak I_L = 12A. (See Fig. 15 and 16)

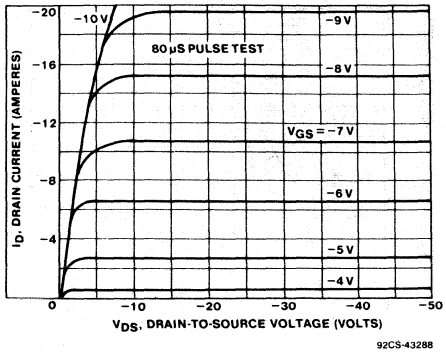


Fig. 1 - Typical Output Characteristics

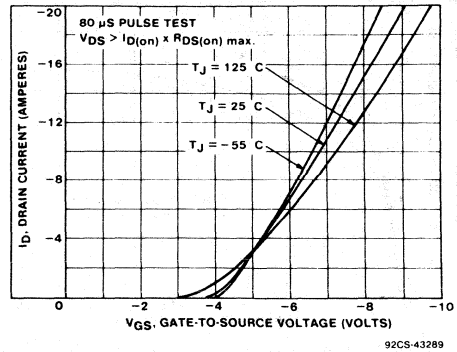


Fig. 2 - Typical Transfer Characteristics

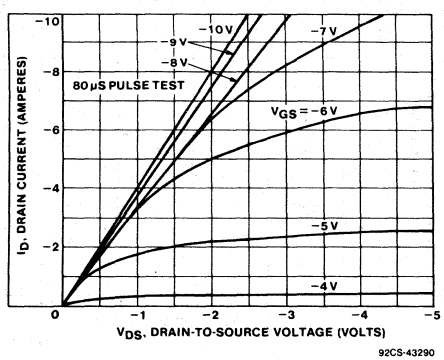


Fig. 3 - Typical Saturation Characteristics

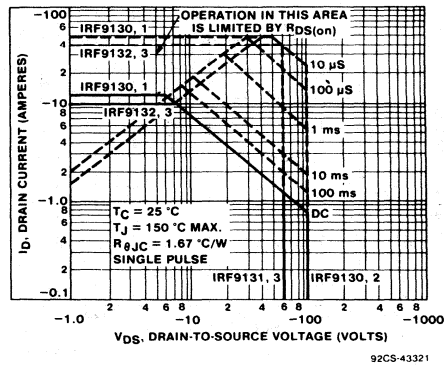


Fig. 4 - Maximum Safe Operating Area

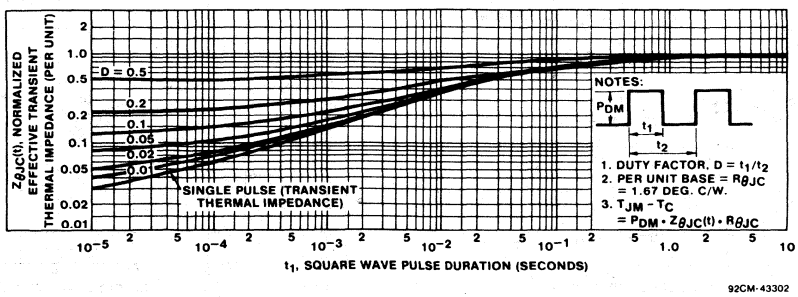


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

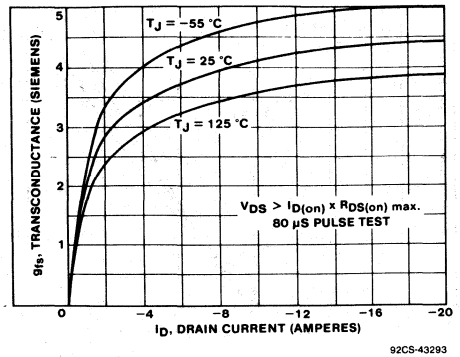


Fig. 6 - Typical Transconductance Vs. Drain Current

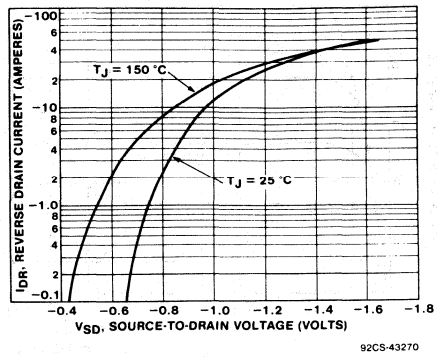


Fig. 7 - Typical Source-Drain Diode Forward Voltage

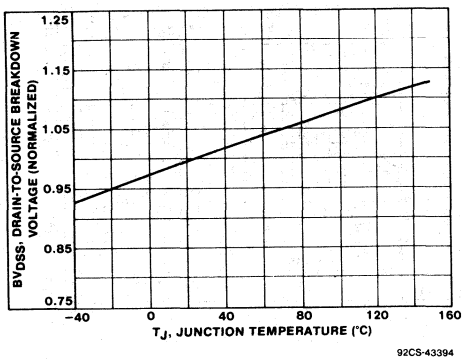


Fig. 8 - Breakdown Voltage Vs. Temperature

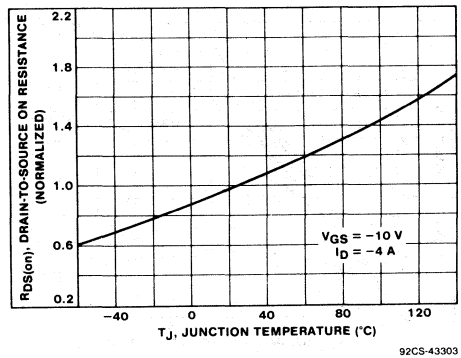


Fig. 9 - Normalized On-Resistance Vs. Temperature

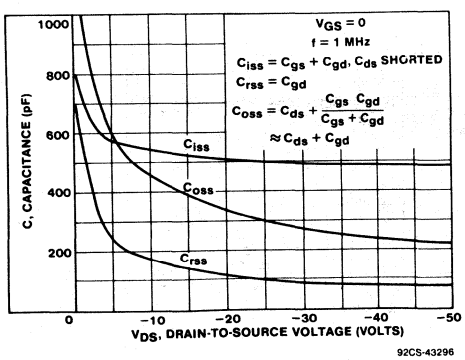


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

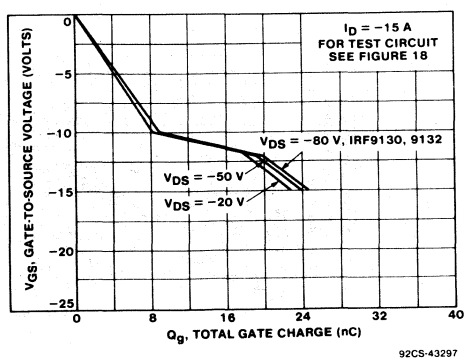


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

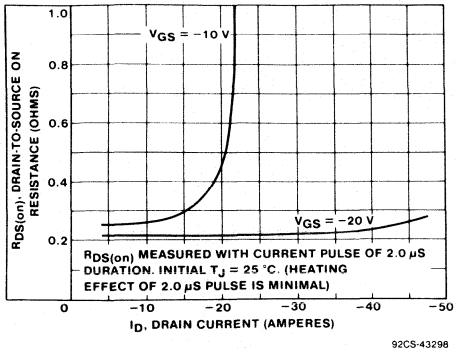


Fig. 12 - Typical On-Resistance Vs. Drain Current

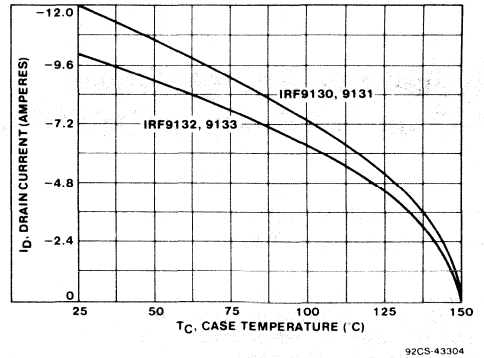


Fig. 13 - Maximum Drain Current Vs. Case Temperature

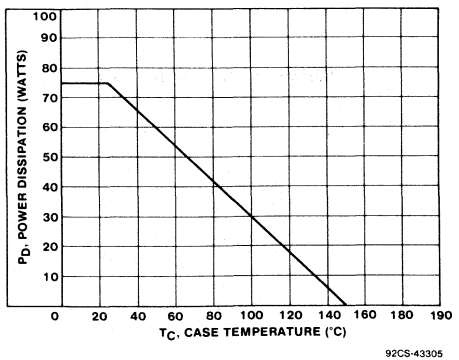


Fig. 14 - Power Vs. Temperature Derating Curve

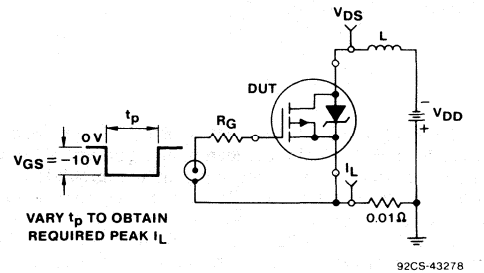


Fig. 15 - Unclamped Inductive Test Circuit

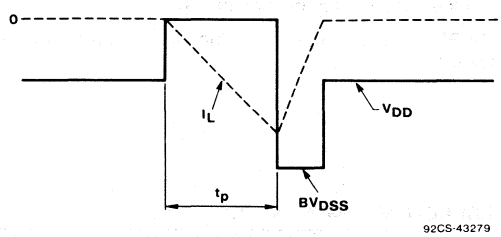


Fig. 16 - Unclamped Inductive Waveforms

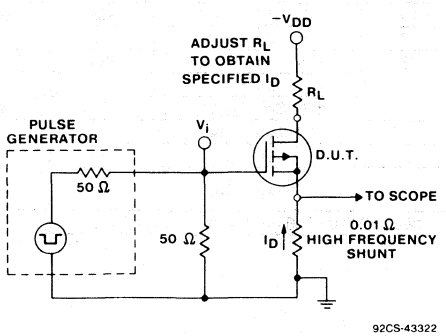


Fig. 17 - Switching Time Test Circuit

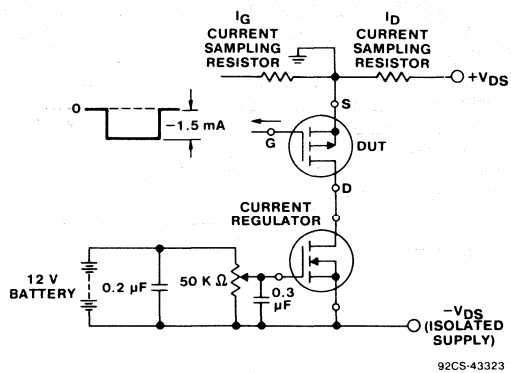


Fig. 18 - Gate Charge Test Circuit

IRF9140, IRF9141
IRF9142, IRF9143

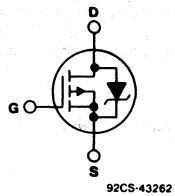
File Number **2278**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-19 A and -15 A, -60 V and -100 V
$r_{DS(on)}$ = 0.20 Ω and 0.30 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

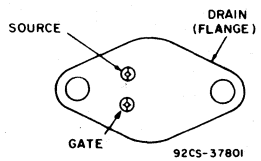


P-CHANNEL ENHANCEMENT MODE

The IRF9140, IRF9141, IRF9142, and IRF9143 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

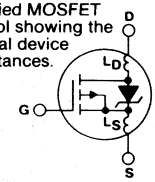
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF9140	IRF9141	IRF9142	IRF9143	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current	I_D @ T_C = 25°C	-19	-19	-15	-15	A
Continuous Drain Current	I_D @ T_C = 100°C	-12	-12	-10	-10	A
Pulsed Drain Current ③	I_{DM}	-76	-76	-60	-60	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	125 (See Fig. 14)				W
Linear Derating Factor		1 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	960				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

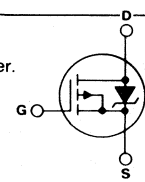
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9140 IRF9142	-100	—	—	V	V_{GS} = 0 V
		IRF9141 IRF9143	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRF9140 IRF9141	-19	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRF9142 IRF9143	-15	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRF9140 IRF9141	—	0.15	0.20	Ω	V_{GS} = 10 V, I_D = -10 A
		IRF9142 IRF9143	—	0.22	0.30	Ω	
Forward Transconductance ②	g_{fs}	ALL	5	7	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = -10 A
Input Capacitance	C_{iss}	ALL	—	1100	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	550	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	250	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	16	20	ns	V_{DD} = 50 V, I_D = -18 A, Z_O = 9.1 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	65	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	47	70	ns	
Fall Time	t_f	ALL	—	28	90	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	70	90	nC	V_{GS} = -15 V, I_D = -24 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	14	21	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	56	84	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	30	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9140 IRF9141	—	—	-19	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9142 IRF9143	—	—	-15	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9140 IRF9141	—	—	-76	A	
		IRF9142 IRF9143	—	—	-60	A	
Diode Forward Voltage ②	V_{SD}	IRF9140 IRF9141	—	—	-1.5	V	T_C = 25°C, I_S = -19 A, V_{GS} = 0 V
		IRF9142 IRF9143	—	—	-1.5	V	T_C = 25°C, I_S = -15 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	170	—	ns	T_J = 150°C, I_F = -19 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.8	—	μC	T_J = 150°C, I_F = -19 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25 V, Starting T_j = 25°C, L = 4 mH, R_G = 25 Ω, Peak I_L = 19 A (See Figs. 15 & 16).

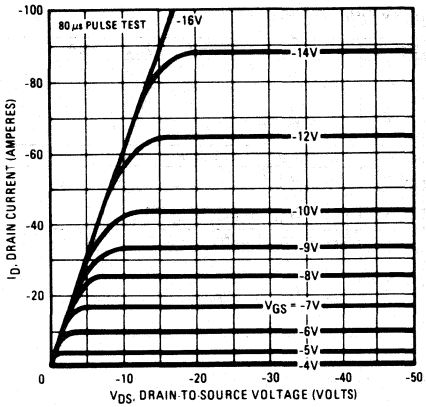


Fig. 1 - Typical output characteristics.

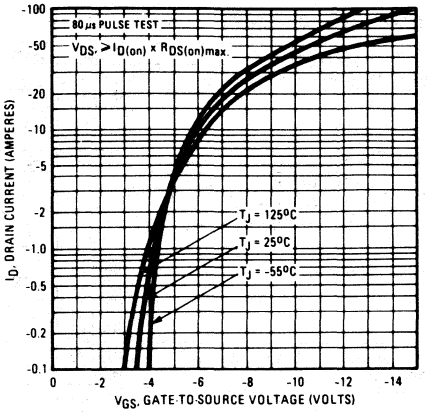


Fig. 2 - Typical transfer characteristics.

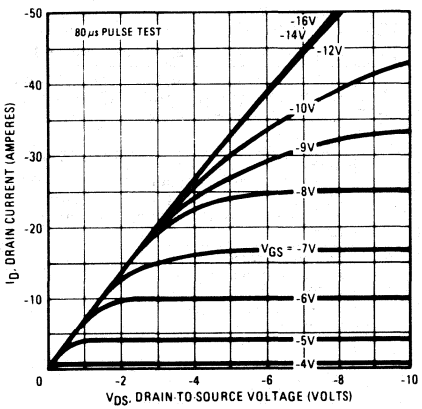


Fig. 3 - Typical saturation characteristics.

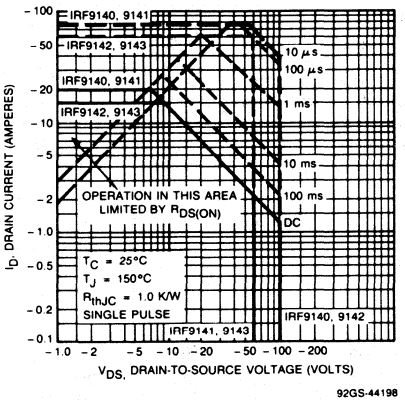


Fig. 4 - Maximum safe operating area.

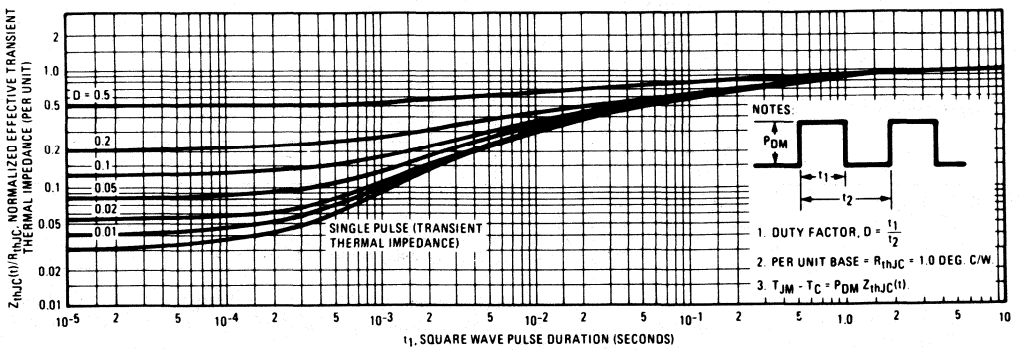


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

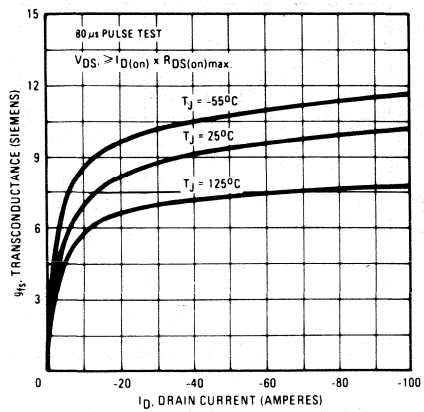


Fig. 6 - Typical transconductance vs. drain current.

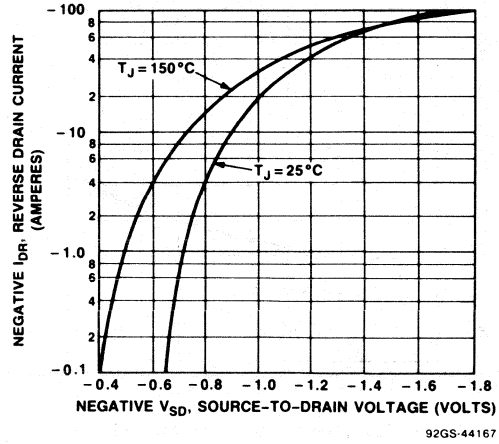


Fig. 7 - Typical source-drain diode forward voltage.

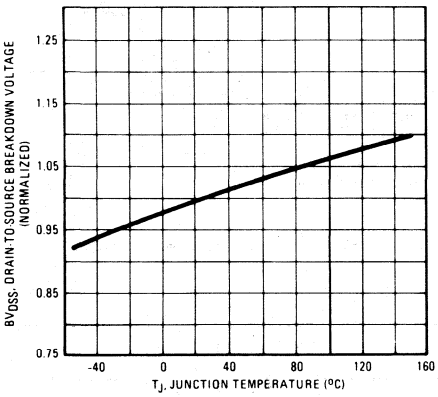


Fig. 8 - Breakdown voltage vs. temperature.

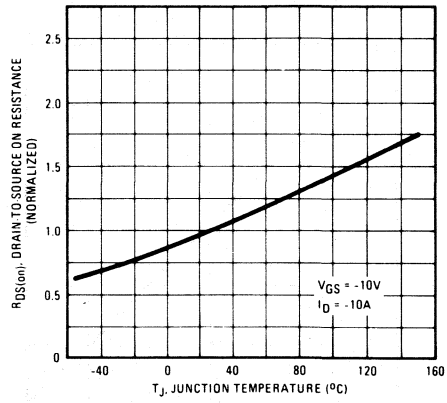


Fig. 9 - Normalized on-resistance vs. temperature.

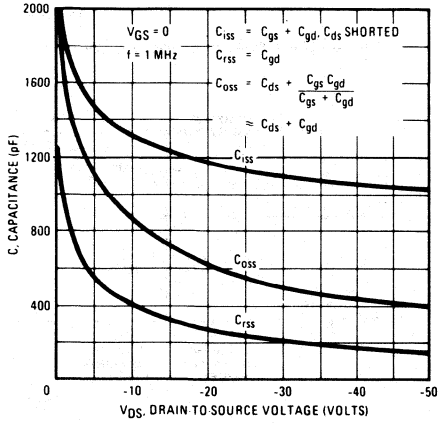


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

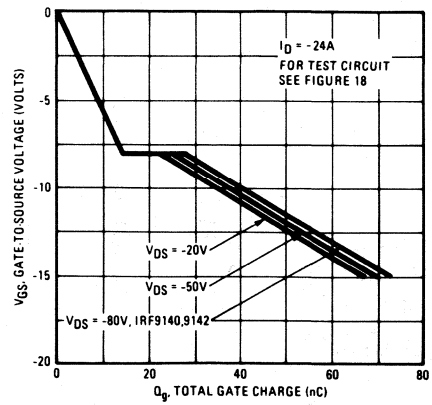


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

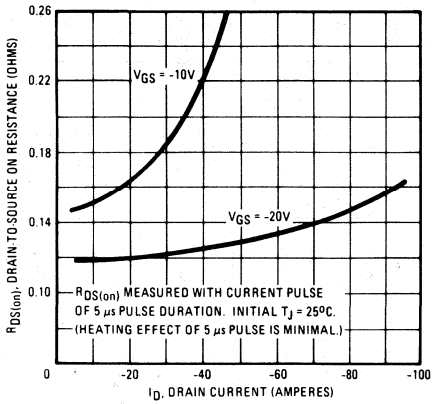


Fig. 12 - Typical on-resistance vs. drain current.

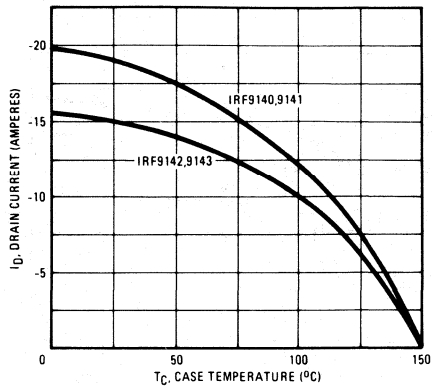


Fig. 13 - Maximum drain current vs. case temperature.

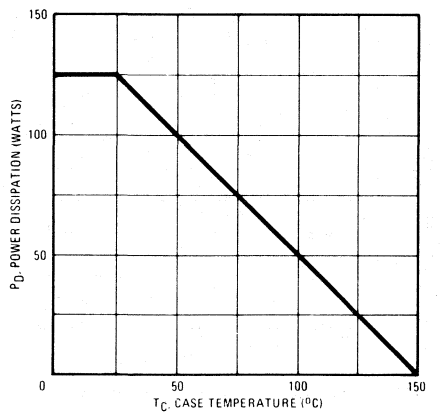


Fig. 14 - Power vs. temperature derating curve.

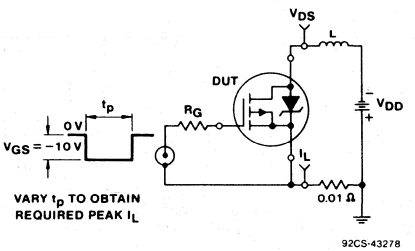


Fig. 15 - Unclamped inductive test circuit.

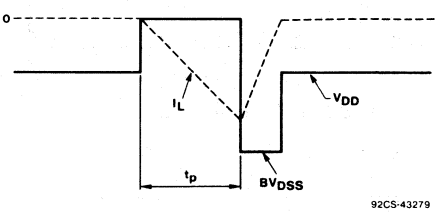


Fig. 16 - Unclamped inductive waveforms.

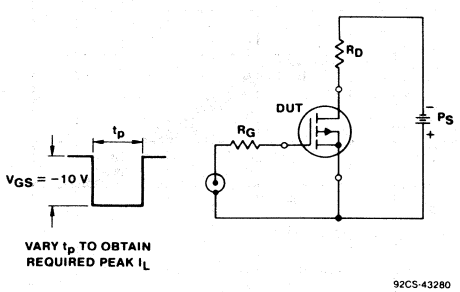


Fig. 17 - Switching time test circuit.

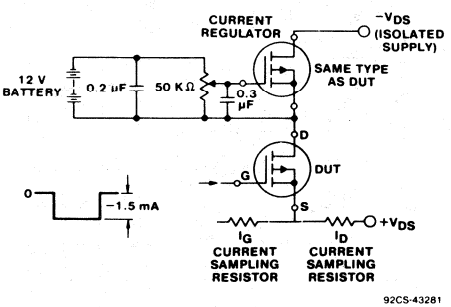


Fig. 18 - Gate charge test circuit.

File Number **2280**

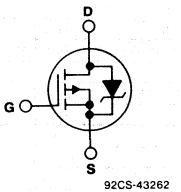
IRF9150, IRF9151

Power MOS Field-Effect Transistors P-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 60 V and 100 V
$r_{DS(on)}$ = 0.150 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *Extreme device ruggedness*
- *Low on resistance*
- *High transconductance*
- *High input impedance*

P-CHANNEL ENHANCEMENT MODE



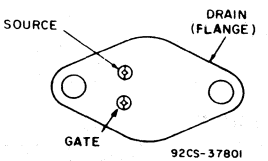
TERMINAL DIAGRAM

The IRF9150 and IRF9151 are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRF9150 is an approximate electrical complement to the N-channel IRF150.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

TERMINAL DESIGNATION



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

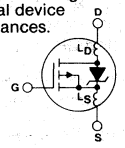
		IRF9150		IRF9151	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-100		-60	V
CONTINUOUS DRAIN CURRENT @ T_C = 25°C	I_D		-25		A
CONTINUOUS DRAIN CURRENT @ T_C = 100°C	I_D		-18		A
PULSE DRAIN CURRENT	I_{DM}		-100		A
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
MAX. POWER DISSIPATION @ T_C = 25°C	P_D		150 (See Fig. 18)		W
LINEAR DERATING FACTOR			1.2		W/°C
SINGLE-PULSE AVALANCHE ENERGY ③	E_{as}		1300 (See Fig. 14)		mJ
AVALANCHE CURRENT (REPETITIVE OR NONREPETITIVE)	I_{AR}		-25		A
OPERATING JUNCTION AND	T_J				°C
STORAGE TEMPERATURE RANGE	T_{stg}		-55 to +150		°C
LEAD TEMPERATURE (0.063 in. [1.6mm] from case for 10 s)			300		°C

IRFP9150, IRFP9151

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTICS		LIMITS TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9150	-100	—	—	V	V_{GS} = 0 V
		IRF9151	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	All	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	All	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	All	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	All	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_J = 125°C
On-State Drain Current ①	$I_{D(on)}$	All	-25	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$ V_{GS} = 10 V
Static Drain-Source On-State Resistance ①	$r_{DS(on)}$	All	—	0.09	0.15	Ω	V_{GS} = -10 V, I_D = -10 A
Forward Transconductance ①	g_{fs}	All	4	10	—	S	V_{DS} = -10 V, I_D = -12.5 A
Input Capacitance	C_{iss}	All	—	2400	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	All	—	850	—	pF	
Reverse Transfer Capacitance	C_{rss}	All	—	400	—	pF	
Turn-On Delay Time	$t_{d(on)}$	All	—	16	24	ns	V_{DD} = -50 V, I_D = -25 A R_G = 6.8 Ω, R_D = 2 Ω See Figs. 16 and 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	All	—	110	160	ns	
Turn-Off Delay Time	$t_{d(off)}$	All	—	65	100	ns	
Fall Time	t_f	All	—	46	70	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	All	—	82	120	nC	V_{GS} = -10 V, I_D = -25 A, V_{DS} = 0.8 Max. Rating. See Figs. 11 and 19 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	All	—	14	21	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	All	—	42	65	nC	
Internal Drain Inductance	L_D	All	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	All	—	13	—	nH	Measured from the source pin, 6mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

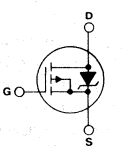


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	All	—	—	0.83	°C/W	
Case-to-Sink	$R_{\theta CS}$	All	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased
Junction-to-Ambient	$R_{\theta JA}$	All	—	—	30	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode) ②	I_S	All	—	—	-25	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
Pulse Source Current (Body Diode) ③	I_{SM}	All	—	—	-100	A	
Diode Forward Voltage ②	V_{SD}	All	—	0.9	1.5	V	T_J = 25°C, I_S = 25 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	All	—	150	300	ns	T_J = 25°C, I_F = 25 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	All	0.30	0.70	1.5	μC	T_J = 25°C, I_F = 25 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	All	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
② Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
③ V_{DD} = 25 V, Starting T_J = 25°C, L = 3.2 mhy, I_{peak} = 25 A, R_{gs} = 25 Ω (See Figs. 14 & 15).

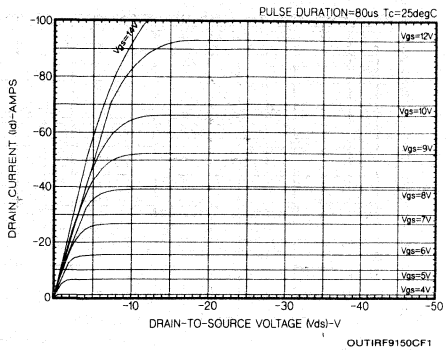


Fig. 1 - Typical output characteristics.

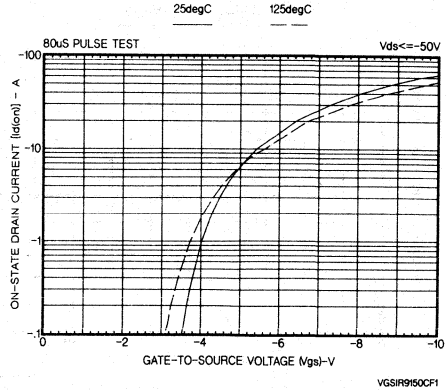


Fig. 2 - Typical transfer characteristics.

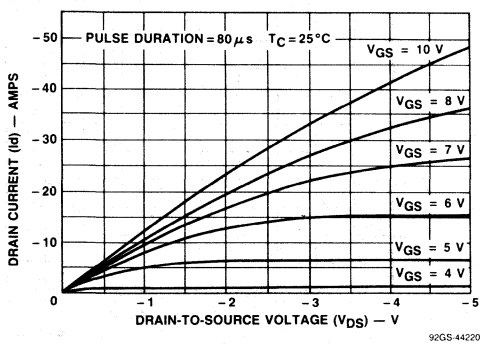


Fig. 3- Typical saturation characteristics.

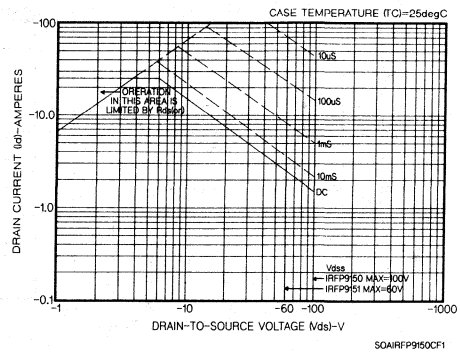


Fig. 4 - Maximum safe operating area.

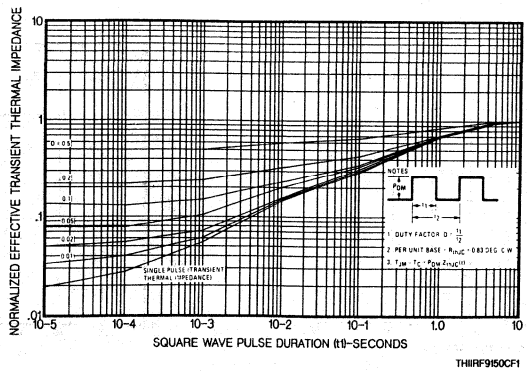


Fig. 5 - Maximum effective transient thermal impedance.

IRFP9150, IRFP9151

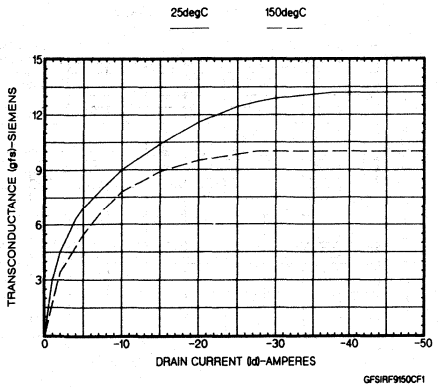


Fig. 6 - Typical transconductance vs. drain current.

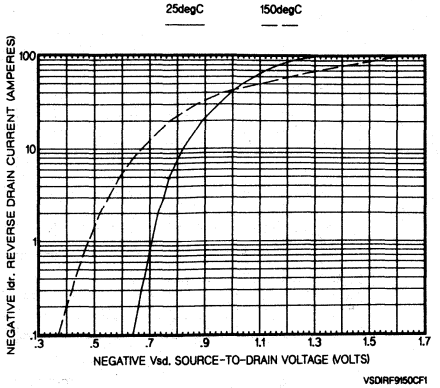


Fig. 7 - Typical source-drain diode forward voltage.

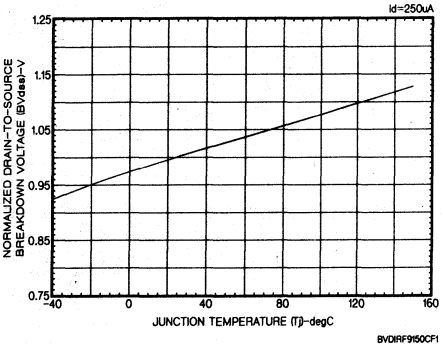


Fig. 8 - Normalized breakdown voltage vs. temperature.

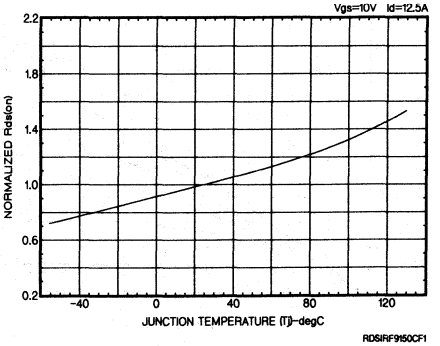


Fig. 9 - Normalized on-resistance vs. temperature.

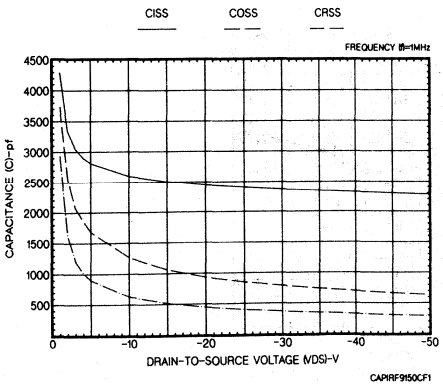


Fig. 10 - Typical capacitance vs. drain-to source voltage.

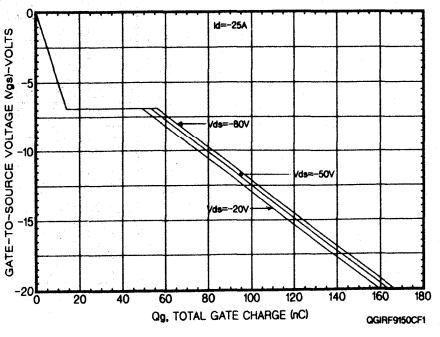


Fig. 11 - Typical gate charge vs. gate-to source voltage.

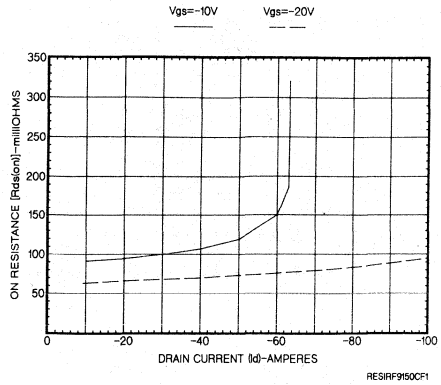


Fig. 12 - Typical on-resistance vs. drain current.

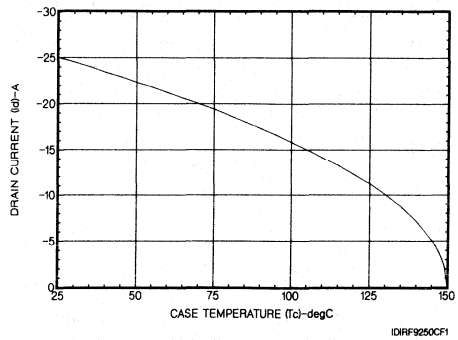


Fig. 13 - Maximum drain current vs. case temperature.

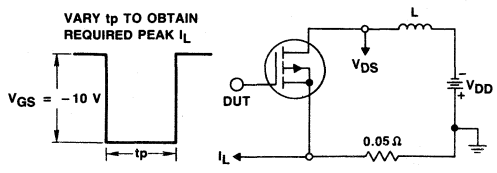


Fig. 14 - Unclamped inductive test circuit.

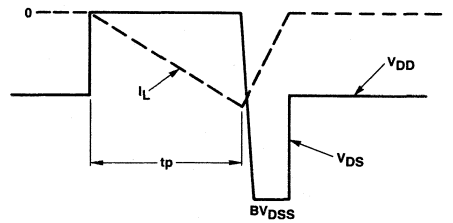


Fig. 15 - Unclamped inductive waveforms.

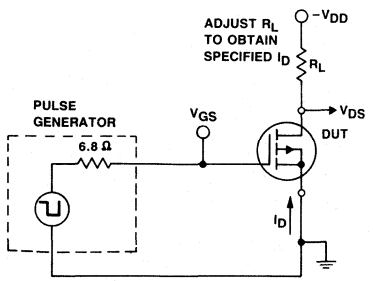


Fig. 16 - Switching time test circuit.

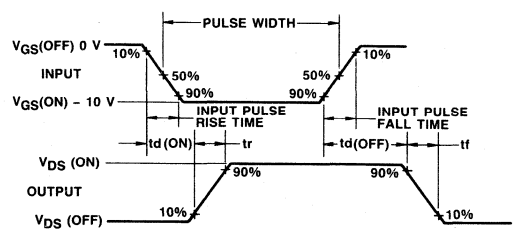


Fig. 17 - Switching time waveforms.

IRFP9150, IRFP9151

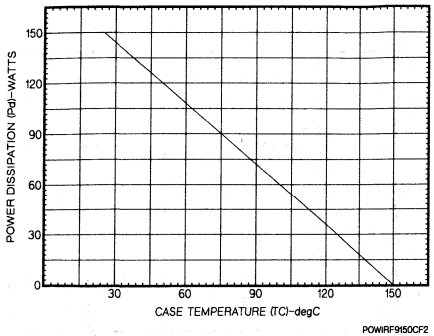


Fig. 18 - Power vs. temperature derating curve.

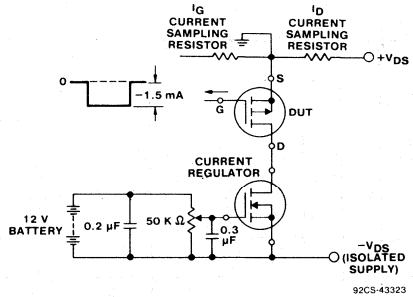


Fig. 19 - Gate charge test circuit.

File Number **2226**

IRF9230, IRF9231, IRF9232, IRF9233

Avalanche-Energy-Rated P-Channel Power MOSFETs

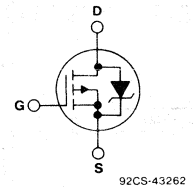
-5.5 A and -6.5 A, -150 V and -200 V
$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

The IRF9230, IRF9231, IRF9232 and IRF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

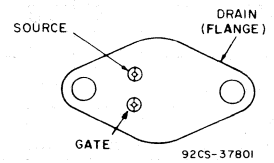
The IRF-types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA

ABSOLUTE-MAXIMUM RATINGS

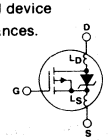
CHARACTERISTIC		IRF9230	IRF9231	IRF9232	IRF9233	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-6.5	-6.5	-5.5	-5.5	A
Continuous Drain Current	I_D @ T_C = 100°C	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current ③	I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	75 (See Fig. 14)				W
Linear Derating Factor		0.6 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	500				mj
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. (1.6 mm) from case for 10s)				°C

IRF9230, IRF9231, IRF9232, IRF9233

ELECTRICAL CHARACTERISTICS, At T_C = 25°C (Unless Otherwise Specified)

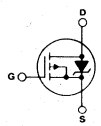
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9230, IRF9232	-200	—	—	V	V_{GS} = 0 V
		IRF9231, IRF9233	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS}(th)$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_D(on)$	IRF9230, IRF9231	-6.5	—	—	A	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., V_{GS} = -10 V
		IRF9232, IRF9233	-5.5	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS}(on)$	IRF9230, IRF9231	—	0.5	0.8	Ω	V_{GS} = -10 V, I_D = -3.5 A
		IRF9232, IRF9233	—	0.8	1.2	Ω	
Forward Transconductance ②	g_{fs}	ALL	2.2	3.5	—	S (℧)	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., I_D = -3.5 A
Input Capacitance	C_{iss}	ALL	—	550	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	170	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	—	pF	
Turn-On Delay Time	$t_d(on)$	ALL	—	30	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -3.5 A, Z_O = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_d(off)$	ALL	—	50	100	ns	
Fall Time	t_f	ALL	—	40	80	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	31	45	nC	V_{GS} = -15 V, I_D = -8.0 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	18	26	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	13	19	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1.67	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	30	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9230, IRF9231	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9232, IRF9233	—	—	-5.5	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9230, IRF9231	—	—	-26	A	
		IRF9232, IRF9233	—	—	-22	A	
Diode Forward Voltage ②	V_{SD}	IRF9230, IRF9231	—	—	-1.5	V	T_C = 25°C, I_S = -6.5 A, V_{GS} = 0 V
		IRF9232, IRF9233	—	—	-1.5	V	T_C = 25°C, I_S = -5.5 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	400	—	ns	T_J = 150°C, I_F = -6.5 A, di_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	2.6	—	μC	T_J = 150°C, I_F = -6.5 A, di_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs. Duty Cycle ≤ 2%

③ Repetitive Rating: Pulse width limited by max. junction temperature See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50 V, Starting T_J = 25°C, L = 17.75 mH, R_G = 25 Ω, Peak I_L = 6.5 A (See Figs. 15 & 16).

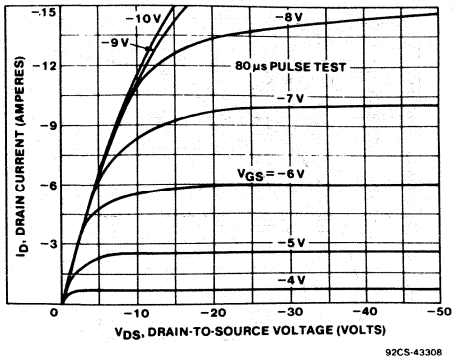


Fig. 1 - Typical output characteristics.

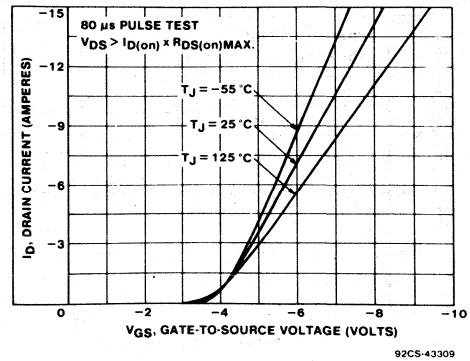


Fig. 2 - Typical transfer characteristics.

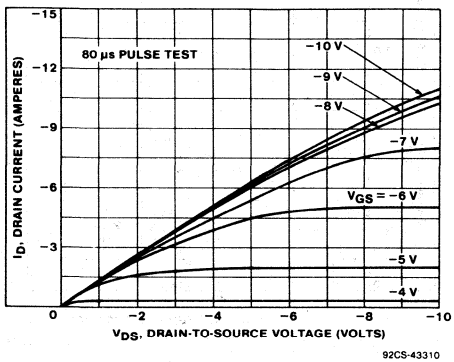


Fig. 3 - Typical saturation characteristics.

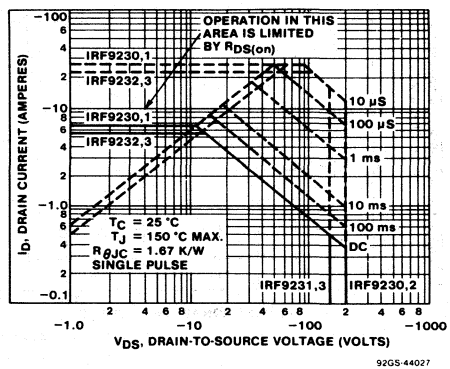


Fig. 4 - Maximum safe operating area.

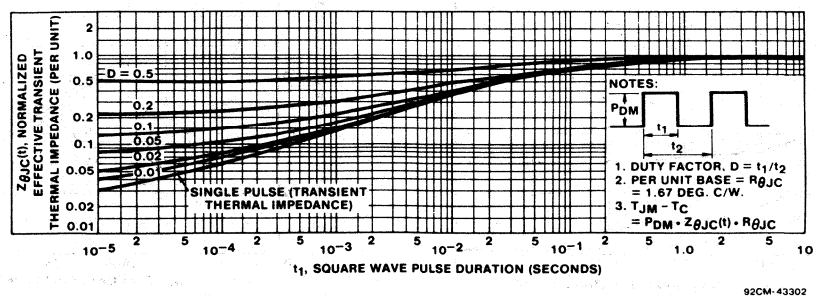


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

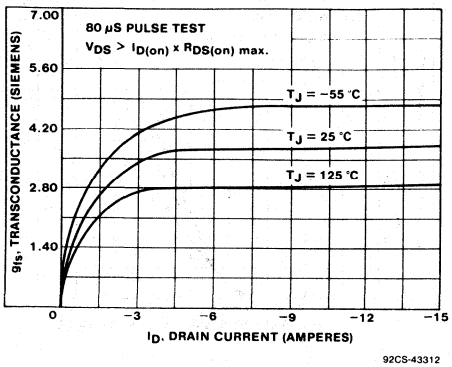


Fig. 6 - Typical transconductance vs. drain current.

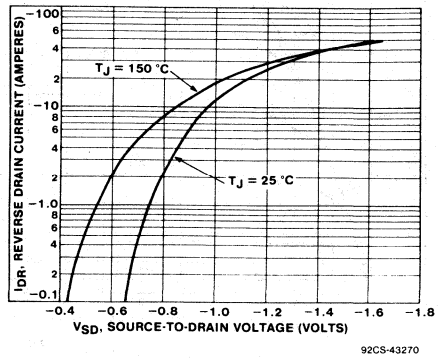


Fig. 7 - Typical source-drain diode forward voltage.

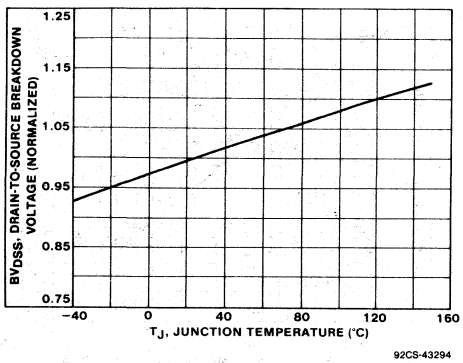


Fig. 8 - Breakdown voltage vs. temperature.

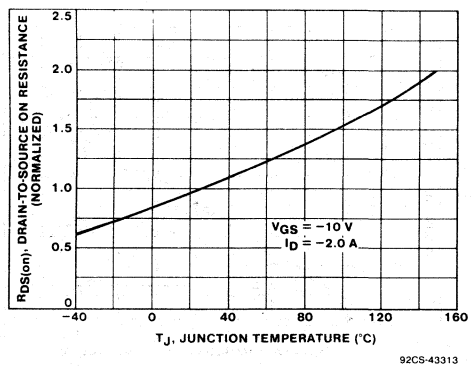


Fig. 9 - Normalized on-resistance vs. temperature.

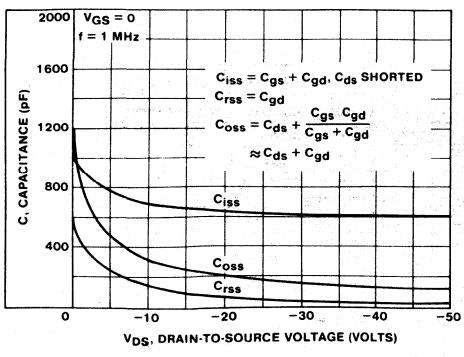


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

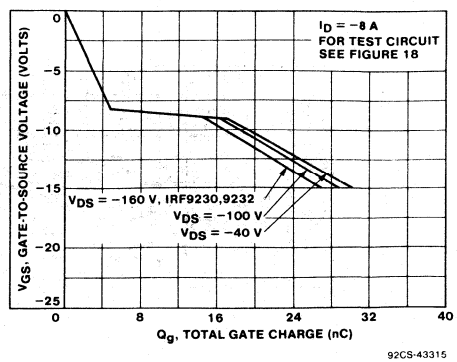


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

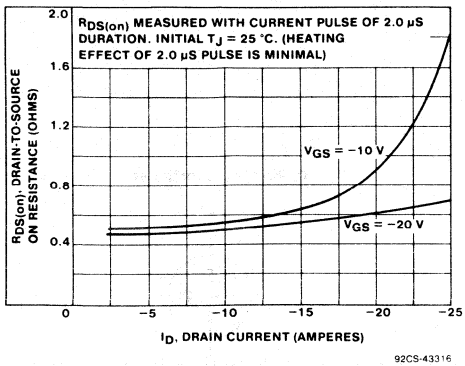


Fig. 12 - Typical on-resistance vs. drain current.

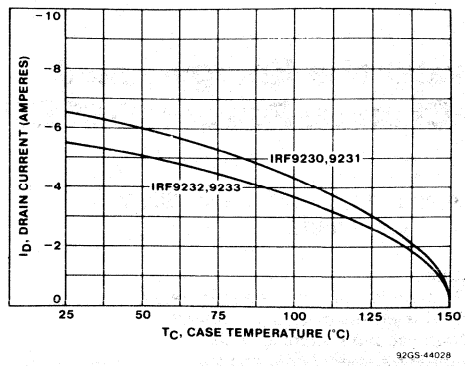


Fig. 13 - Maximum drain current vs. case temperature.

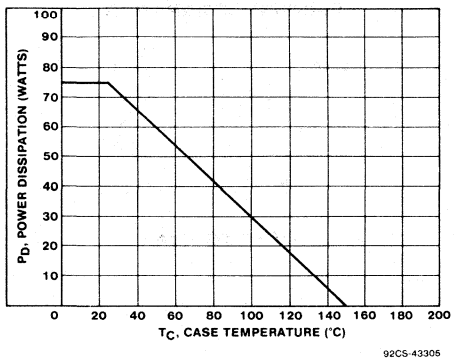


Fig. 14 - Power vs. temperature derating curve.

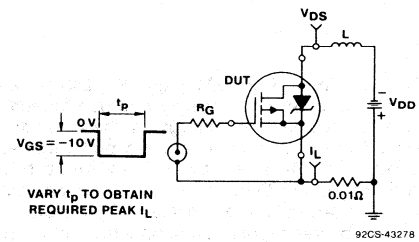


Fig. 15 - Unclamped inductive test circuit.

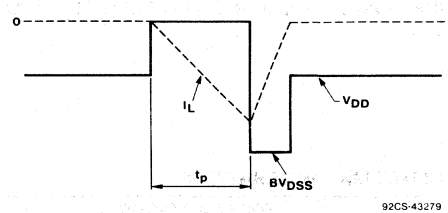


Fig. 16 - Unclamped inductive waveforms.

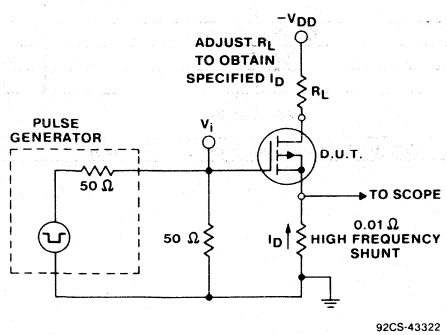


Fig. 17 - Switching time test circuit.

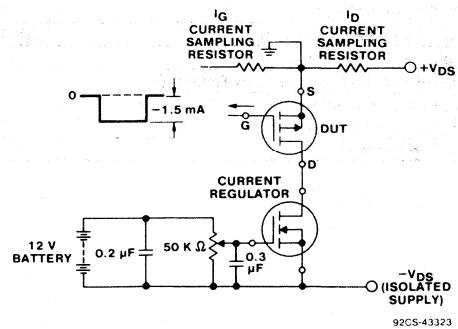


Fig. 18 - Gate charge test circuit.

IRF9240, IRF9241
IRF9242, IRF9243

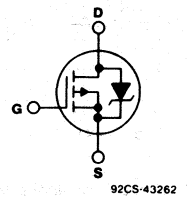
File Number **2279**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-9 A and -11 A, -150 V and -200 V
$r_{DS(on)}$ = 0.5 Ω and 0.7 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

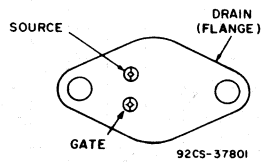


P-CHANNEL ENHANCEMENT MODE

The IRF9240, IRF9241, IRF9242, and IRF9243 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

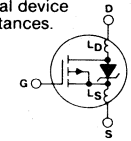
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF9240	IRF9241	IRF9242	IRF9243	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-11	-11	-9	-9	A
Continuous Drain Current	I_D @ T_C = 100°C	-7	-7	-6	-6	A
Pulsed Drain Current ③	I_{DM}	-44	-44	-36	-36	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	125 (See Fig. 14)				W
Linear Derating Factor		1 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	790				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

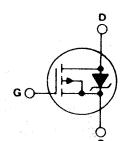
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9240 IRF9242	-200	—	—	V	V_{GS} = 0 V
		IRF9241 IRF9243	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRF9240 IRF9241	-11	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRF9242 IRF9243	-9	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRF9240 IRF9241	—	0.35	0.5	Ω	V_{GS} = 10 V, I_D = -6 A
		IRF9242 IRF9243	—	0.55	0.7	Ω	
Forward Transconductance ②	g_{fs}	ALL	4	6	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = -6 A
Input Capacitance	C_{iss}	ALL	—	1100	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	375	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	150	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	18	22	ns	V_{DD} = 100 V, I_D = -11 A, Z_O = 9.1 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	45	68	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	75	90	ns	
Fall Time	t_f	ALL	—	29	44	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	70	90	nC	V_{GS} = -15 V, I_D = -11 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	55	83	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	15	23	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	30	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9240 IRF9241	—	—	-11	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9242 IRF9243	—	—	-9	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9240 IRF9241	—	—	-44	A	
		IRF9242 IRF9243	—	—	-36	A	
Diode Forward Voltage ②	V_{SD}	IRF9240 IRF9241	—	—	-1.5	V	T_C = 25°C, I_S = -11 A, V_{GS} = 0 V
		IRF9242 IRF9243	—	—	-1.5	V	T_C = 25°C, I_S = -9 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	270	—	ns	T_J = 150°C, I_F = -11 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	2	—	μC	T_J = 150°C, I_F = -11 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_j = 25°C, L = 9.8 mH, R_G = 25 Ω, Peak I_L = 11 A (See Figs. 15 & 16).

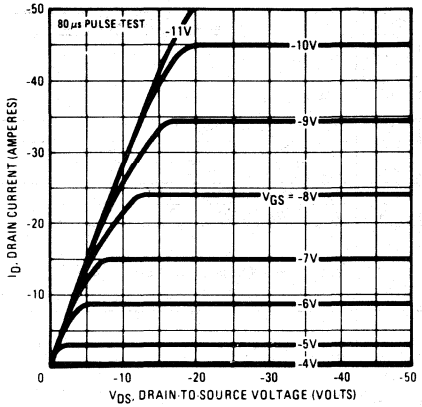


Fig. 1 - Typical output characteristics.

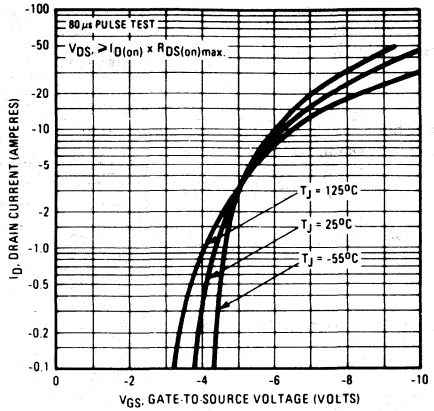


Fig. 2 - Typical transfer characteristics.

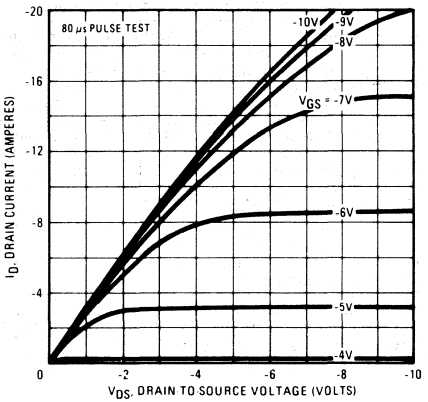


Fig. 3 - Typical saturation characteristics.

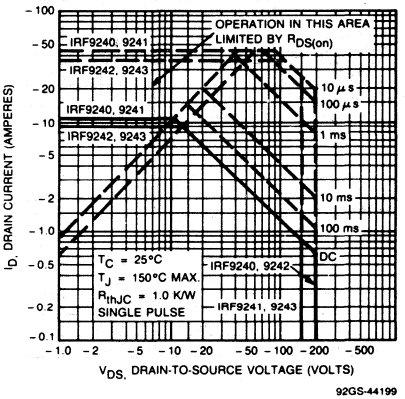


Fig. 4 - Maximum safe operating area.

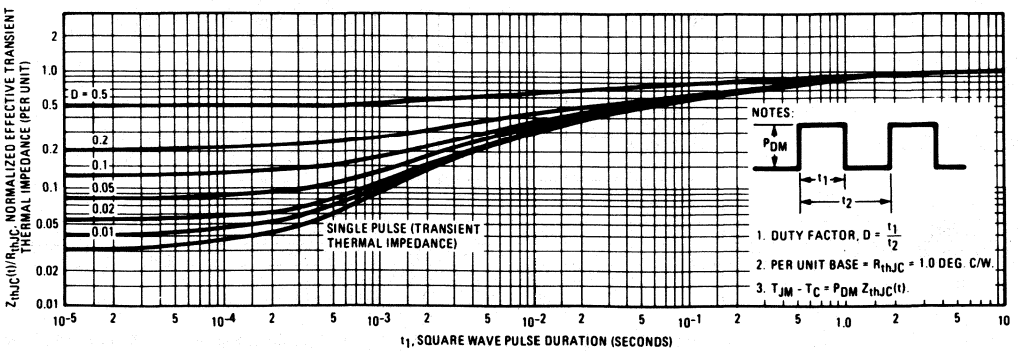


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

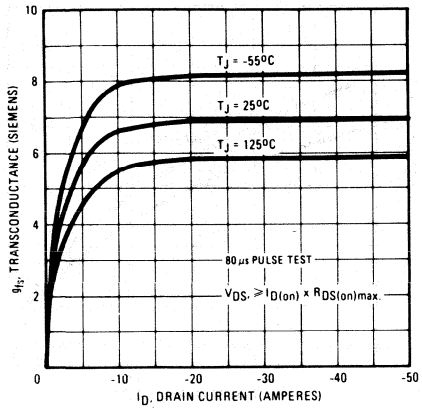


Fig. 6 - Typical transconductance vs. drain current.

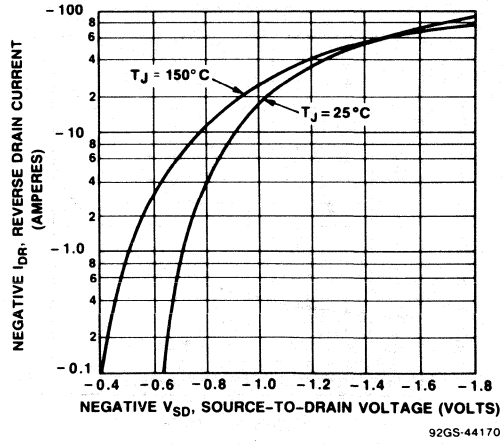


Fig. 7 - Typical source-drain diode forward voltage.

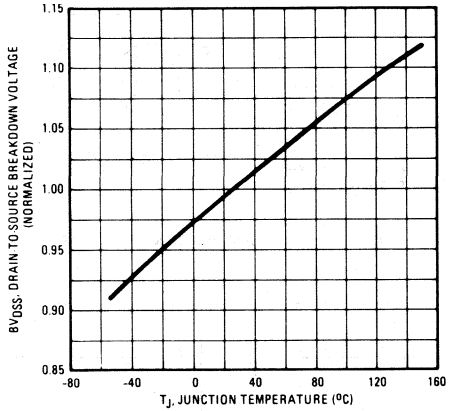


Fig. 8 - Breakdown voltage vs. temperature.

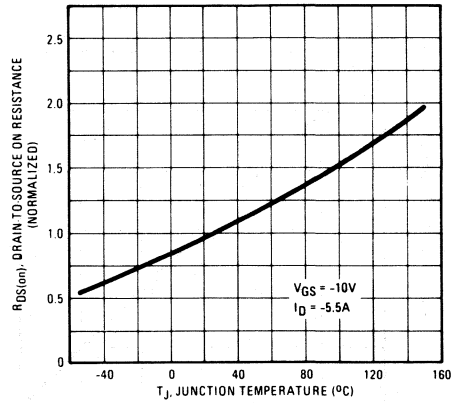


Fig. 9 - Normalized on-resistance vs. temperature.

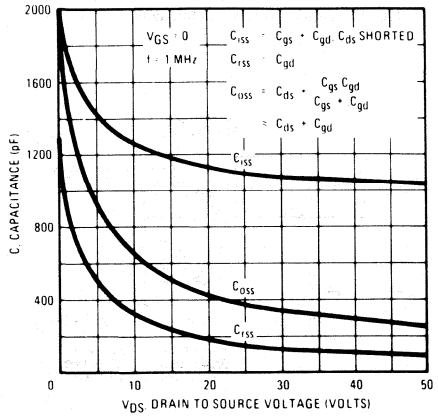


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

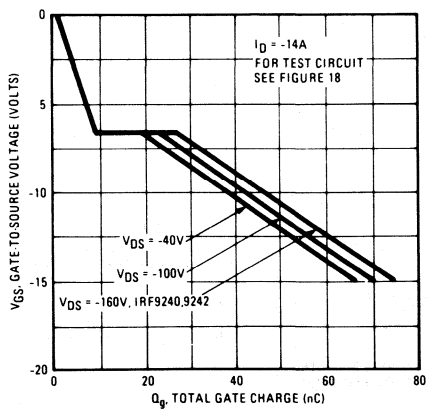


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

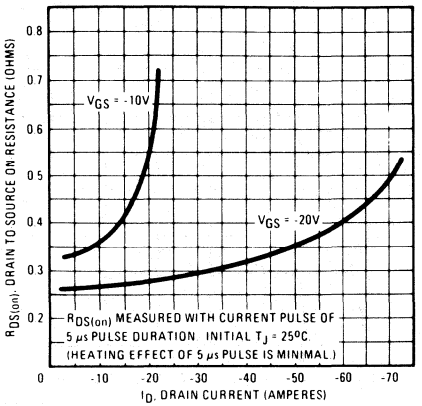


Fig. 12 - Typical on-resistance vs. drain current.

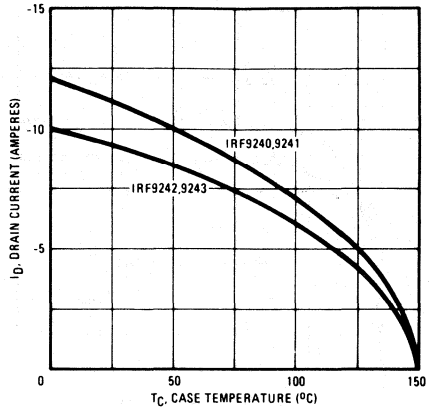


Fig. 13 - Maximum drain current vs. case temperature.

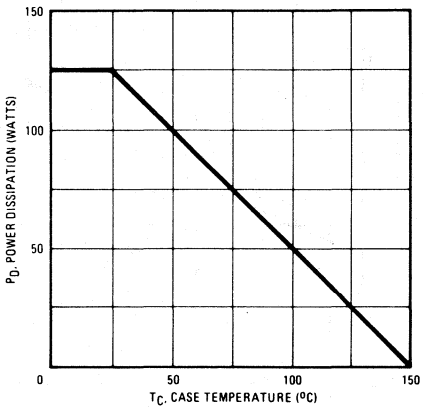


Fig. 14 - Power vs. temperature derating curve.

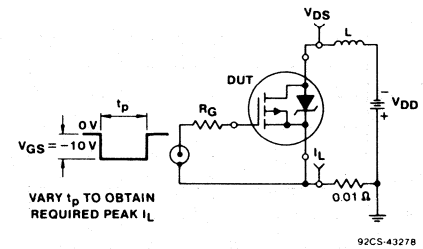


Fig. 15 - Unclamped inductive test circuit.

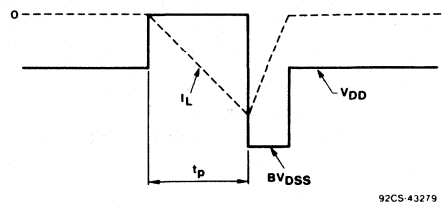


Fig. 16 - Unclamped inductive waveforms.

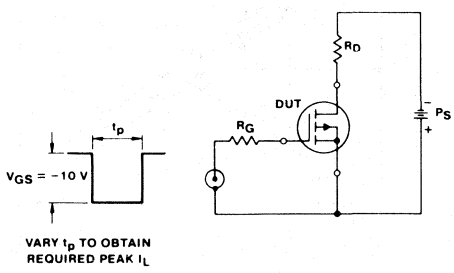


Fig. 17 - Switching time test circuit.

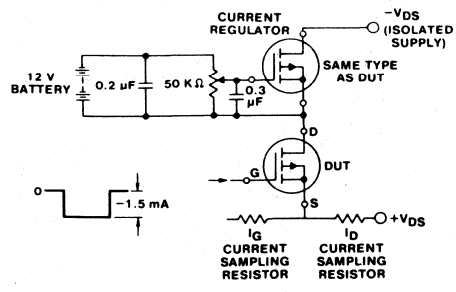


Fig. 18 - Gate charge test circuit.

File Number **2214**

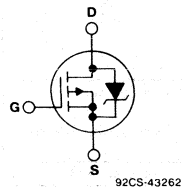
IRF9510, IRF9511
IRF9512, IRF9513

Avalanche-Energy-Rated P-Channel Power MOSFETs

-2.5A, and -3.0A, -60V and -100V
$r_{DS(on)}$ = 1.2Ω and 1.6Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

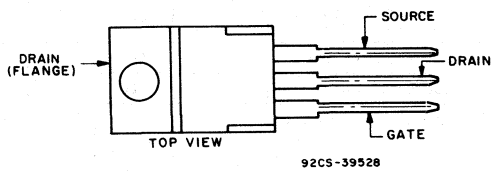


P-CHANNEL ENHANCEMENT MODE

The IRF9510, IRF9511, IRF9512 and IRF9513 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-220AB

Absolute Maximum Ratings

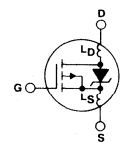
Parameter		IRF9510	IRF9511	IRF9512	IRF9513	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-3.0	-3.0	-2.5	-2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	-2.0	-2.0	-1.5	-1.5	A
I_{DM}	Pulsed Drain Current ③	-12	-12	-10	-10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
E_{AS}	Single Pulse Avalanche Energy ④	190				mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF9510, IRF9511, IRF9512, IRF9513

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9510 IRF9512	-100	–	–	V	V_{GS} = 0V
		IRF9511 IRF9513	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	-500	nA	V_{GS} = -20V
I_{GDS}	Gate - Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9510 IRF9511	-3.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRF9512 IRF9513	-2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9510 IRF9511	–	1.0	1.2	Ω	V_{GS} = -10V, I_D = -1.5A
		IRF9512 IRF9513	–	1.2	1.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.1	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max.}$, I_D = -1.5A
C_{iss}	Input Capacitance	ALL	–	180	—	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	85	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	15	30	ns	V_{DD} ≈ -50V, I_D = -1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	20	40	ns	
t_f	Fall Time	ALL	–	20	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	8.5	11	nC	V_{GS} = -15V, I_D = -4A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	3.8	4.9	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.7	6.1	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

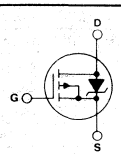


Thermal Resistance

$R_{\theta JC}$	Junction-to-Case	ALL	–	–	6.4	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
$R_{\theta JA}$	Junction-to-Ambient	ALL	–	–	80	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9510 IRF9511	–	–	-3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9512 IRF9513	–	–	-2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9510 IRF9511	–	–	-12	A	
		IRF9512 IRF9513	–	–	-10	A	
V_{SD}	Diode Forward Voltage ②	IRF9510 IRF9511	–	–	-1.5	V	T_C = 25°C, I_S = -3.0A, V_{GS} = 0V
		IRF9512 IRF9513	–	–	-1.5	V	T_C = 25°C, I_S = -2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	120	–	ns	T_J = 150°C, I_F = -3.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.0	–	μC	T_J = 150°C, I_F = -3.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C.

②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 25V, Starting T_J = 25°C, L = 31.7 mH, R_G = 25Ω, Peak I_L = 3.0A, (See Fig. 15 and 16).

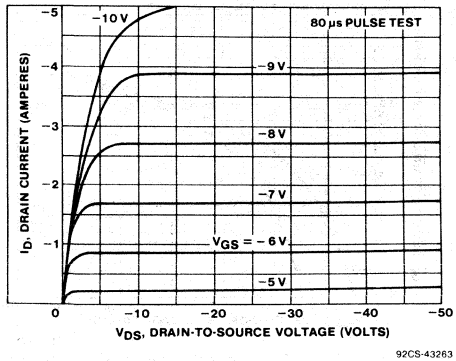


Fig. 1 - Typical Output Characteristics

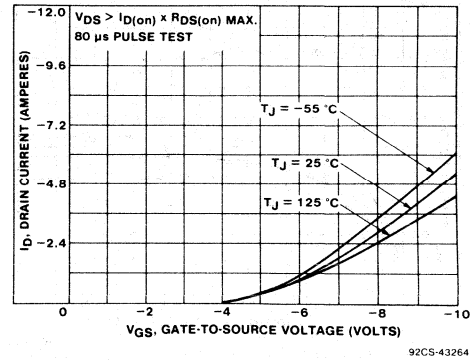


Fig. 2 - Typical Transfer Characteristics

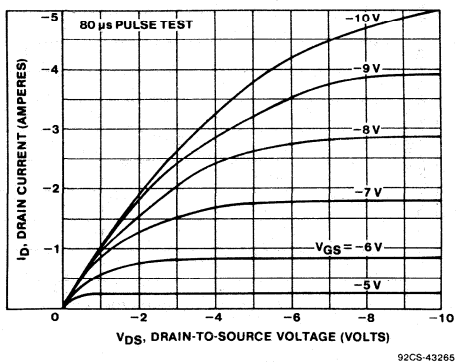


Fig. 3 - Typical saturation characteristic.

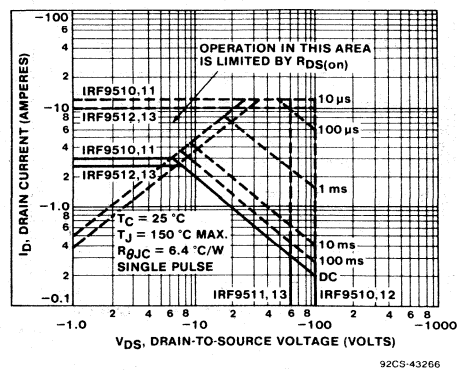


Fig. 4 - Maximum safe operating area.

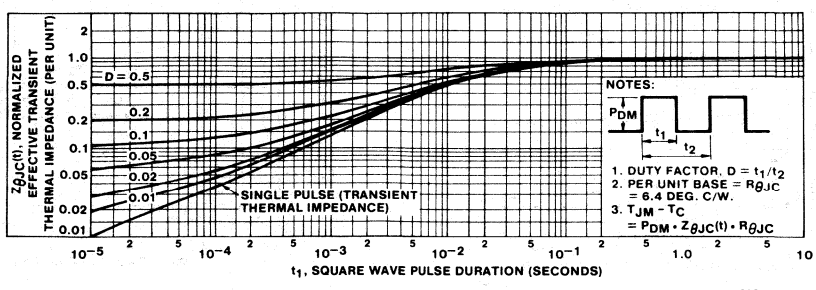


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

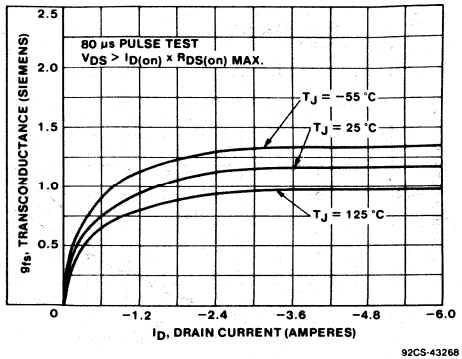


Fig. 6 - Typical transconductance vs. drain current.

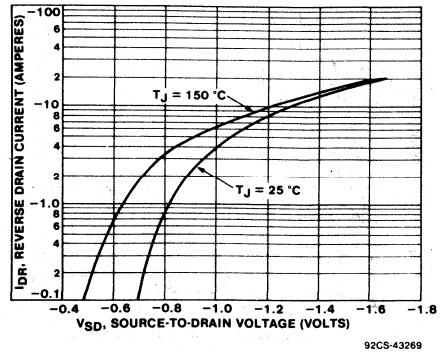


Fig. 7 - Typical source-drain diode forward voltage.

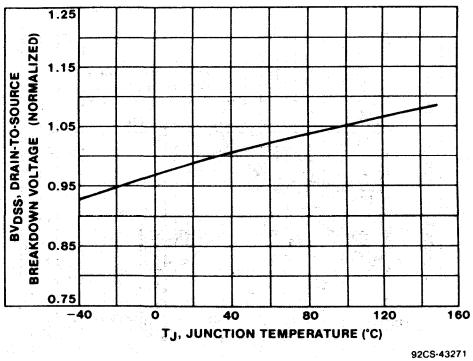


Fig. 8 - Breakdown voltage vs. temperature.

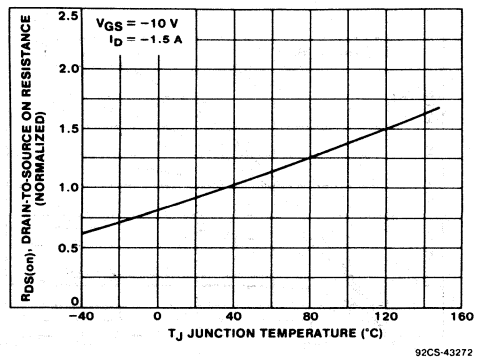


Fig. 9 - Normalized on-resistance vs. temperature.

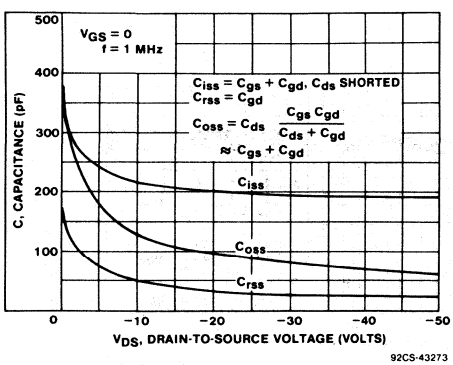


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

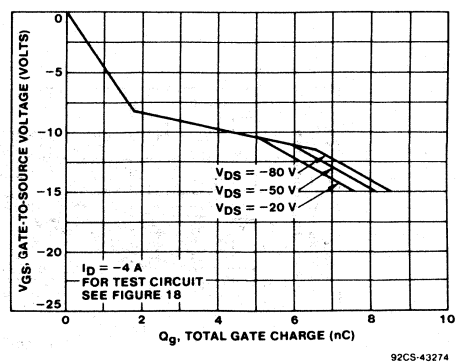


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

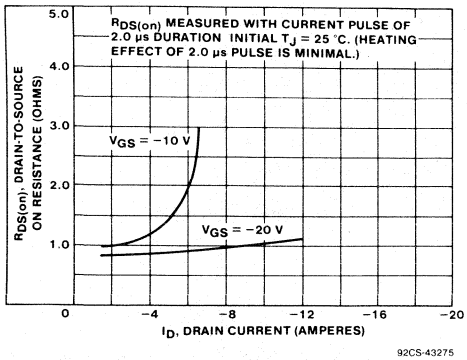


Fig. 12 - Typical on-resistance vs. drain current.

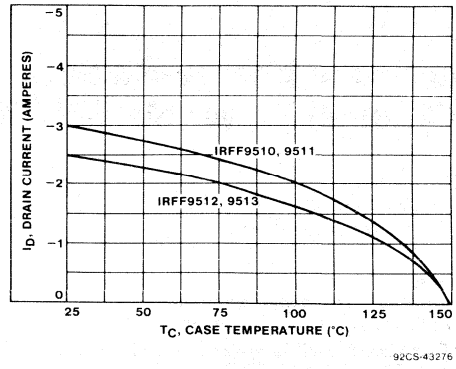


Fig. 13 - Maximum drain current vs. case temperature.

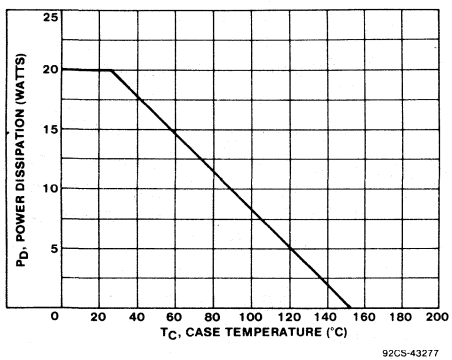


Fig. 14 - Power vs. temperature derating curve.

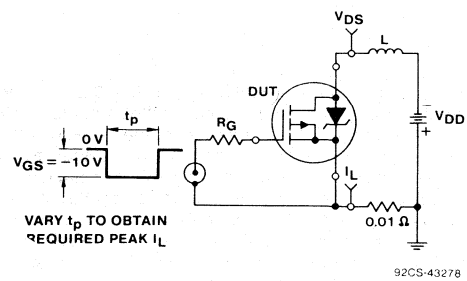


Fig. 15 - Unclamped inductive test circuit.

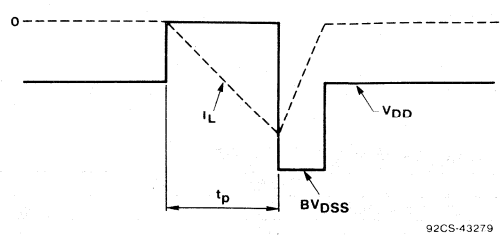


Fig. 16 - Unclamped inductive waveforms.

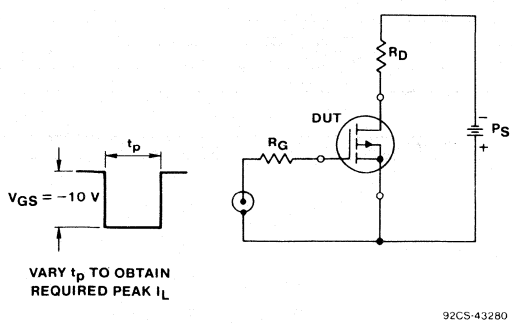


Fig. 17 - Switching time test circuit.

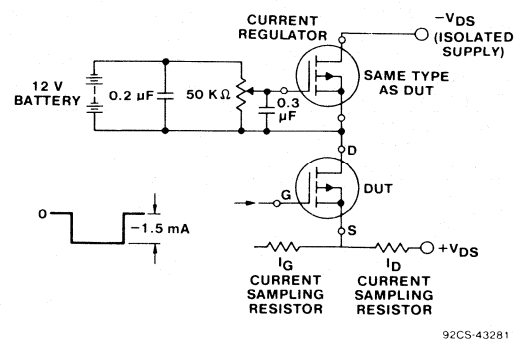


Fig. 18 - Gate charge test circuit.

IRF9520, IRF9521
IRF9522, IRF9523

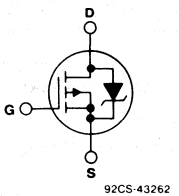
File Number **2281**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-5 A and -6 A, -60 V and -100 V
$r_{DS(on)}$ = 0.60 Ω and 0.80 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



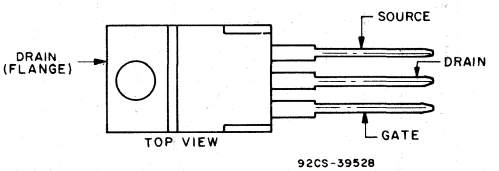
92CS-43262

P-CHANNEL ENHANCEMENT MODE

The IRF9520, IRF9521, IRF9522 and IRF9523 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

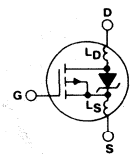
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF9520	IRF9521	IRF9522	IRF9523	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current	I_D @ T_C = 25°C	-6	-6	-5	-5	A
Continuous Drain Current	I_D @ T_C = 100°C	-4	-4	-3.5	-3.5	A
Pulsed Drain Current ③	I_{DM}	-24	-24	-20	-20	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	40 (See Fig. 14)				W
Linear Derating Factor		0.32 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	370				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

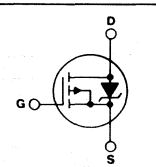
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9520 IRF9522	-100	—	—	V	V_{GS} = 0 V
		IRF9521 IRF9523	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRF9520 IRF9521	-6	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRF9522 IRF9523	-5	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRF9520 IRF9521	—	0.5	0.6	Ω	V_{GS} = 10 V, I_D = -3.5 A
		IRF9522 IRF9523	—	0.6	0.8	Ω	
Forward Transconductance ②	g_{fs}	ALL	0.9	2	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = -3.5 A
Input Capacitance	C_{iss}	ALL	—	300	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	200	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	25	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -3.5 A, Z_O = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	50	100	ns	
Fall Time	t_f	ALL	—	50	100	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	22	nC	V_{GS} = -15 V, I_D = -8.0 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	9	13.5	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	7	10.5	nC	
Internal Drain Inductance	L_D	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	**Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.**
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	3.12	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9520 IRF9521	—	—	-6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9522 IRF9523	—	—	-5	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9520 IRF9521	—	—	-24	A	
		IRF9522 IRF9523	—	—	-20	A	
Diode Forward Voltage ②	V_{SD}	IRF9520 IRF9521	—	—	-1.5	V	T_C = 25°C, I_S = -6 A, V_{GS} = 0 V
		IRF9522 IRF9523	—	—	-1.5	V	T_C = 25°C, I_S = -5 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	230	—	ns	T_J = 150°C, I_F = -6 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	1.3	—	μC	T_J = 150°C, I_F = -6 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25 V, Starting T_j = 25°C, L = 15.4 mH, R_G = 25 Ω, Peak I_L = 6 A (See Figs. 15 & 16).

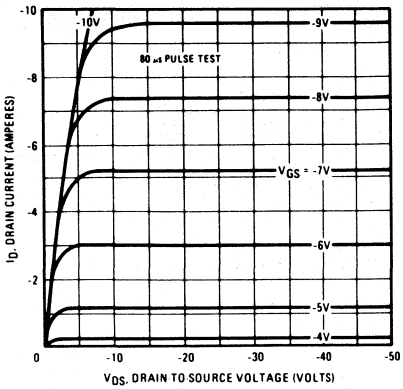


Fig. 1 - Typical output characteristics.

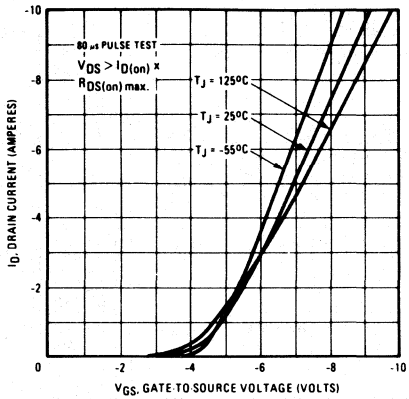


Fig. 2 - Typical transfer characteristics.

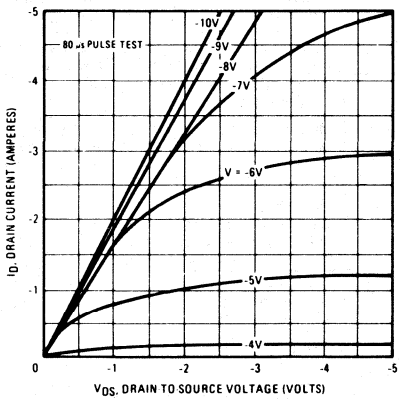


Fig. 3 - Typical saturation characteristics.

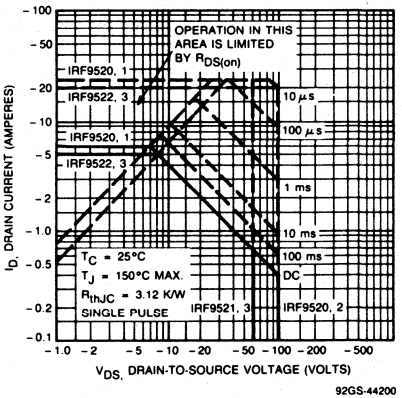
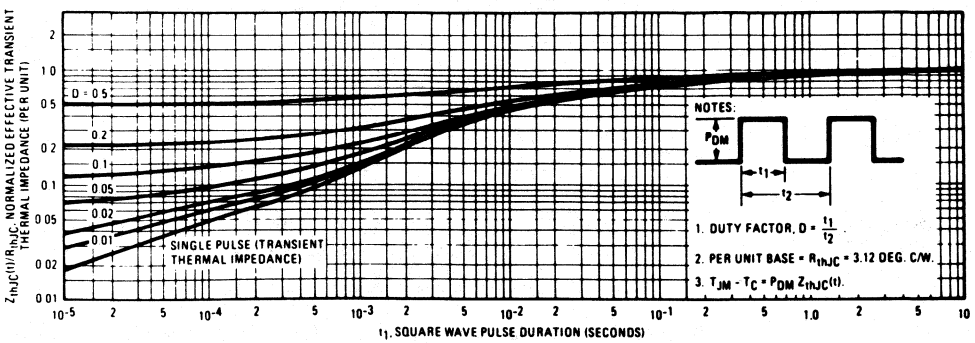


Fig. 4 - Maximum safe operating area.



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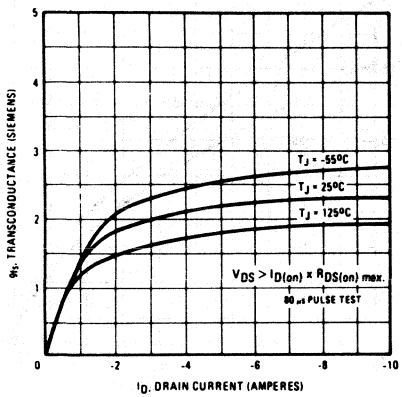


Fig. 6 - Typical transconductance vs. drain current.

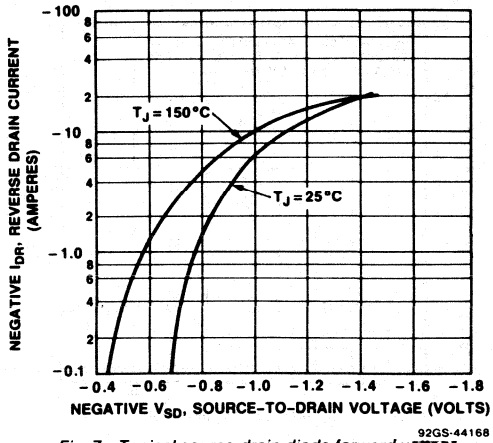


Fig. 7 - Typical source-drain diode forward voltage.

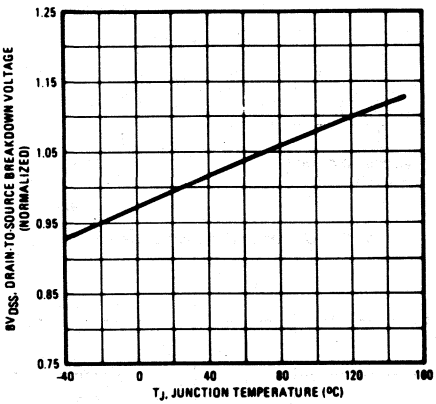


Fig. 8 - Breakdown voltage vs. temperature.

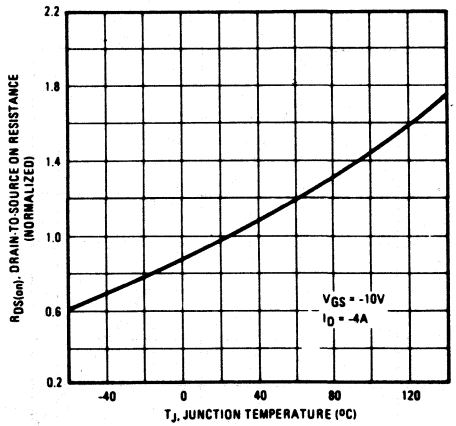


Fig. 9 - Normalized on-resistance vs. temperature.

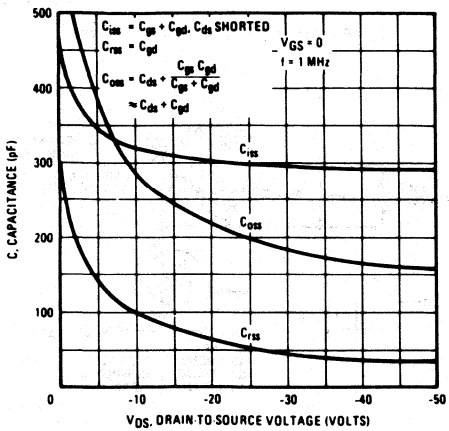


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

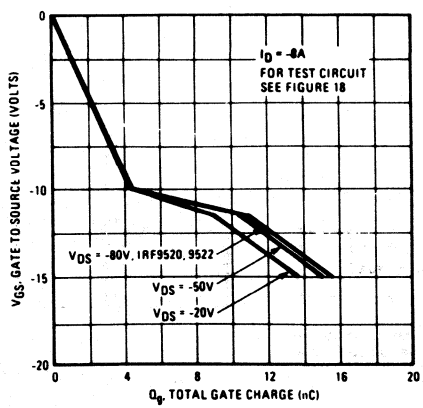


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

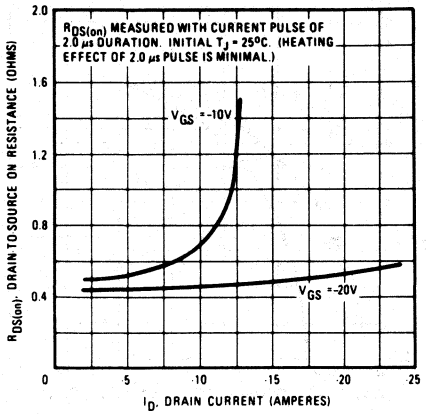


Fig. 12 - Typical on-resistance vs. drain current.

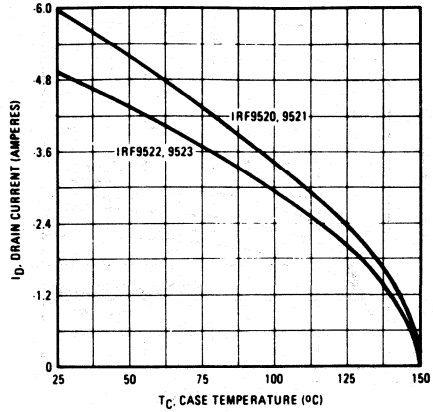


Fig. 13 - Maximum drain current vs. case temperature.

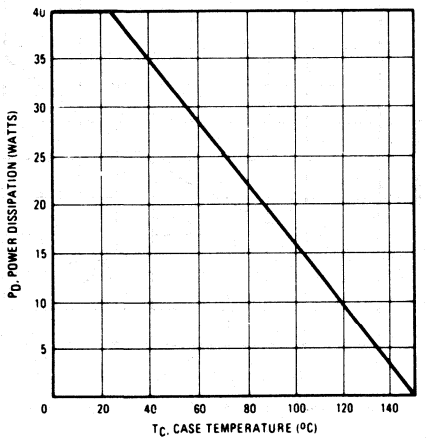


Fig. 14 - Power vs. temperature derating curve.

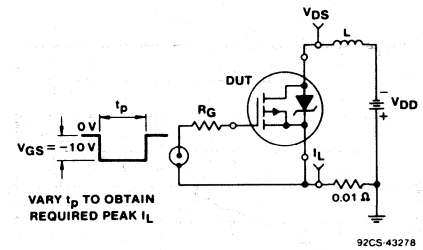


Fig. 15 - Unclamped inductive test circuit.

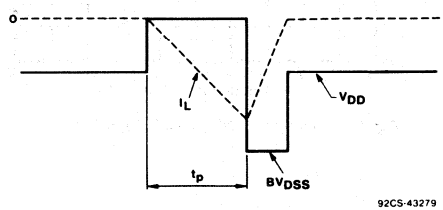


Fig. 16 - Unclamped inductive waveforms.

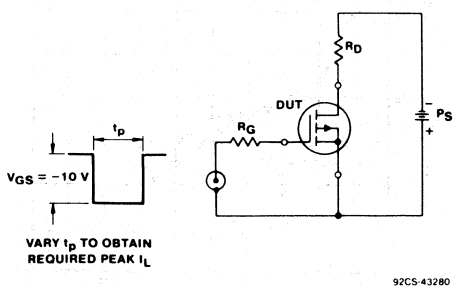


Fig. 17 - Switching time test circuit.

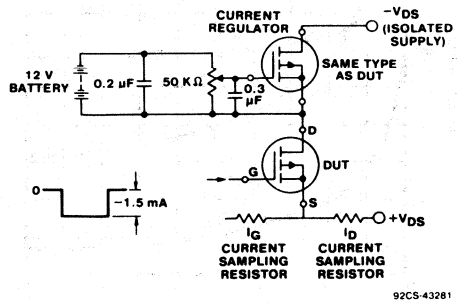


Fig. 18 - Gate charge test circuit.

File Number **2221**

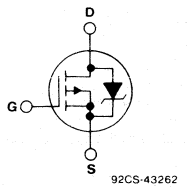
IRF9530, IRF9531, IRF9532, IRF9533

Avalanche-Energy-Rated P-Channel Power MOSFETs

-10A, and -12A, -60V and -100V
$r_{DS(on)}$ = 0.30Ω and 0.40Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



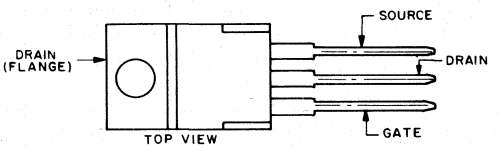
92CS-43262

P-CHANNEL ENHANCEMENT MODE

The IRF9530, IRF9531, IRF9532 and IRF9533 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

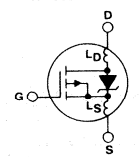
Parameter		IRF9530	IRF9531	IRF9532	IRF9533	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-12	-12	-10	-10	A
I_D @ T_C = 100°C	Continuous Drain Current	-7.5	-7.5	-6.5	-6.5	A
I_{DM}	Pulsed Drain Current ③	-48	-48	-40	-40	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
E_{AS}	Single Pulse Avalanche Energy ④	500				mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF9530, IRF9531, IRF9532, IRF9533

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9530 IRF9532	-100	–	–	V	V_{GS} = 0V
		IRF9531 IRF9533	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9530 IRF9531	-12	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF9532 IRF9533	-10	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9530 IRF9531	–	0.25	0.30	Ω	V_{GS} = -10V, I_D = -6.5A
		IRF9532 IRF9533	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.0	3.8	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 6.5A
C_{iss}	Input Capacitance	ALL	–	500	—	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = -6.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	70	140	ns	
t_f	Fall Time	ALL	–	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	25	45	nC	V_{GS} = -15V, I_D = -15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	12	22	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

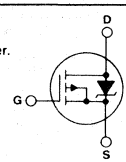


Thermal Resistance

$R_{\theta JC}$	Junction-to-Case	ALL	–	–	1.67	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
$R_{\theta JA}$	Junction-to-Ambient	ALL	–	–	80	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9530 IRF9531	–	–	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9532 IRF9533	–	–	-10	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9530 IRF9531	–	–	-48	A	
		IRF9532 IRF9533	–	–	-40	A	
V_{SD}	Diode Forward Voltage ②	IRF9530 IRF9531	–	–	-1.5	V	T_C = 25°C, I_S = -12A, V_{GS} = 0V
		IRF9532 IRF9533	–	–	-1.5	V	T_C = 25°C, I_S = -10A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = -12A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.8	–	μC	T_J = 150°C, I_F = -12A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating; Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 25V, Starting T_J = 25°C, L = 5.2 mH, R_G = 25Ω, Peak I_L = 12A, (See Fig. 15 and 16).

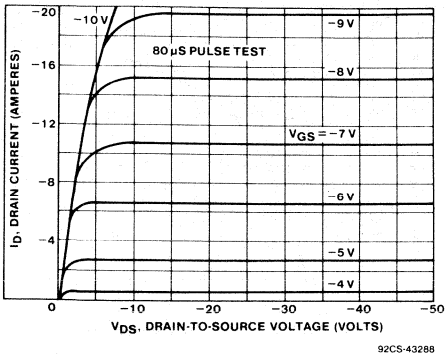


Fig. 1 - Typical Output Characteristics

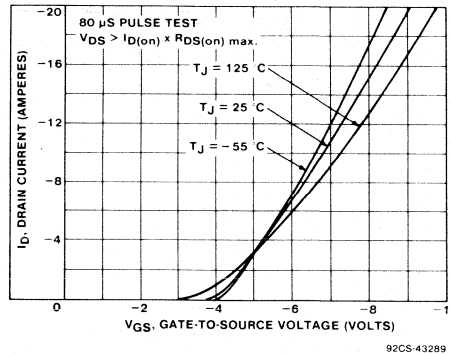


Fig. 2 - Typical Transfer Characteristics

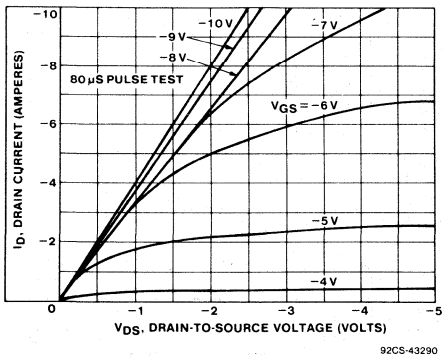


Fig. 3 - Typical saturation characteristic.

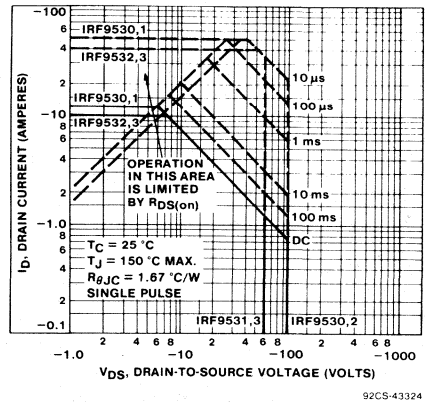


Fig. 4 - Maximum safe operating area.

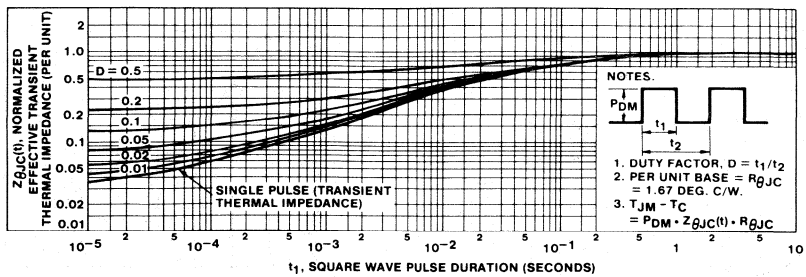


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

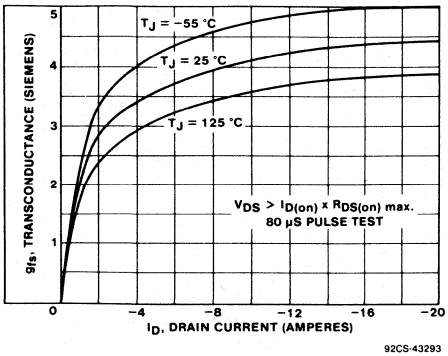


Fig. 6 - Typical transconductance vs. drain current.

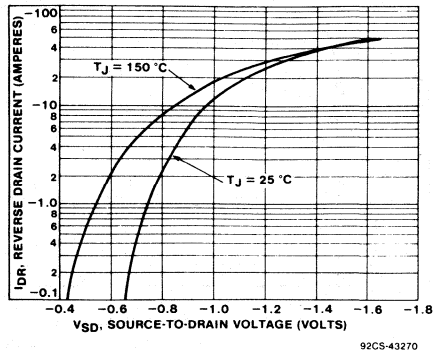


Fig. 7 - Typical source-drain diode forward voltage.

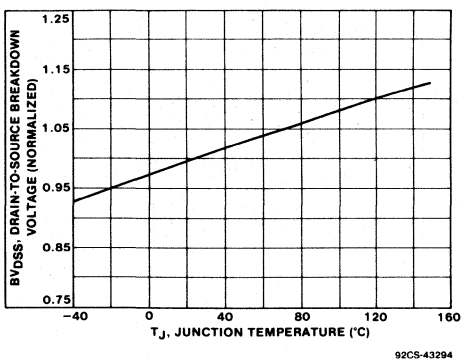


Fig. 8 - Breakdown voltage vs. temperature.

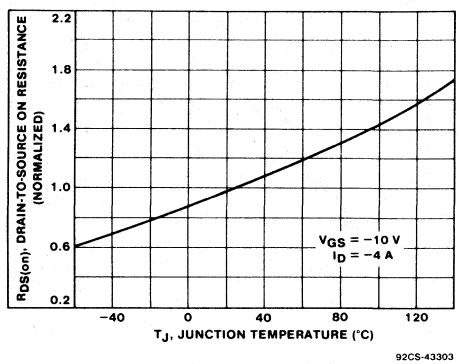


Fig. 9 - Normalized on-resistance vs. temperature.

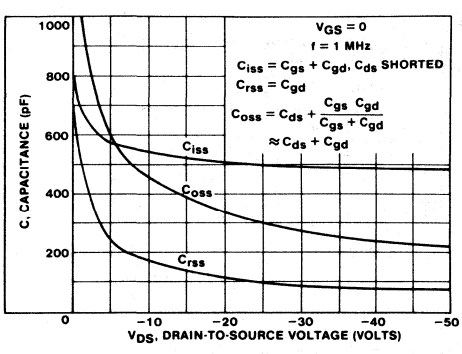


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

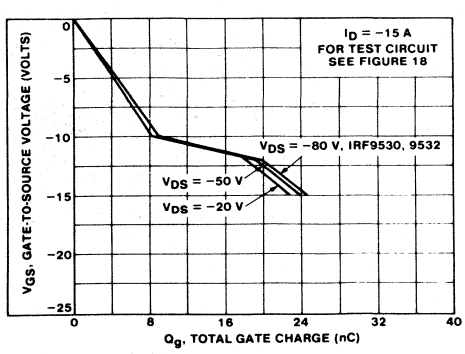


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

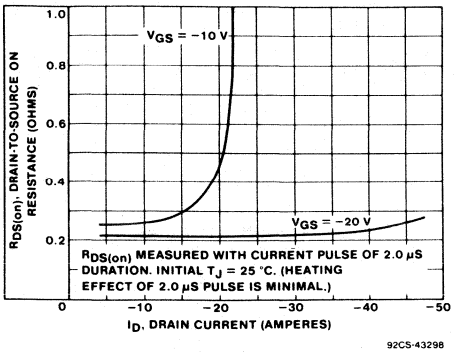


Fig. 12 - Typical on-resistance vs. drain current.

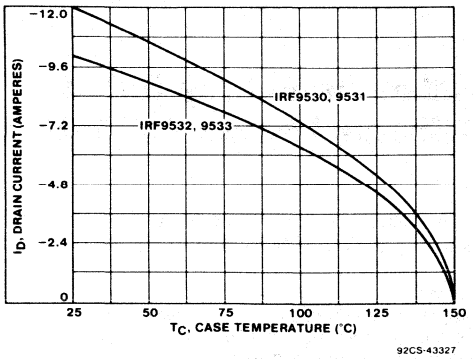


Fig. 13 - Maximum drain current vs. case temperature.

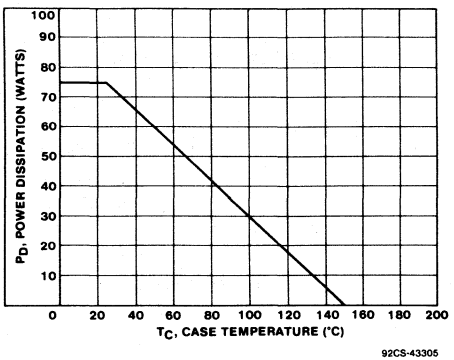


Fig. 14 - Power vs. temperature derating curve.

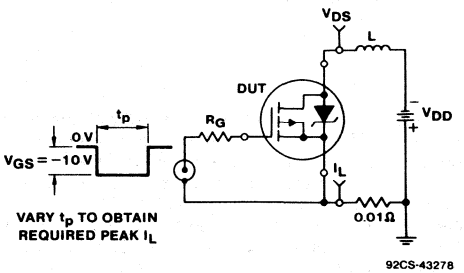


Fig. 15 - Unclamped inductive test circuit.

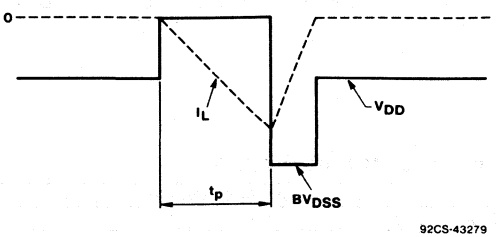


Fig. 16 - Unclamped inductive waveforms.

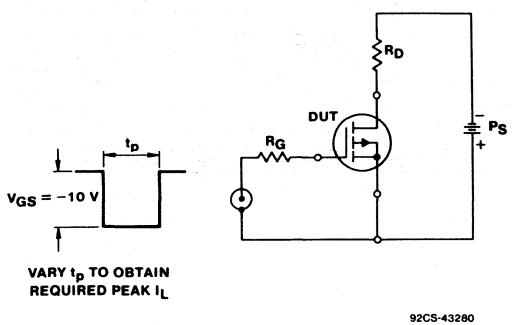


Fig. 17 - Switching time test circuit.

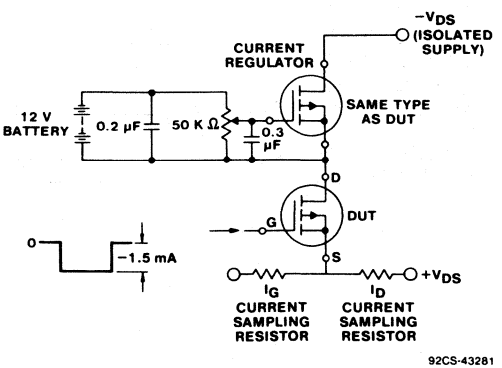


Fig. 18 - Gate charge test circuit.

IRF9540, IRF9541
IRF9542, IRF9543

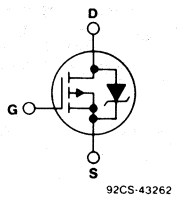
File Number **2282**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-15 A and -19 A, -60 V and -100 V
$r_{DS(on)}$ = 0.20 Ω and 0.30 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



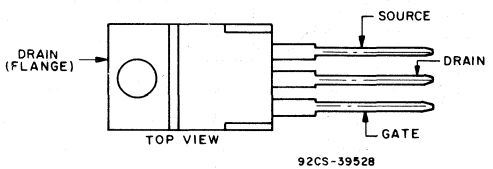
92CS-43262

P-CHANNEL ENHANCEMENT MODE

The IRF9540, IRF9541, IRF9542 and IRF9543 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

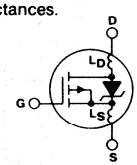
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF9540	IRF9541	IRF9542	IRF9543	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current	I_D @ T_C = 25°C	-19	-19	-15	-15	A
Continuous Drain Current	I_D @ T_C = 100°C	-12	-12	-10	-10	A
Pulsed Drain Current ③	I_{DM}	-76	-76	-60	-60	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	125 (See Fig. 14)				W
Linear Derating Factor		1 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	960				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

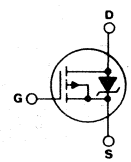
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9540 IRF9542	-100	—	—	V	V_{GS} = 0 V
		IRF9541 IRF9543	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRF9540 IRF9541	-19	—	—	A	V_{DS} > $I_{D(on)}$ x $r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRF9542 IRF9543	-15	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRF9540 IRF9541	—	0.15	0.20	Ω	V_{GS} = -10 V, I_D = -10 A
		IRF9542 IRF9543	—	0.22	0.30	Ω	
Forward Transconductance ②	g_{fs}	ALL	5	7	—	S (℧)	V_{DS} > $I_{D(on)}$ x $r_{DS(on)\ max.}$, I_D = -6 A
Input Capacitance	C_{iss}	ALL	—	1100	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	550	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	250	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	16	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -18 A, Z_O = 9.1 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	65	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	47	70	ns	
Fall Time	t_f	ALL	—	28	70	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	70	90	nC	V_{GS} = -15 V, I_D = -24 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	14	21	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	56	84	nC	
Internal Drain Inductance	L_D	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	**Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.**
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9540 IRF9541	—	—	-19	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9542 IRF9543	—	—	-15	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9540 IRF9541	—	—	-76	A	
		IRF9542 IRF9543	—	—	-60	A	
Diode Forward Voltage ②	V_{SD}	IRF9540 IRF9541	—	—	-1.5	V	T_C = 25°C, I_S = -19 A, V_{GS} = 0 V
		IRF9542 IRF9543	—	—	-1.5	V	T_C = 25°C, I_S = -15 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	170	—	ns	T_J = 150°C, I_F = 19 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.8	—	μC	T_J = 150°C, I_F = 19 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25 V, Starting T_j = 25°C, L = 4 mHμ, R_G = 25 Ω, Peak I_L = 19 A (See Figs. 15 & 16).

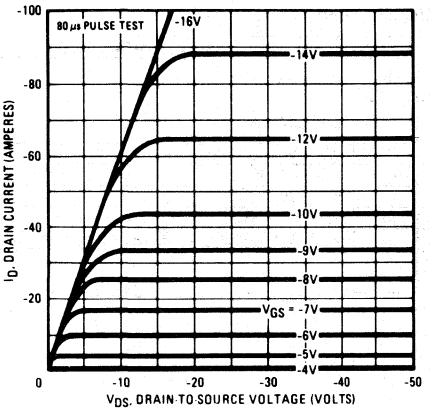


Fig. 1 - Typical output characteristics.

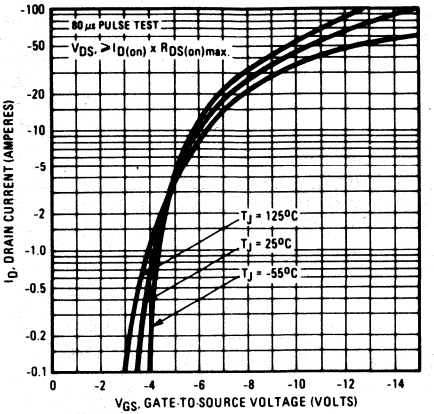


Fig. 2 - Typical transfer characteristics.

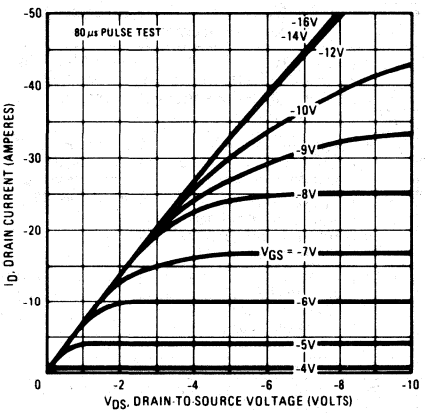


Fig. 3 - Typical saturation characteristics.

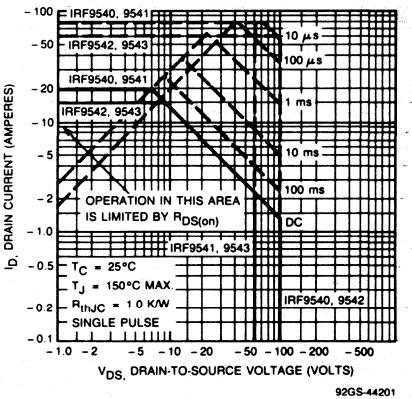


Fig. 4 - Maximum safe operating area.

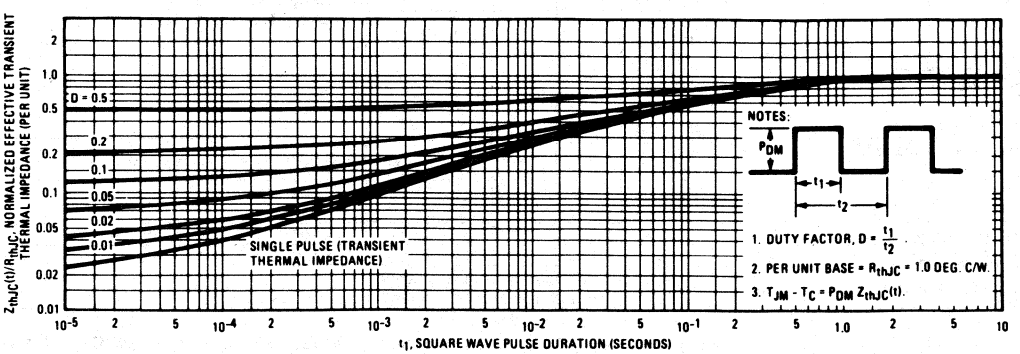


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

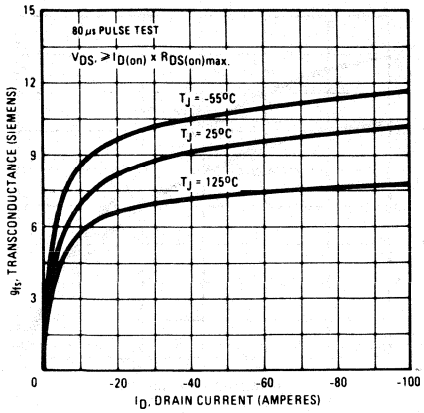


Fig. 6 - Typical transconductance vs. drain current.

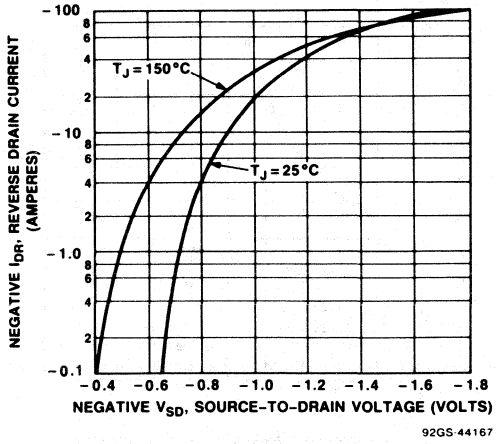


Fig. 7 - Typical source-drain diode forward voltage.

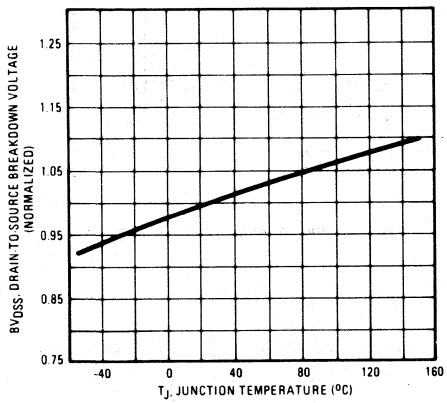


Fig. 8 - Breakdown voltage vs. temperature.

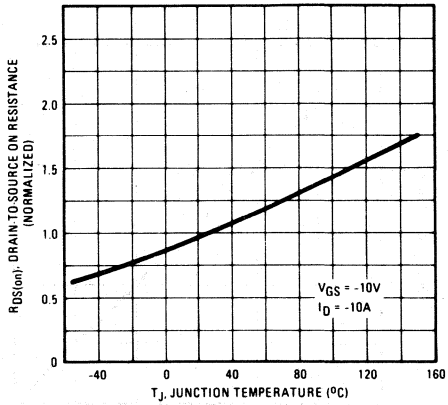


Fig. 9 - Normalized on-resistance vs. temperature.

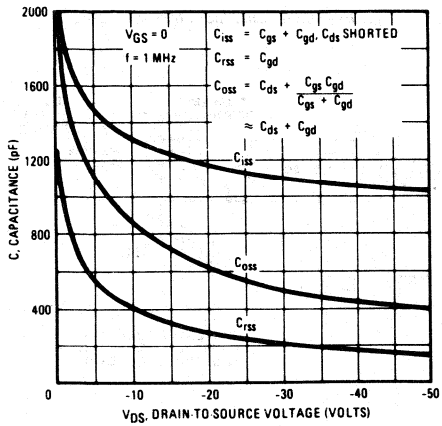


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

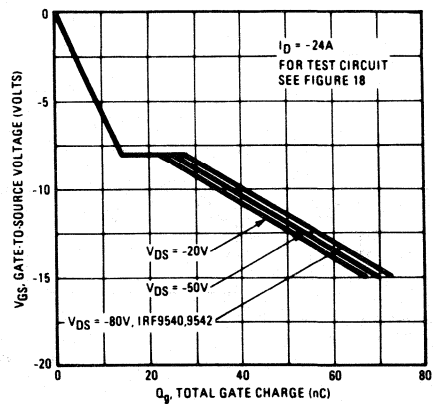


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

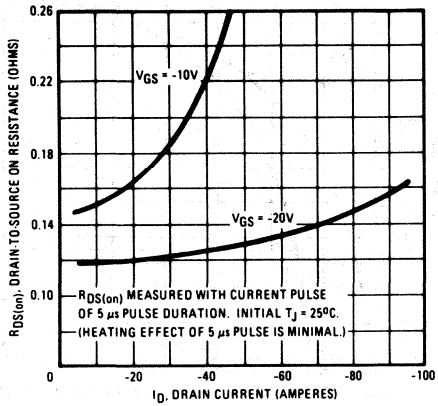


Fig. 12 - Typical on-resistance vs. drain current.

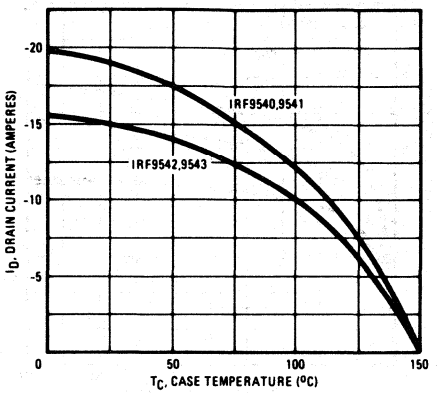


Fig. 13 - Maximum drain current vs. case temperature.

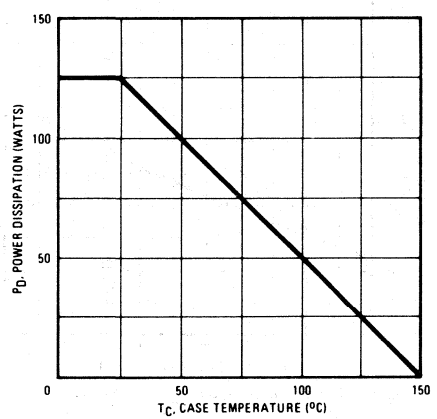


Fig. 14 - Power vs. temperature derating curve.

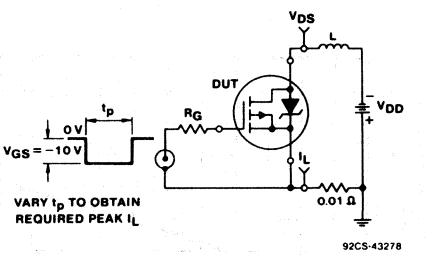


Fig. 15 - Unclamped inductive test circuit.

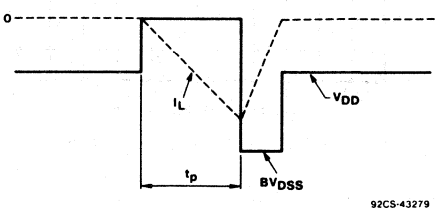


Fig. 16 - Unclamped inductive waveforms.

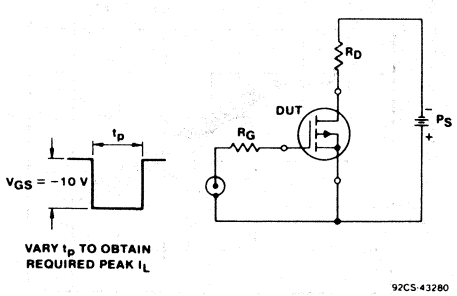


Fig. 17 - Switching time test circuit.

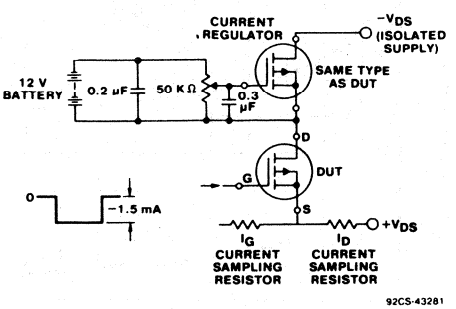


Fig. 18 - Gate charge test circuit.

File Number **2283**

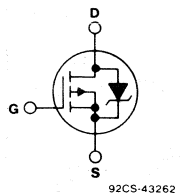
IRF9620, IRF9621
IRF9622, IRF9623

Avalanche-Energy-Rated P-Channel Power MOSFETs

-3 A and -3.5 A, -150 V and -200 V
$r_{DS(on)}$ = 1.5 Ω and 2.4 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

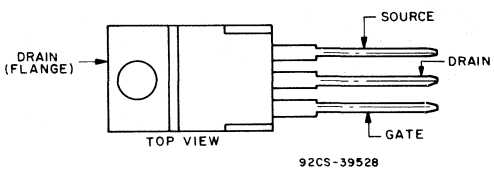


P-CHANNEL ENHANCEMENT MODE

The IRF9620, IRF9621, IRF9622 and IRF9623 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



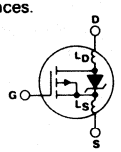
JEDEC TO-220AB

ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF9620	IRF9621	IRF9622	IRF9623	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-3.5	-3.5	-3	-3	A
Continuous Drain Current	I_D @ T_C = 100°C	-2	-2	-1.5	-1.5	A
Pulsed Drain Current ③	I_{DM}	-14	-14	-12	-12	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	40 (See Fig. 14)				W
Linear Derating Factor		0.32 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	290				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

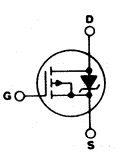
ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9620 IRF9622	-200	—	—	V	V_{GS} = 0 V
		IRF9621 IRF9623	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRF9620 IRF9621	-3.5	—	—	A	V_{DS} > $I_{D(on)}$ x $r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRF9622 IRF9623	-3	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRF9620 IRF9621	—	1.0	1.5	Ω	V_{GS} = -10 V, I_D = 1.5 A
		IRF9622 IRF9623	—	1.5	2.4	Ω	
Forward Transconductance ②	g_{fs}	ALL	1	1.8	—	S(℧)	V_{DS} > $I_{D(on)}$ x $r_{DS(on)\ max.}$, I_D = 1.5 A
Input Capacitance	C_{iss}	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	100	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	30	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	30	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -1.5 A, Z_O = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	80	120	ns	
Fall Time	t_f	ALL	—	50	75	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	22	nC	V_{GS} = -15 V, I_D = -4 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	9	13.5	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	7	10.5	nC	
Internal Drain Inductance	L_D	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	3.12	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Typical socket mount.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9620 IRF9621	—	—	-3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9622 IRF9623	—	—	-3	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9620 IRF9621	—	—	-14	A	
		IRF9622 IRF9623	—	—	-12	A	
Diode Forward Voltage ②	V_{SD}	IRF9620 IRF9621	—	—	-1.5	V	T_C = 25°C, I_S = -3.5 A, V_{GS} = 0 V
		IRF9622 IRF9623	—	—	-1.5	V	T_C = 25°C, I_S = -3 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	300	—	ns	T_J = 150°C, I_F = -3.5 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	1.9	—	μC	T_J = 150°C, I_F = -3.5 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_j = 25°C, L = 35.5 mH, R_G = 25 Ω, Peak I_L = 3.5 A (See Figs. 15 & 16).

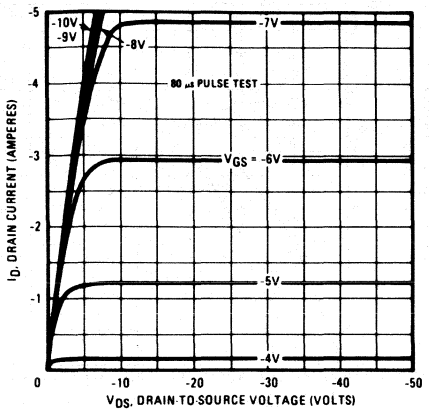


Fig. 1 - Typical output characteristics.

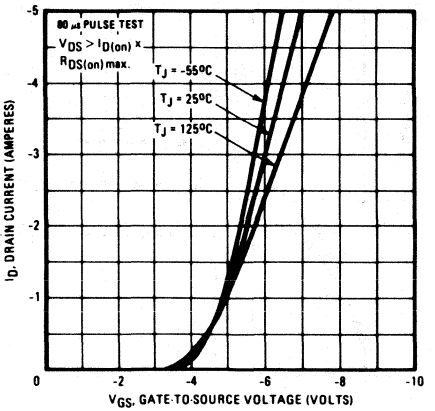


Fig. 2 - Typical transfer characteristics.

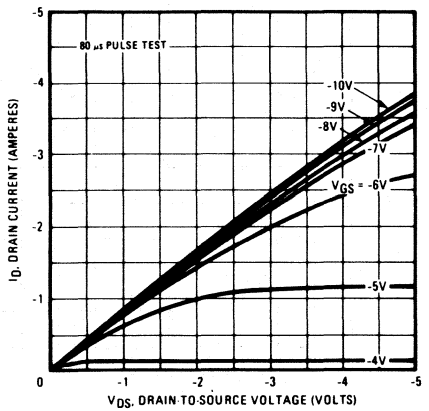


Fig. 3 - Typical saturation characteristics.

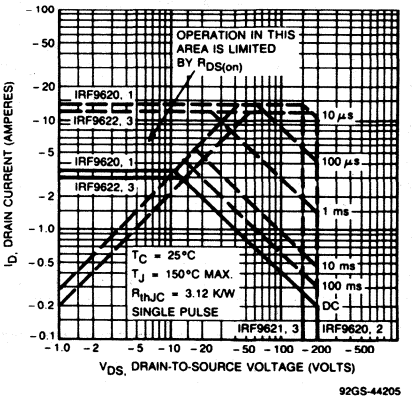


Fig. 4 - Maximum safe operating area.

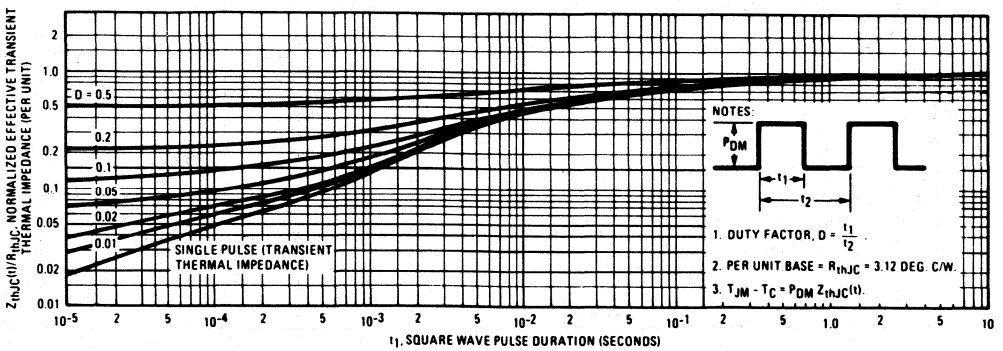


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

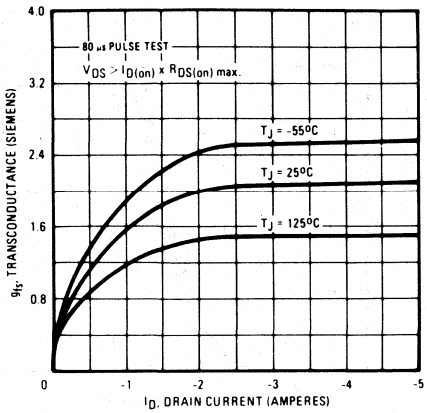


Fig. 6 - Typical transconductance vs. drain current.

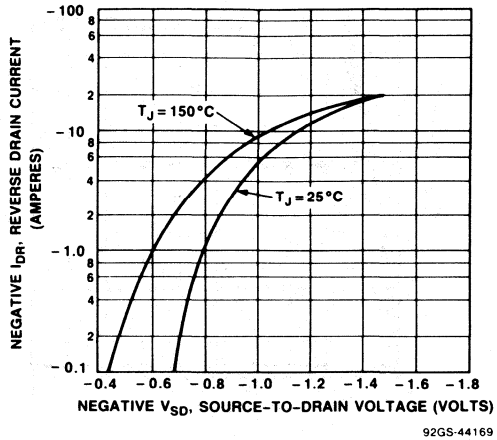


Fig. 7 - Typical source-drain diode forward voltage.

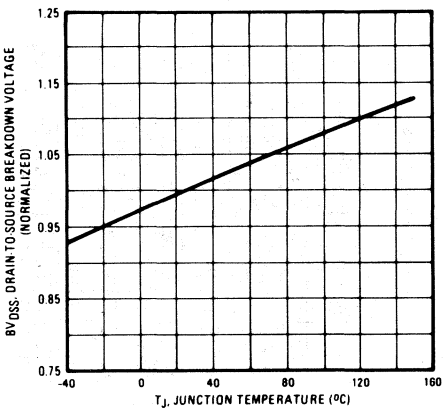


Fig. 8 - Breakdown voltage vs. temperature.

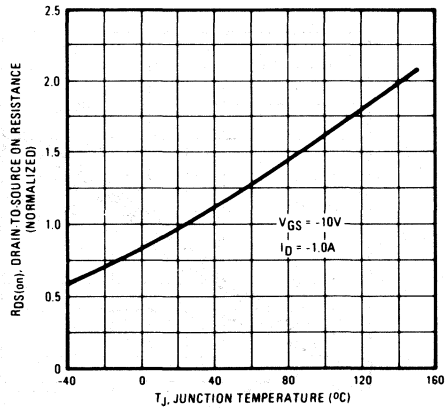


Fig. 9 - Normalized on-resistance vs. temperature.

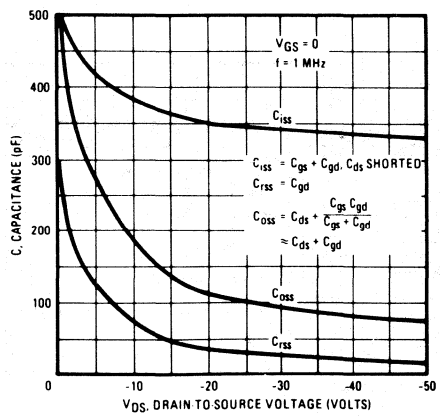


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

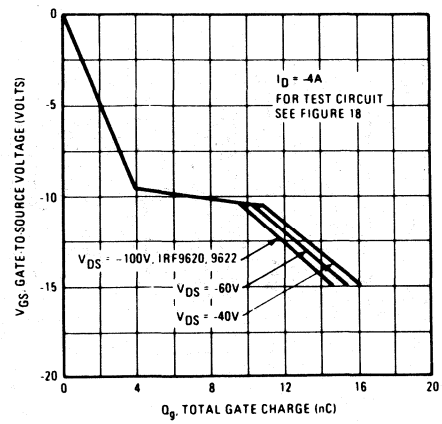


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

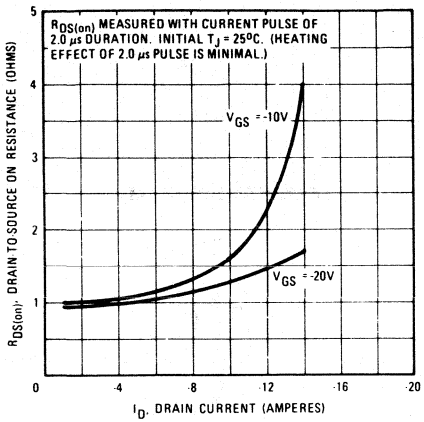


Fig. 12 - Typical on-resistance vs. drain current.

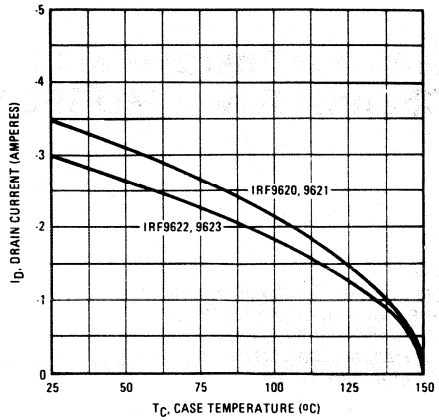


Fig. 13 - Maximum drain current vs. case temperature.

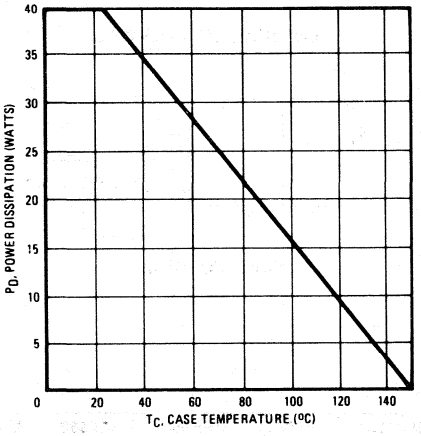


Fig. 14 - Power vs. temperature derating curve.

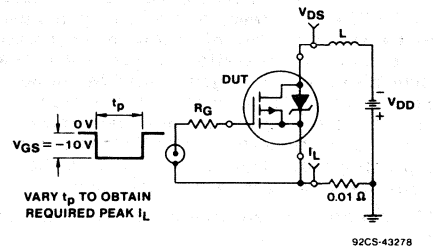


Fig. 15 - Unclamped inductive test circuit.

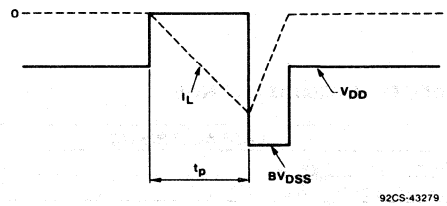


Fig. 16 - Unclamped inductive waveforms.

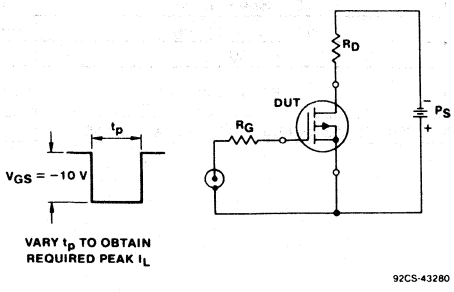


Fig. 17 - Switching time test circuit.

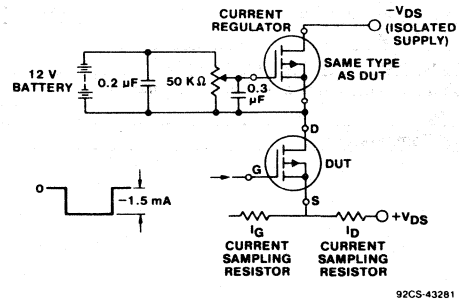


Fig. 18 - Gate charge test circuit.

IRF9630, IRF9631, IRF9632, IRF9633

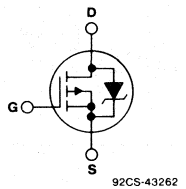
File Number **2224**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-5.5 A and -6.5 A, -150 V and -200 V
$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



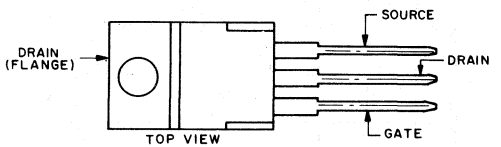
92CS-43262

P-CHANNEL ENHANCEMENT MODE

The IRF9630, IRF9631, IRF9632 and IRF9633 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

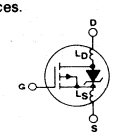
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF9630	IRF9631	IRF9632	IRF9633	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-6.5	-6.5	-5.5	-5.5	A
Continuous Drain Current	I_D @ T_C = 100°C	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current ③	I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	75 (See Fig. 14)				W
Linear Derating Factor		0.6 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	500				mj
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. (1.6 mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS, At T_C = 25°C (Unless Otherwise Specified)

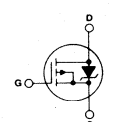
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9630, IRF9632	-200	—	—	V	V_{GS} = 0 V
		IRF9631, IRF9633	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS}(th)$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_D(on)$	IRF9630, IRF9631	-6.5	—	—	A	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., V_{GS} = -10 V
		IRF9632, IRF9633	-5.5	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS}(on)$	IRF9630, IRF9631	—	0.5	0.8	Ω	V_{GS} = -10 V, I_D = -3.5 A
		IRF9632, IRF9633	—	0.8	1.2	Ω	
Forward Transconductance ②	g_{fs}	ALL	2.2	3.5	—	S (℧)	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., I_D = -3.5 A
Input Capacitance	C_{iss}	ALL	—	550	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	170	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	—	pF	
Turn-On Delay Time	$t_d(on)$	ALL	—	30	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -3.5 A, Z_o = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_d(off)$	ALL	—	50	100	ns	
Fall Time	t_f	ALL	—	40	80	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	31	45	nC	V_{GS} = -15 V, I_D = -8.0 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	18	26	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	13	19	nC	
Internal Drain Inductance	L_D	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1.67	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9630, IRF9631	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9632, IRF9633	—	—	-5.5	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9630, IRF9631	—	—	-26	A	
		IRF9632, IRF9633	—	—	-22	A	
Diode Forward Voltage ②	V_{SD}	IRF9630, IRF9631	—	—	-1.5	V	T_C = 25°C, I_S = -6.5 A, V_{GS} = 0 V
		IRF9632, IRF9633	—	—	-1.5	V	T_C = 25°C, I_S = -5.5 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	400	—	ns	T_J = 150°C, I_F = -6.5 A, di_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	2.6	—	μC	T_J = 150°C, I_F = -6.5 A, di_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs. Duty Cycle ≤ 2%

③ Repetitive Rating: Pulse width limited by max. junction temperature See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50 V, Starting T_J = 25°C, L = 17.75 mH, R_G = 25 Ω, Peak I_L = 6.5 A (See Figs. 15 & 16).

IRF9630, IRF9631, IRF9632, IRF9633

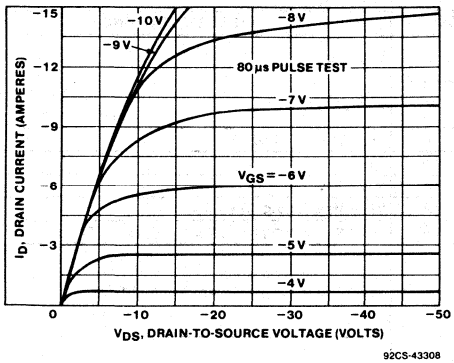


Fig. 1 - Typical output characteristics.

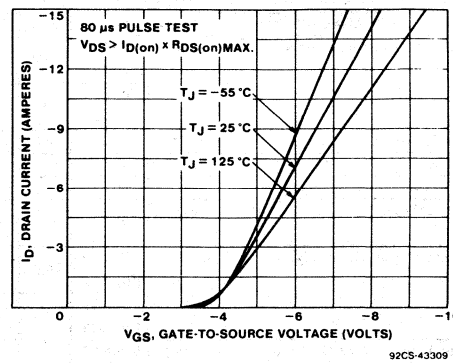


Fig. 2 - Typical transfer characteristics.

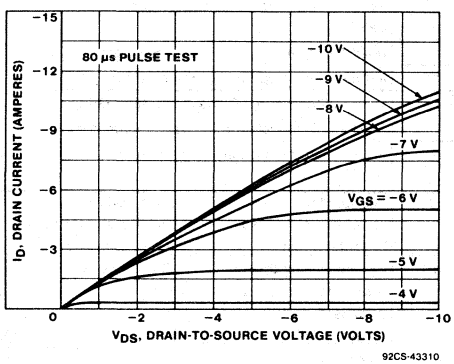


Fig. 3 - Typical saturation characteristics.

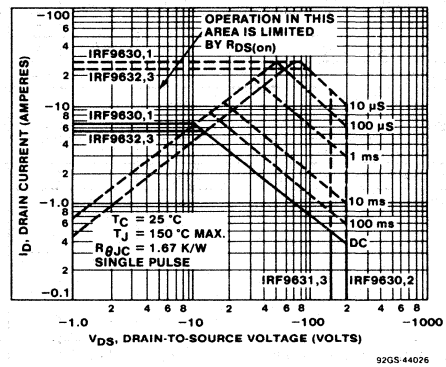


Fig. 4 - Maximum safe operating area.

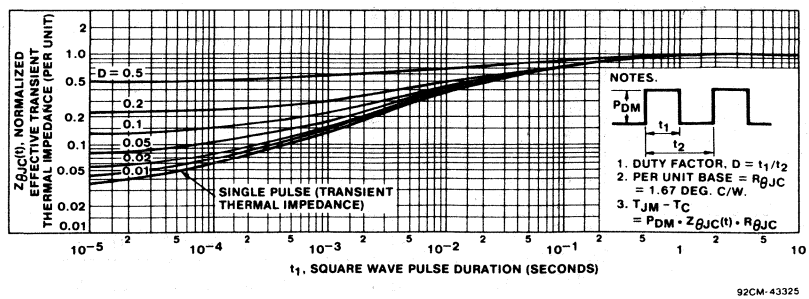


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

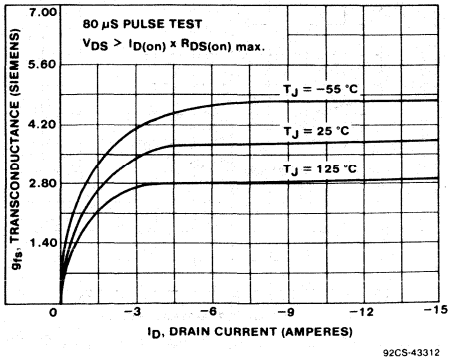


Fig. 6 - Typical transconductance vs. drain current.

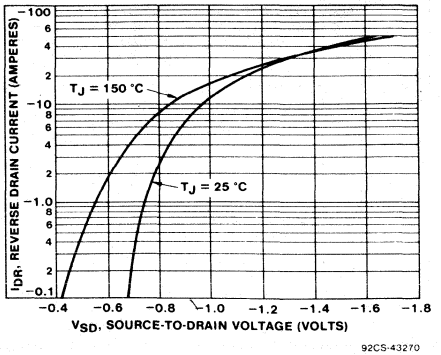


Fig. 7 - Typical source-drain diode forward voltage.

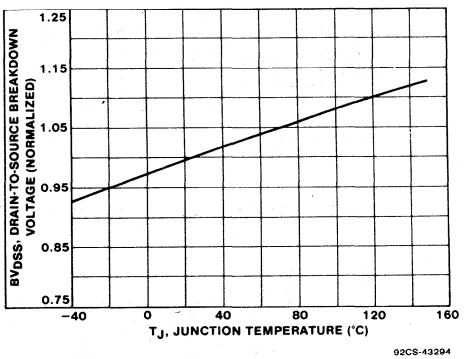


Fig. 8 - Breakdown voltage vs. temperature.

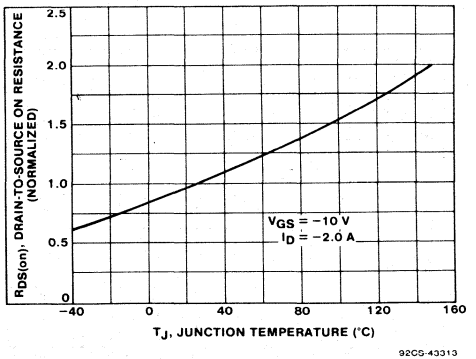


Fig. 9 - Normalized on-resistance vs. temperature.

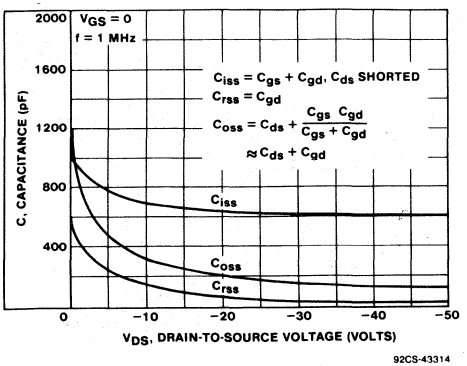


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

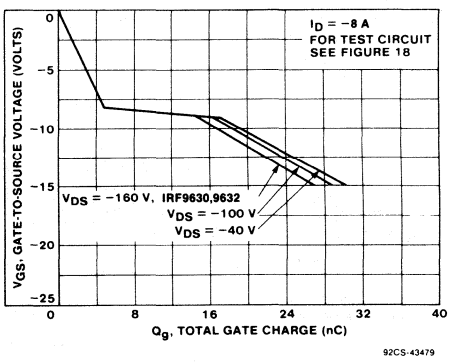


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

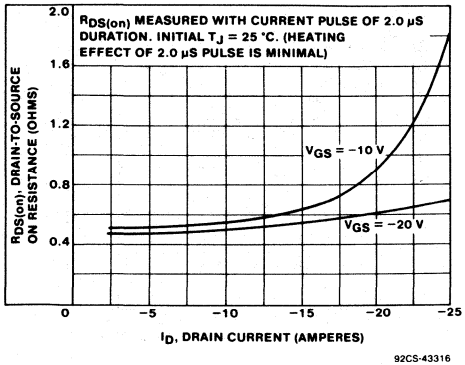


Fig. 12 - Typical on-resistance vs. drain current.

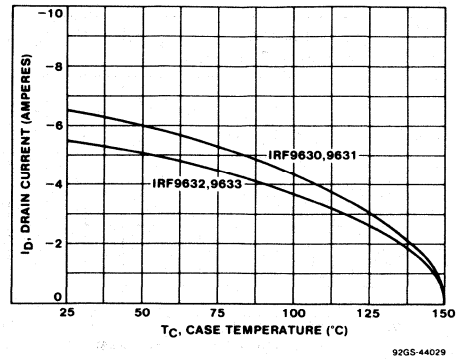


Fig. 13 - Maximum drain current vs. case temperature.

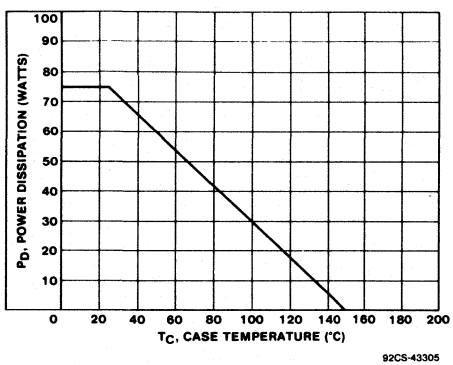


Fig. 14 - Power vs. temperature derating curve.

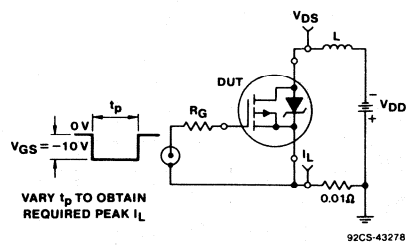


Fig. 15 - Unclamped inductive test circuit.

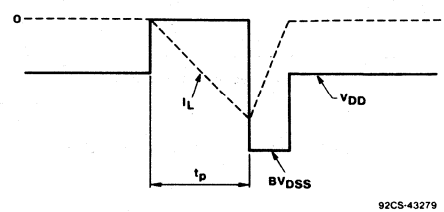


Fig. 16 - Unclamped inductive waveforms.

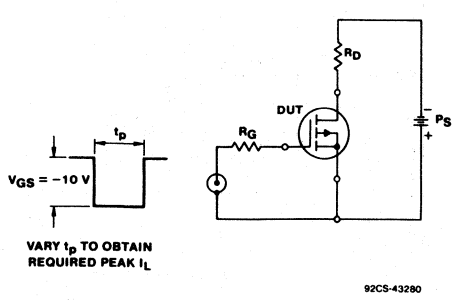


Fig. 17 - Switching time test circuit.

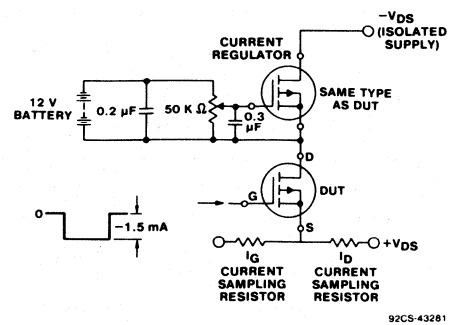


Fig. 18 - Gate charge test circuit.

File Number **2284**

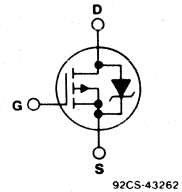
IRF9640, IRF9641
IRF9642, IRF9643

Avalanche-Energy-Rated P-Channel Power MOSFETs

-9 A and -11 A, -150 V and -200 V
$r_{DS(on)}$ = 0.5 Ω and 0.7 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

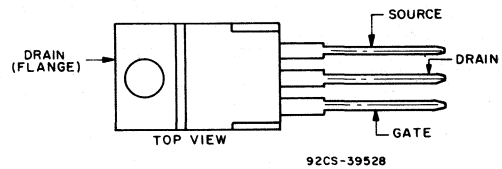


P-CHANNEL ENHANCEMENT MODE

The IRF9640, IRF9641, IRF9642 and IRF9643 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



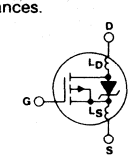
JEDEC TO-220AB

ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRF9640	IRF9641	IRF9642	IRF9643	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-11	-11	-9	-9	A
Continuous Drain Current	I_D @ T_C = 100°C	-7	-7	-6	-6	A
Pulsed Drain Current ③	I_{DM}	-44	-44	-36	-36	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	125 (See Fig. 14)				W
Linear Derating Factor		1 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	790				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

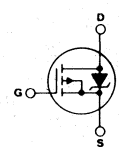
ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9640 IRF9642	-200	—	—	V	V_{GS} = 0 V
		IRF9641 IRF9643	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRF9640 IRF9641	-11	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRF9642 IRF9643	-9	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRF9640 IRF9641	—	0.35	0.5	Ω	V_{GS} = -10 V, I_D = -6 A
		IRF9642 IRF9643	—	0.55	0.7	Ω	
Forward Transconductance ②	g_{fs}	ALL	4	6	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = -6 A
Input Capacitance	C_{iss}	ALL	—	1100	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	375	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	150	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	18	22	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -11 A, Z_O = 9.1 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	45	68	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	75	90	ns	
Fall Time	t_f	ALL	—	29	44	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	70	90	nC	V_{GS} = -15 V, I_D = -22 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	55	82.5	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	15	22.5	nC	
Internal Drain Inductance	L_D	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	7.5	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	1	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	80	°C/W	Typical socket mount.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRF9640 IRF9641	—	—	-11	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9642 IRF9643	—	—	-9	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRF9640 IRF9641	—	—	-44	A	
		IRF9642 IRF9643	—	—	-36	A	
Diode Forward Voltage ②	V_{SD}	IRF9640 IRF9641	—	—	-1.5	V	T_C = 25°C, I_S = -11 A, V_{GS} = 0 V
		IRF9642 IRF9643	—	—	-1.5	V	T_C = 25°C, I_S = -9 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	300	—	ns	T_J = 150°C, I_F = -11 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	1.9	—	μC	T_J = 150°C, I_F = -11 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_j = 25°C, L = 9.8 mH, R_G = 25 Ω, Peak I_L = 11 A (See Figs. 15 & 16).

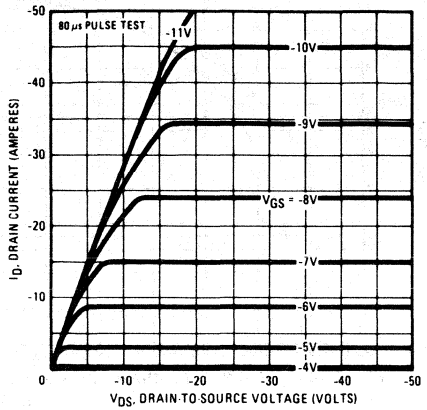


Fig. 1 - Typical output characteristics.

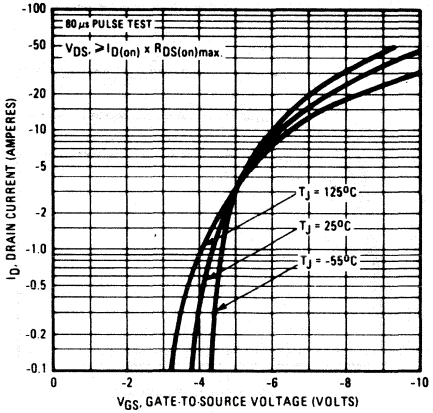


Fig. 2 - Typical transfer characteristics.

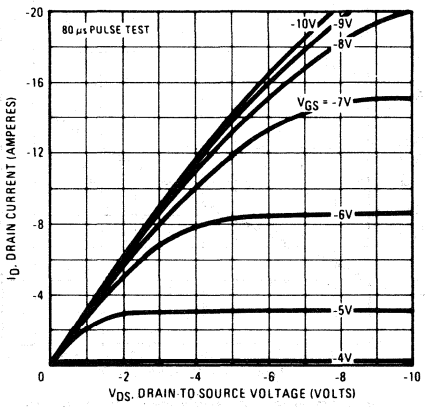


Fig. 3 - Typical saturation characteristics.

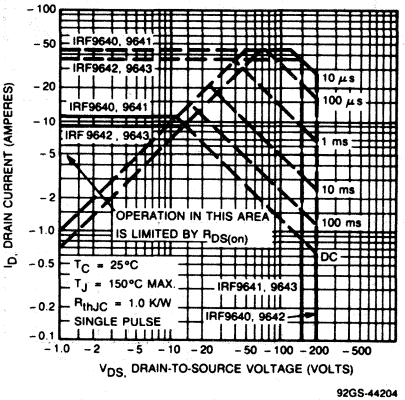


Fig. 4 - Maximum safe operating area.

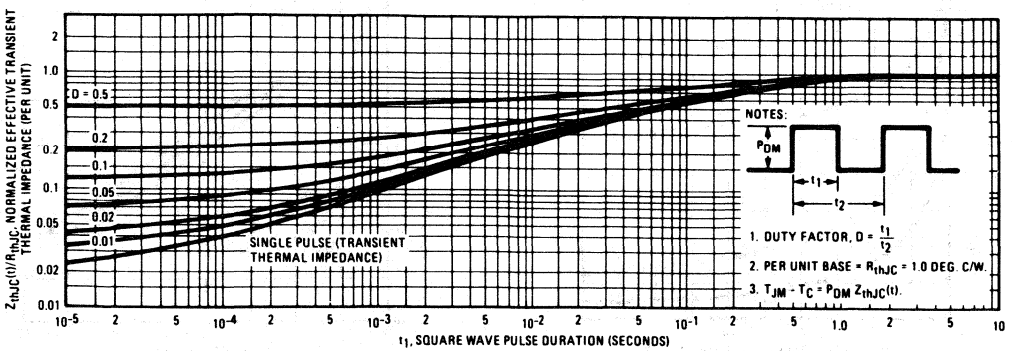


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

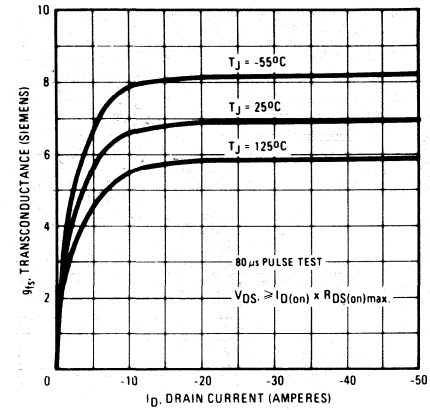


Fig. 6 - Typical transconductance vs. drain current.

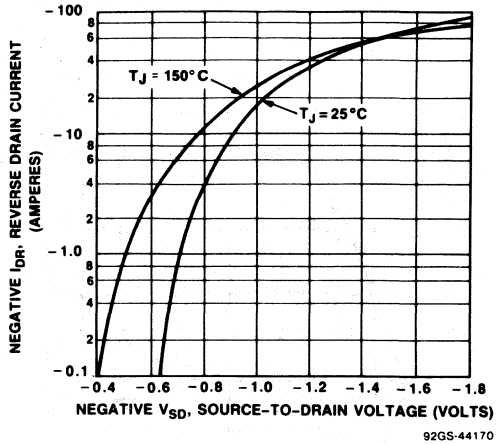


Fig. 7 - Typical source-drain diode forward voltage.

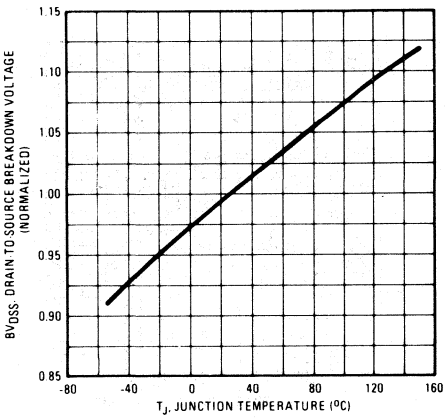


Fig. 8 - Breakdown voltage vs. temperature.

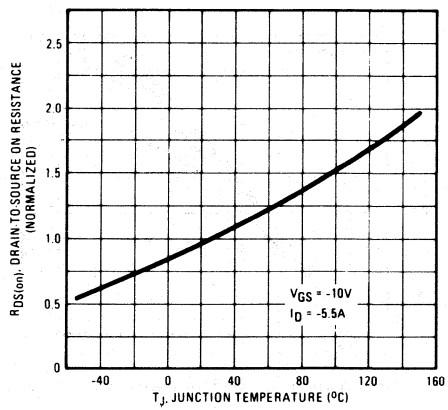


Fig. 9 - Normalized on-resistance vs. temperature.

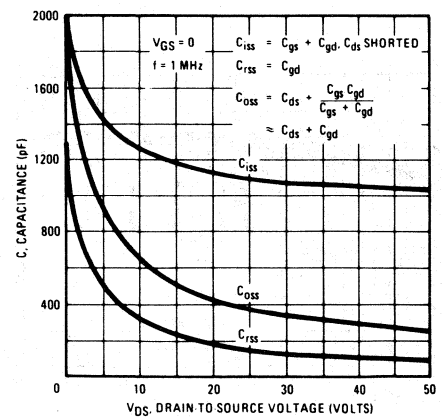


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

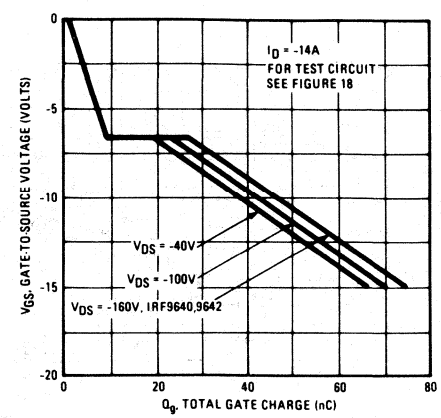


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

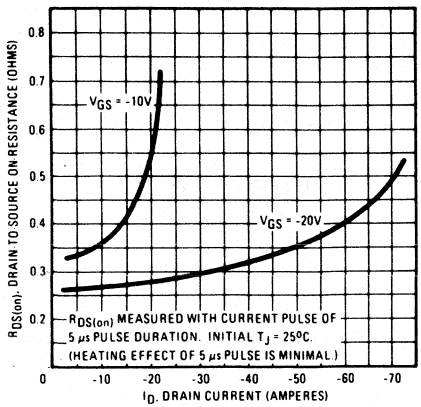


Fig. 12 - Typical on-resistance vs. drain current.

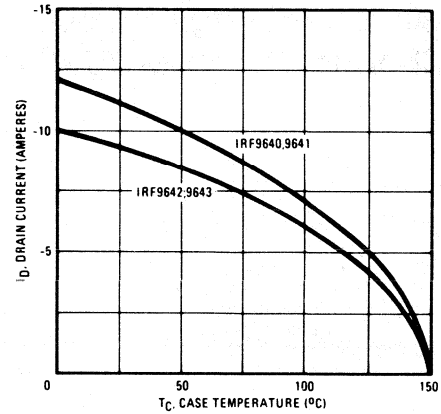


Fig. 13 - Maximum drain current vs. case temperature.

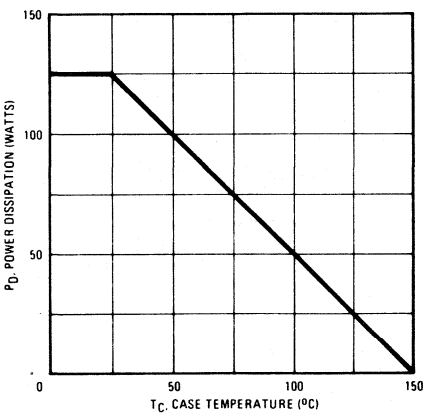


Fig. 14 - Power vs. temperature derating curve.

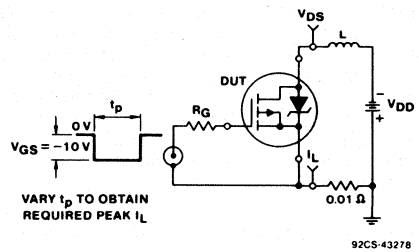


Fig. 15 - Unclamped inductive test circuit.

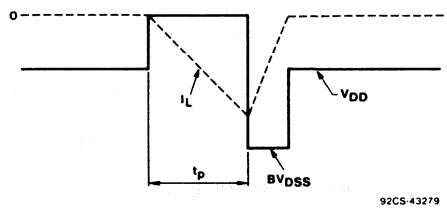


Fig. 16 - Unclamped inductive waveforms.

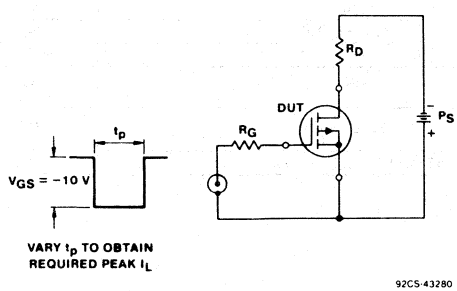


Fig. 17 - Switching time test circuit.

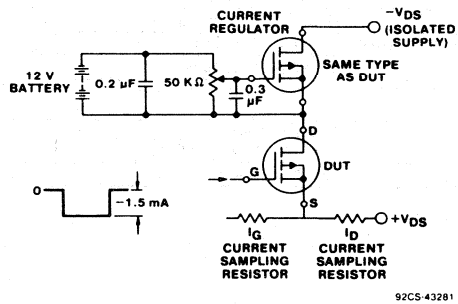


Fig. 18 - Gate charge test circuit.

IRFD9110, IRFD9113

File Number **2215**

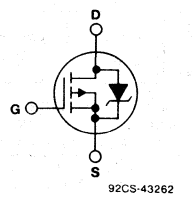
Avalanche-Energy-Rated P-Channel Power MOSFETs

-0.6A and -0.7A, -60V and -100V
r_{DS} (on) = 1.2Ω, and 1.6Ω

Features:

- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



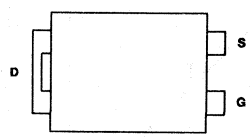
92CS-43262

P-CHANNEL ENHANCEMENT MODE

The IRFD9110 and IRFD9113 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

TERMINAL DESIGNATION



TOP VIEW

4-PIN DIP

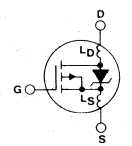
Absolute Maximum Ratings

	Parameter	IRFD9110	IRFD9113	Units
V_{DS}	Drain – Source Voltage ①	-100	-60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	V
I_D @ T_A = 25°C	Continuous Drain Current	-0.7	-0.6	A
I_{DM}	Pulsed Drain Current	-3.0	-2.5	A
V_{GS}	Gate – Source Voltage	± 20		V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)		W
	Linear Derating Factor	0.01 (See Fig. 13)		W/°C
E_{AS}	Single Pulse Avalanche Energy ③	190		mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFD9110	-100	–	–	V	V_{GS} = 0V
		IRFD9113	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	-500	nA	V_{GS} = -20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD9110	-0.7	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRFD9113	-0.6	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFD9110	–	1.0	1.2	Ω	V_{GS} = -10V, I_D = -0.3A
		IRFD9113	–	1.2	1.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.59	0.88	–	S (℧)	V_{DS} ≤ 50V, I_D = -0.6A
C_{iss}	Input Capacitance	ALL	–	180	—	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	85	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	15	30	ns	V_{DD} ≈ 0.5 I_D = -0.3A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	20	40	ns	
t_f	Fall Time	ALL	–	20	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = -15V, I_D = -1.5A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.7	7.8	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	5.3	7.2	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 2.0mm (0.08 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

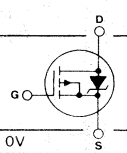


Thermal Resistance

$R\theta_{JA}$	Junction-to-Ambient	ALL	–	–	120	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD9110	–	–	-0.7	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD9113	–	–	-0.6	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD9110	–	–	-3.0	A	
		IRFD9113	–	–	-2.5	A	
V_{SD}	Diode Forward Voltage ②	IRFD9110	–	–	-1.5	V	T_C = 25°C, I_S = -0.7A, V_{GS} = 0V
		IRFD9113	–	–	-1.5	V	T_C = 25°C, I_S = -0.6A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	120	–	ns	T_J = 150°C, I_F = -0.7A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.0	–	μC	T_J = 150°C, I_F = -0.7A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ V_{DD} = 25V, starting T_J = 25°C, L = 582 mH, R_G = 25Ω, Peak I_L = 0.7A. (See Fig. 14 and 15)

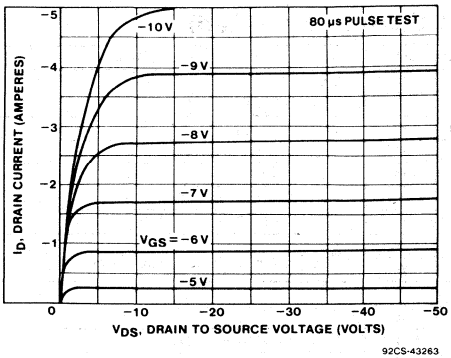


Fig. 1 - Typical Output Characteristics

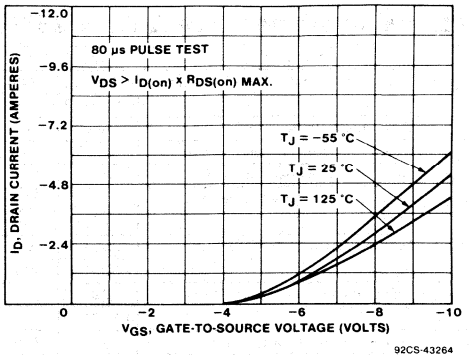


Fig. 2 - Typical Transfer Characteristics

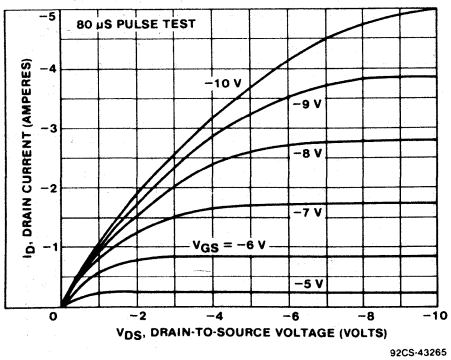


Fig. 3 - Typical Saturation Characteristics

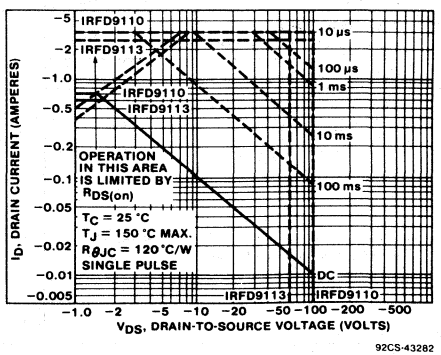


Fig. 4 - Maximum Safe Operating Area

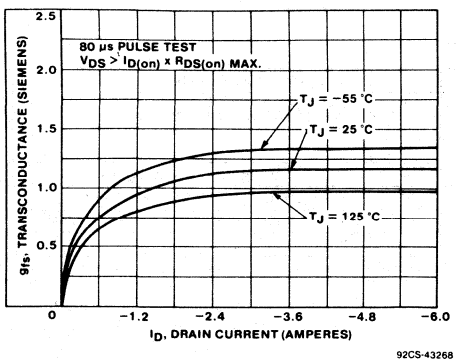


Fig. 5 - Typical Transconductance Vs. Drain Current

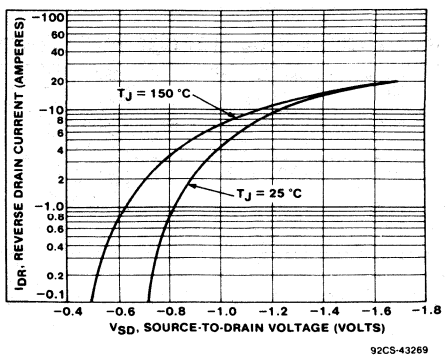


Fig. 6 - Typical Source-Drain Diode Forward Voltage

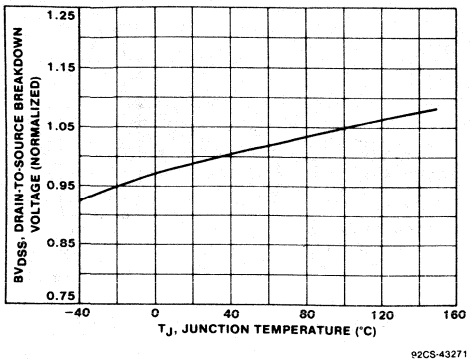


Fig. 7 - Breakdown Voltage Vs. Temperature

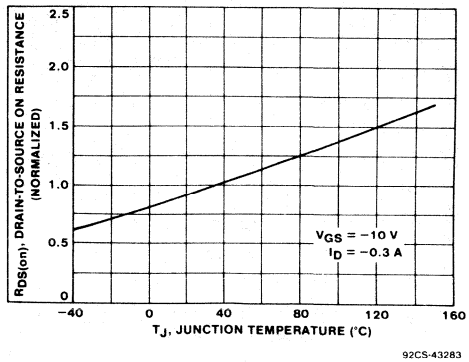


Fig. 8 - Normalized On-Resistance Vs. Temperature

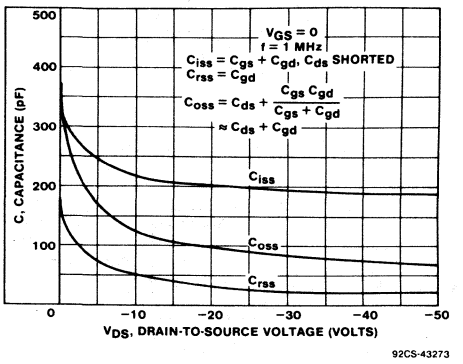


Fig. 9 - Typical Capacitance Vs. Drain-to-Source Voltage

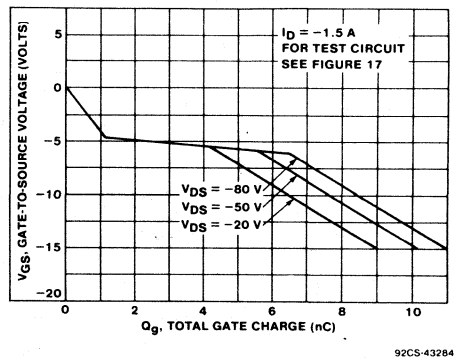


Fig. 10 - Typical Gate Charge Vs. Gate-to-Source Voltage

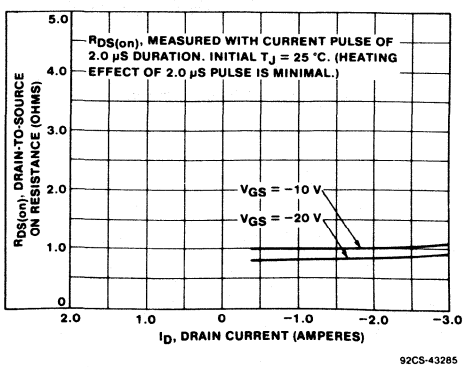


Fig. 11 - Typical On-Resistance Vs. Drain Current

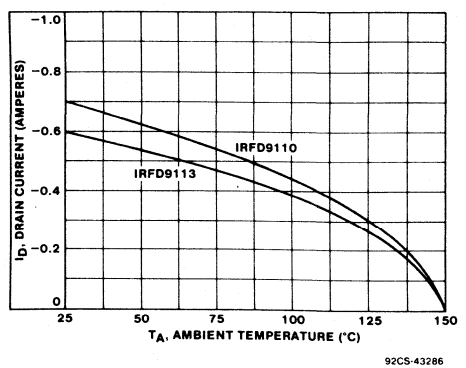


Fig. 12 - Maximum Drain Current Vs. Case Temperature

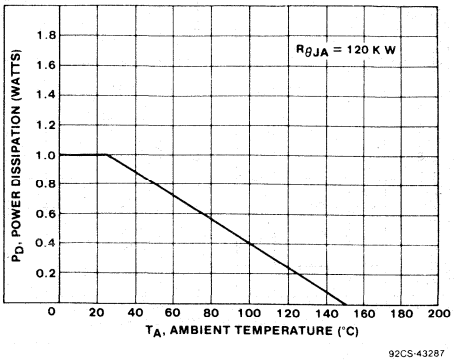


Fig. 13 - Power Vs. Temperature Derating Curve

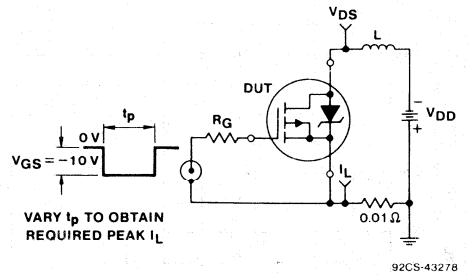


Fig. 14 - Unclamped Inductive Test Circuit

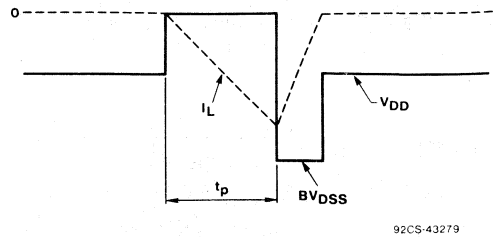


Fig. 15 - Unclamped Inductive Waveforms

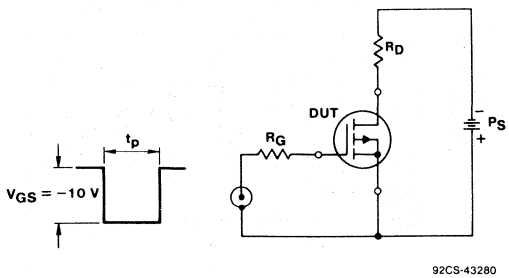


Fig. 16 - Switching Time Test Circuit

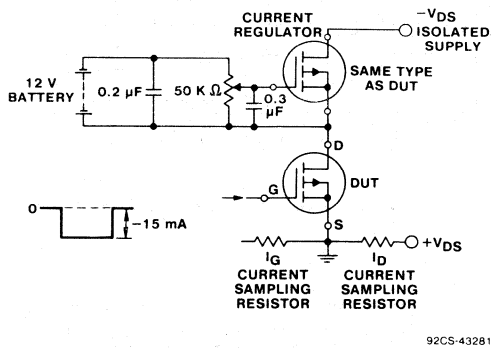


Fig. 17 - Gate Charge Test Circuit

File Number **2285**

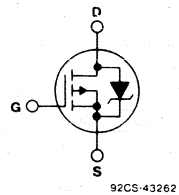
IRFD9120
IRFD9123

Avalanche-Energy-Rated P-Channel Power MOSFETs

-1.0 A and -0.8 A, -60 V and -100 V
$r_{DS(on)}$ = 0.6 Ω and 0.8 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

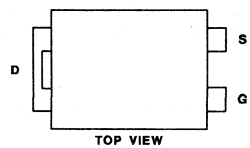


P-CHANNEL ENHANCEMENT MODE

The IRFD9120 and IRFD9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

TERMINAL DESIGNATION



4-PIN DIP

ABSOLUTE-MAXIMUM RATINGS

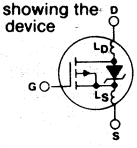
CHARACTERISTIC		IRFD9120	IRFD9123	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-100	-60	V
Continuous Drain Current	I_D @ T_C = 25°C	-1	-0.8	A
Pulsed Drain Current ③	I_{DM}	-8	-6.4	A
Gate-Source Voltage	V_{GS}	±20		V
Maximum Power Dissipation	P_D @ T_C = 25°C	1.0 (See Fig. 13)		W
Linear Derating Factor		0.008 (See Fig. 13)		W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	370		mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150		°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)		°C

IRFD9120
IRFD9123

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFD9120	-100	—	—	V	V_{GS} = 0 V
		IRFD9123	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFD9120	-1	—	—	A	V_{DS} > $I_{D(on)}$ x $r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFD9123	-0.08	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFD9120	—	0.5	0.6	Ω	V_{GS} = 10 V, I_D = -0.8A
		IRFD9123	—	0.6	0.8	Ω	
Forward Transconductance ②	g_{fs}	ALL	0.8	1.2	—	S(℧)	V_{DS} ≤ 50 V, I_D = -0.8 A
Input Capacitance	C_{iss}	ALL	—	300	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 9
Output Capacitance	C_{oss}	ALL	—	200	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	25	50	ns	V_{DD} = 0.5 I_D = -0.8 A, Z_O = 50 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	50	100	ns	
Fall Time	t_f	ALL	—	50	100	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	20	nC	V_{GS} = -15 V, I_D = -4 A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	9	13.5	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	7	10.5	nC	
Internal Drain Inductance	L_D	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from header to center die.
Internal Source Inductance	L_S	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device

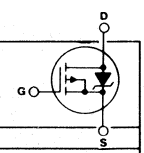


THERMAL RESISTANCE

Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	120	°C/W	Typical socket mount

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFD9120	—	—	-1	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD9123	—	—	-0.8	A	
Pulse Source Current (Body Diode)	I_{SM}	IRFD9120	—	—	-8	A	
		IRFD9123	—	—	-6.4	A	
Diode Forward Voltage ②	V_{SD}	IRFD9120	—	—	-1.5	V	T_C = 25°C, I_S = -1 A, V_{GS} = 0 V
		IRFD9123	—	—	-1.5	V	T_C = 25°C, I_S = -0.8 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	150	—	ns	T_J = 150°C, I_F = -4 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.9	—	μC	T_J = 150°C, I_F = -4 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.

④ V_{DD} = 25 V, Starting T_j = 25°C, L = 555 mH, R_G = 25 Ω, Peak I_L = 1 A (See Figs. 14 & 15).

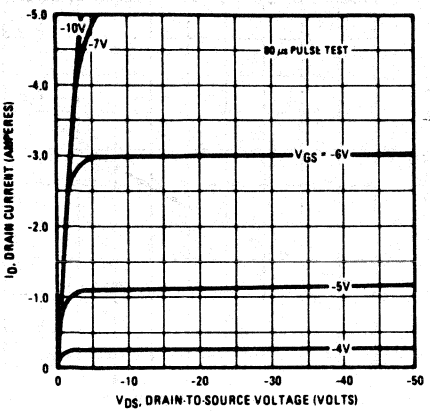


Fig. 1 - Typical output characteristics.

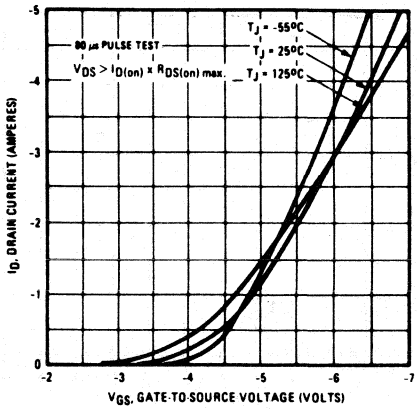


Fig. 2 - Typical transfer characteristics.

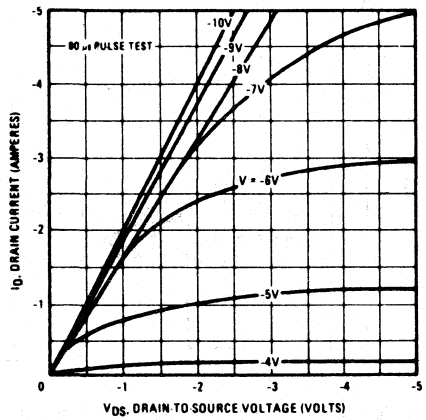


Fig. 3 - Typical saturation characteristics.

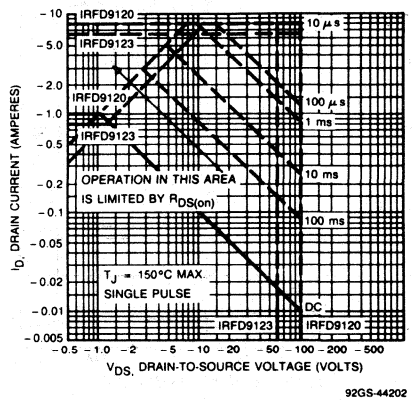


Fig. 4 - Maximum safe operating area.

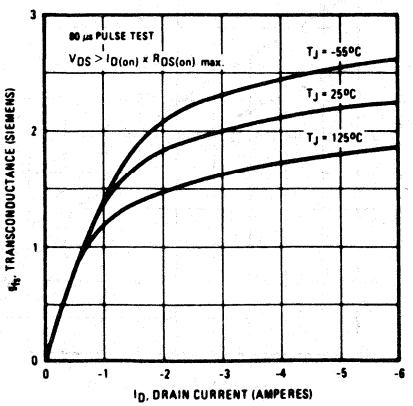


Fig. 5 - Typical transconductance vs. drain current.

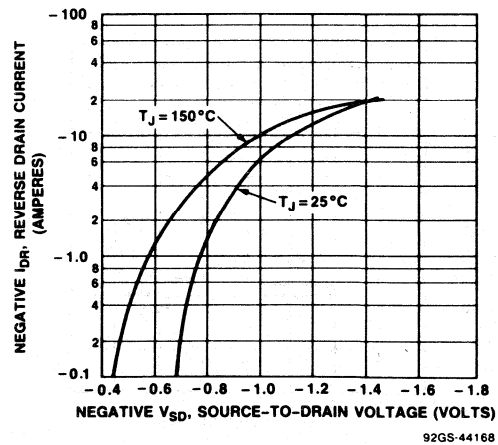


Fig. 6 - Typical source-drain diode forward voltage.

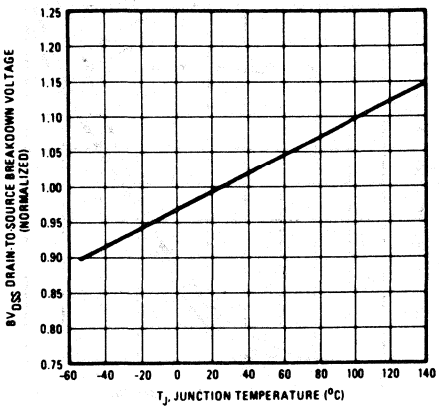


Fig. 7 - Breakdown voltage vs. temperature.

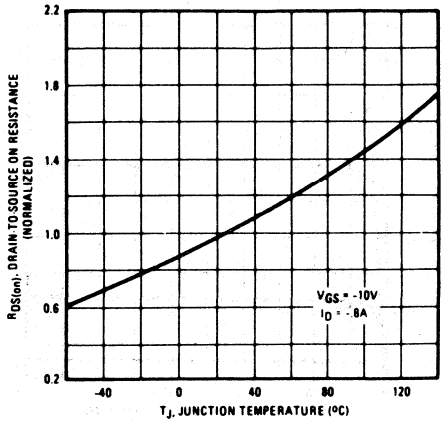


Fig. 8 - Normalized on-resistance vs. temperature.

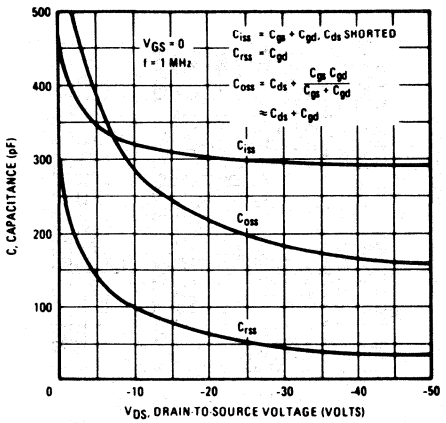


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

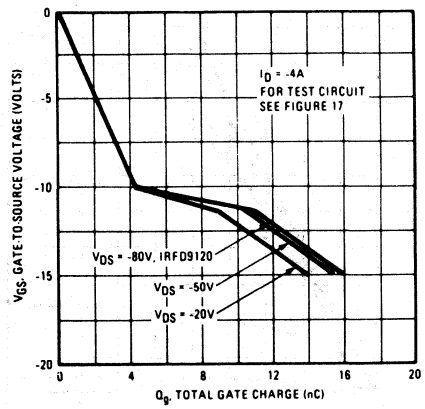


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

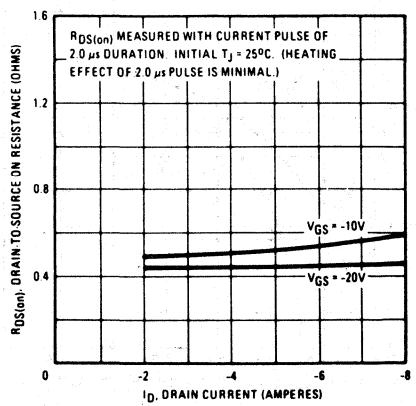


Fig. 11 - Typical on-resistance vs. drain current.

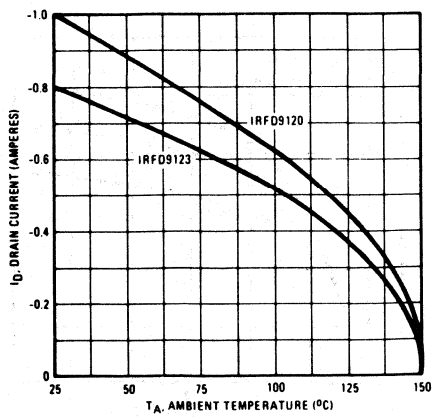


Fig. 12 - Maximum drain current vs. case temperature.

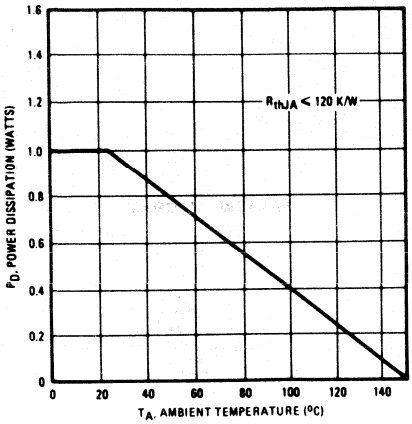


Fig. 13 - Power vs. temperature derating curve.

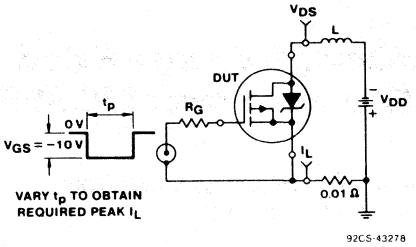


Fig. 14 - Unclamped inductive test circuit.

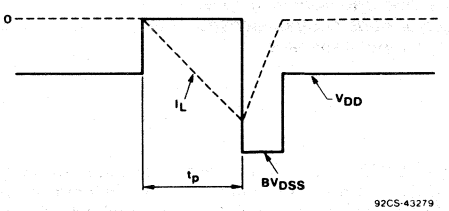


Fig. 15 - Unclamped inductive waveforms.

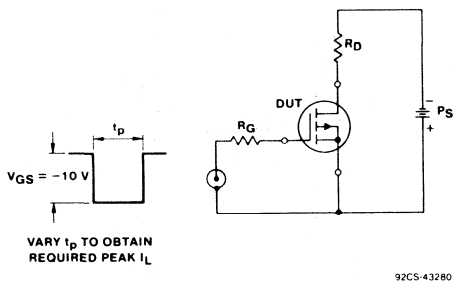


Fig. 16 - Switching time test circuit.

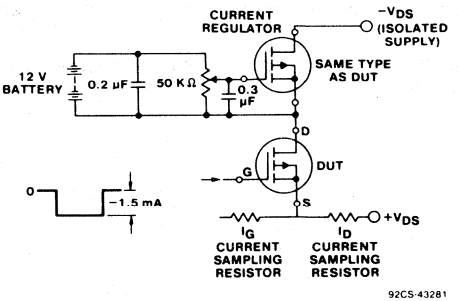


Fig. 17 - Gate charge test circuit.

IRFD9220
IRFD9223

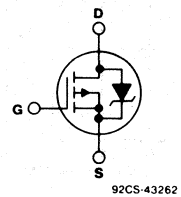
File Number **2286**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-0.45 A and -0.6 A, -150 V and -200 V
$r_{DS(on)}$ = 1.5 Ω and 2.4 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



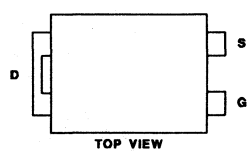
92CS-43262

P-CHANNEL ENHANCEMENT MODE

The IRFD9220 and IRFD9223 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

TERMINAL DESIGNATION



TOP VIEW

4-PIN DIP

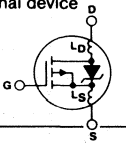
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRFD9220	IRFD9223	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-0.6	-0.45	A
Pulsed Drain Current ③	I_{DM}	-4.8	-3.6	A
Gate-Source Voltage	V_{GS}	±20		V
Maximum Power Dissipation	P_D @ T_C = 25°C	1.0 (See Fig. 13)		W
Linear Derating Factor		0.008 (See Fig. 13)		W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	290		mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150		°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)		°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFD9220	-200	—	—	V	V_{GS} = 0 V
		IRFD9223	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFD9220	-0.6	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFD9223	-0.45	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFD9220	—	1.0	1.5	Ω	V_{GS} = -10 V, I_D = -0.3 A
		IRFD9223	—	1.5	2.4	Ω	
Forward Transconductance ②	g_{fs}	ALL	0.6	1.0	—	S(℧)	$V_{DS} \leq 50$ V, I_D = -0.3 A
Input Capacitance	C_{iss}	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 9
Output Capacitance	C_{oss}	ALL	—	100	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	30	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	15	40	ns	V_{DD} = 0.5 I_D = -0.3 A, Z_O = 50 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	25	50	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	80	120	ns	
Fall Time	t_f	ALL	—	50	75	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	22	nC	V_{GS} = -15 V, I_D = -3.6 A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	10	15	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	4	6	nC	
Internal Drain Inductance	L_D	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from header to center die.
Internal Source Inductance	L_S	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device

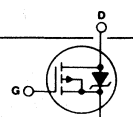


THERMAL RESISTANCE

Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	120	°C/W	Typical socket mount

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFD9220	—	—	-0.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD9223	—	—	-0.45	A	
Pulse Source Current (Body Diode)	I_{SM}	IRFD9220	—	—	-4.8	A	
		IRFD9223	—	—	-3.6	A	
Diode Forward Voltage ②	V_{SD}	IRFD9220	—	—	-1.5	V	T_C = 25°C, I_S = -0.6 A, V_{GS} = 0 V
		IRFD9223	—	—	-1.5	V	T_C = 25°C, I_S = -0.45 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	150	—	ns	T_J = 150°C, I_F = -0.6 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.5	—	μC	T_J = 150°C, I_F = -0.6 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25 V, Starting T_J = 25°C, L = 1210 mH, R_G = 25 Ω, Peak I_L = 0.6 A (See Figs. 14 & 15).

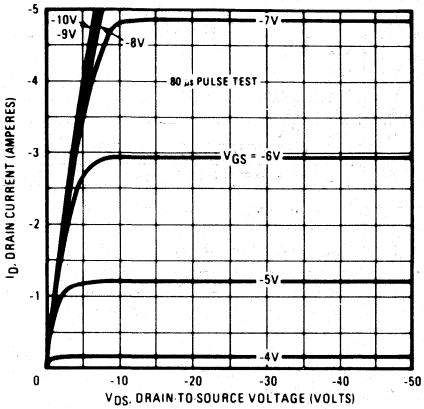


Fig. 1 - Typical output characteristics.

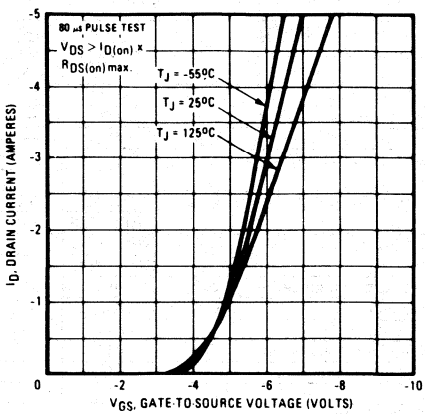


Fig. 2 - Typical transfer characteristics.

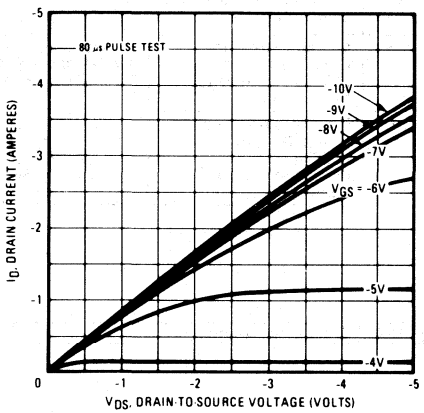


Fig. 3 - Typical saturation characteristics.

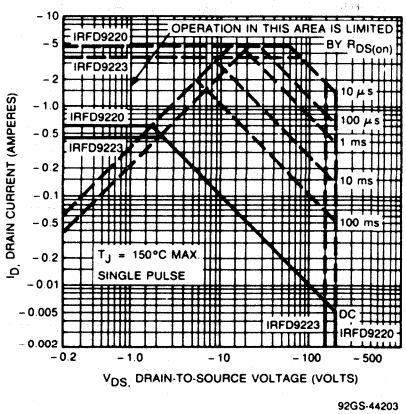


Fig. 4 - Maximum safe operating area.

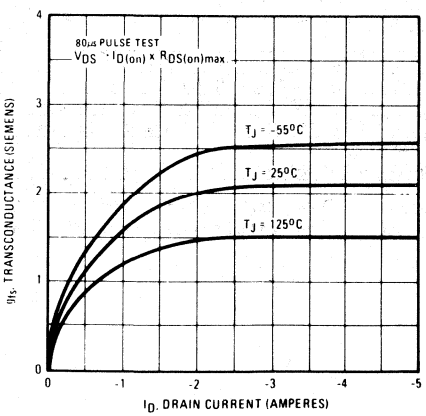


Fig. 5 - Typical transconductance vs. drain current.

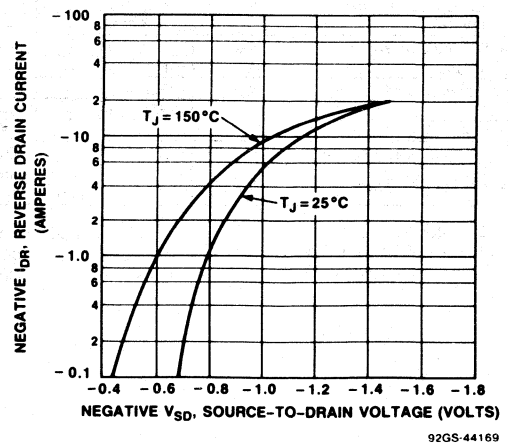


Fig. 6 - Typical source-drain diode forward voltage.

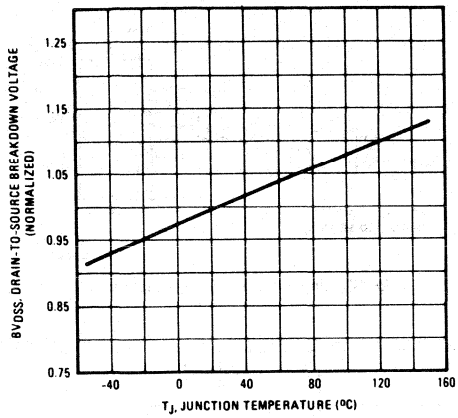


Fig. 7 - Breakdown voltage vs. temperature.

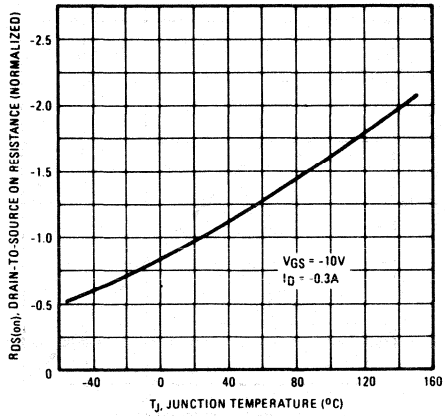


Fig. 8 - Normalized on-resistance vs. temperature.

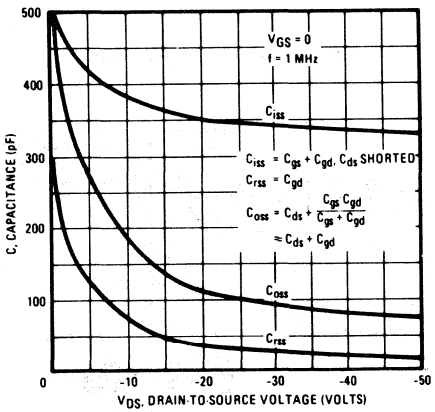


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

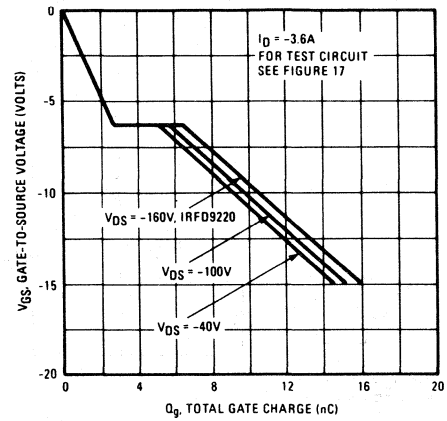


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

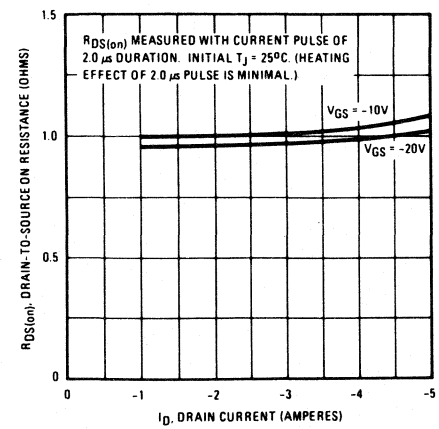


Fig. 11 - Typical on-resistance vs. drain current.

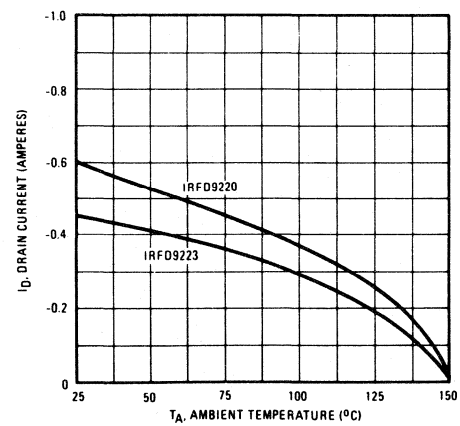


Fig. 12 - Maximum drain current vs. case temperature.

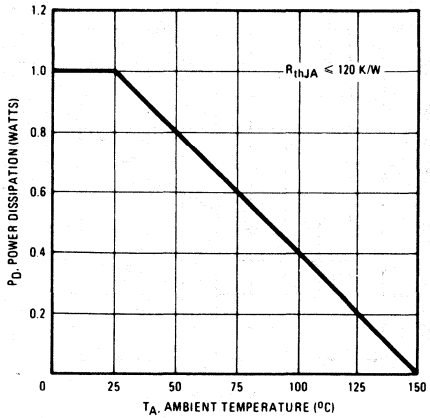


Fig. 13 - Power vs. temperature derating curve.

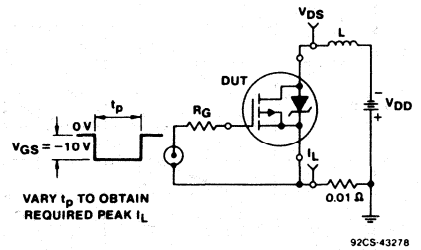


Fig. 14 - Unclamped inductive test circuit.

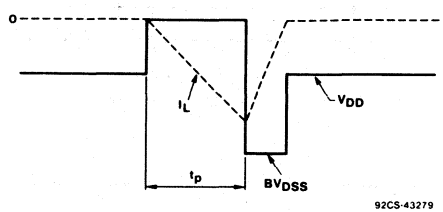


Fig. 15 - Unclamped inductive waveforms.

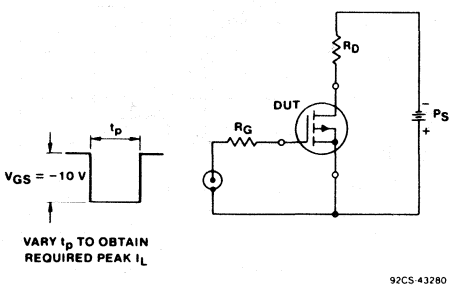


Fig. 16 - Switching time test circuit.

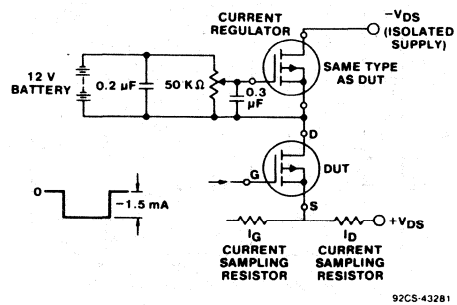


Fig. 17 - Gate charge test circuit.

File Number **2287**

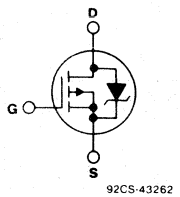
IRFF9120, IRFF9121
IRFF9122, IRFF9123

Avalanche-Energy-Rated P-Channel Power MOSFETs

-3.5 A and -4 A, -60 V, -100 V
$r_{DS(on)}$ = 0.60 Ω and 0.80 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

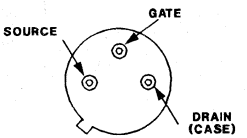


P-CHANNEL ENHANCEMENT MODE

The IRFF9120, IRFF9121, IRFF9122 and IRFF9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

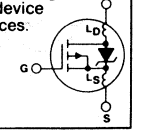
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRFF9120	IRFF9121	IRFF9122	IRFF9123	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current	I_D @ T_C = 25°C	-4	-4	-3.5	-3.5	A
Pulsed Drain Current ③	I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	20 (See Fig. 14)				W
Linear Derating Factor		0.16 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	370				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFF9120 IRFF9122	-100	—	—	V	V_{GS} = 0 V
		IRFF9121 IRFF9123	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFF9120 IRFF9121	-4	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFF9122 IRFF9123	-3.5	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFF9120 IRFF9121	—	0.5	0.6	Ω	V_{GS} = -10 V, I_D = -2 A
		IRFF9122 IRFF9123	—	0.6	0.8	Ω	
Forward Transconductance ②	g_{fs}	ALL	1.25	2	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = -2 A
Input Capacitance	C_{iss}	ALL	—	300	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	200	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	25	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -2 A, Z_O = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	50	100	ns	
Fall Time	t_f	ALL	—	50	100	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	22	nC	V_{GS} = -15 V, I_D = -8 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	9	13.5	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	7	10.5	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
Internal Source Inductance	L_S	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

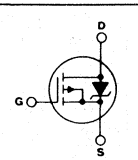


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	6.25	°C/W	
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	175	°C/W	Typical socket mount.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFF9120 IRFF9121	—	—	-4	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF9122 IRFF9123	—	—	-3.5	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFF9120 IRFF9121	—	—	-16	A	
		IRFF9122 IRFF9123	—	—	-14	A	
Diode Forward Voltage ②	V_{SD}	IRFF9120 IRFF9121	—	—	-1.5	V	T_C = 25°C, I_S = -4 A, V_{GS} = 0 V
		IRFF9122 IRFF9123	—	—	-1.5	V	T_C = 25°C, I_S = -3.5 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	230	—	ns	T_J = 150°C, I_F = -4 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	1.3	—	μC	T_J = 150°C, I_F = -4 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25 V, Starting T_j = 25°C, L = 34.7 mH, R_G = 25 Ω, Peak I_L = 4 A (See Figs. 15 & 16).

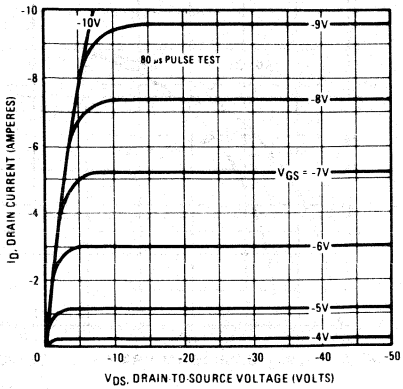


Fig. 1 - Typical output characteristics.

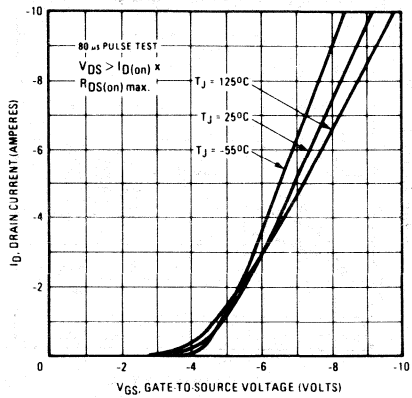


Fig. 2 - Typical transfer characteristics.

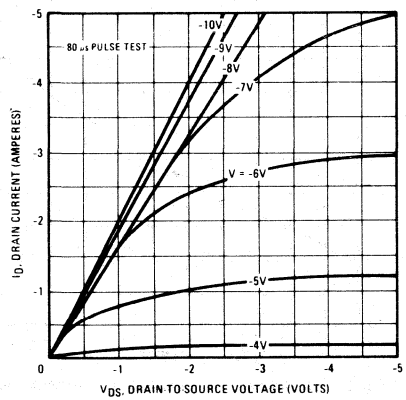


Fig. 3 - Typical saturation characteristics.

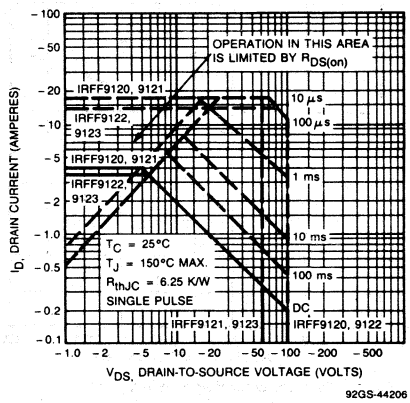


Fig. 4 - Maximum safe operating area.

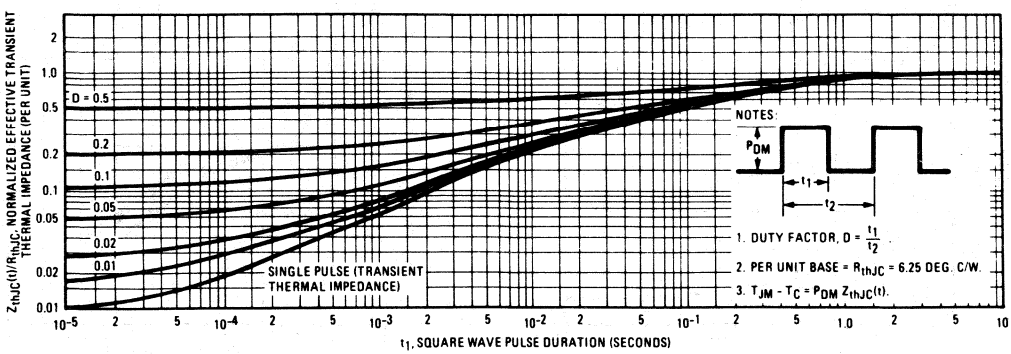


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

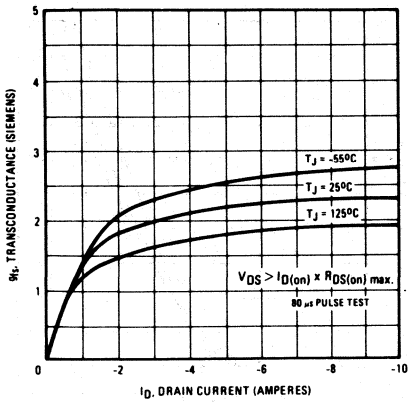


Fig. 6 - Typical transconductance vs. drain current.

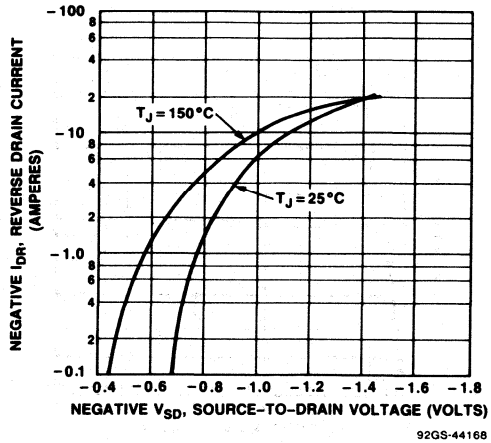


Fig. 7 - Typical source-drain diode forward voltage.

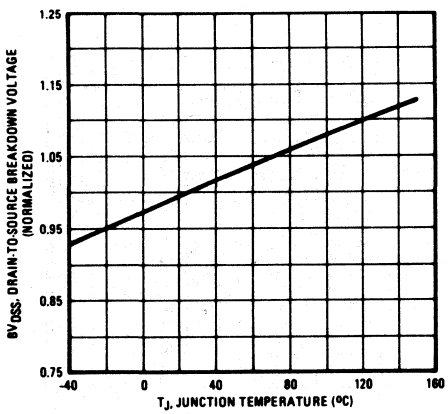


Fig. 8 - Breakdown voltage vs. temperature.

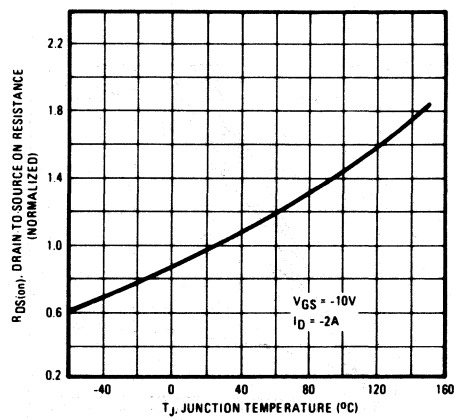


Fig. 9 - Normalized on-resistance vs. temperature.

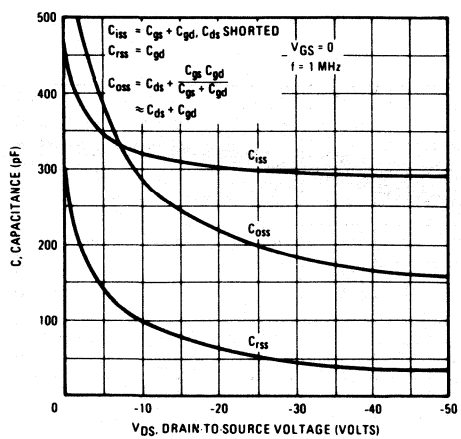


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

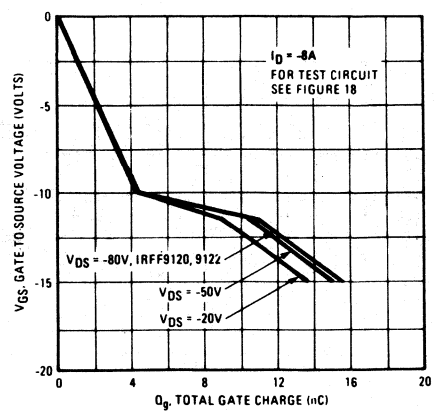


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

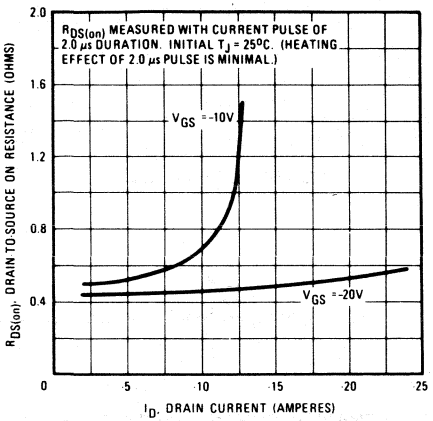


Fig. 12 - Typical on-resistance vs. drain current.

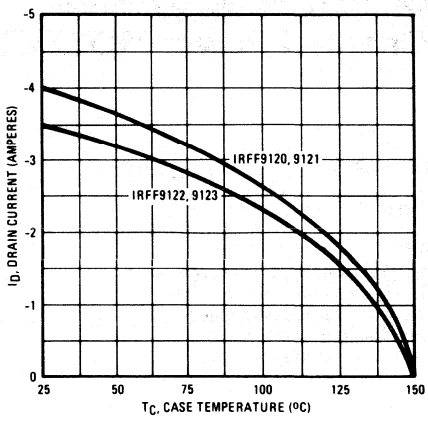


Fig. 13 - Maximum drain current vs. case temperature.

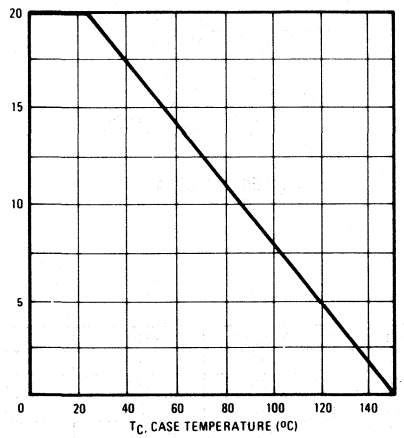


Fig. 14 - Power vs. temperature derating curve.

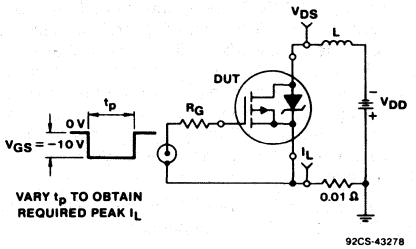


Fig. 15 - Unclamped inductive test circuit.

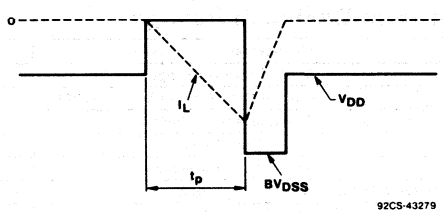


Fig. 16 - Unclamped inductive waveforms.

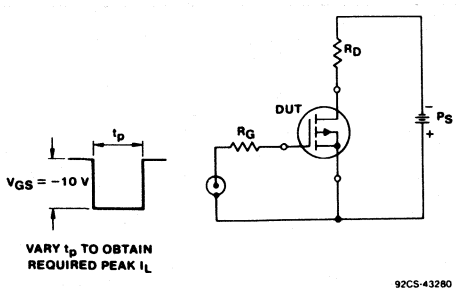


Fig. 17 - Switching time test circuit.

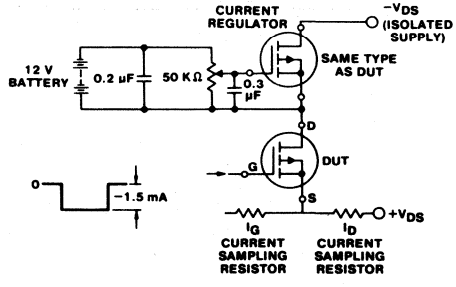


Fig. 18 - Gate charge test circuit.

IRFF9130, IRFF9131
IRFF9132, IRFF9133

File Number **2216**

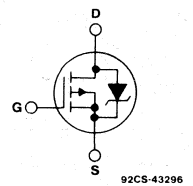
Avalanche-Energy-Rated P-Channel Power MOSFETs

-5.5A and -6.5A, -60V and -100V
r_{DS} (on) = 0.30Ω and 0.40Ω

Features:

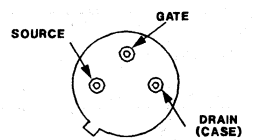
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF9130, IRFF9131, IRFF9132 and IRFF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

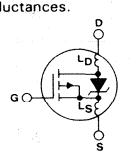
Absolute Maximum Ratings

Parameter		IRFF9130	IRFF9131	IRFF9132	IRFF9133	Units
V_{DS}	Drain – Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-6.5	-6.5	-5.5	-5.5	A
I_{DM}	Pulsed Drain Current ③	-26	-26	-22	-22	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
E_{AS}	Single Pulse Avalanche Energy ④	500				mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFF9130 IRFF9132	-100	–	–	V	V_{GS} = 0V
		IRFF9131 IRFF9133	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	-100	nA	V_{GS} = -20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF9130 IRFF9131	-6.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRFF9132 IRFF9133	-5.5	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFF9130 IRFF9131	–	0.25	0.30	Ω	V_{GS} = -10V, I_D = -3.0A
		IRFF9132 IRFF9133	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -3.0A
C_{iss}	Input Capacitance	ALL	–	500	—	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = -3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	70	140	ns	
t_f	Fall Time	ALL	–	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	25	45	nC	V_{GS} = -15V, I_D = -15A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	12	22	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

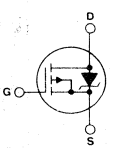


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	ALL	–	–	5.0	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	ALL	–	–	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF9130 IRFF9131	–	–	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF9132 IRFF9133	–	–	-5.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF9130 IRFF9131	–	–	-26	A	
		IRFF9132 IRFF9133	–	–	-22	A	
V_{SD}	Diode Forward Voltage ②	IRFF9130 IRFF9131	–	–	-1.5	V	T_C = 25°C, I_S = -6.5A, V_{GS} = 0V
		IRFF9132 IRFF9133	–	–	-1.5	V	T_C = 25°C, I_S = -5.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.8	–	μC	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 25V, starting T_J = 25°C, L = 17.75 mH, R_G = 25Ω, Peak I_L = 6.5A. (See Fig. 15 and 16)

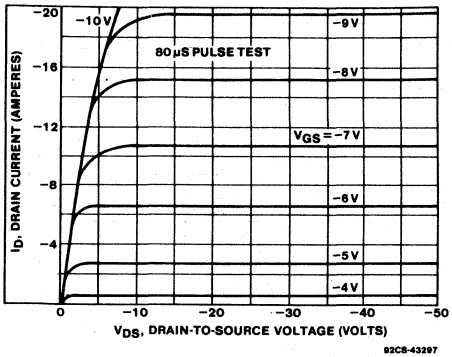


Fig. 1 - Typical Output Characteristics

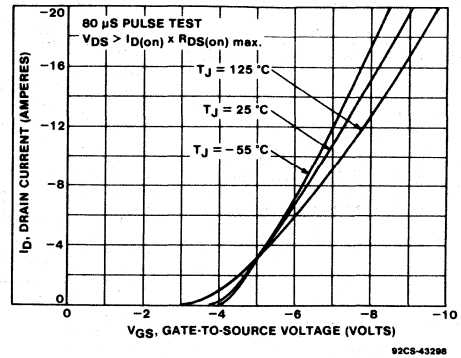


Fig. 2 - Typical Transfer Characteristics

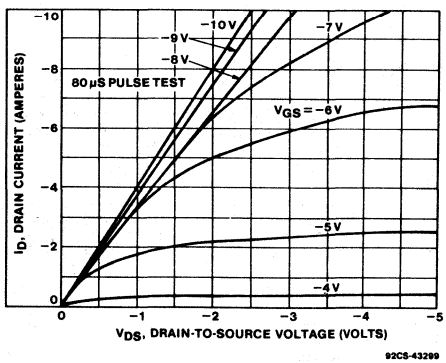


Fig. 3 - Typical Saturation Characteristics

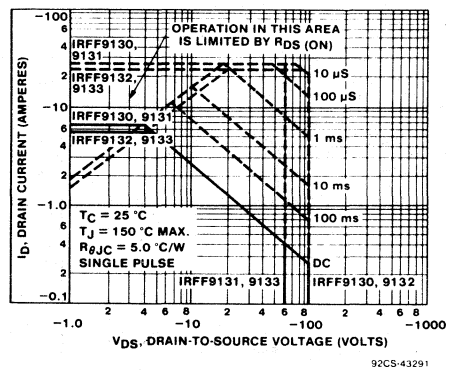


Fig. 4 - Maximum Safe Operating Area

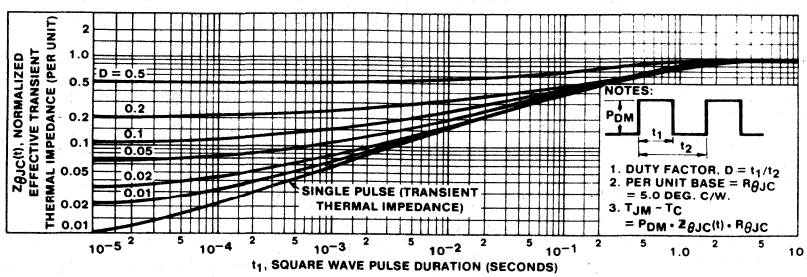


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

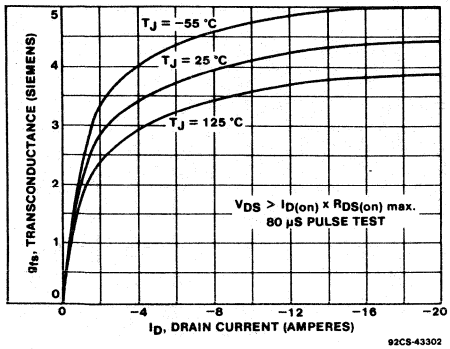


Fig. 6 - Typical Transconductance Vs. Drain Current

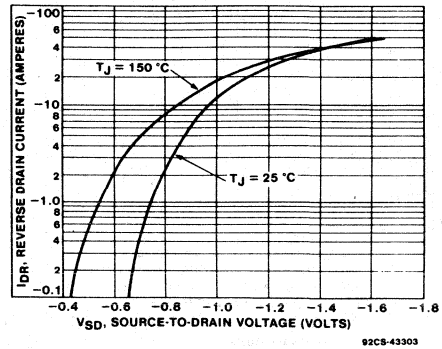


Fig. 7 - Typical Source-Drain Diode Forward Voltage

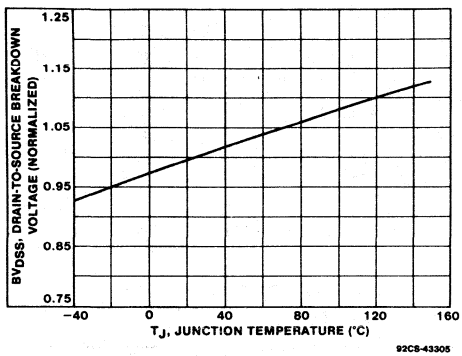


Fig. 8 - Breakdown Voltage Vs. Temperature

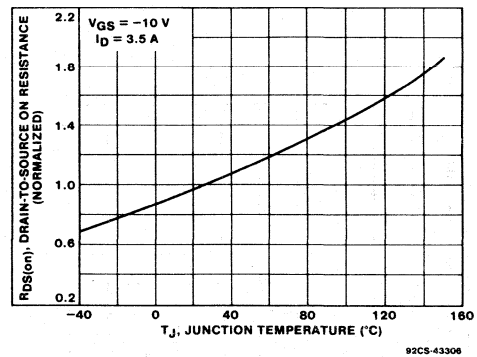


Fig. 9 - Normalized On-Resistance Vs. Temperature

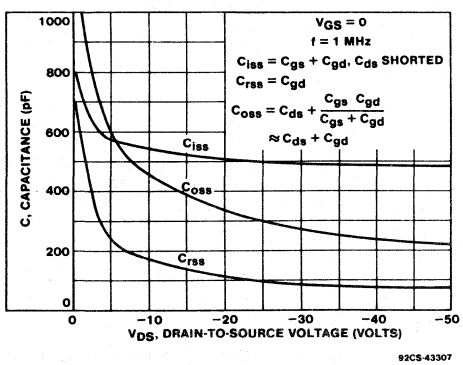


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

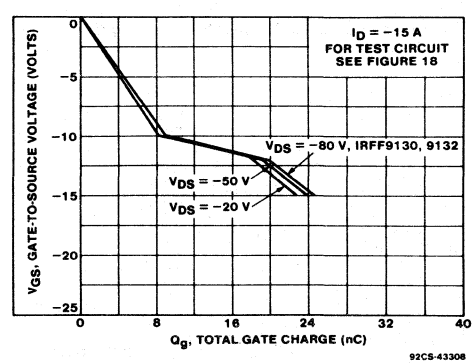


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

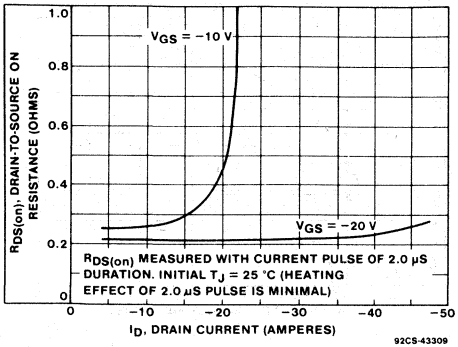


Fig. 12 - Typical On-Resistance Vs. Drain Current

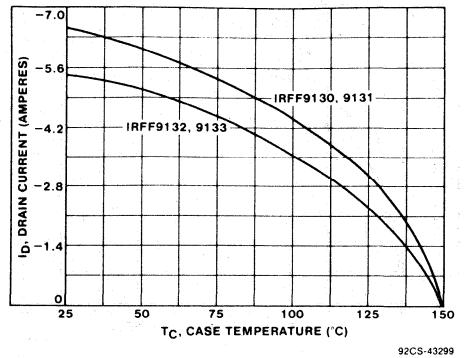


Fig. 13 - Maximum Drain Current Vs. Case Temperature

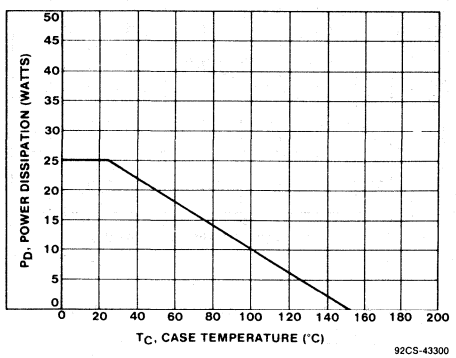


Fig. 14 - Power Vs. Temperature Derating Curve

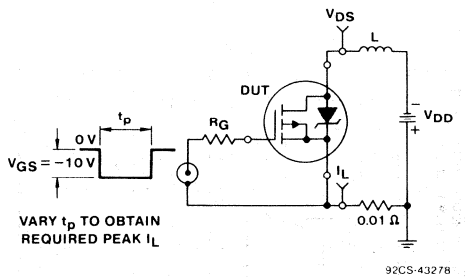


Fig. 15 - Unclamped Inductive Test Circuit

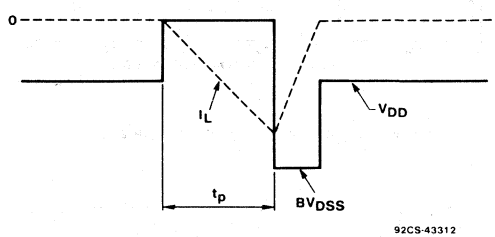


Fig. 16 - Unclamped Inductive Waveforms

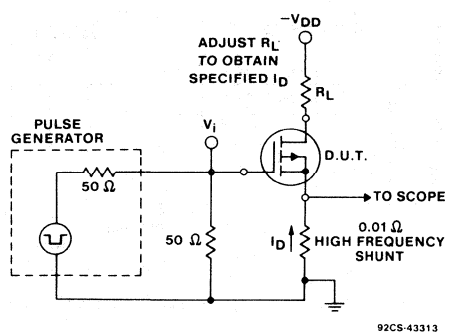


Fig. 17 - Switching Time Test Circuit

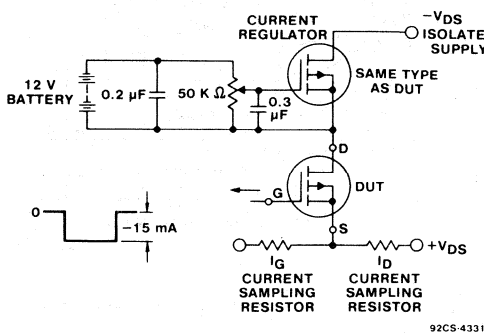


Fig. 18 - Gate Charge Test Circuit

File Number **2288**

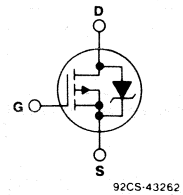
IRFF9220, IRFF9221
IRFF9222, IRFF9223

Avalanche-Energy-Rated P-Channel Power MOSFETs

-2 A and -2.5 A, -150 V and -200 V
$r_{DS(on)}$ = 1.5 Ω and 2.4 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

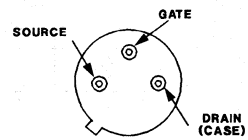


P-CHANNEL ENHANCEMENT MODE

The IRFF9220, IRFF9221, IRFF9222, and IRFF9223 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (Low-Profile TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

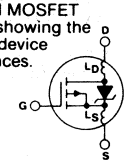
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRFF9220	IRFF9221	IRFF9222	IRFF9223	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-2.5	-2.5	-2	-2	A
Pulsed Drain Current ③	I_{DM}	-10	-10	-8	-8	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	20 (See Fig. 14)				W
Linear Derating Factor		0.16 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	290				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

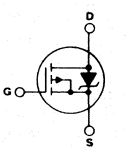
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFF9220 IRFF9222	-200	—	—	V	V_{GS} = 0 V
		IRFF9221 IRFF9223	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFF9220 IRFF9221	-2.5	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFF9222 IRFF9223	-2	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFF9220 IRFF9221	—	1	1.5	Ω	V_{GS} = 10 V, I_D = 1.5 A
		IRFF9222 IRFF9223	—	1.5	2.4	Ω	
Forward Transconductance ②	g_{fs}	ALL	1	1.8	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = 1.5 A
Input Capacitance	C_{iss}	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	100	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	30	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	15	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -1.5 A, Z_O = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	25	50	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	80	120	ns	
Fall Time	t_f	ALL	—	50	75	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	22	nC	V_{GS} = -15 V, I_D = -4 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	9	13.5	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	7	10.5	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
Internal Source Inductance	L_S	ALL	—	15.0	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header and source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	6.25	°C/W	
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	175	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFF9220 IRFF9221	—	—	-2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF9222 IRFF9223	—	—	-2	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFF9220 IRFF9221	—	—	-10	A	
		IRFF9222 IRFF9223	—	—	-7	A	
Diode Forward Voltage ②	V_{SD}	IRFF9220 IRFF9221	—	—	-1.5	V	T_C = 25°C, I_S = -2.5 A, V_{GS} = 0 V
		IRFF9222 IRFF9223	—	—	-1.5	V	T_C = 25°C, I_S = -2 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	300	—	ns	T_J = 150°C, I_F = -2.5 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	1.9	—	μC	T_J = 150°C, I_F = -2.5 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_j = 25°C, L = 69.6 mH, R_G = 25 Ω, Peak I_L = 2.5 A (See Figs. 15 & 16).

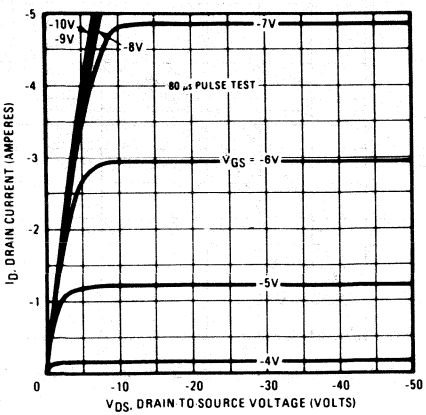


Fig. 1 - Typical output characteristics.

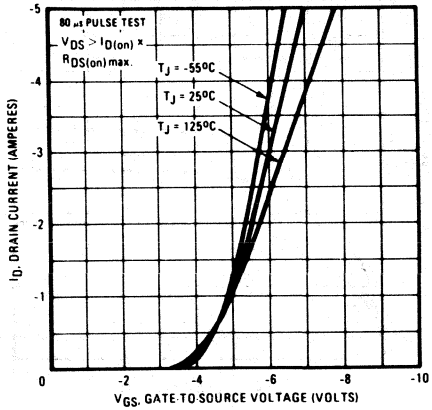


Fig. 2 - Typical transfer characteristics.

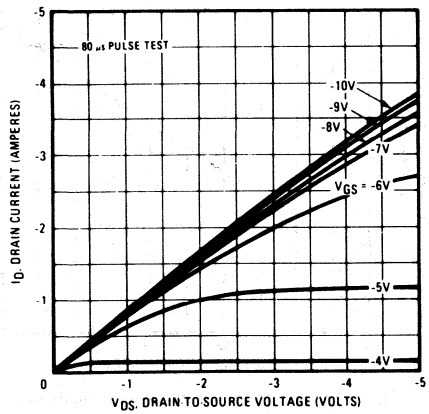


Fig. 3 - Typical saturation characteristics.

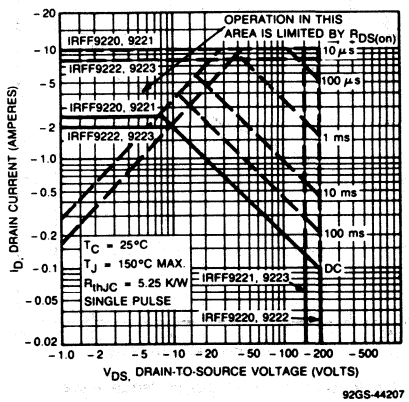


Fig. 4 - Maximum safe operating area.

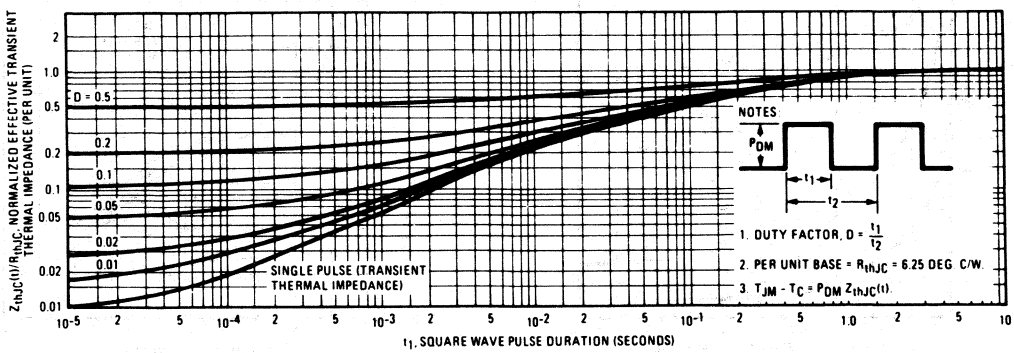


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

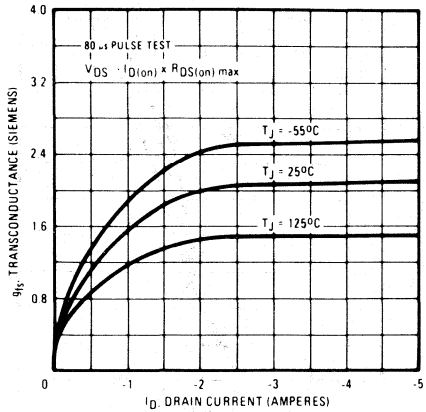


Fig. 6 - Typical transconductance vs. drain current.

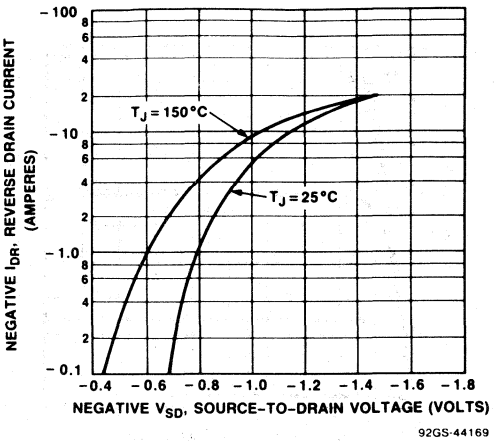


Fig. 7 - Typical source-drain diode forward voltage.

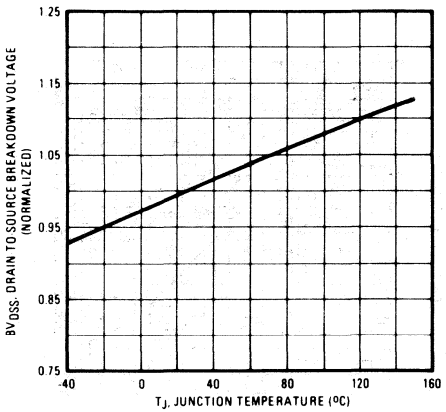


Fig. 8 - Breakdown voltage vs. temperature.

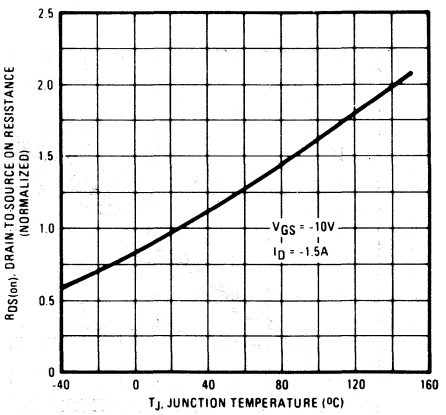


Fig. 9 - Normalized on-resistance vs. temperature.

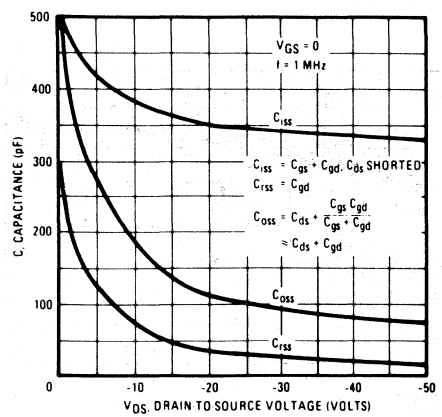


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

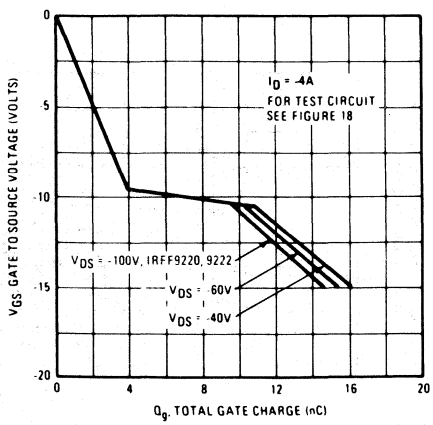


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

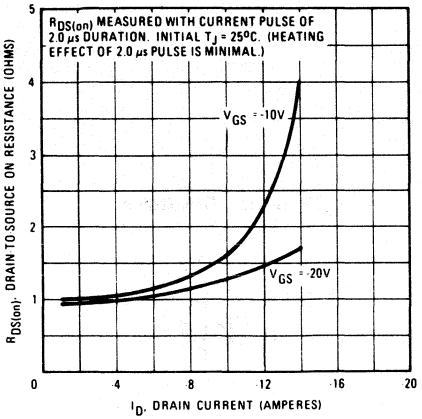


Fig. 12 - Typical on-resistance vs. drain current.

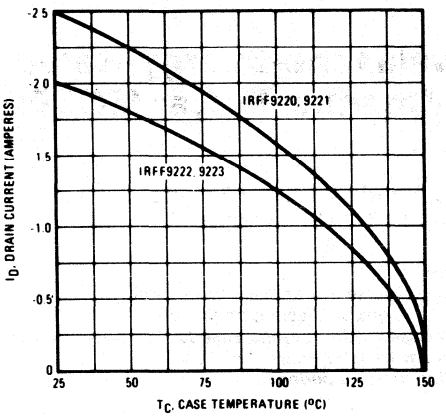


Fig. 13 - Maximum drain current vs. case temperature.

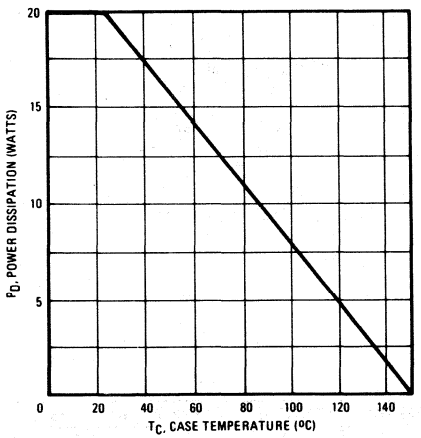


Fig. 14 - Power vs. temperature derating curve.

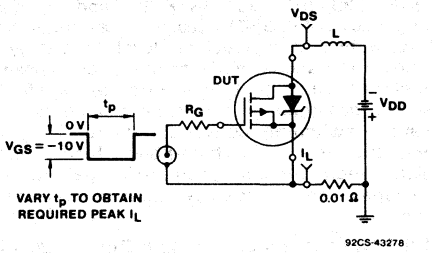


Fig. 15 - Unclamped inductive test circuit.

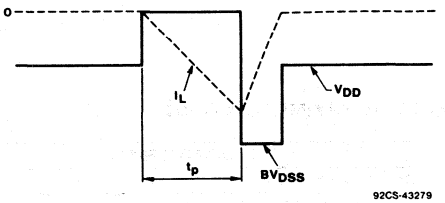


Fig. 16 - Unclamped inductive waveforms.

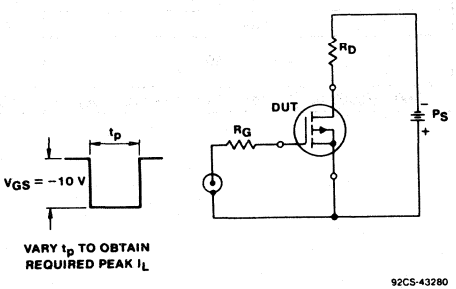


Fig. 17 - Switching time test circuit.

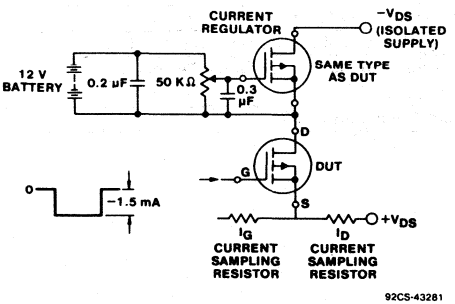


Fig. 18 - Gate charge test circuit.

IRFF9230, IRFF9231, IRFF9232, IRFF9233

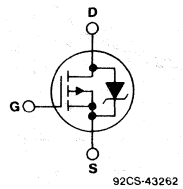
File Number **2225**

Avalanche-Energy-Rated P-Channel Power MOSFETs

-3.5 A and -4.0 A, -150 V and -200 V
$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



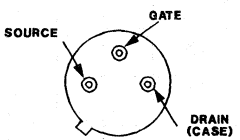
92CS-43262

P-CHANNEL ENHANCEMENT MODE

The IRFF9230, IRFF9231, IRFF9232 and IRFF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (Low-Profile TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

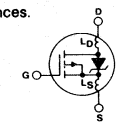
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRFF9230	IRFF9231	IRFF9232	IRFF9233	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current ③	I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	25 (See Fig. 14)				W
Linear Derating Factor		0.2 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	500				mj
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. (1.6 mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS, At T_C = 25°C (Unless Otherwise Specified)

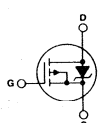
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFF9230 IRFF9232	-200	—	—	V	V_{GS} = 0 V
		IRFF9231 IRFF9233	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS}(th)$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_D(on)$	IRFF9230 IRFF9231	-4.0	—	—	A	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., V_{GS} = -10 V
		IRFF9232 IRFF9233	-3.5	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS}(on)$	IRFF9230 IRFF9231	—	0.5	0.8	Ω	V_{GS} = -10 V, I_D = -2.0 A
		IRFF9232 IRFF9233	—	0.8	1.2	Ω	
Forward Transconductance ②	g_{fs}	ALL	2.2	3.5	—	S (℧)	$V_{DS} > I_D(on) \times r_{DS}(on)$ max., I_D = 2.0 A
Input Capacitance	C_{iss}	ALL	—	550	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	170	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	—	pF	
Turn-On Delay Time	$t_d(on)$	ALL	—	30	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0 A, Z_o = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_d(off)$	ALL	—	50	100	ns	
Fall Time	t_f	ALL	—	40	80	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	31	45	nC	V_{GS} = -15 V, I_D = -8.0 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	18	26	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	13	19	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
Internal Source Inductance	L_S	ALL	—	15.0	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.
Junction-to-Case	$R_{\theta JC}$	ALL	—	—	5.0	°C/W	
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	175	°C/W	Typical socket mount.

Modified MOSFET symbol showing the internal device inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFF9230 IRFF9231	—	—	-4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF9232 IRFF9233	—	—	-3.5	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFF9230 IRFF9231	—	—	-16	A	
		IRFF9232 IRFF9233	—	—	-14	A	
Diode Forward Voltage ②	V_{SD}	IRFF9230 IRFF9231	—	—	-1.5	V	T_C = 25°C, I_S = -4.0 A, V_{GS} = 0 V
		IRFF9232 IRFF9233	—	—	-1.5	V	T_C = 25°C, I_S = -3.5 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	400	—	ns	T_J = 150°C, I_F = -4.0 A, di_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	2.6	—	μC	T_J = 150°C, I_F = -4.0 A, di_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300 μs. Duty Cycle ≤ 2%

③ Repetitive Rating: Pulse width limited by max. junction temperature See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50 V, Starting T_J = 25°C, L = 46.9 mH, R_G = 25 Ω, Peak I_L = 4.0 A (See Figs. 15 & 16).

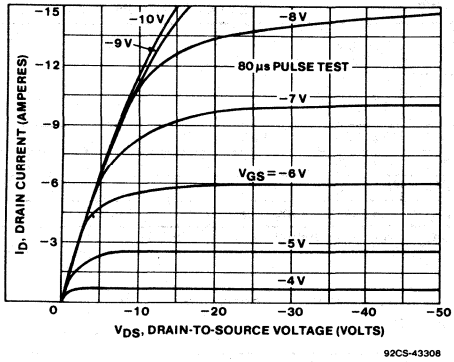


Fig. 1 - Typical output characteristics.

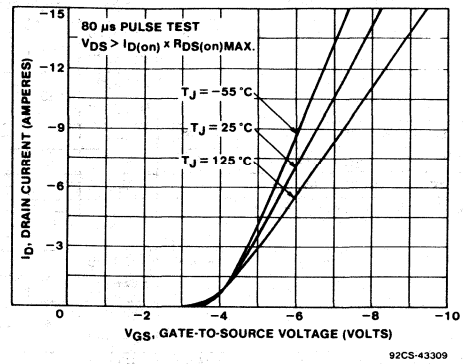


Fig. 2 - Typical transfer characteristics.

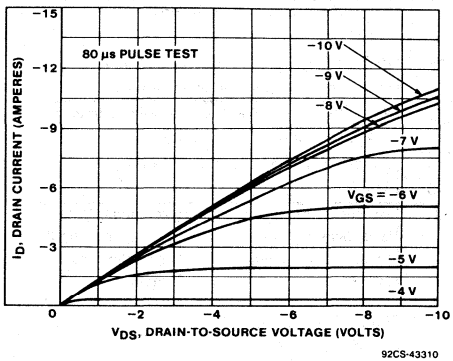


Fig. 3 - Typical saturation characteristics.

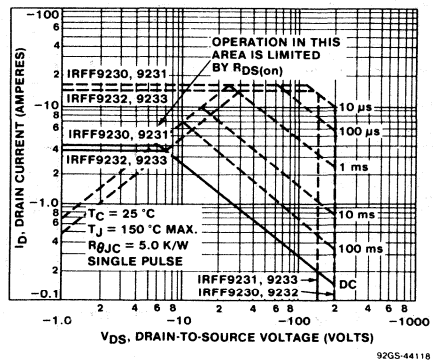


Fig. 4 - Maximum safe operating area.

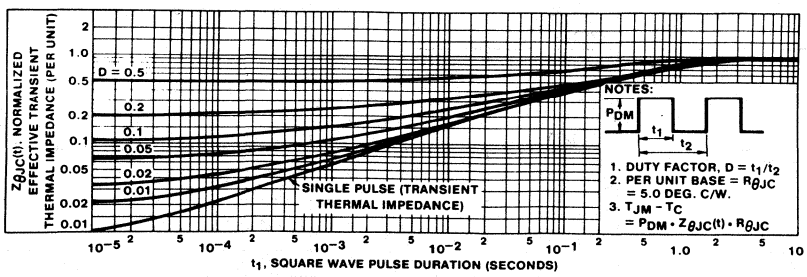


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

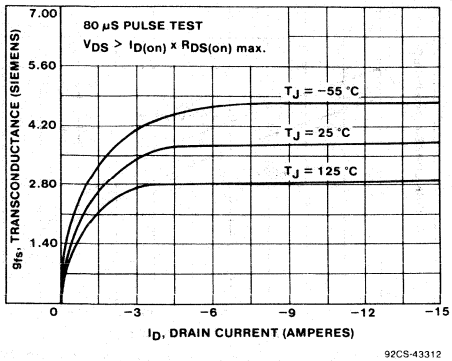


Fig. 6 - Typical transconductance vs. drain current.

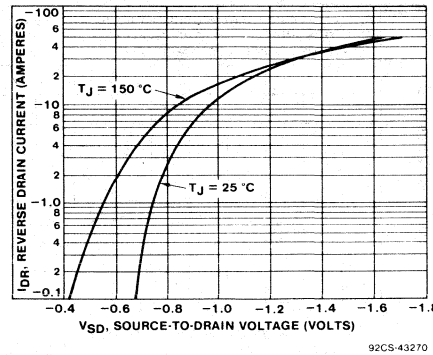


Fig. 7 - Typical source-drain diode forward voltage.

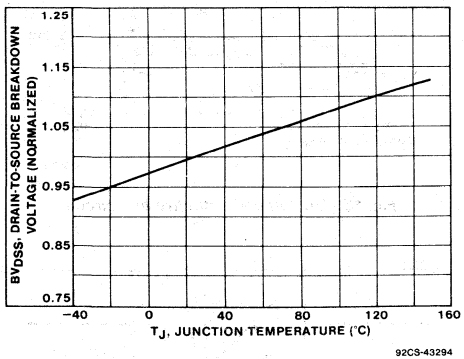


Fig. 8 - Breakdown voltage vs. temperature.

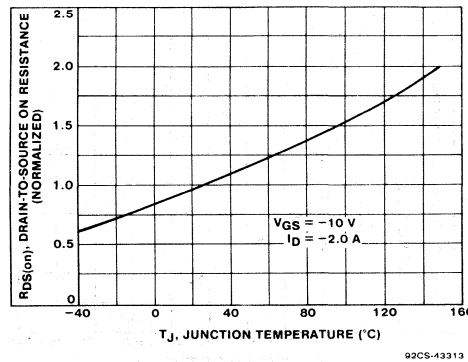


Fig. 9 - Normalized on-resistance vs. temperature.

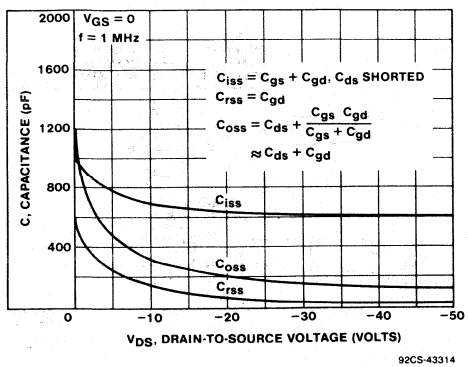


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

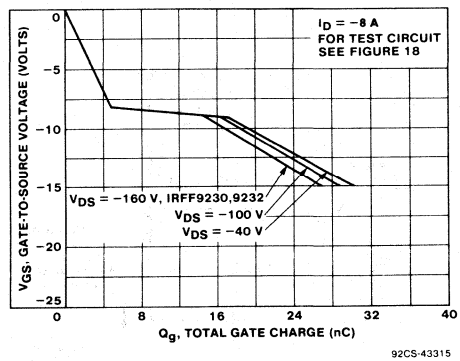


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

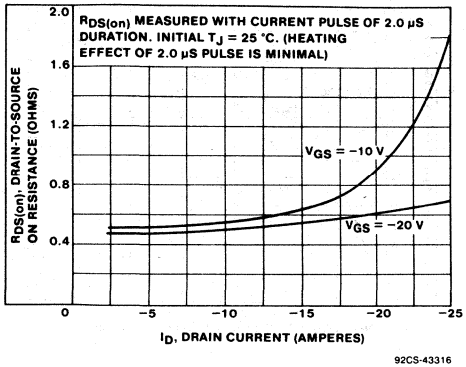


Fig. 12 - Typical on-resistance vs. drain current.

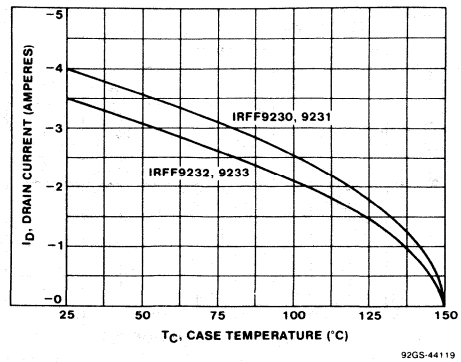


Fig. 13 - Maximum drain current vs. case temperature.

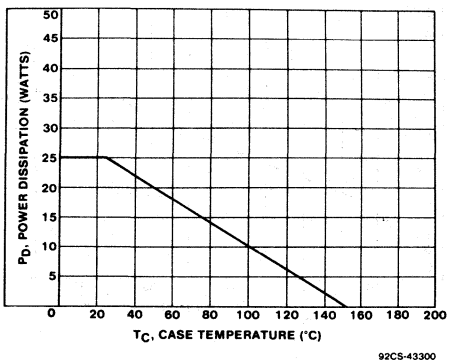


Fig. 14 - Power vs. temperature derating curve.

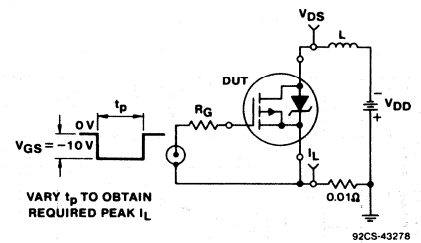


Fig. 15 - Unclamped inductive test circuit.

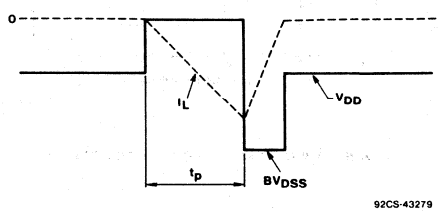


Fig. 16 - Unclamped inductive waveforms.

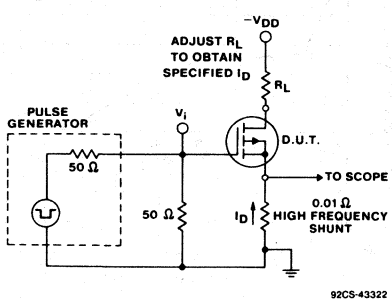


Fig. 17 - Switching time test circuit.

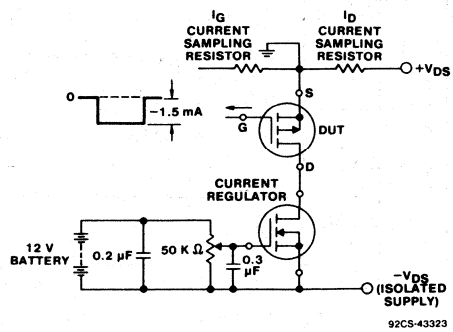


Fig. 18 - Gate charge test circuit.

File Number **2292**

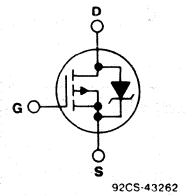
IRFP9140R, IRFP9141R, IRFP9142R, IRFP9143R

Avalanche-Energy-Rated P-Channel Power MOSFETs

-19 A and -16 A, -60 V, -100 V
$r_{DS(on)}$ = 0.20 Ω and 0.30 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

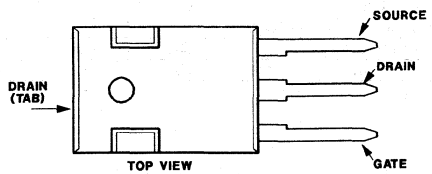


P-CHANNEL ENHANCEMENT MODE

The IRFP9140R, IRFP9141R, IRFP9142R and IRFP9143R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

ABSOLUTE-MAXIMUM RATINGS

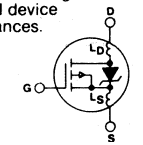
CHARACTERISTIC		IRFP9140R	IRFP9141R	IRFP9142R	IRFP9143R	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current	I_D @ T_C = 25°C	-19	-19	-16	-16	A
Continuous Drain Current	I_D @ T_C = 100°C	-12	-12	-10	-10	A
Pulsed Drain Current ③	I_{DM}	-76	-76	-64	-64	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	150 (See Fig. 14)				W
Linear Derating Factor		1.2 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	960				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

IRFP9140R, IRFP9141R, IRFP9142R, IRFP9143R

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFP9140R IRFP9142R	-100	—	—	V	V_{GS} = 0 V
		IRFP9141R IRFP9143R	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFP9140R IRFP9141R	-19	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\,max.}$, V_{GS} = -10 V
		IRFP9142R IRFP9143R	-16	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFP9140R IRFP9141R	—	0.14	0.20	Ω	V_{GS} = -10 V, I_D = -10 A
		IRFP9142R IRFP9143R	—	0.20	0.30	Ω	
Forward Transconductance ②	g_{fs}	ALL	3.8	5.7	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\,max.}$, I_D = 15 A
Input Capacitance	C_{iss}	ALL	—	1200	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	570	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	160	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	16	20	ns	V_{DD} = -50 V, I_D = -18 A, Z_O = 9.1 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	65	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	47	70	ns	
Fall Time	t_f	ALL	—	28	70	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	37	55	nC	V_{GS} = -10 V, I_D = -18 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	8.7	13	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	22	34	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	ALL	—	13	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

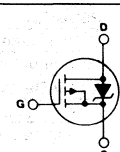


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	0.83	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.24	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	30	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFP9140R IRFP9141R	—	—	-19	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP9142R IRFP9143R	—	—	-19	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFP9140R IRFP9141R	—	—	-76	A	
		IRFP9142R IRFP9143R	—	—	-76	A	
Diode Forward Voltage ②	V_{SD}	IRFP9140R IRFP9141R	—	—	-1.5	V	T_C = 25°C, I_S = -19 A, V_{GS} = 0 V
		IRFP9142R IRFP9143R	—	—	-1.5	V	T_C = 25°C, I_S = -19 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	210	—	ns	T_J = 150°C, I_F = -19 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	2.0	—	μC	T_J = 150°C, I_F = -19 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_j = 25°C, L = 4.2 mHμ, R_{GS} = 25 Ω, I_{PEAK} = 19 A (See Figs. 15 & 16).

IRFP9140R, IRFP9141R, IRFP9142R, IRFP9143R

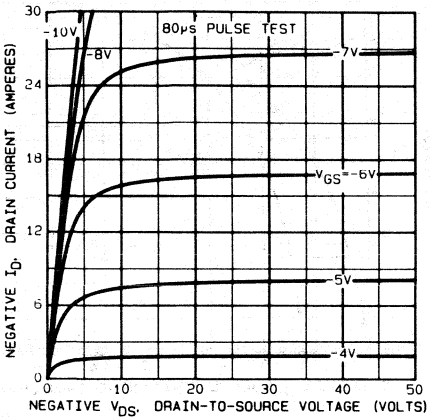


Fig. 1 - Typical output characteristics.

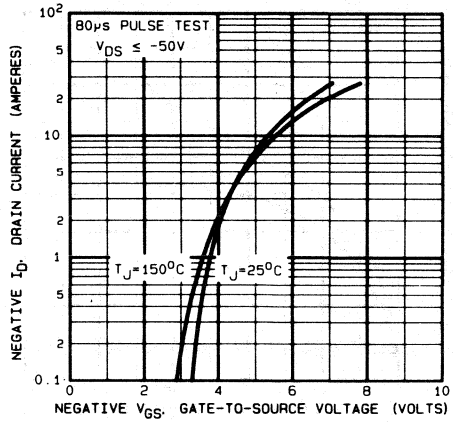


Fig. 2 - Typical transfer characteristics.

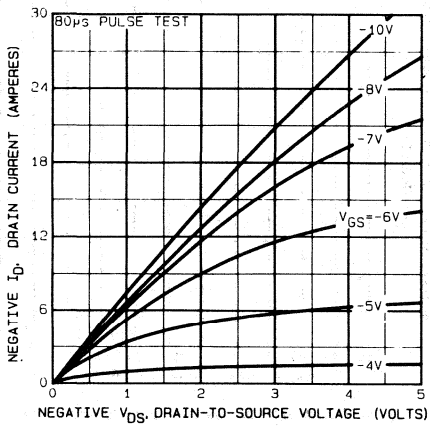


Fig. 3 - Typical saturation characteristics.

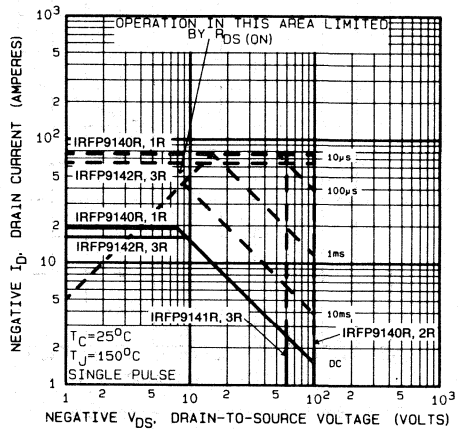


Fig. 4 - Maximum safe operating area.

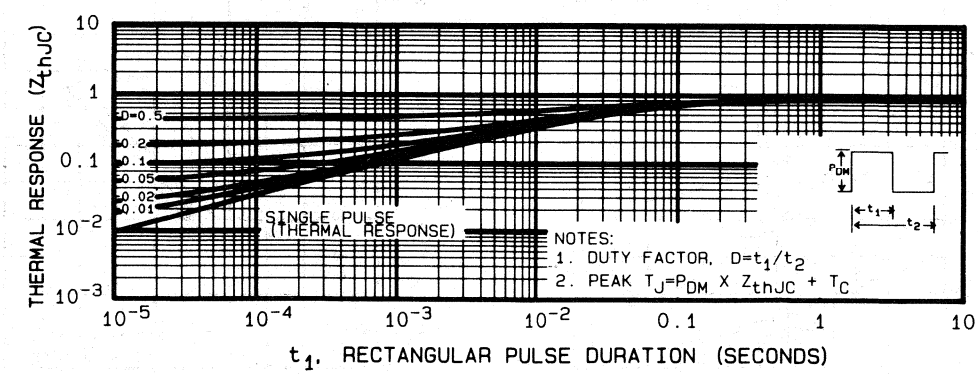


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFP9140R, IRFP9141R, IRFP9142R, IRFP9143R

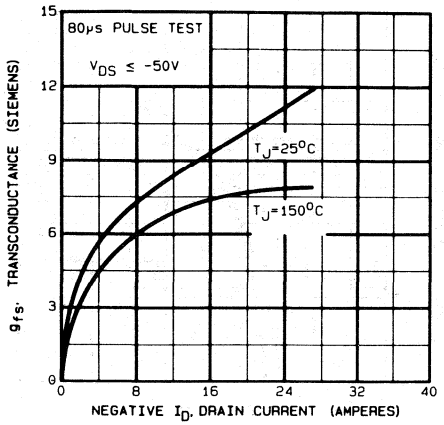


Fig. 6 - Typical transconductance vs. drain current.

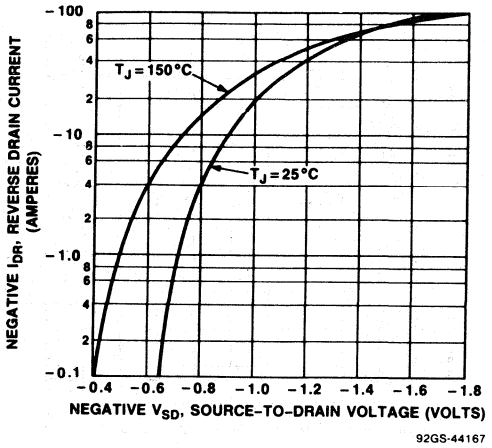


Fig. 7 - Typical source-drain diode forward voltage.

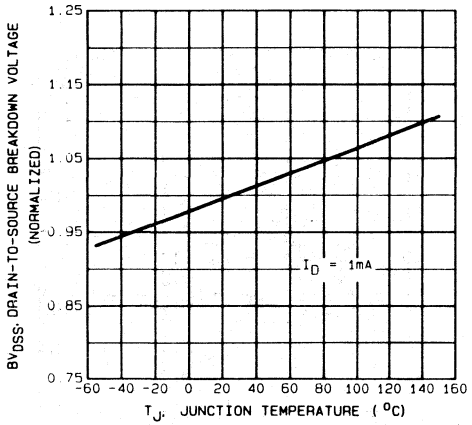


Fig. 8 - Breakdown voltage vs. temperature.

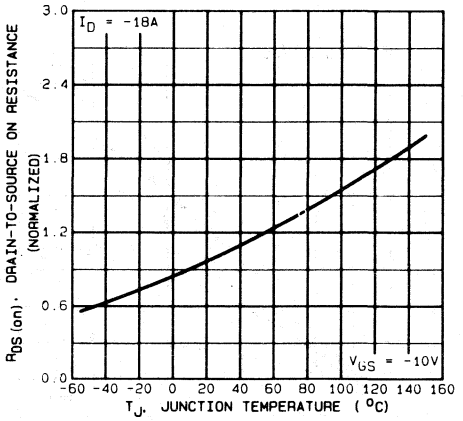


Fig. 9 - Normalized on-resistance vs. temperature.

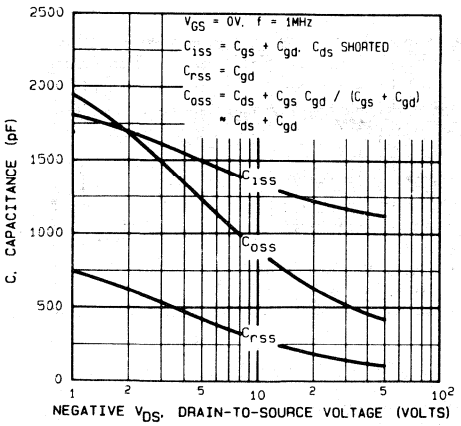


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

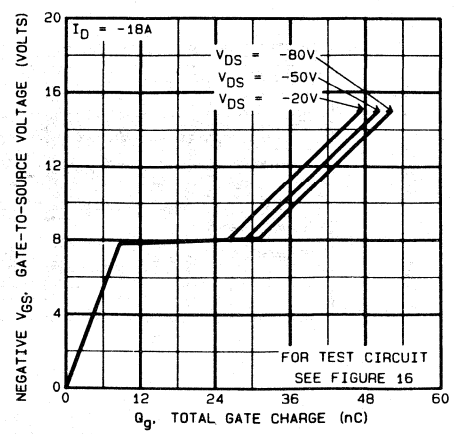


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

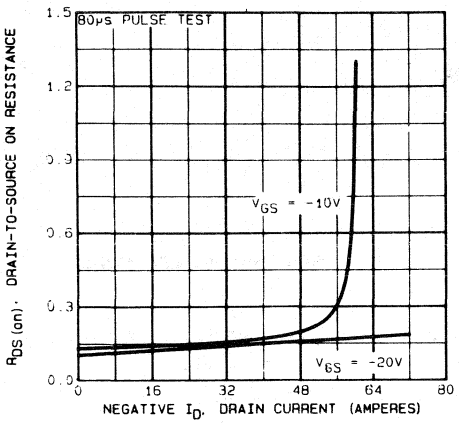


Fig. 12 - Typical on-resistance vs. drain current.

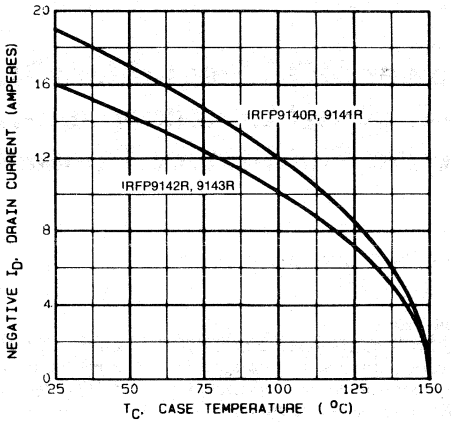


Fig. 13 - Maximum drain current vs. case temperature.

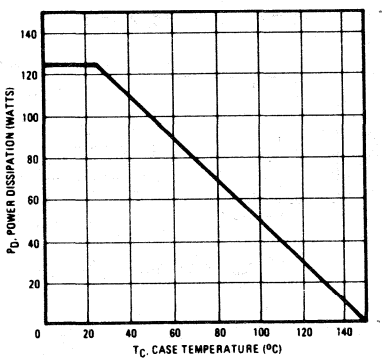


Fig. 14 - Power vs. temperature derating curve.

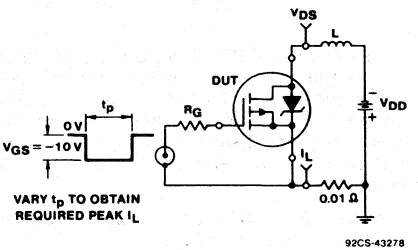


Fig. 15 - Unclamped inductive test circuit.

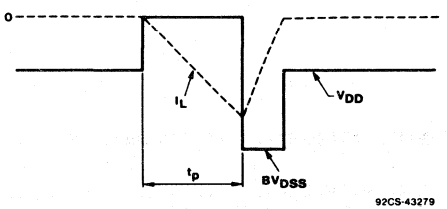


Fig. 16 - Unclamped inductive waveforms.

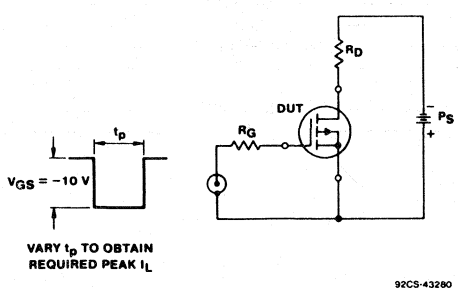


Fig. 17 - Switching time test circuit.

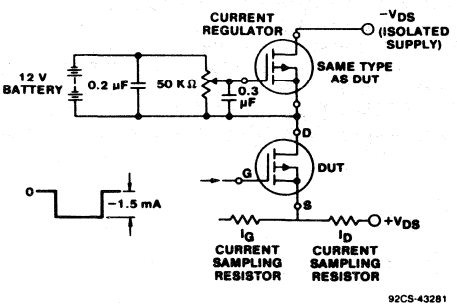


Fig. 18 - Gate charge test circuit.

IRFP9150, IRFP9151

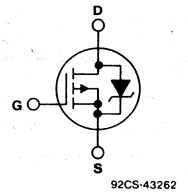
File No. 2293

Power MOS Field-Effect Transistors
P-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 60 V and 100 V
$r_{DS(on)}$ = 0.150 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *Extreme device ruggedness*
- *Low on resistance*
- *High transconductance*
- *High input impedance*

P-CHANNEL ENHANCEMENT MODE



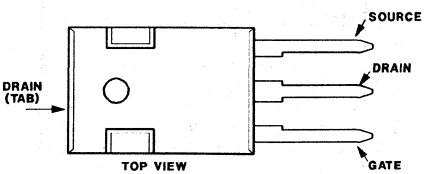
TERMINAL DIAGRAM

The IRFP9150 and IRFP9151 are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRFP9150 is an approximate electrical complement to the N-channel IRF150.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

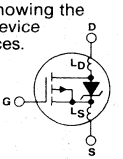
MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IRFP9150		IRFP9151	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-100		-60	V
CONTINUOUS DRAIN CURRENT @ T_C = 25°C	I_D		-25		A
CONTINUOUS DRAIN CURRENT @ T_C = 100°C	I_D		-18		A
PULSE DRAIN CURRENT	I_{DM}		-100		A
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
MAX. POWER DISSIPATION @ T_C = 25°C	P_D		150 (See Fig. 18)		W
LINEAR DERATING FACTOR			1.2		W/°C
SINGLE-PULSE AVALANCHE ENERGY ③	E_{as}		1300 (See Fig. 14)		mJ
AVALANCHE CURRENT (REPETITIVE OR NONREPETITIVE)	I_{AR}		-25		A
OPERATING JUNCTION AND	T_J				°C
STORAGE TEMPERATURE RANGE	T_{stg}		-55 to +150		°C
LEAD TEMPERATURE (0.063 in. [1.6mm] from case for 10 s)			300		°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTICS		LIMITS TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFP9150	-100	—	—	V	V_{GS} = 0 V
		IRFP9151	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	All	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	All	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	All	—	—	-100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	All	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_J = 125°C
On-State Drain Current ①	$I_{D(on)}$	All	-25	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, V_{GS} = 10 V
Static Drain-Source On-State Resistance ①	$r_{DS(on)}$	All	—	0.09	0.15	Ω	V_{GS} = -10 V, I_D = -10 A
Forward Transconductance ①	g_{fs}	All	4	10	—	S	V_{DS} = -10 V, I_D = -12.5 A
Input Capacitance	C_{iss}	All	—	2400	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	All	—	850	—	pF	
Reverse Transfer Capacitance	C_{rss}	All	—	400	—	pF	
Turn-On Delay Time	$t_{d(on)}$	All	—	16	24	ns	V_{DD} = -50 V, I_D = -25 A R_G = 6.8 Ω, R_D = 2 Ω See Figs. 16 and 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	All	—	110	160	ns	
Turn-Off Delay Time	$t_{d(off)}$	All	—	65	100	ns	
Fall Time	t_f	All	—	46	70	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	All	—	82	120	nC	V_{GS} = -10 V, I_D = -25 A, V_{DS} = 0.8 Max. Rating. See Figs. 11 and 19 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	All	—	14	21	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	All	—	42	65	nC	
Internal Drain Inductance	L_D	All	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	All	—	13	—	nH	Measured from the source pin, 6mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

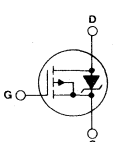


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	All	—	—	0.83	°C/W	
Case-to-Sink	$R_{\theta CS}$	All	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased
Junction-to-Ambient	$R_{\theta JA}$	All	—	—	30	°C/W	Free Air Operation
Mounting Torque		All	—	—	10	lbs	Standard 4-40 screw

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode) ②	I_S	All	—	—	-25	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
Pulse Source Current (Body Diode) ③	I_{SM}	All	—	—	-100	A	
Diode Forward Voltage ②	V_{SD}	All	—	0.9	1.5	V	T_J = 25°C, I_S = 25 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	All	—	150	300	ns	T_J = 25°C, I_F = 25 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	All	0.30	0.70	1.5	μC	T_J = 25°C, I_F = 25 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	All	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25 V, Starting T_J = 25°C, L = 3.2 mhy, I_{peak} = 25 A, R_{gs} = 25 Ω (See Figs. 14 & 15).

IRF9150, IRF9151

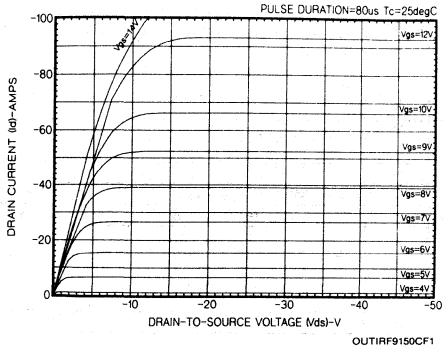


Fig. 1 - Typical output characteristics.

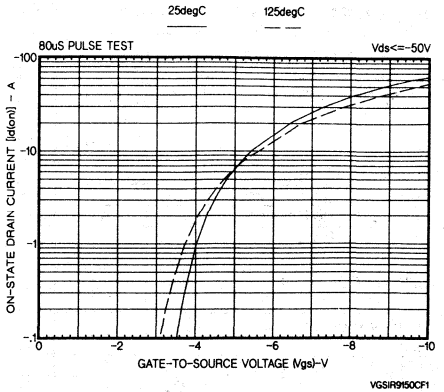


Fig. 2 - Typical transfer characteristics.

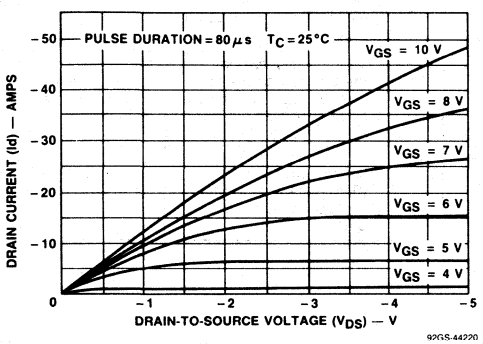


Fig. 3- Typical saturation characteristics.

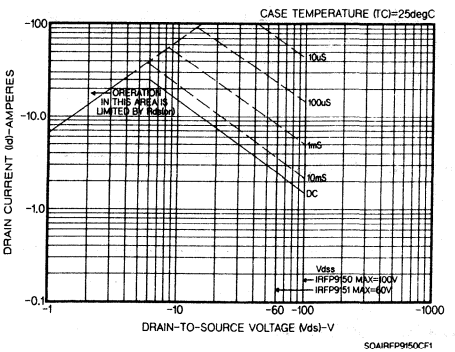


Fig. 4 - Maximum safe operating area.

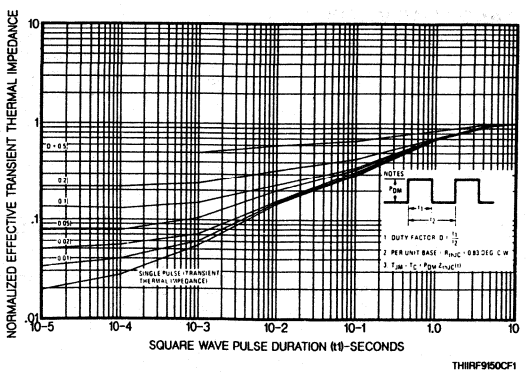


Fig. 5 - Maximum effective transient thermal impedance.

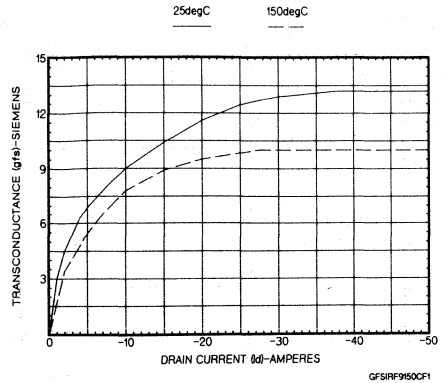


Fig. 6 - Typical transconductance vs. drain current.

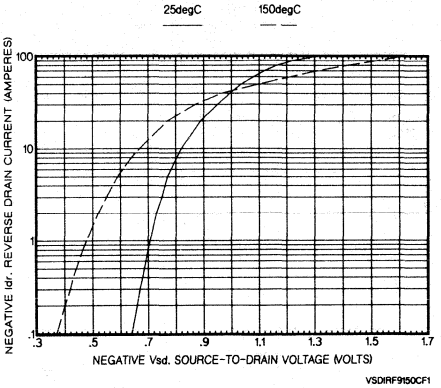


Fig. 7 - Typical source-drain diode forward voltage.

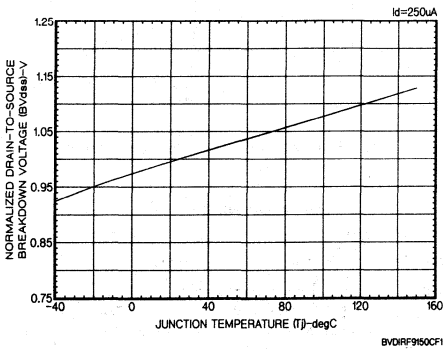


Fig. 8 - Normalized breakdown voltage vs. temperature.

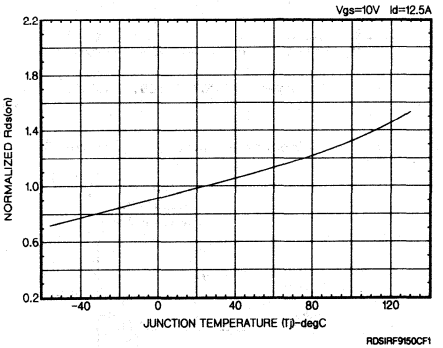


Fig. 9 - Normalized on-resistance vs. temperature.

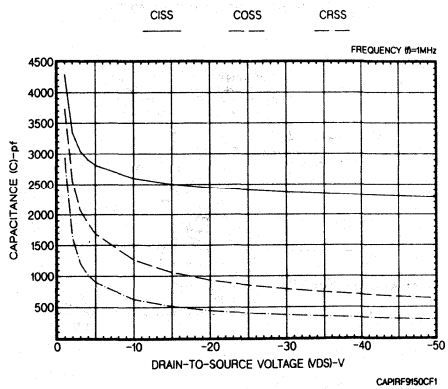


Fig. 10 - Typical capacitance vs. drain-to source voltage.

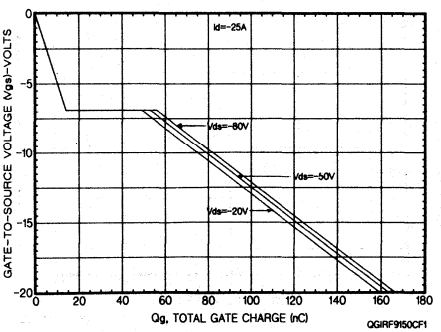


Fig. 11 - Typical gate charge vs. gate-to source voltage.

IRF9150, IRF9151

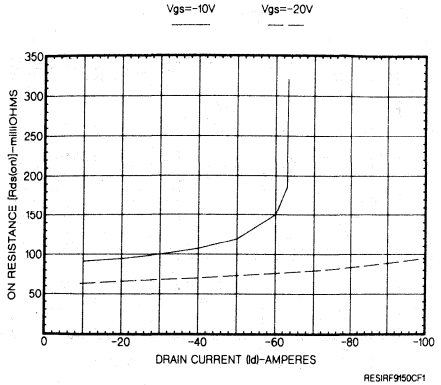


Fig. 12 - Typical on-resistance vs. drain current.

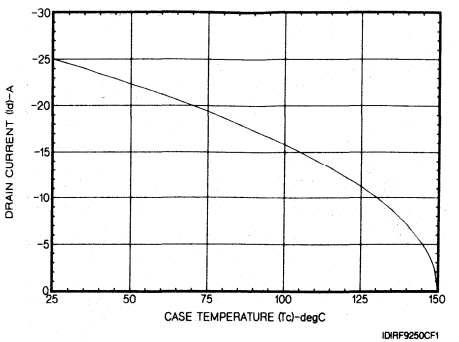


Fig. 13 - Maximum drain current vs. case temperature.

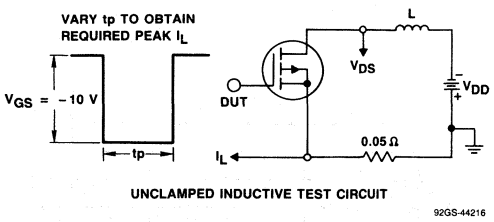


Fig. 14 - Unclamped inductive test circuit.

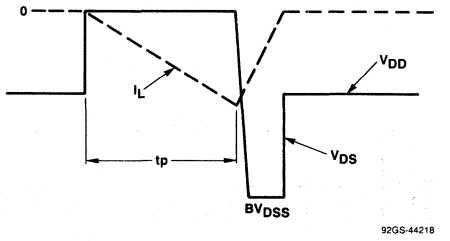


Fig. 15 - Unclamped inductive waveforms.

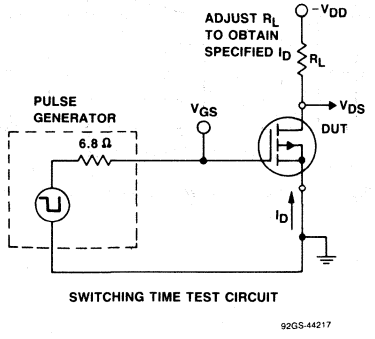


Fig. 16 - Switching time test circuit.

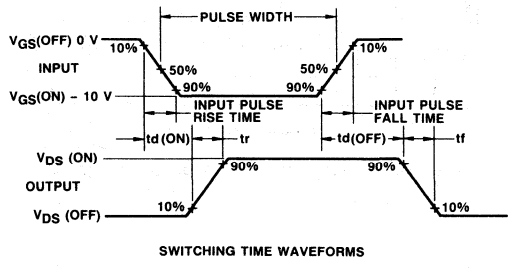


Fig. 17 - Switching time waveforms.

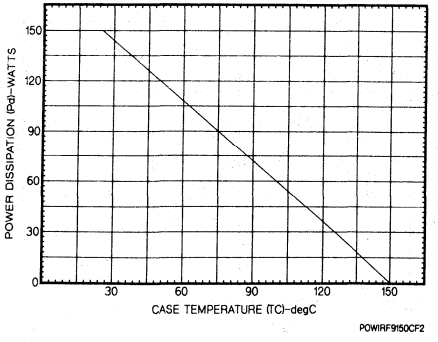


Fig. 18 - Power vs. temperature derating curve.

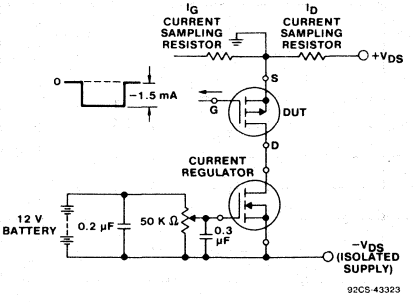


Fig. 19 - Gate charge test circuit.

File Number **2294**

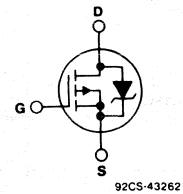
IRFP9240R, IRFP9241R, IRFP9242R, IRFP9243R

Avalanche-Energy-Rated P-Channel Power MOSFETs

-10 A and -12 A, 200 V and 150 V
$r_{DS(on)}$ = 0.50 Ω and 0.70 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

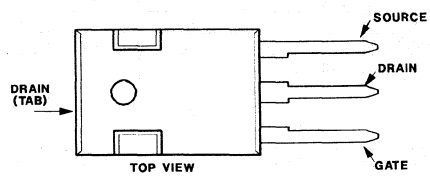


P-CHANNEL ENHANCEMENT MODE

The IRFP9240R, IRFP9241R, IRFP9242R and IRFP9243R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

ABSOLUTE-MAXIMUM RATINGS

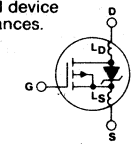
CHARACTERISTIC		IRFP9240R	IRFP9241R	IRFP9242R	IRFP9243R	UNITS
Drain-Source Voltage ①	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current	I_D @ T_C = 25°C	-12	-12	-10	-10	A
Continuous Drain Current	I_D @ T_C = 100°C	-7.5	-7.5	-6.3	-6.3	A
Pulsed Drain Current ③	I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	150 (See Fig. 14)				W
Linear Derating Factor		1.2 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	790				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

IRFP9240R, IRFP9241R, IRFP9242R, IRFP9243R

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFP9240R IRFP9242R	-200	—	—	V	V_{GS} = 0 V
		IRFP9241R IRFP9243R	-150	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFP9240R IRFP9241R	-12	—	—	A	V_{DS} > $I_{D(on)}$ x $r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFP9242R IRFP9243R	-10	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFP9240R IRFP9241R	—	0.38	0.50	Ω	V_{GS} = -10 V, I_D = -6.3 A
		IRFP9242R IRFP9243R	—	0.50	0.70	Ω	
Forward Transconductance ②	g_{fs}	ALL	3.8	5.7	—	S(℧)	V_{DS} > $I_{D(on)}$ x $r_{DS(on)\ max.}$, I_D = 10 A
Input Capacitance	C_{iss}	ALL	—	1400	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	350	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	140	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	18	22	ns	V_{DD} = -100 V, I_D = -11 A, Z_O = 9.1 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	45	68	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	75	90	ns	
Fall Time	t_f	ALL	—	29	44	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	38	57	nC	V_{GS} = -10 V, I_D = -11 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	8	12	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	21	32	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

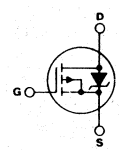


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	0.83	°C/W	
Case-to-Sink	$R_{\theta CS}$	ALL	—	0.24	—	°C/W	Mounting surface flat, smooth, and greased.
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	30	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFP9240R IRFP9241R	—	—	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP9242R IRFP9243R	—	—	-12	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFP9240R IRFP9241R	—	—	-48	A	
		IRFP9242R IRFP9243R	—	—	-48	A	
Diode Forward Voltage ②	V_{SD}	IRFP9240R IRFP9241R	—	—	-1.5	V	T_C = 25°C, I_S = -12 A, V_{GS} = 0 V
		IRFP9242R IRFP9243R	—	—	-1.5	V	T_C = 25°C, I_S = -12 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	210	—	ns	T_J = 150°C, I_F = -12 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	2.0	—	μC	T_J = 150°C, I_F = -12 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50 V, Starting T_j = 25°C, L = 8.2 mH, R_{GS} = 50 Ω, I_{PEAK} = 12 A (See Figs. 15 & 16).

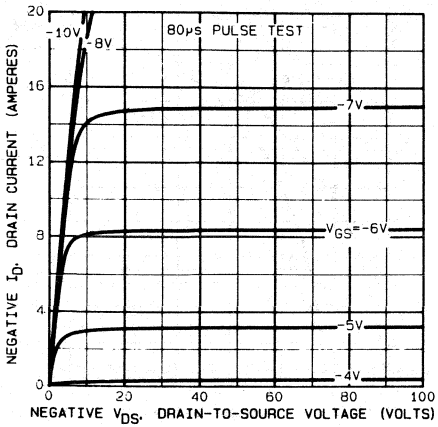


Fig. 1 - Typical output characteristics.

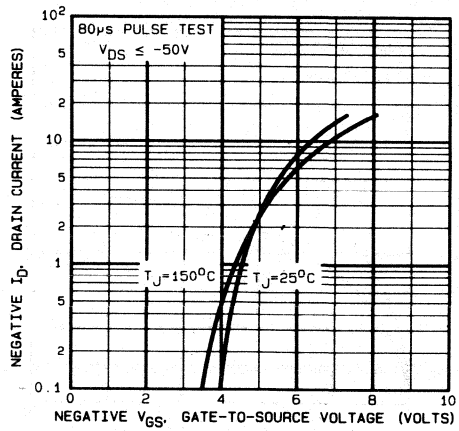


Fig. 2 - Typical transfer characteristics.

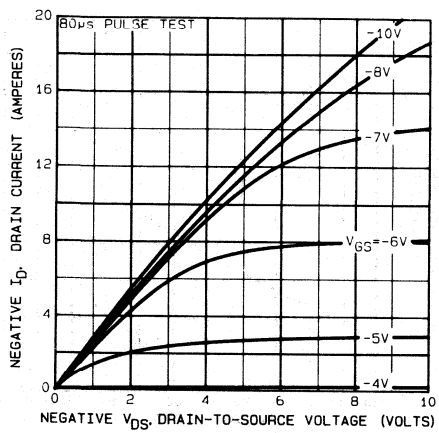


Fig. 3 - Typical saturation characteristics.

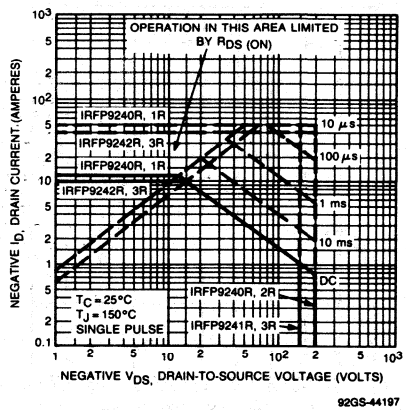


Fig. 4 - Maximum safe operating area.

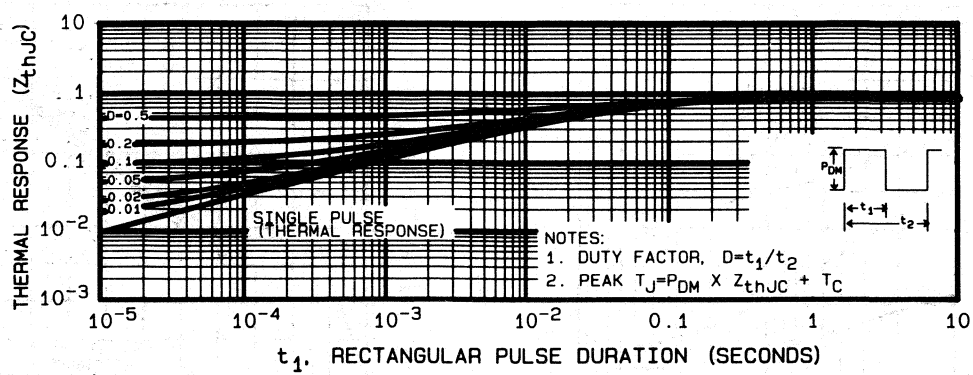


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFP9240R, IRFP9241R, IRFP9242R, IRFP9243R

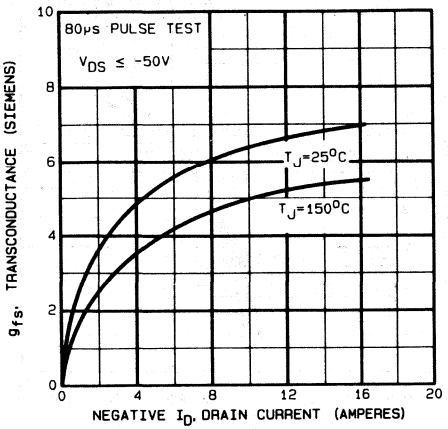


Fig. 6 - Typical transconductance vs. drain current.

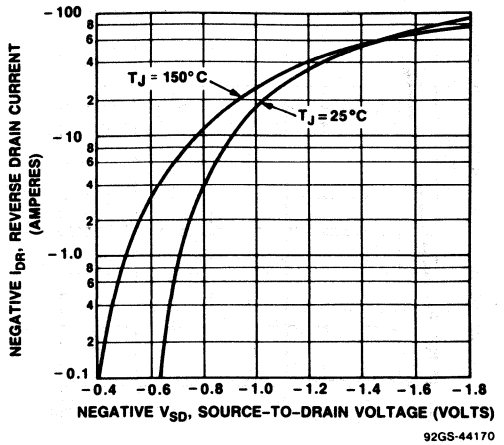


Fig. 7 - Typical source-drain diode forward voltage.

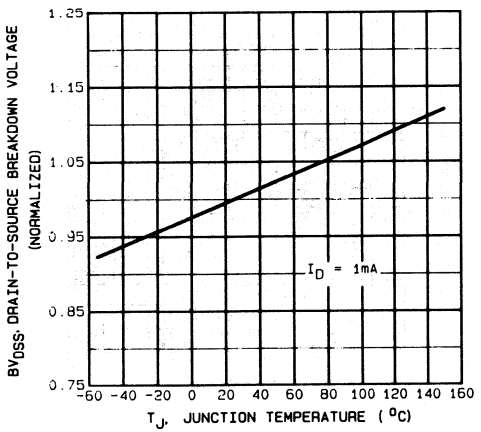


Fig. 8 - Breakdown voltage vs. temperature.

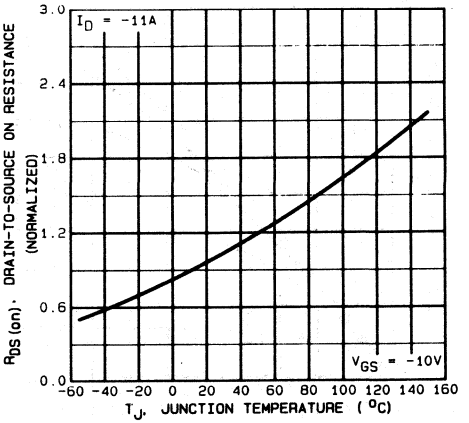


Fig. 9 - Normalized on-resistance vs. temperature.

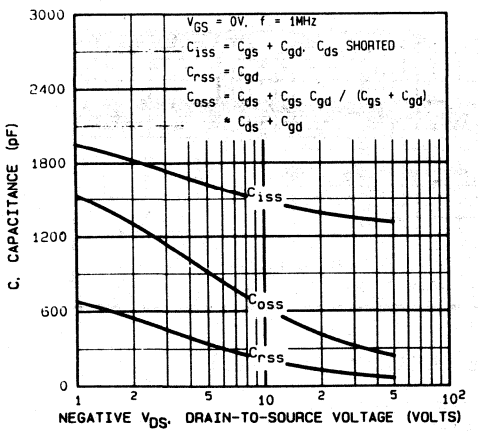


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

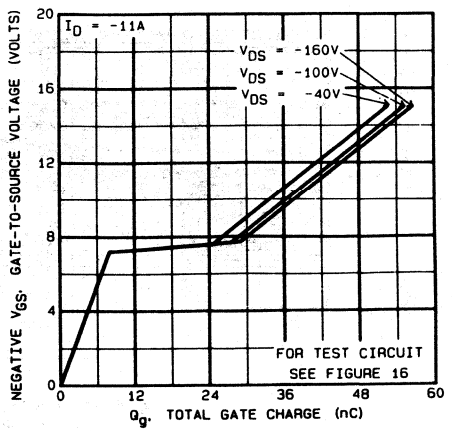


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

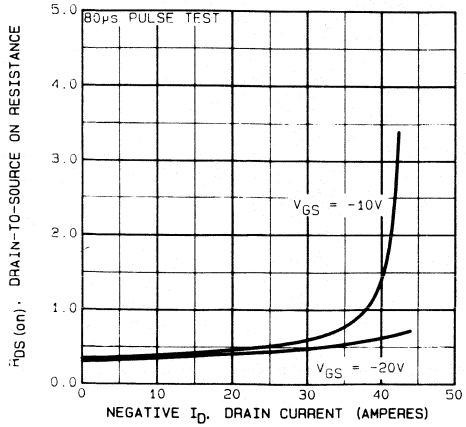


Fig. 12 - Typical on-resistance vs. drain current.

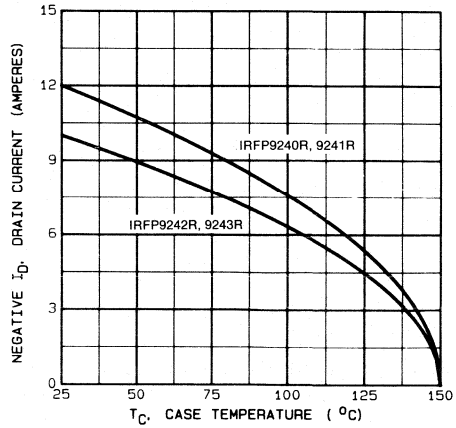


Fig. 13 - Maximum drain current vs. case temperature.

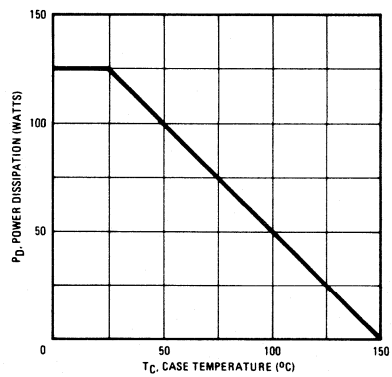


Fig. 14 - Power vs. temperature derating curve.

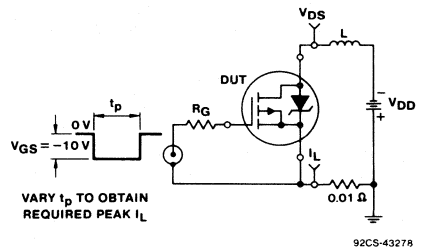


Fig. 15 - Unclamped inductive test circuit.

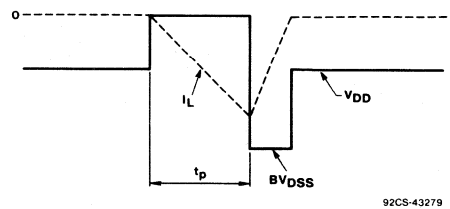


Fig. 16 - Unclamped inductive waveforms.

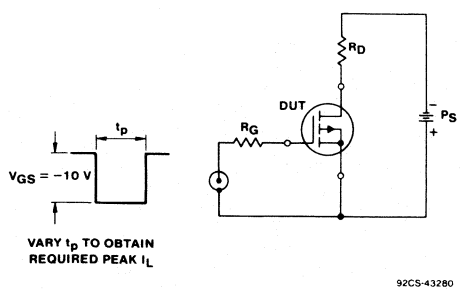


Fig. 17 - Switching time test circuit.

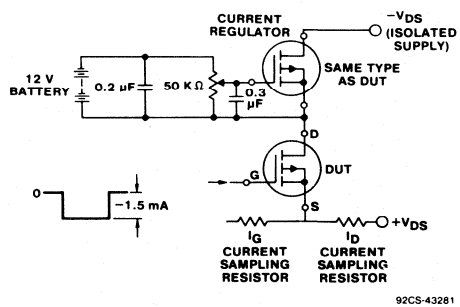


Fig. 18 - Gate charge test circuit.

Insulated-Gate Bipolar Transistors

GSI510, IGT5E10CS

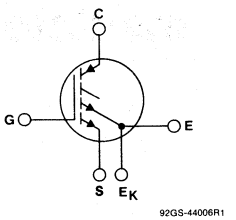
File Number **2326**

Current Sensing IGT™ Transistors
Insulated Gate Bipolar Transistors

10 A, 500 V
$r_{DS(on)}$ = 0.27 Ω

Features:
- *Low $V_{CE(sat)}$ - 2.5 V typ. @ 10 A*
- *Ultra-fast turn-on - 100 ns typical*
- *Polysilicon MOS gate - voltage controlled turn on/off*
- *High current handling - 10 A @ 100° C case*
- *Current sensing pilot*

TERMINAL DIAGRAM



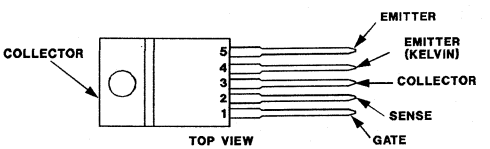
92GS-44006R1

N-CHANNEL ENHANCEMENT MODE

The GSI510 and/or IGT5E10CS Series IGT™ Transistor (Insulated Gate Bipolar Transistor) is a MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs, bipolar transistors, and current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $r_{ds(on)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

The IGT™ Transistor is ideal for many high-voltage switching applications operating at low frequencies and where low conduction losses are essential, such as AC and DC motor controls, power supplies and drivers for solenoids, relays, and contactors.

TERMINAL DESIGNATION



TO-220 (5 LEAD)

MAXIMUM RATINGS

COLLECTOR-EMITTER VOLTAGE (V_{GE} = 0 V)	V_{CES}	500	V
COLLECTOR-GATE VOLTAGE (R_{GE} = 1 MΩ)	V_{CGR}	500	V
CONTINUOUS DRAIN CURRENT	I_C		
At T_c = 100° C		10	A
At T_c = 25° C		18	A
PULSED COLLECTOR CURRENT	I_{CM}•	40	A
GATE-EMITTER VOLTAGE	V_{GE}	±25	V
TOTAL POWER DISSIPATION	P_D		
At T_C = 25° C		75	W
Derate Above 25° C		0.6	W/° C
OPERATING AND STORAGE JUNCTION TEMPERATURE RANGE	T_J, T_{stg}	-55 to +150	° C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R_{\theta JC}$	1.67	° C/W
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES	T_L		
1/8 inch from case for 5 seconds		260	° C

•Repetitive Rating: Pulse width limited by maximum junction temperature.
Gate control turn-off not allowed above 50 amperes.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS T_C = 25° C Unless Otherwise Specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 25 μA	500	—	—	V
Collector Cut-off Current	I_{CES}	V_{CE} = Max. Rating, V_{GE} = 0 V, T_C = 25° C	—	—	250	μA
		V_{CE} = Max. Rating x 0.8, V_{GE} = 0 V, T_C = 150° C[1]	—	—	4	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V	—	—	±500	nA
ON CHARACTERISTICS[2]						
Gate Threshold Voltage	$V_{GE(th)}$	V_{CE} = V_{GE}, I_C = 250 μA, T_C = 25°C	2	4	5	V
		T_C = 150°C	—	2.5	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_{GE} = 15 V, I_C = 10 A, T_C = 25°C	—	2.5	2.7	
		V_{GE} = 15 V, I_C = 10 A, T_C = 150°C	—	2.8	—	
		V_{GE} = 10 V, I_C = 10 A, T_C = 25°C	—	2.9	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ies}	V_{GE} = 0 V	—	1050	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25 V	—	340	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	10	—	
SWITCHING CHARACTERISTICS[2] (See Figs. 8 & 9)						
Turn-On Delay Time	$t_{d(on)}$	Resistive Load, T_J = 125°C	—	100	—	ns
Rise Time	t_r	I_C = 10 A, V_{CE} = 400 V	—	100	—	
Turn-Off Delay Time	$t_{d(off)}$	V_{GE} = 15 V	—	0.4	—	μs
Fall Time	t_f	$R_{G(on)}$ = 50 Ω, $R_{G(off)}$ = 100 Ω	—	2.5	—	
Turn-Off Delay Time	$t_{d(off)}$	Inductive Load, T_J = 125°C	—	0.8	1.2	μs
Fall Time	t_f	L = 45 μH, I_C = 10 A	—	0.8	1.0	
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(clamp)}$ = 400 V, V_{GE} = 15 V	—	0.6	0.8	
Turn-Off Switching Losses	E_f	$R_{G(on)}$ = 50 Ω, $R_{G(off)}$ = 100 Ω	—	1.6	2.0	mJ
PILOT CHARACTERISTICS[2] [3] [4]						
Pilot - Emitter Kelvin Voltage	V_{PEK}	V_{GE} = 15 Vdc, R_P = 2 KΩ				
I_C = 5 A			—	1.25	—	V
I_C = 10 A			1.4	1.67	1.8	
I_C = 20 A			—	2.06	—	

[1] Applies for 3.3°C per watt maximum thermal resistance, case-to-ambient.
[2] Pulse test: Pulse widths ≤ 300 μs, duty cycle ≤ 2%.
[3] Refer to Fig. 10.
[4] When Not in Use Connect E_P to Emitter.

GSI510, IGT5E10CS

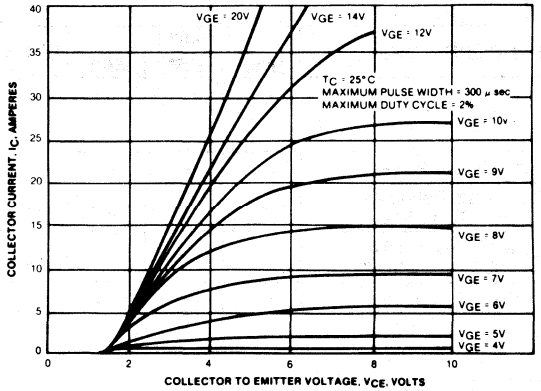


Fig. 1 - Typical output characteristics.

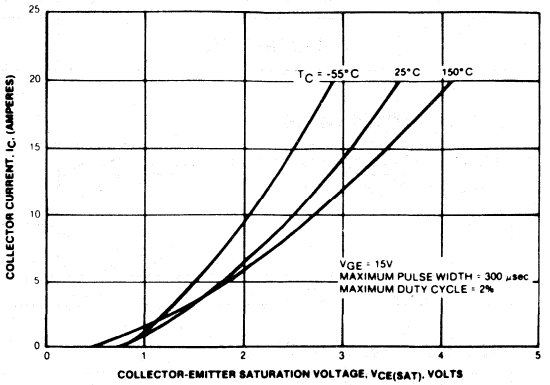


Fig. 2 - Typical collector-emitter saturation voltage.

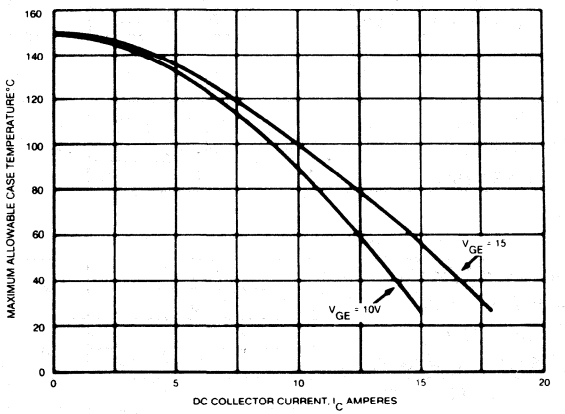


Fig. 3 - Maximum allowable case temperature vs. DC collector current.

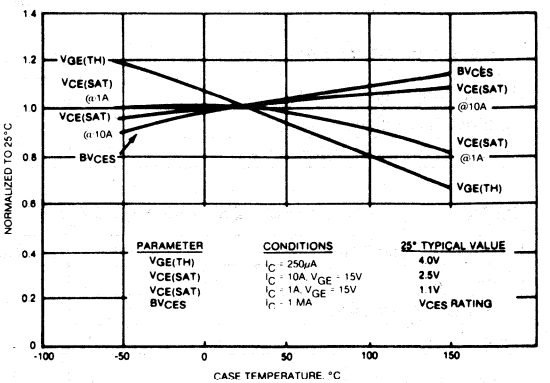


Fig. 4 - Typical temperature dependence of parameters.

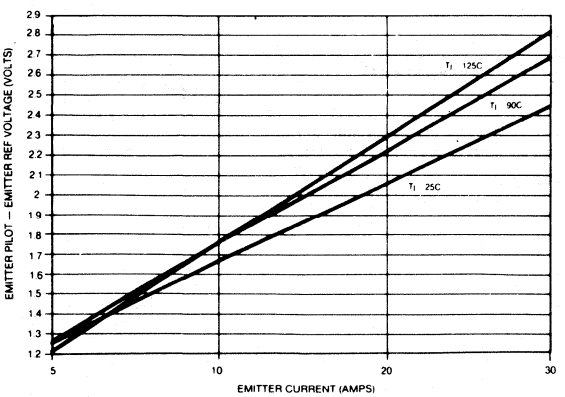


Fig. 5A - Typical emitter pilot characteristics 2 Kohm pilot resistor.

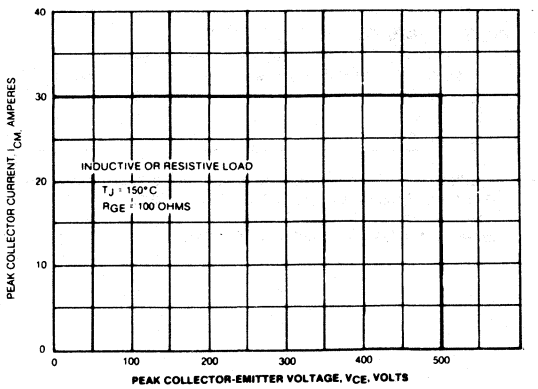


Fig. 5B - Turn-off safe operating area.

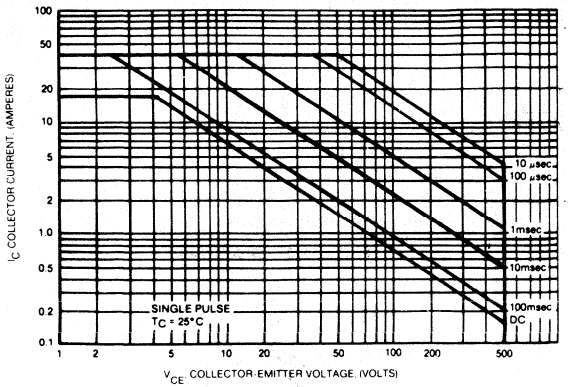


Fig. 6 - Turn-on safe operating area.

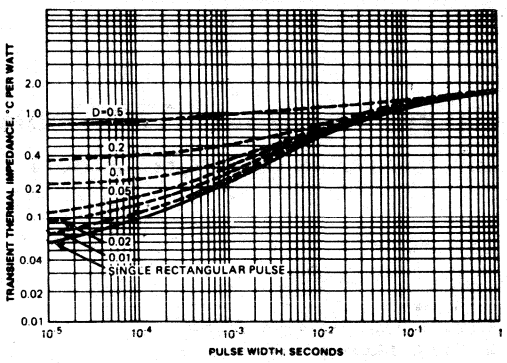


Fig. 7 - Maximum transient thermal impedance.

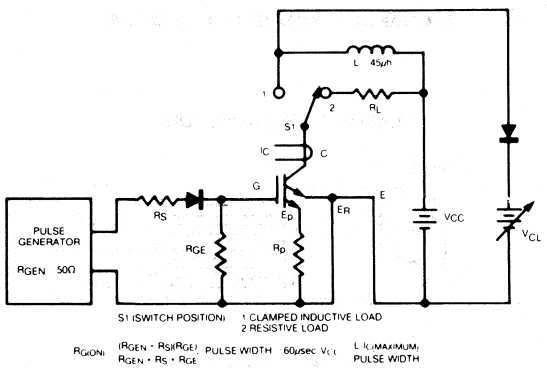


Fig. 8 - Basic switching test circuit.

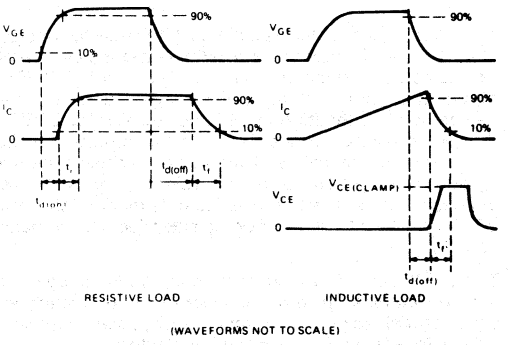


Fig. 9 - Switching waveforms.

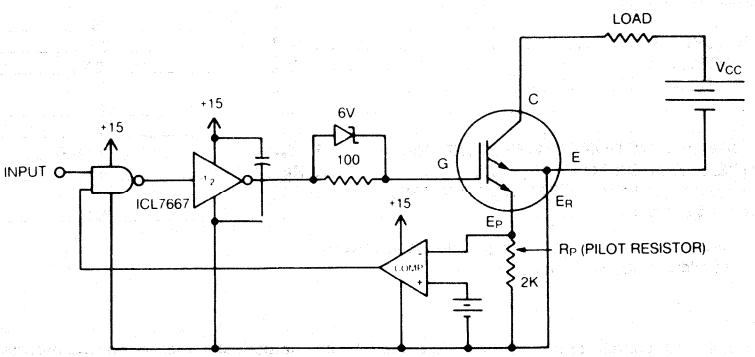


Fig. 10 - Typical circuit utilizing the emitter pilot for overcurrent protection

GSI525, IGT7E20CS

File Number **2327**

Current Sensing IGT™ Transistors

Insulated Gate Bipolar Transistors

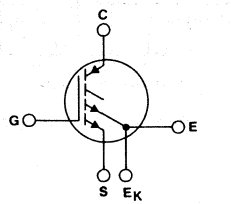
25 A, 500 V

$r_{DS}(on)$ = 0.105 Ω

Features:

- *Low $V_{CE}(sat)$ - 1.8 V typ. @ 25 A*
- *Ultra-fast turn-on - 150 ns typical*
- *Polysilicon MOS gate - voltage controlled turn on/off*
- *High current handling - 25 A @ 85° C case*
- *Current sensing pilot*

TERMINAL DIAGRAM



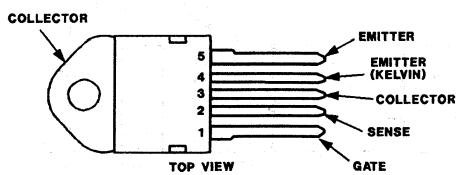
92GS-44006R1

N-CHANNEL ENHANCEMENT MODE

The GSI525 and/or IGT7E20CS IGT™ Transistor (Insulated-Gate Bipolar Transistor) is a MOS-Gated power-switching device combining the best features of power MOSFETs and bipolar transistors with current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses of bipolar transistors. The gate characteristics of the IGT™ Transistor are similar to power MOSFETs but its equivalent $r_{ds}(on)$ drain resistance is ten times lower and varies only moderately between 25° C and 150° C, thus offering extended power handling capability.

The IGT™ Transistor is ideal for many high voltage switching applications up to 5 kHz where low conduction losses are essential; ac and dc motor controls, power supplies and drivers for solenoids, relays, and contactors.

TERMINAL DESIGNATION



TO-218 (5 LEAD)

MAXIMUM RATINGS

COLLECTOR-EMITTER VOLTAGE (V_{GE} = 0 V)	V_{CES}	500	V
COLLECTOR-GATE VOLTAGE (R_{GE} = 1 MΩ)	V_{CGR}	500	V
CONTINUOUS DRAIN CURRENT	I_C		
At T_C = 85° C		25	A
PULSED COLLECTOR CURRENT	I_{CM}•	80	A
GATE-EMITTER VOLTAGE	V_{GE}	±20	V
TOTAL POWER DISSIPATION	P_D		
At T_C = 25° C		125	W
Derate Above 25° C		1	W/° C
OPERATING AND STORAGE JUNCTION TEMPERATURE RANGE	T_J, T_{stg}	-40 to +150	°C
THERMAL RESISTANCE, JUNCTION TO CASE	$R_{\theta JC}$	1	°C/W
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES	T_L		
1/8 inch from case for 5 seconds		260	°C

•Repetitive Rating: Pulse width limited by maximum junction temperature. Gate control turn-off not allowed above 50 amperes.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, T_C = 25° C Unless Otherwise Specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 250 μA	500	—	—	V
Collector Cut-off Current	I_{CES}	V_{CE} = Max. Rating V_{GE} = 0 V, T_C = 25° C	—	—	250	μA
		V_{CE} = Max. Rating x 0.8 V_{GE} = 0 V, T_C = 125° C(1)	—	—	4	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V	—	—	±500	nA
ON CHARACTERISTICS(2)						
Gate Threshold Voltage	$V_{GE}(th)$	V_{CE} = V_{GE}, I_C = 500 μA				V
		T_C = 25° C	2	4	5.5	
		T_C = 150° C	—	2	—	
Collector-Emitter Saturation Voltage	$V_{CE}(sat)$	V_{GE} = 15 V, I_C = 25 A				
		T_C = 25° C	—	1.8	2.6	
		T_C = 150° C	—	1.9	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ies}	V_{GE} = 0 V	—	2300	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25 V	—	250	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	35	—	
SWITCHING CHARACTERISTICS(2) (See Figs. 8 & 9)						
Turn-on Delay Time	$t_{d}(on)$	Resistive Load, T_J = 150° C	—	100	—	ns
Rise Time	t_r	I_C = 25 A, V_{CE} = 400 V	—	150	—	
Turn-off Delay Time	$t_{d}(off)$	V_{GE} = 15 V	—	0.6	—	μs
Fall Time	t_f	$R_G(on)$ = 50 Ω, $R_G(off)$ = 50 Ω	—	3	—	
Turn-off Delay Time	$t_{d}(off)$	Inductive Load, T_J = 150° C L = 45 μH, I_C = 25 A	—	1.5	2.5	μs
Fall Time	t_f	V_{CE}(clamp) = 400 V, V_{GE} = 15 V	—	1.2	1.6	
Turn-off Switching Losses	E_f	$R_G(on)$ = 50 Ω, $R_G(off)$ = 50 Ω	—	5	8	mJ
PILOT CHARACTERISTICS(2)(3)(4)						
Pilot - Emitter Kelvin Voltage	V_{PEK}	V_{GE} = 15 Vdc, R_P = 1 KΩ				
I_C = 20 A			1	1.3	1.6	V
I_C = 30 A			—	1.45	—	
I_C = 40 A			—	1.7	—	

(1) Applies for 3.3° C per watt maximum thermal resistance, case to ambient.

(2) Pulse test: Pulse widths ≤ 300 μs, duty cycle ≤ 2%.

(3) Refer to Fig. 5(a).

(4) When not in use connect P to Emitter.

GSI525, IGT7E20CS

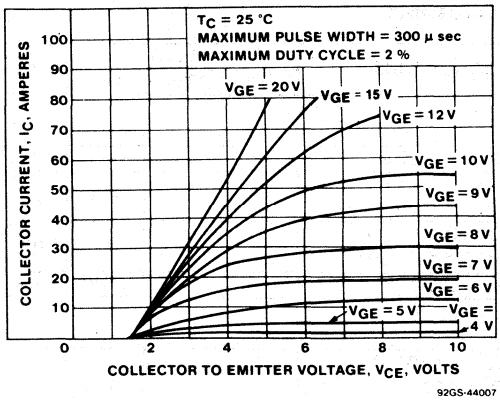


Fig. 1 - Typical output characteristics.

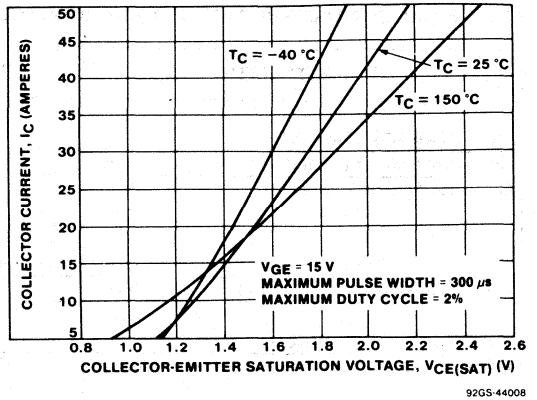


Fig. 2 - Typical collector-emitter saturation voltage

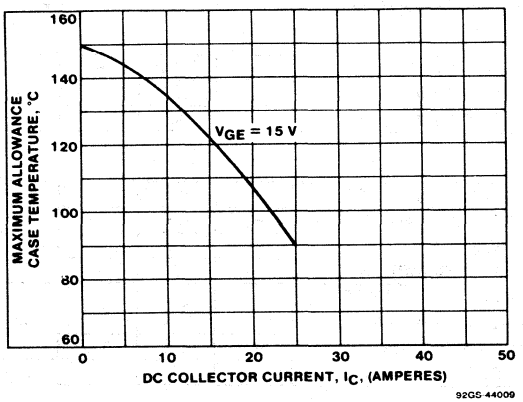


Fig. 3 - Maximum allowable dc collector current vs. case temperature.

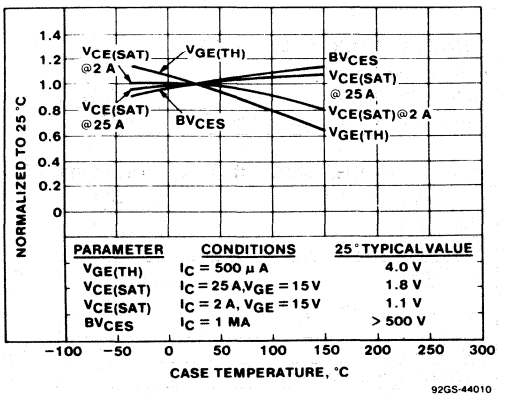


Fig. 4 - Typical temperature dependence of parameters.

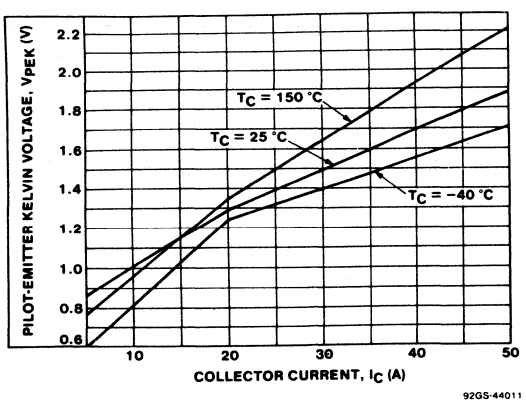


Fig. 5(a) - Typical emitter pilot characteristics - 1 KΩ pilot resistor.

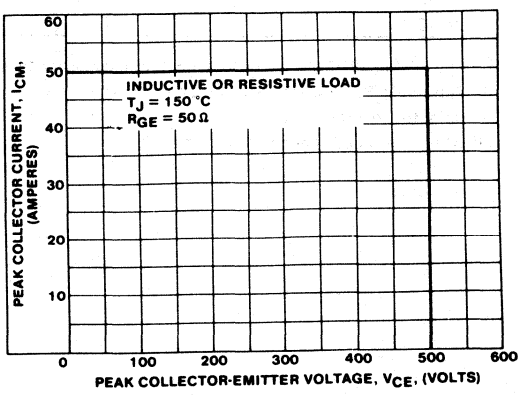


Fig. 5(b) - Turn-off safe operating area.

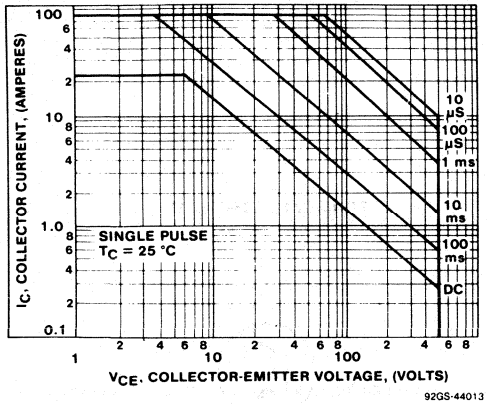


Fig. 6 - Active region safe operating area.

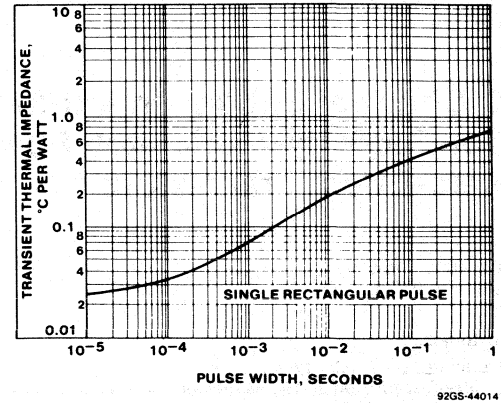


Fig. 7 - Maximum transient thermal impedance.

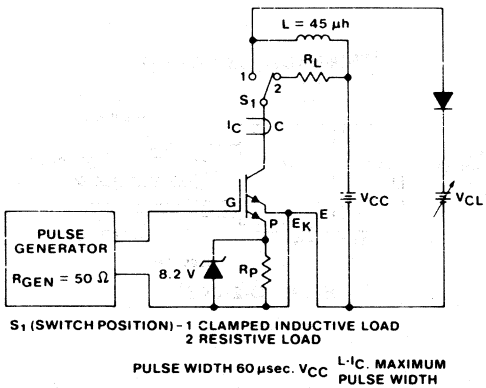


Fig. 8 - Basic switching test circuit.

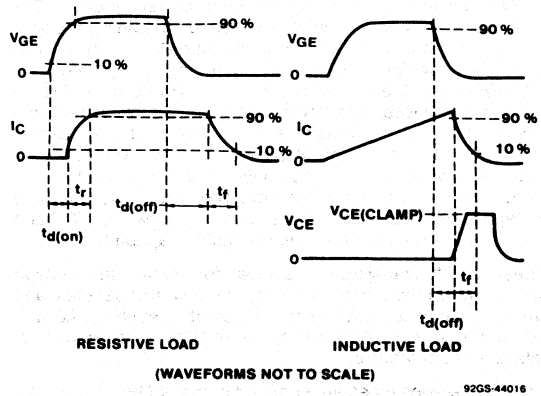


Fig. 9 - Switching waveforms.

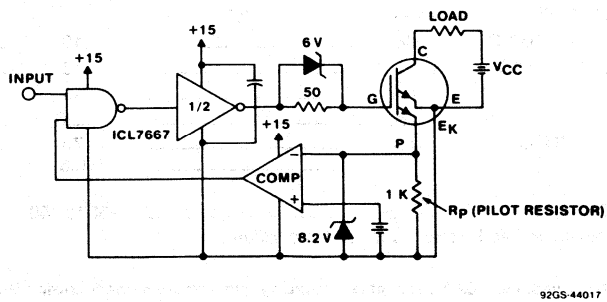


Fig. 10 - Typical circuit utilizing the pilot for overcurrent protection.

IGT4D10, IGT4E10

File Number **2123**

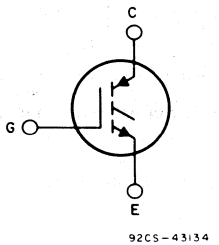
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

10A, 400V and 500V
r_{DS} (on) = 0.27 Ω

Features:

- *Low $V_{CE(SAT)}$ — 2.5V type @ 10A*
- *Ultra-fast turn-on — 150 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 10 amps @ 100°C*

TERMINAL DIAGRAM



92CS-43134

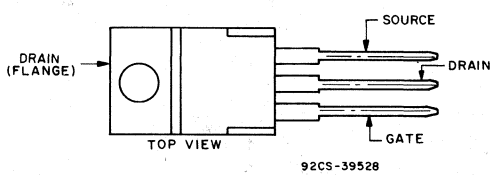
N-CHANNEL ENHANCEMENT MODE

The IGT4D10 and IGT4E10 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25°C and 150°C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IGT4D10		IGT4E10	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 100°C	I_C		10		A
@ T_C = 25°C			18		A
Pulsed Collector Current[1]	I_{CM}		40		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25°C	P_D		75		W
Derate Above 25°C			0.6		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = OV, IGT4D10	400	—	—	V
		I_C = 250 μA, V_{GE} = OV, IGT4E10	500	—	—	
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}, T_C = 25°C	2	4.0	5	V
		I_C = 250μA, V_{CE} = V_{GE}, T_C = 150°C	—	2.5	—	
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C	—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]	—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V	—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10A, V_{GE} = 15V, T_C = 25°C	—	2.5	2.7	V
		I_C = 10A, V_{GE} = 15V, T_C = 150°C	—	2.8	—	
		I_C = 10A, V_{GE} = 10V, T_C = 25°C	—	2.9	—	
Input Capacitance	C_{ies}	V_{GE} = 0V, V_{CE} = 25V, f = 1 MHz	—	1050	—	pF
Output Capacitance	C_{oes}		—	340	—	
Reverse Transfer Capacitance	C_{res}		—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =150°C, I_C = 10A, V_{CE} = Rated V_{CES}, V_{GE} = 15V, $R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	100	—	ns
Rise Time	t_r		—	150	—	
Turn-off Delay Time	$t_{d(off)}$		—	0.5	—	μs
Fall Time	t_f		—	4	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 150°C, L = 550μH, I_C = 10A, $V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V, $R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	1.0	1.8	μs
Fall Time	t_f		—	4.5	6.5	
Equivalent Fall Time	$t_{f(eq)}$		—	3.5	5.0	
Turn-off Switching Losses	E_f	IGT4D10	—	—	10	mJ
		IGT4E10	—	—	12.5	
Thermal Resistance, Junction to Case	$R_{\theta JC}$		1.67		1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L		260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 3.3°C per watt maximum thermal resistance, case to ambient.

IGT4D10, IGT4E10

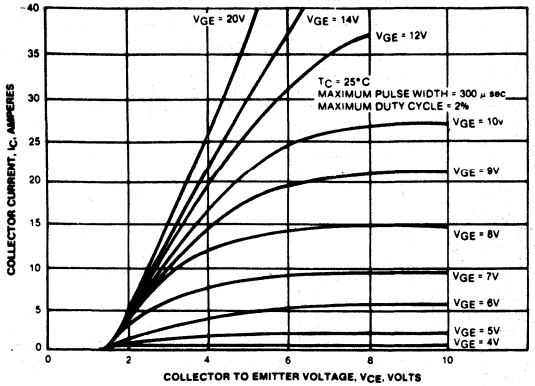


Fig. 1 - Typical Output Characteristics

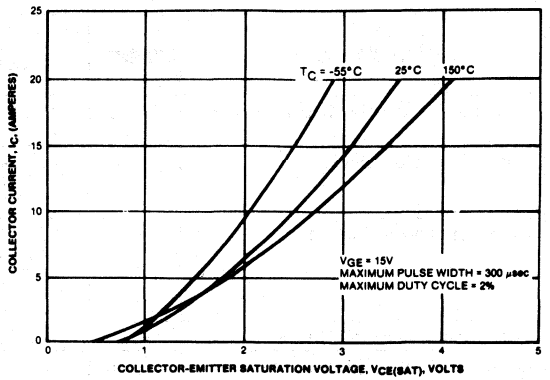


Fig. 2 - Typical Collector-Emitter Saturation Voltage

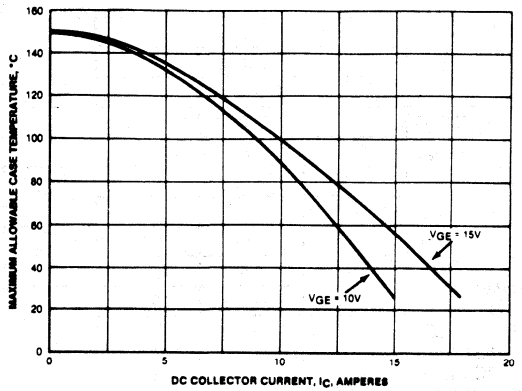


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

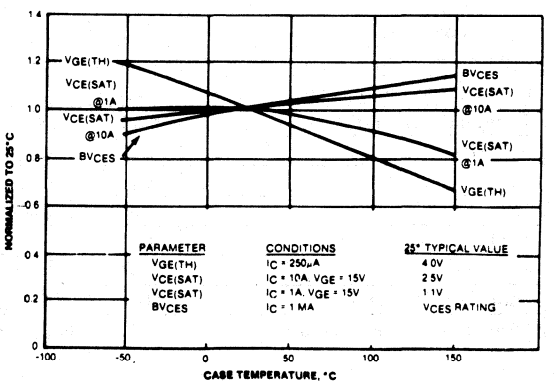


Fig. 4 - Typical Temperature Dependence of Parameters

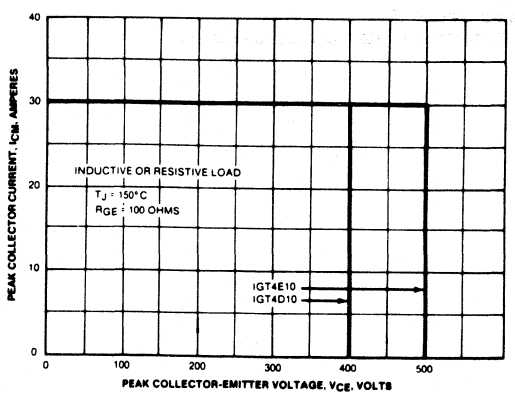


Fig. 5 - Turn-off Safe Operating Area

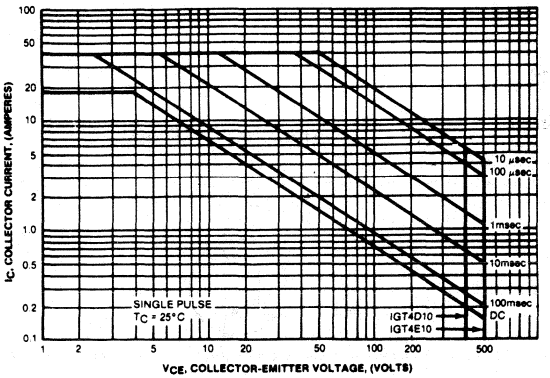


Fig. 6 - Turn-on Safe Operating Area

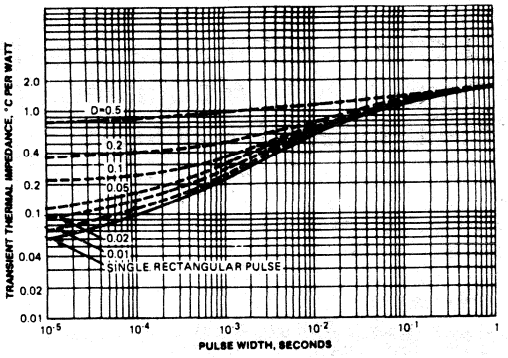
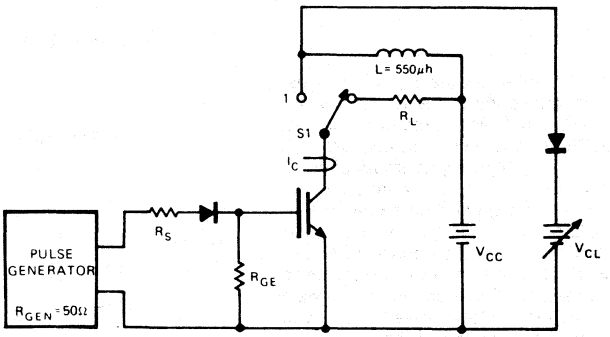


Fig. 7 - Maximum Transient Thermal Impedance



$$R_{G(ON)} = \frac{(R_{GEN}+R_S)(R_{GE})}{R_{GEN}+R_S+R_{GE}}, \text{ PULSE WIDTH} \cdot 60\mu\text{sec}, V_{CC} = \frac{L \cdot I_{C(MAXIMUM)}}{\text{PULSE WIDTH}}$$

Fig. 8 - Basic Switching Test Circuit

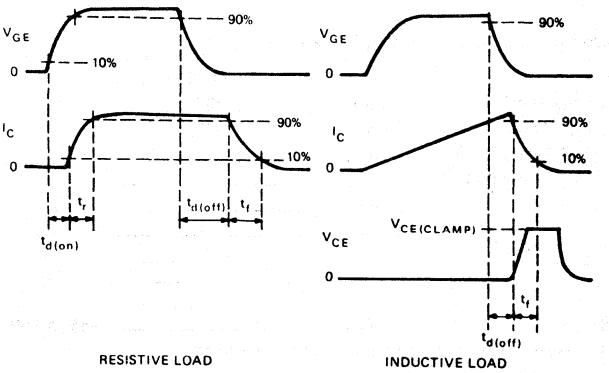


Fig. 9 - Switching Waveforms

IGT4D11, IGT4E11

File Number **2124**

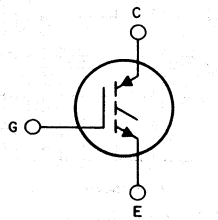
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

10A, 400V and 500V
r_{DS} (on) = 0.27 Ω

Features:

- *Low $V_{CE(SAT)}$ — 2.5V typ. @ 10A*
- *Ultra-fast turn-on — 150 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 10 amps @ 100° C*

TERMINAL DIAGRAM



92CS-43134

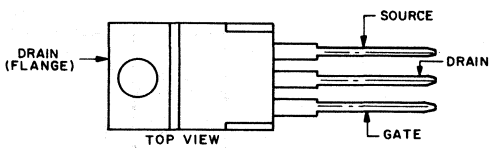
N-CHANNEL ENHANCEMENT MODE

The IGT4D11 and IGT4E11 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IGT4D11		IGT4E11	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 100° C	I_C		10		A
@ T_C = 25° C			18		A
Pulsed Collector Current[1]	I_{CM}		40		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25° C	P_D		75		W
Derate Above 25° C			0.6		W/° C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0V; IGT4D11	400	—	—	V
		IGT4E11	500	—	—	
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}, T_C = 25°C	2	4.0	5	V
		T_C = 150°C	—	2.5	—	
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C	—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]	—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V	—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10A, V_{GE} = 15V, T_C = 25°C	—	2.5	2.7	V
		I_C = 10A, V_{GE} = 15V, T_C = 150°C	—	2.8	—	
		I_C = 10A, V_{GE} = 10V, T_C = 25°C	—	2.9	—	
Input Capacitance	C_{ies}	V_{GE} = 0V	—	1050	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25V	—	340	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =125°C	—	100	—	ns
Rise Time	t_r	I_C = 10A, V_{CE} = Rated V_{CES}	—	100	—	
Turn-off Delay Time	$t_{d(off)}$	V_{GE} = 15V	—	0.4	—	μs
Fall Time	t_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	2.5	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 150°C	—	0.8	1.6	μs
Fall Time	t_f	L = 550μH, I_C = 10A,	—	0.8	1.0	
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V	—	0.6	0.8	
Turn-off Switching Losses	E_f	$R_{G(on)}$ = 50Ω, R_{GE} = 100Ω; IGT4D11	—	1.3	1.6	mJ
		IGT4E11	—	1.6	2.0	
Thermal Resistance, Junction to Case	$R_{\theta JC}$		1.67		1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L		260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 3.3°C per watt maximum thermal resistance, case to ambient.

IGT4D11, IGT4E11

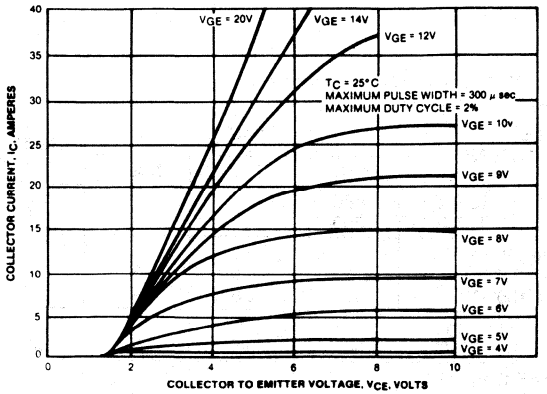


Fig. 1 - Typical Output Characteristics

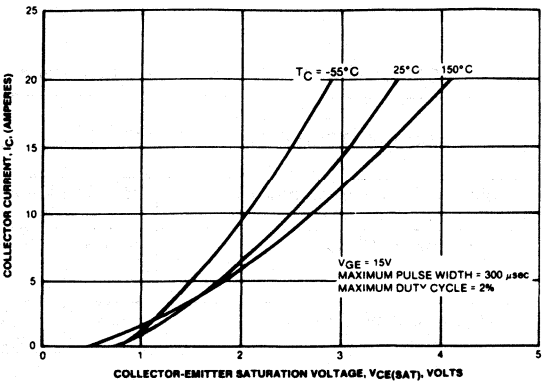


Fig. 2 - Typical Collector-Emitter Saturation Voltage

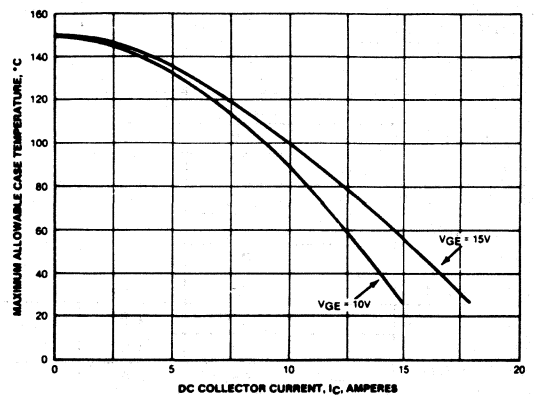


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

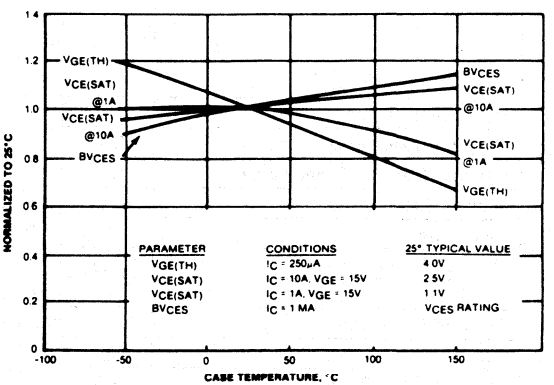


Fig. 4 - Typical Temperature Dependence of Parameters

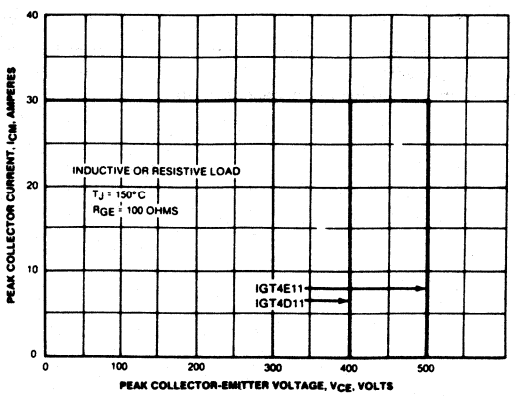


Fig. 5 - Turn-off Safe Operating Area

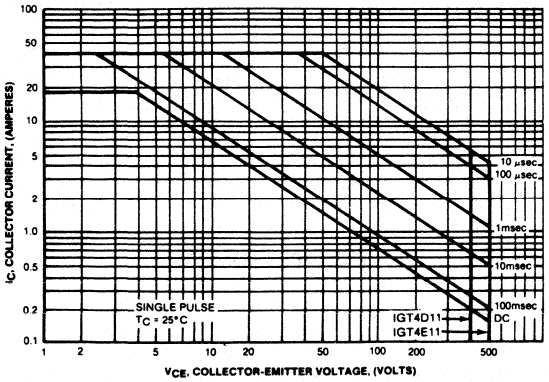


Fig. 6 - Turn-on Safe Operating Area

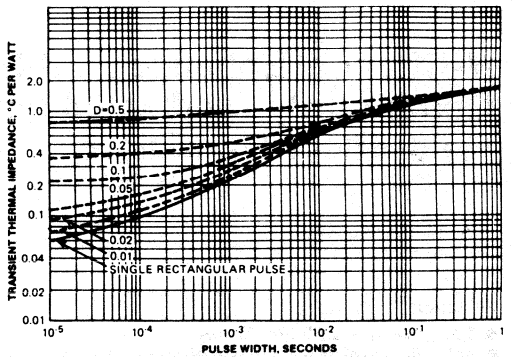


Fig. 7 - Maximum Transient Thermal Impedance

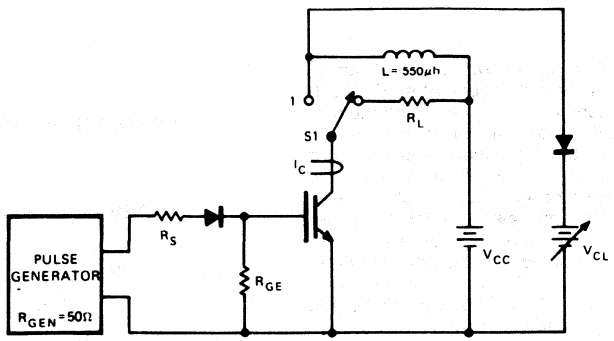


Fig. 8 - Basic Switching Test Circuit

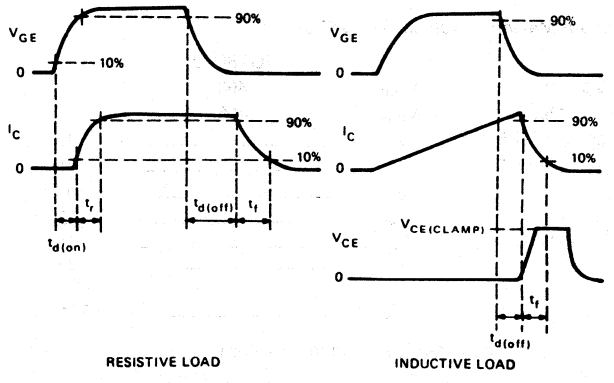


Fig. 9 - Switching Waveforms

IGT6D10, IGT6E10

File Number **2125**

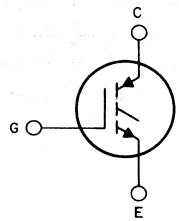
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

10A, 400V and 500V
r_{DS} (on) = 0.27 Ω

Features:

- *Low $V_{CE(SAT)}$ — 2.5V typ. @ 10A*
- *Ultra-fast turn-on — 150 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 10 amps @ 100° C*

TERMINAL DIAGRAM



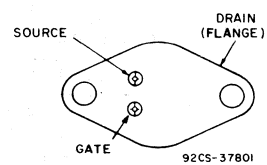
N-CHANNEL ENHANCEMENT MODE

The IGT6D10 and IGT6E10 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IGT6D10		IGT6E10	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 100° C	I_C		10		A
@ T_C = 25° C			18		A
Pulsed Collector Current[1]	I_{CM}		40		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25° C	P_D		75		W
Derate Above 25° C			0.6		W/° C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0V	IGT6D10	400	—	—	V
			IGT6E10	500	—	—	
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}, T_C = 25°C		2	4.0	5	V
		T_C = 150°C		—	2.5	—	
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C		—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]		—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10A, V_{GE} = 15V, T_C = 25°C		—	2.5	2.7	V
		I_C = 10A, V_{GE} = 15V, T_C = 150°C		—	2.8	—	
		I_C = 10A, V_{GE} = 10V, T_C = 25°C		—	2.9	—	
Input Capacitance	C_{ies}	V_{GE} = 0V		—	1050	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25V		—	340	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz		—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =150°C		—	100	—	ns
Rise Time	t_r	I_C = 10A, V_{CE} = Rated V_{CES}		—	150	—	
Turn-off Delay Time	$t_{d(off)}$	V_{GE} = 15V		—	0.5	—	μs
Fall Time	t_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω		—	4	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 150°C		—	1.0	1.8	μs
Fall Time	t_f	L = 550μH, I_C = 10A,		—	4.5	6.5	
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V		—	3.5	5.0	
Turn-off Switching Losses	E_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	IGT6D10	—	—	10	mJ
			IGT6E10	—	—	12.5	
Thermal Resistance, Junction to Case	$R_{\theta JC}$			1.67		1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L			260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 3.3°C per watt maximum thermal resistance, case to ambient.

IGT6D10, IGT6E10

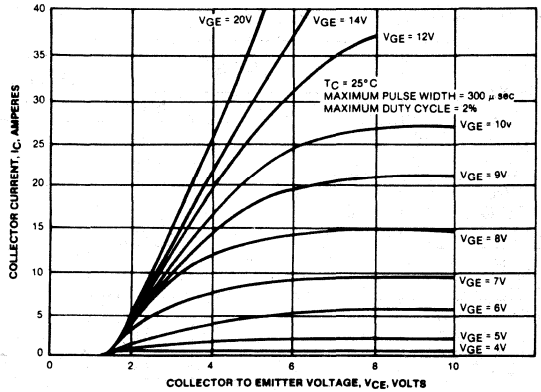


Fig. 1 - Typical Output Characteristics

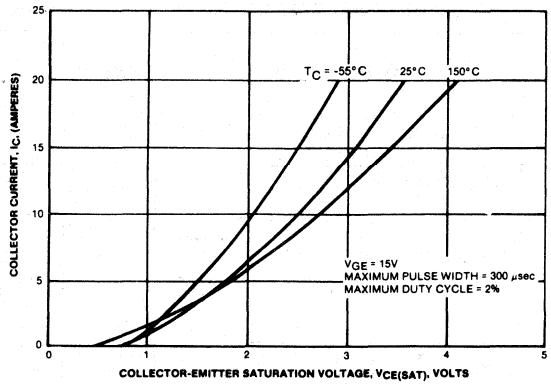


Fig. 2 - Typical Collector-Emitter Saturation Voltage

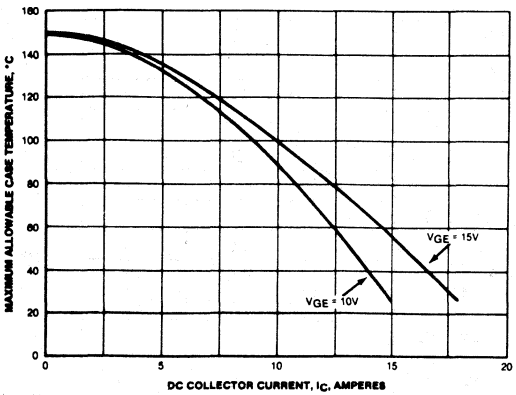


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

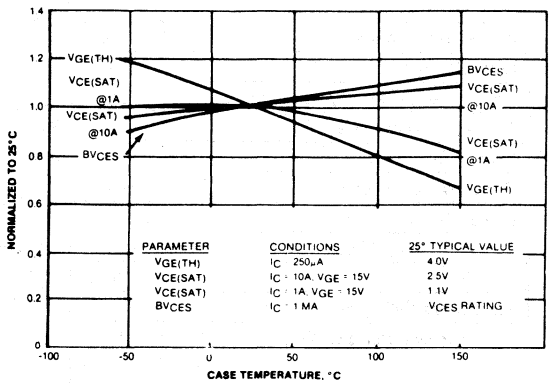


Fig. 4 - Typical Temperature Dependence of Parameters

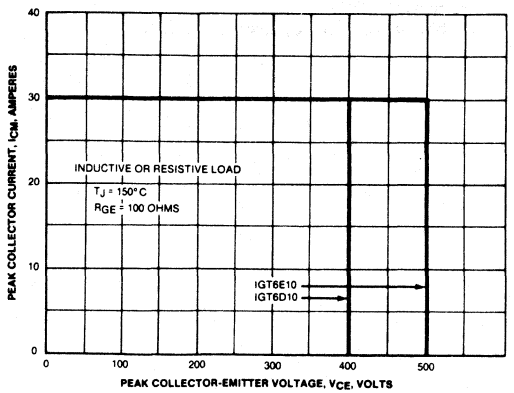


Fig. 5 - Turn-off Safe Operating Area

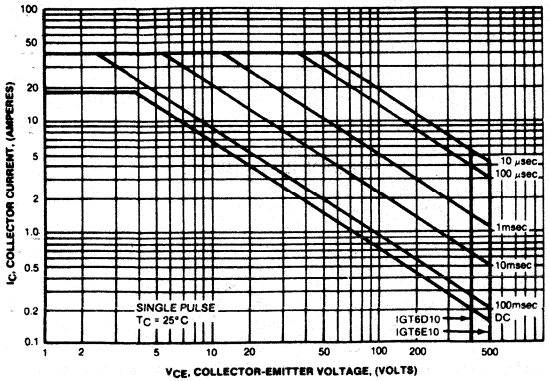


Fig. 6 - Turn-on Safe Operating Area

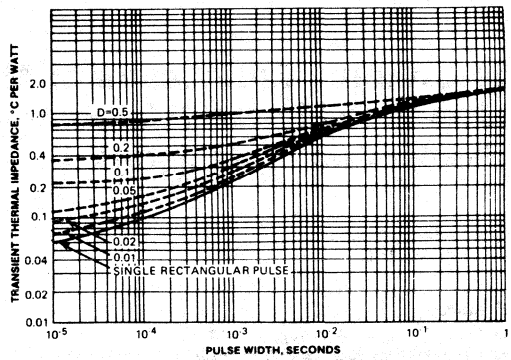
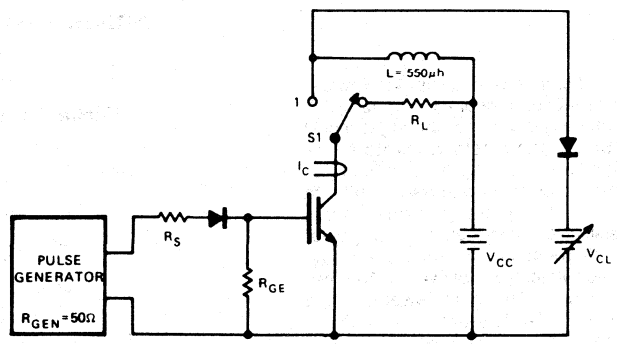


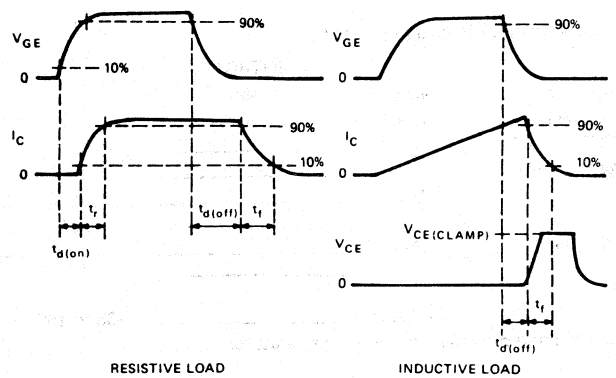
Fig. 7 - Maximum Transient Thermal Impedance



S1 (SWITCH POSITION) –1 CLAMPED INDUCTIVE LOAD
–2 RESISTIVE LOAD

$$R_{G(ON)} = \frac{(R_{GEN}+R_S)(R_{GE})}{R_{GEN}+R_S+R_{GE}}, \text{ PULSE WIDTH} \geq 60\mu\text{sec}, V_{CC} = \frac{L \cdot I_{C(MAXIMUM)}}{\text{PULSE WIDTH}}$$

Fig. 8 - Basic Switching Test Circuit



(WAVEFORMS NOT TO SCALE)

Fig. 9 - Switching Waveforms

IGT6D11, IGT6E11

File Number **2126**

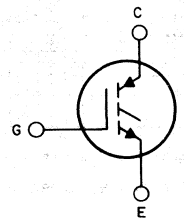
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

10A, 400V and 500V
r_{DS} (on) = 0.27 Ω

Features:

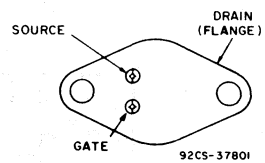
- *Low $V_{CE(SAT)}$ — 2.5V typ. @ 10A*
- *Ultra-fast turn-on — 150 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 10 amps @ 100°C*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA

The IGT6D11 and IGT6E11 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25°C and 150°C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-204AA steel package.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

		IGT6D11		IGT6E11	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 100°C	I_C		10		A
@ T_C = 25°C			18		A
Pulsed Collector Current(1)	I_{CM}		40		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25°C	P_D		75		W
Derate Above 25°C			0.6		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0V — IGT6D11	400	—	—	V
		IGT6E11	500	—	—	
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}, T_C = 25°C	2	4.0	5	V
		T_C = 150°C	—	2.5	—	
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C	—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]	—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V	—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10A, V_{GE} = 15V, T_C = 25°C	—	2.5	2.7	V
		I_C = 10A, V_{GE} = 15V, T_C = 150°C	—	2.8	—	
		I_C = 10A, V_{GE} = 10V, T_C = 25°C	—	2.9	—	
Input Capacitance	C_{ies}	V_{GE} = 0V	—	1050	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25V	—	340	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =125°C	—	100	—	ns
Rise Time	t_r	I_C = 10A, V_{CE} = Rated V_{CES}	—	100	—	
Turn-off Delay Time	$t_{d(off)}$	V_{GE} = 15V	—	0.4	—	μs
Fall Time	t_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	2.5	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 125°C	—	0.8	1.6	μs
Fall Time	t_f	L = 550μH, I_C = 10A,	—	0.8	1.0	
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V	—	0.6	0.8	
Turn-off Switching Losses	E_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω, IGT6D11	—	1.3	1.6	mJ
		IGT6E11	—	1.6	2.0	
Thermal Resistance, Junction to Case	$R_{\theta JC}$		1.67		1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L		260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 3.3°C per watt maximum thermal resistance, case to ambient.

IGT6D11, IGT6E11

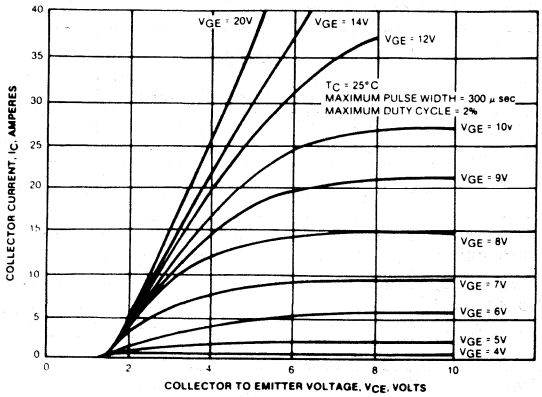


Fig. 1 - Typical Output Characteristics

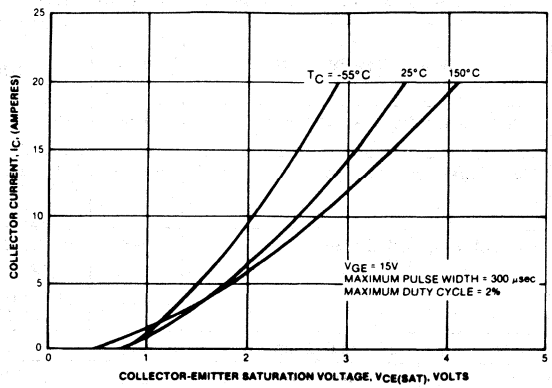


Fig. 2 - Typical Collector-Emitter Saturation Voltage

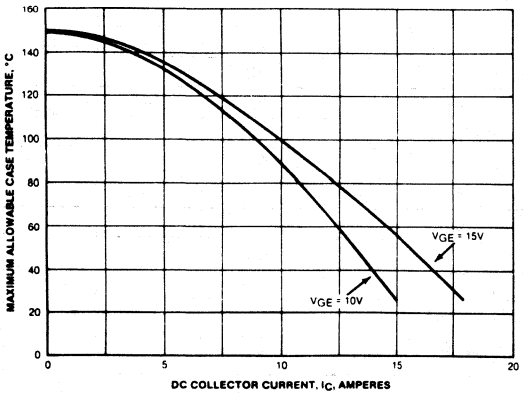


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

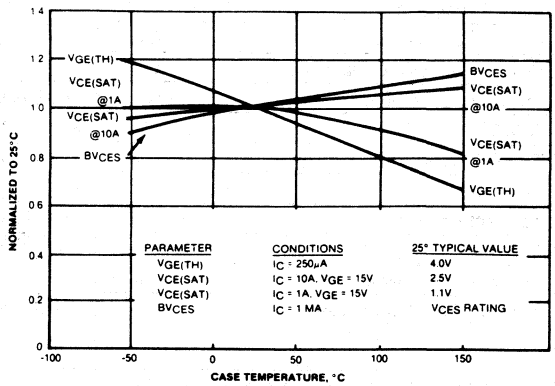


Fig. 4 - Typical Temperature Dependence of Parameters

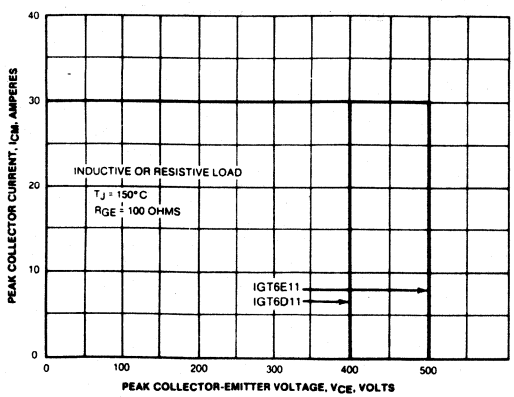


Fig. 5 - Turn-off Safe Operating Area

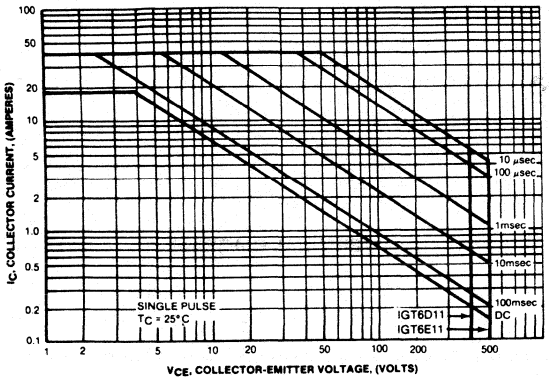


Fig. 6 - Turn-on Safe Operating Area

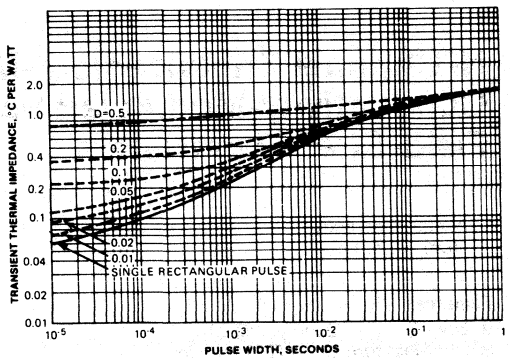


Fig. 7 - Maximum Transient Thermal Impedance

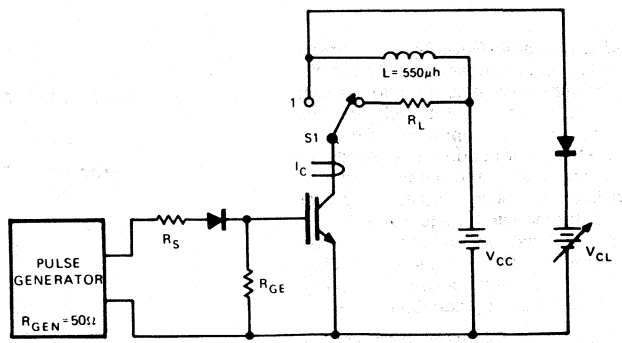


Fig. 8 - Basic Switching Test Circuit

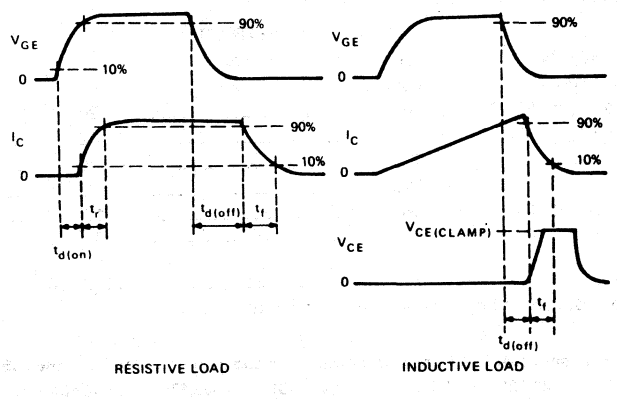


Fig. 9 - Switching Waveforms

IGT6D20, IGT6E20

File Number **2127**

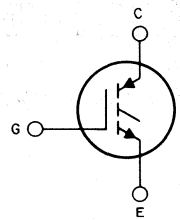
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

20A, 400V and 500V
r_{DS} (on) = 0.12 Ω

Features:

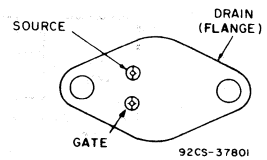
- *Low $V_{CE(SAT)}$ — 2.3V typ. @ 20A*
- *Ultra-fast turn-on — 200 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 20 amps @ 100° C*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA

The IGT6D20 and IGT6E20 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-204AA steel package.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IGT6D20		IGT6E20	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 100° C	I_C		20		A
@ T_C = 25° C			32		A
Pulsed Collector Current(1)	I_{CM}		80		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25° C	P_D		125		W
Derate Above 25° C			1.0		W/° C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0V, IGT6D20	400	—	—	V
		I_C = 250 μA, V_{GE} = 0V, IGT6E20	500	—	—	
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}, T_C = 25°C	2	4.0	5	V
		I_C = 250μA, V_{CE} = V_{GE}, T_C = 150°C	—	2	—	
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C	—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]	—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V	—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20A, V_{GE} = 15V, T_C = 25°C	—	2.3	2.4	V
		I_C = 20A, V_{GE} = 15V, T_C = 150°C	—	2.4	—	
		I_C = 20A, V_{GE} = 10V, T_C = 25°C	—	2.8	—	
Input Capacitance	C_{ies}	V_{GE} = 0V, V_{CE} = 25V, f = 1 MHz	—	2300	—	pF
Output Capacitance	C_{oes}		—	700	—	
Reverse Transfer Capacitance	C_{res}		—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =150°C, I_C = 20A, V_{CE} = Rated V_{CES}, V_{GE} = 15V, $R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	100	—	ns
Rise Time	t_r		—	200	—	
Turn-off Delay Time	$t_{d(off)}$		—	0.65	—	μs
Fall Time	t_f		—	5.0	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 150°C, L = 550μH, I_C = 20A, $V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V, $R_{G(on)}$ = 50Ω, R_{GE} = 100Ω	—	1.0	2	μs
Fall Time	t_f		—	4.5	6.5	
Equivalent Fall Time	$t_{f(eq)}$		—	3.5	5.0	
Turn-off Switching Losses	E_f	IGT6D20	—	14	20	mJ
		IGT6E20	—	17.5	25	
Thermal Resistance, Junction to Case	$R_{\theta JC}$		1.0		1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L		260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 4° C per watt maximum thermal resistance, case to ambient.

IGT6D20, IGT6D20

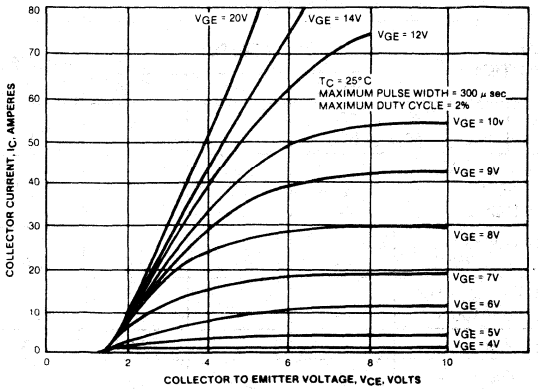


Fig. 1 - Typical Output Characteristics

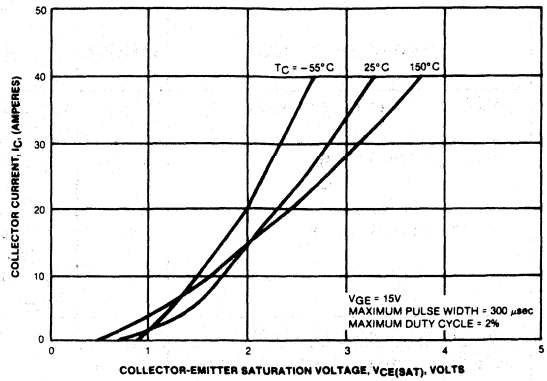


Fig. 2 - Typical Collector-Emitter Saturation Voltage

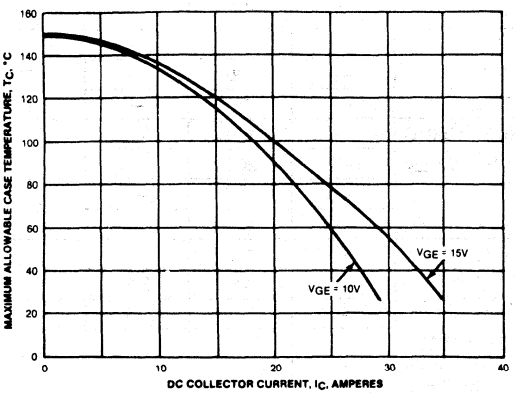


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

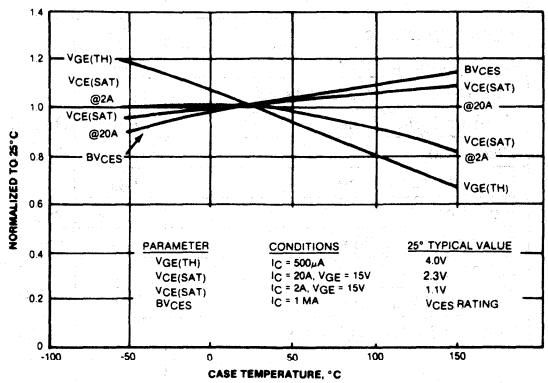


Fig. 4 - Typical Temperature Dependence of Parameters

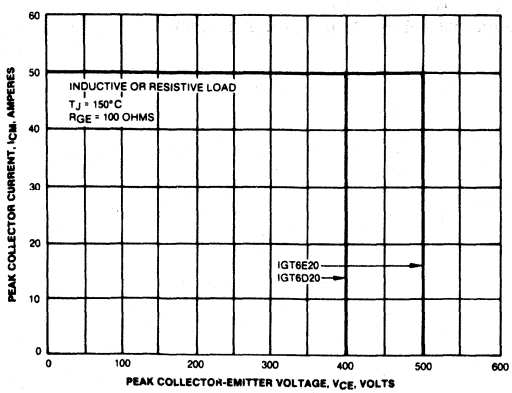


Fig. 5 - Turn-off Safe Operating Area

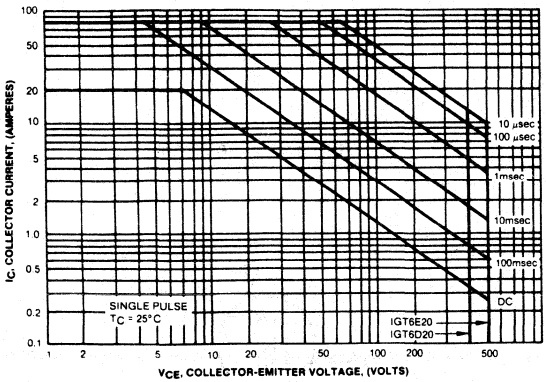


Fig. 6 - Turn-on Safe Operating Area

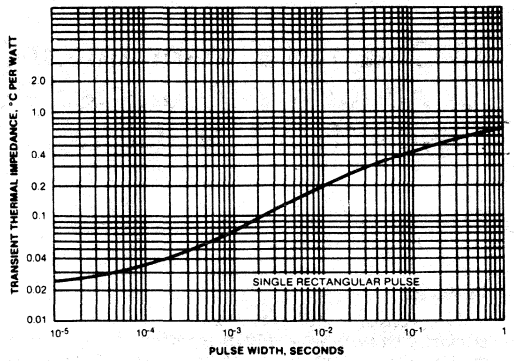
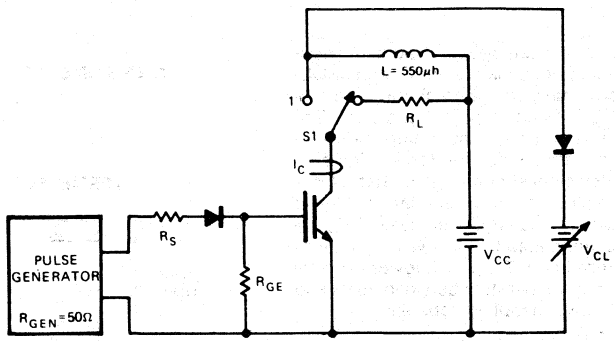


Fig. 7 - Maximum Transient Thermal Impedance



$$R_{G(ON)} = \frac{(R_{GEN}+R_S)(R_{GE})}{R_{GEN}+R_S+R_{GE}}, \text{ PULSE WIDTH} \geq 60\mu\text{sec}, V_{CC} = \frac{L \cdot I_{C\,(MAXIMUM)}}{\text{PULSE WIDTH}}$$

Fig. 8 - Basic Switching Test Circuit

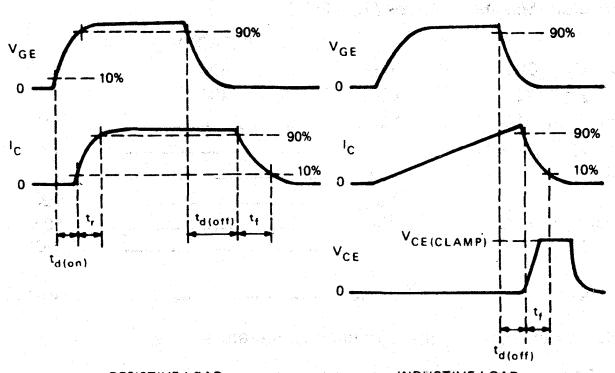


Fig. 9 - Switching Waveforms

IGT6D21, IGT6E21

File Number **2128**

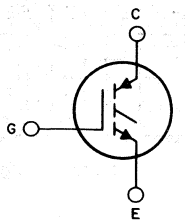
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

20A, 400V and 500V
r_{DS} (on) = 0.145 Ω

Features:

- *Low $V_{CE(SAT)}$ — 2.5V typ. @ 20A*
- *Ultra-fast turn-on — 150 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 20 amps @ 90° C*

TERMINAL DIAGRAM



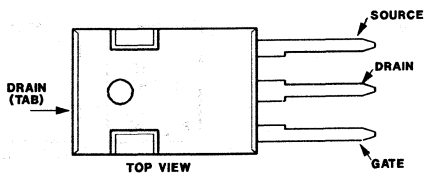
The IGT6D21 and IGT6E21 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-247 steel package.

N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-247

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IGT6D21		IGT6E21	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 90° C	I_C		20		A
@ T_C = 25° C			32		A
Pulsed Collector Current[1]	I_{CM}		80		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25° C	P_D		125		W
Derate Above 25° C			1.0		W/° C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0V; IGT6D21	400	—	—	V
		IGT6E21	500	—	—	
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}, T_C = 25°C	2	4.0	5	V
		T_C = 150°C	—	2	—	
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C	—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]	—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V	—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20A, V_{GE} = 15V, T_C = 25°C	—	2.5	2.9	V
		I_C = 20A, V_{GE} = 15V, T_C = 150°C	—	2.6	—	
		I_C = 20A, V_{GE} = 10V, T_C = 25°C	—	3.0	—	
Input Capacitance	C_{ies}	V_{GE} = 0V	—	2300	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25V	—	700	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =125°C	—	100	—	ns
Rise Time	t_r	I_C = 20A, V_{CE} = Rated V_{CES}	—	150	—	
Turn-off Delay Time	$t_{d(off)}$	V_{GE} = 15V	—	0.60	—	μs
Fall Time	t_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	3.0	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 125°C	—	0.8	1.8	μs
Fall Time	t_f	L = 550μH, I_C = 20A,	—	0.8	1.0	
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V	—	0.6	0.8	
Turn-off Switching Losses	E_f	$R_{G(on)}$ = 50Ω, R_{GE} = 100Ω; IGT6D21	—	2.6	3.2	mJ
		IGT6E21	—	3.2	4.0	
Thermal Resistance, Junction to Case	$R_{\theta JC}$		1.0		1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L		260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 4°C per watt maximum thermal resistance, case to ambient.

IGT6D21, IGT6E21

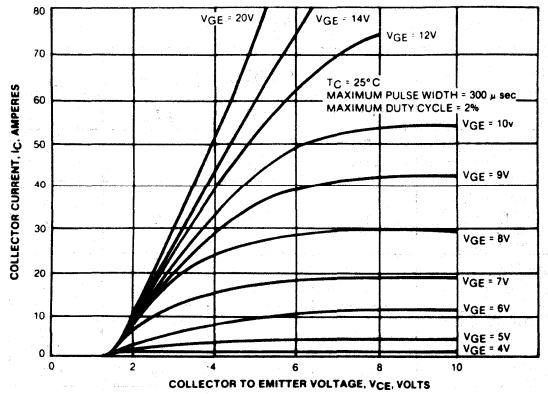


Fig. 1 - Typical Output Characteristics

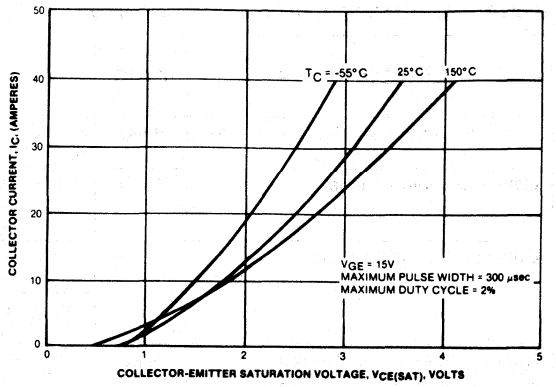


Fig. 2 - Typical Collector-Emitter Saturation Voltage

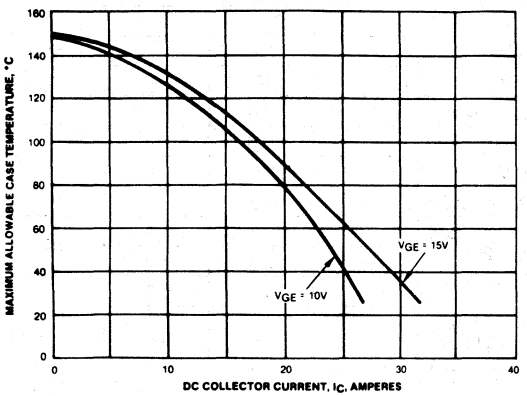


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

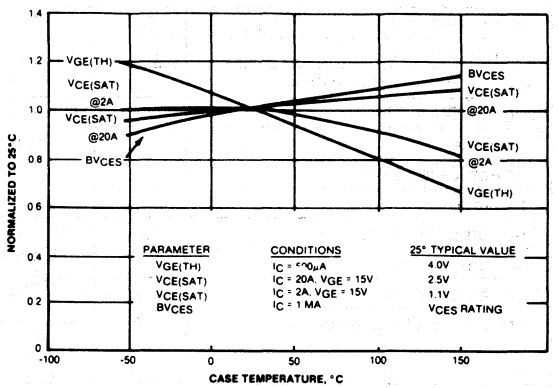


Fig. 4 - Typical Temperature Dependence of Parameters

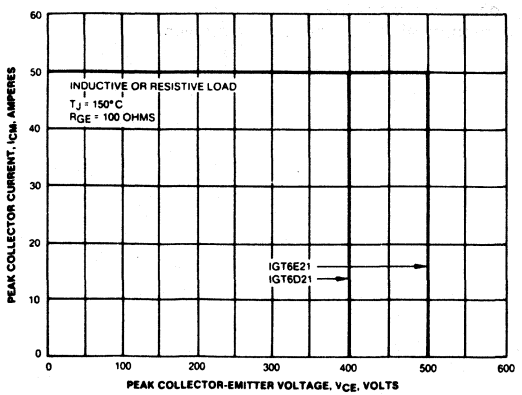


Fig. 5 - Turn-off Safe Operating Area

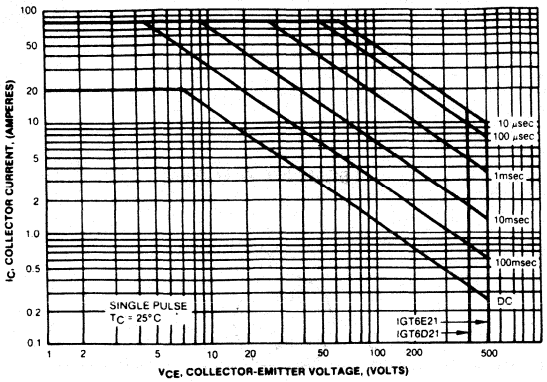


Fig. 6 - Turn-on Safe Operating Area

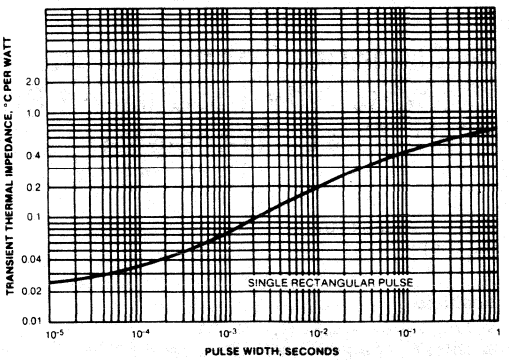
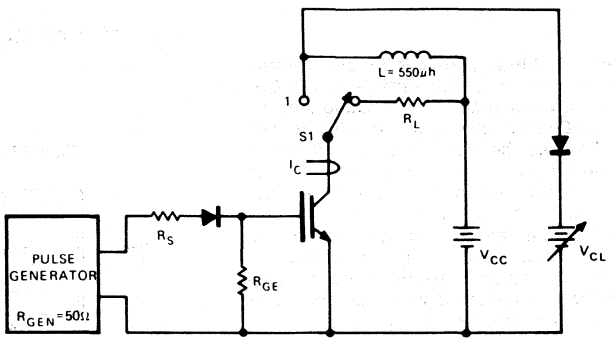


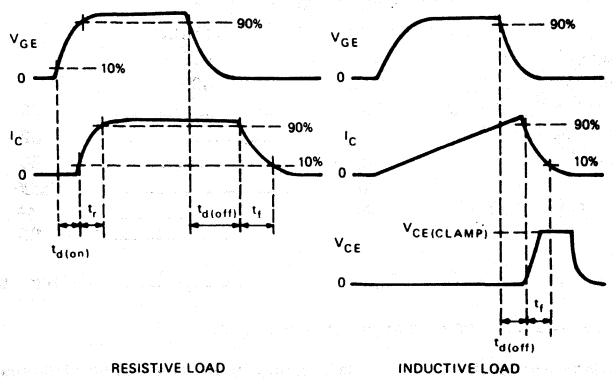
Fig. 7 - Maximum Transient Thermal Impedance



S1 (SWITCH POSITION) –1 CLAMPED INDUCTIVE LOAD
–2 RESISTIVE LOAD

$$R_{G(ON)} = \frac{(R_{GEN}+R_S)(R_{GE})}{R_{GEN}+R_S+R_{GE}}, \text{ PULSE WIDTH} \geq 60\mu\text{sec}, V_{CC} = \frac{L \cdot I_{C(MAXIMUM)}}{\text{PULSE WIDTH}}$$

Fig. 8 - Basic Switching Test Circuit



(WAVEFORMS NOT TO SCALE)

Fig. 9 - Switching Waveforms

IGT8D20, IGT8E20

File Number **2129**

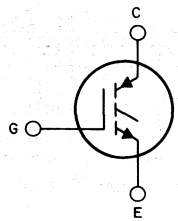
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

20A, 400V and 500V
r_{DS} (on) = 0.12 Ω

Features:

- *Low $V_{CE(SAT)}$ — 2.3V typ. @ 20A*
- *Ultra-fast turn-on — 200 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 20 amps @ 100° C*

TERMINAL DIAGRAM



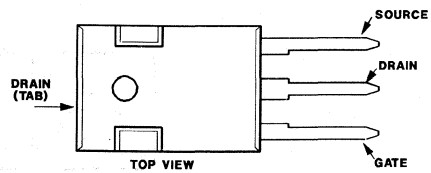
N-CHANNEL ENHANCEMENT MODE

The IGT8D20 and IGT8E20 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IGT8D20		IGT8E20	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 100° C	I_C		20		A
@ T_C = 25° C			32		A
Pulsed Collector Current(1)	I_{CM}		80		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25° C	P_D		125		W
Derate Above 25° C			1.0		W/° C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0V; IGT8D20 / IGT8E20	400 500	— —	— —	V
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}; T_C = 25°C / T_C = 150°C	2 —	4.0 2	5 —	V
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C	—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]	—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V	—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20A, V_{GE} = 15V, T_C = 25°C	—	2.3	2.4	V
		I_C = 20A, V_{GE} = 15V, T_C = 150°C	—	2.4	—	
		I_C = 20A, V_{GE} = 10V, T_C = 25°C	—	2.8	—	
Input Capacitance	C_{ies}	V_{GE} = 0V, V_{CE} = 25V, f = 1 MHz	—	2300	—	pF
Output Capacitance	C_{oes}		—	700	—	
Reverse Transfer Capacitance	C_{res}		—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =150°C	—	100	—	ns
Rise Time	t_r	I_C = 20A, V_{CE} = Rated V_{CES}	—	200	—	
Turn-off Delay Time	$t_{d(off)}$	V_{GE} = 15V	—	0.65	—	μs
Fall Time	t_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	5.0	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 150°C	—	1.0	2	μs
Fall Time	t_f	L = 550μH, I_C = 20A,	—	4.5	6.5	
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V	—	3.5	5.0	
Turn-off Switching Losses	E_f	$R_{G(on)}$ = 50Ω, R_{GE} = 100Ω; IGT8D20 / IGT8E20	— —	14 17.5	20 25	mJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$		1.0		1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L		260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 4° C per watt maximum thermal resistance, case to ambient.

IGT8D20, IGT8E20

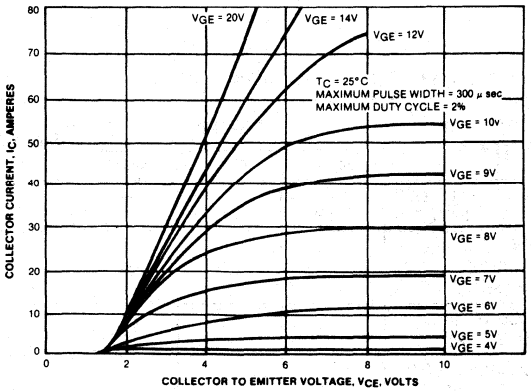


Fig. 1 - Typical Output Characteristics

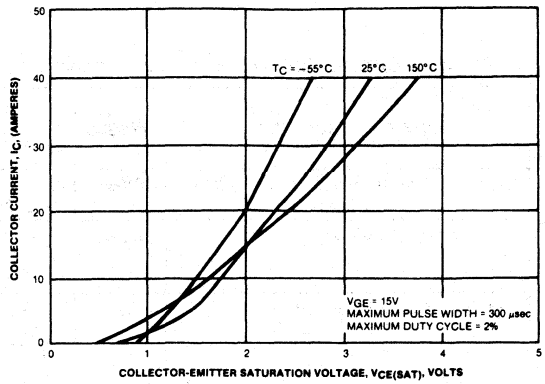


Fig. 2 - Typical Collector-Emitter Saturation Voltage

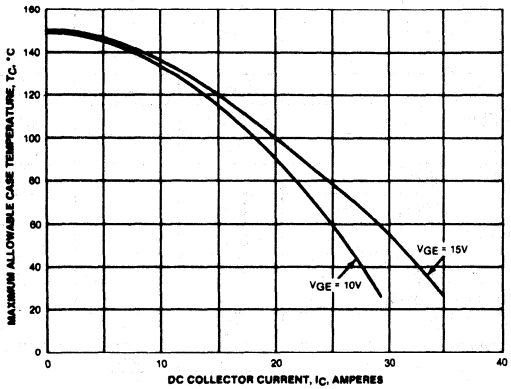


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

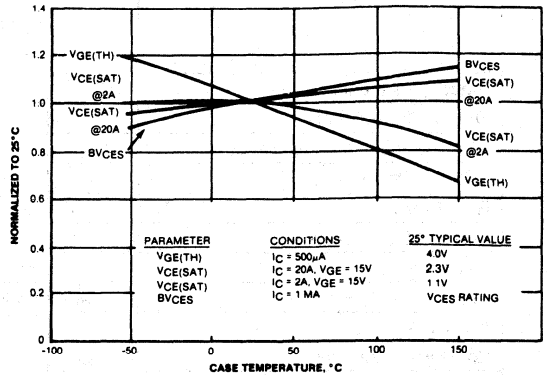


Fig. 4 - Typical Temperature Dependence of Parameters

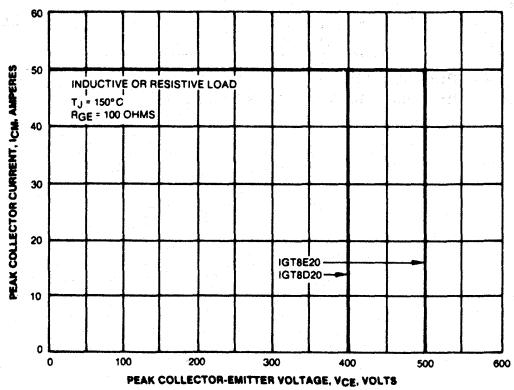


Fig. 5 - Turn-off Safe Operating Area

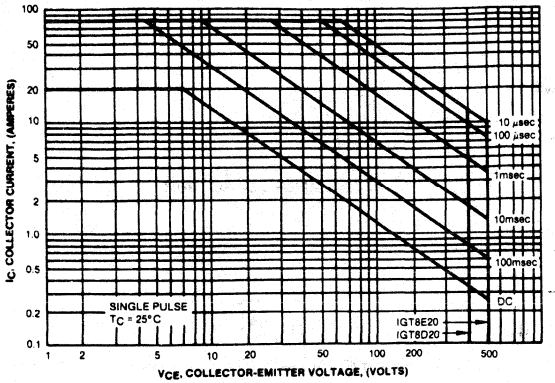


Fig. 6 - Turn-on Safe Operating Area

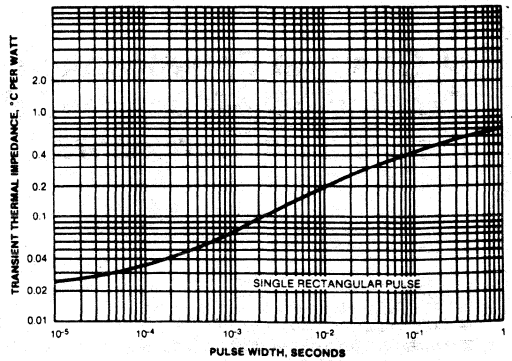
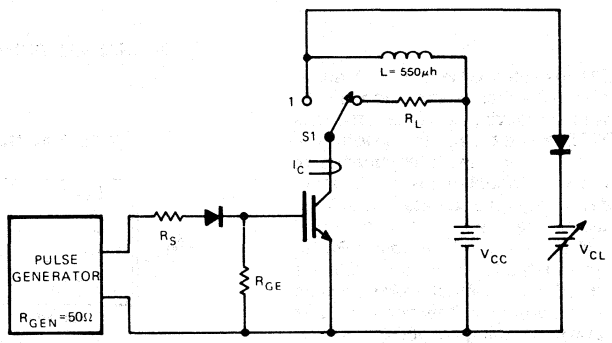


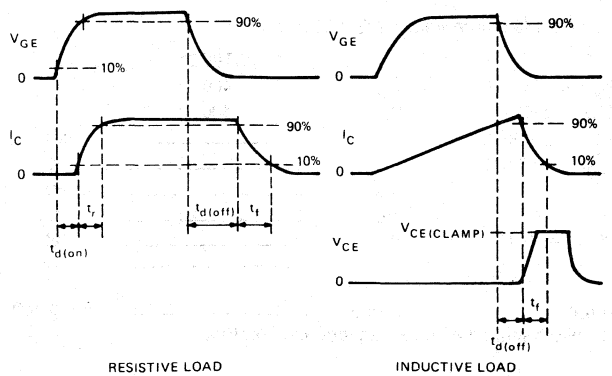
Fig. 7 - Maximum Transient Thermal Impedance



S1 (SWITCH POSITION) –1 CLAMPED INDUCTIVE LOAD
–2 RESISTIVE LOAD

$$R_{G(ON)} = \frac{(R_{GEN}+R_S)(R_{GE})}{R_{GEN}+R_S+R_{GE}}, \text{ PULSE WIDTH} > 60\mu\text{sec}, V_{CC} = \frac{L \cdot I_{C(MAXIMUM)}}{\text{PULSE WIDTH}}$$

Fig. 8 - Basic Switching Test Circuit



(WAVEFORMS NOT TO SCALE)

Fig. 9 - Switching Waveforms

IGT8D21, IGT8E21, IGT8D21, IGT8E21

File Number **2130**

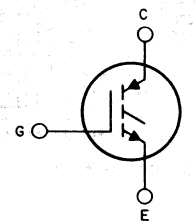
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

20A, 400V and 500V
r_{DS} (on) = 0.145 Ω

Features:

- *Low $V_{CE(SAT)}$ — 2.5V typ. @ 20A*
- *Ultra-fast turn-on — 150 ns typical*
- *Polysilicon MOS gate — Voltage controlled turn on/off*
- *High current handling — 20 amps @ 90° C*

TERMINAL DIAGRAM



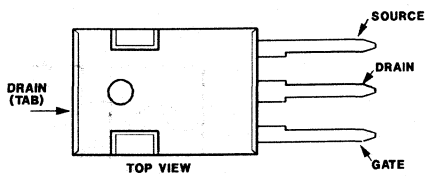
N-CHANNEL ENHANCEMENT MODE

The IGT8D21 and IGT8E21 Insulated-Gate Bipolar Transistors are a new type of n-channel enhancement-mode MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $R_{DS(ON)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

These IGT™ Transistors are ideal for many high voltage switching applications operating at low frequencies and where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The IGT™-series types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		IGT8D21		IGT8E21	
Collector-Emitter Voltage, V_{GE} = 0V	V_{CES}	400		500	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	400		500	V
Continuous Drain Current @ T_C = 90° C	I_C		20		A
@ T_C = 25° C			32		A
Pulsed Collector Current(1)	I_{CM}		80		A
Gate-Emitter Voltage	V_{GE}		±25		V
Total Power Dissipation @ T_C = 25° C	P_D		125		W
Derate Above 25° C			1.0		W/° C
Operating and Storage Junction Temperature Range	T_J, T_{STG}		-55 to 150		°C

(1) Repetitive Rating: Pulse width limited by max. junction temperature.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0V; IGT8D21	400	—	—	V
		IGT8E21	500	—	—	
Gate Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}, T_C = 25°C	2	4.0	5	V
		T_C = 150°C	—	2	—	
Collector Cut-off Current	I_{CES}	V_{CE} = Max Rating, V_{GE} = 0V, T_C = 25°C	—	—	250	μA
		V_{CE} = Max Rating, x 0.8, V_{GE} = 0V, T_C = 150°C[1]	—	—	4.0	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V	—	—	±500	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20A, V_{GE} = 15V, T_C = 25°C	—	2.5	2.9	V
		I_C = 20A, V_{GE} = 15V, T_C = 150°C	—	2.6	—	
		I_C = 20A, V_{GE} = 10V, T_C = 25°C	—	3.0	—	
Input Capacitance	C_{ies}	V_{GE} = 0V	—	2300	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25V	—	700	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	10	—	
Turn-on Delay Time	$t_{d(on)}$	Resistive Load, T_C =125° C	—	100	—	ns
Rise Time	t_r	I_C = 20A, V_{CE} = Rated V_{CES}	—	150	—	
Turn-off Delay Time	$t_{d(off)}$	V_{GE} = 15V	—	0.60	—	μs
Fall Time	t_f	$R_{G(ON)}$ = 50Ω, R_{GE} = 100Ω	—	3.0	—	
Turn-off Delay Time	$t_{d(off)}$	Inductive Load, T_C = 150° C	—	0.8	1.8	μs
Fall Time	t_f	L = 550μH, I_C = 20A,	—	0.8	1.0	
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(CLAMP)}$ = Rated V_{CES}, V_{GE} = 15V	—	0.6	0.8	mJ
Turn-off Switching Losses	E_f	$R_{G(on)}$ = 50Ω, R_{GE} = 100Ω; IGT8D21	—	2.6	3.2	
		IGT8E21	—	3.2	4.0	
Thermal Resistance, Junction to Case	$R_{\theta JC}$		1.0		1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L		260		260	°C

*Pulse test: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.
[1]Applies for 3.3° C per watt maximum thermal resistance, case to ambient.

IGT8D21, IGT8E21, IGT8D21, IGT8E21

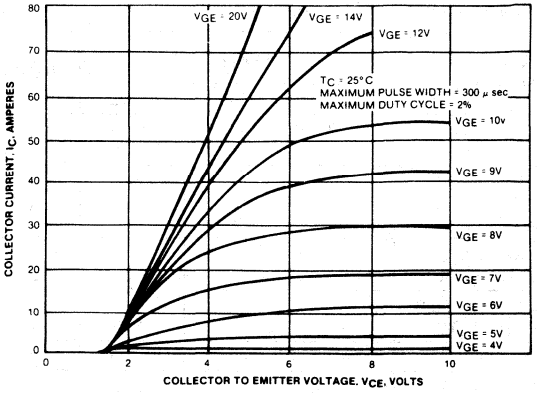


Fig. 1 - Typical Output Characteristics

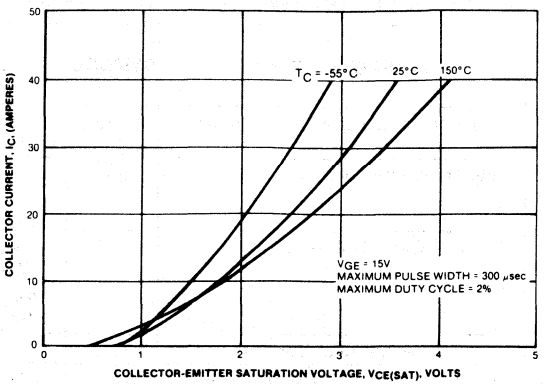


Fig. 2 - Typical Collector-Emitter Saturation Voltage

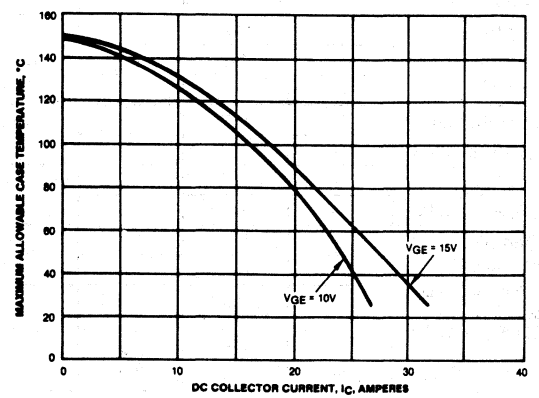


Fig. 3 - Maximum Allowable Case Temperature vs. DC Collector Current

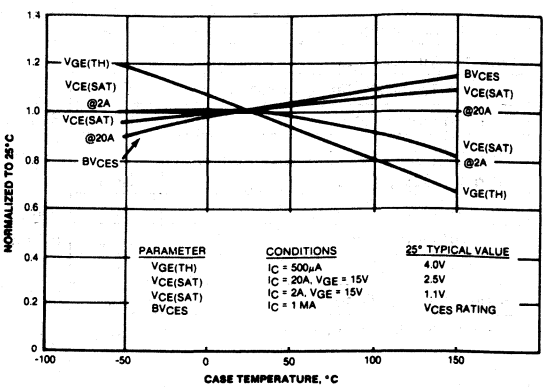


Fig. 4 - Typical Temperature Dependence of Parameters

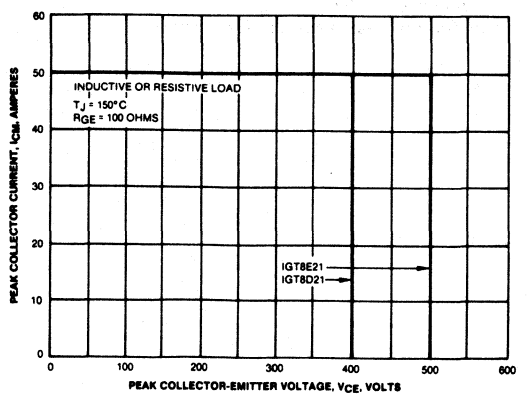


Fig. 5 - Turn-off Safe Operating Area

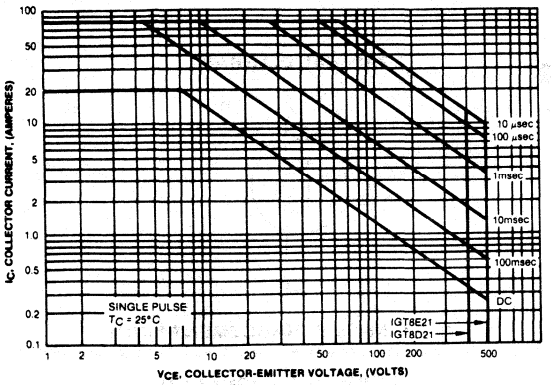


Fig. 6 - Turn-on Safe Operating Area

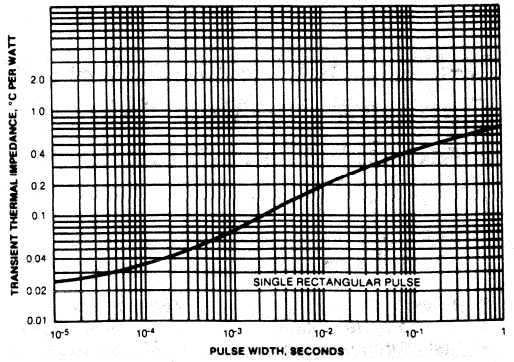
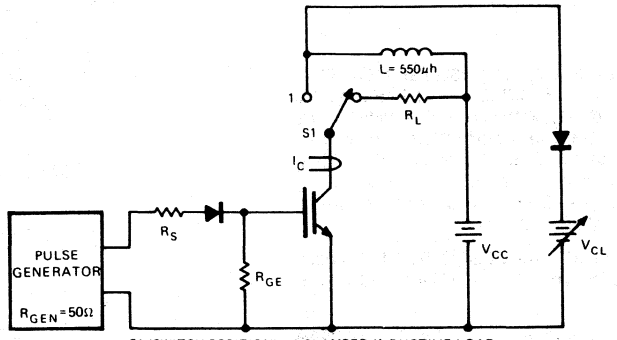


Fig. 7 - Maximum Transient Thermal Impedance



$$R_{G(ON)} = \frac{(R_{GEN}+R_S)(R_{GE})}{R_{GEN}+R_S+R_{GE}}, \text{ PULSE WIDTH} > 60\mu\text{sec}, V_{CC} = \frac{L \cdot I_{C(MAXIMUM)}}{\text{PULSE WIDTH}}$$

Fig. 8 - Basic Switching Test Circuit

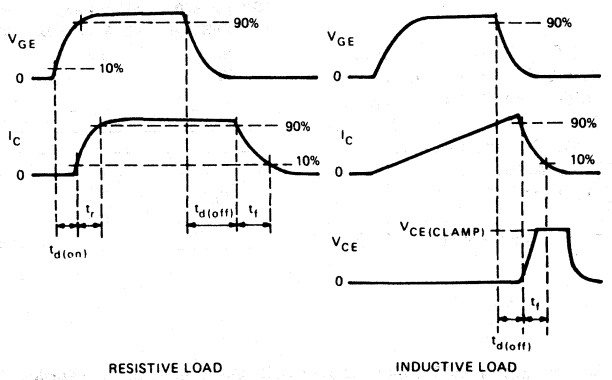


Fig. 9 - Switching Waveforms

IGTH10N40 IGTM10N40 IGTP10N40
IGTH10N40A IGTM10N40A IGTP10N40A
IGTH10N50 IGTM10N50 IGTP10N50
IGTH10N50A IGTM10N50A IGTP10N50A

File Number **1697**

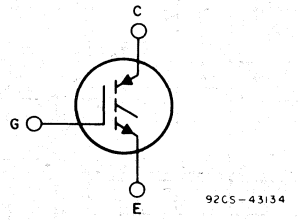
N-Channel Enhancement Mode Conductivity-Modulated Power Field-Effect Transistors

10 A, 400 V and 500 V
$V_{CE}(on)$: 2.5 V
T_{fi}: 1 μs, 0.5 μs

Features:
- *Low on-state voltage*
- *Fast switching speeds*
- *High input impedance*
- *No anti-parallel diode*

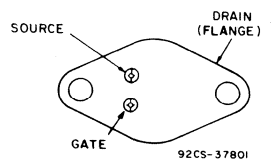
Applications:
- *Power supplies*
- *Motor drives*
- *Protective circuits*

TERMINAL DIAGRAM

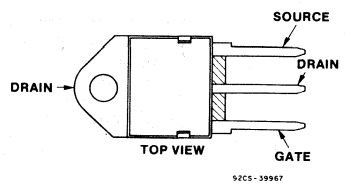


N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA



JEDEC TO-218AC

The IGTH10N40, IGTH10N40A, IGTH10N50, IGHTH10N50A, IGTP10N40, IGTP10N40A, IGTP10N50, IGTP10N50A, IGTM10N40A, IGTM10N50, IGTM10N50A* are n-channel enhancement-mode conductivity-modulated power field-effect transistors (COMFETs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

The IGTH-types are supplied in the JEDEC TO-218AC plastic package and the IGTP-types in the JEDEC TO-220AB plastic package.

The IGTM-types are supplied in the JEDEC TO-204AA steel package.

*The IGTH and IGTP series were formerly RCA Development Type Nos. TA9687 and TA9438, respectively. The IGTM series was formerly RCA Development Type No. TA9437.

MAXIMUM RATINGS,

Absolute-Maximum Values (T_C = 25° C):

	IGTH10N40 IGTH10N40A IGTM10N40 IGTM10N40A	IGTH10N50 IGTH10N50A IGTM10N50 IGTM10N50A	IGTP10N40 IGTP10N40A	IGTP10N50 IGTP10N50A	
COLLECTOR-EMITTER VOLTAGE, V_{CES}	400	500	400	500	V
COLLECTOR-GATE VOLTAGE (R_{GE} = 1 MΩ), V_{CGR}	400	500	400	500	V
REVERSE COLLECTOR-EMITTER VOLTAGE, V_{CES}(rev.)	-5				V
GATE-EMITTER VOLTAGE, V_{GE}	±20				V
COLLECTOR CURRENT, RMS Continuous, I_C	10				A
Pulsed, I_{CM}	17.5				A
POWER DISSIPATION @ T_C = 25°C, P_T	75	75	60	60	W
Derate above T_C = 25°C	0.6	0.6	0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150				°C

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

IGTH10N40 IGTH10N40A IGTH10N50 IGTH10N50A
IGTM10N40 IGTM10N40A IGTM10N50 IGTM10N50A
IGTP10N40 IGTP10N40A IGTP10N50 IGTP10N50A

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C = 25°C) unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			IGTH10N40 IGTM10N40 IGTP10N40	IGTH10N40A IGTM10N40A IGTP10N40A	IGTH10N50 IGTM10N50 IGTP10N50	IGTH10N50A IGTM10N50A IGTP10N50A	
			Min.	Max.	Min.	Max.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5 3 (typ.)	2	4.5 3 (typ.)	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V V_{CE} = 500 V	— —	250 —	— —	— 250	μA
		T_C = 125°C V_{CE} = 400 V V_{CE} = 500 V	— — —	— 1000 —	— — —	— — 1000	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On Voltage	$V_{CE}(on)$	I_D = 10 A V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 17.5 A V_{GE} = 20 V	—	3.2	—	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5 A V_{CE} = 10 V	—	6 (typ.)	—	6 (typ.)	V
On-State Gate Charge	$Q_g(on)$	I_C = 5 A V_{CE} = 10 V	—	19 (typ.)	—	19 (typ.)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 10 A $V_{CE(CLP)}$ = 300 V L = 50 μH T_J = 100°C V_{GE} = 10 V R_g = 50 Ω	—	50	—	50	ns
Rise Time	t_r		—	50	—	50	ns
Turn-Off Delay Time	$t_d(off)$		—	400	—	400	ns
Fall Time	t_{fi} 10N40 10N50		Typ. 680	1000	Typ. 680	1000	ns
	10N40A 10N50A		400	500	400	500	ns
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off} 10N40 10N50	I_C = 10 A $V_{CE(CLP)}$ = 300 V L = 50 μH T_J = 100°C V_{GE} = 10 V R_g = 50 Ω	680 (typ.)				μJ
	10N40A 10N50A		400 (typ.)				μJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	IGTH/IGTM	—	1.67	—	1.67	°C/W
		IGTP	—	2.083	—	2.083	°C/W

IGTH10N40 IGTH10N40A IGTH10N50 IGTH10N50A
IGTM10N40 IGTM10N40A IGTM10N50 IGTM10N50A
IGTP10N40 IGTP10N40A IGTP10N50 IGTP10N50A

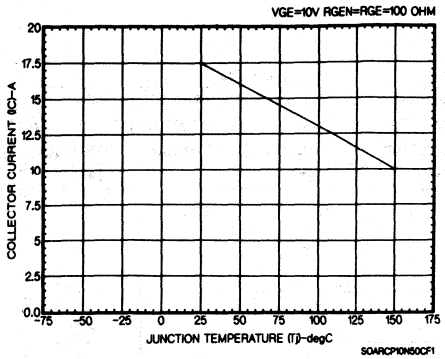


Fig. 1 - Maximum switching current level for all types. $R_g = 50\ \Omega$, $V_{GE} = 0$ V are the minimum allowable values.

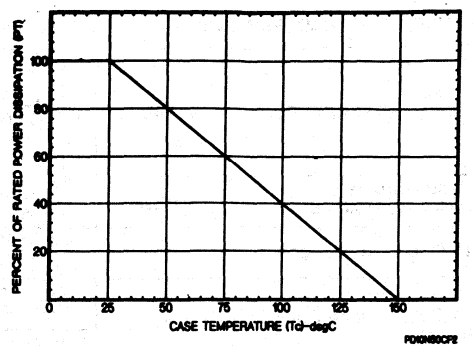


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

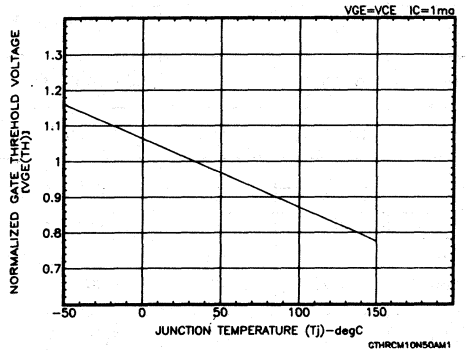


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

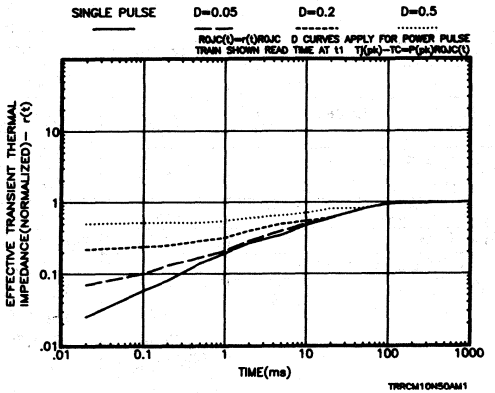


Fig. 4 - Normalized thermal response characteristics for all types.

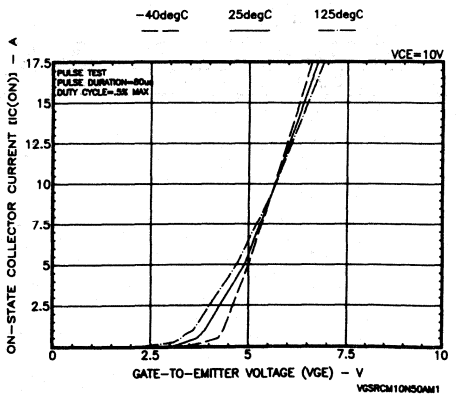


Fig. 5 - Typical transfer characteristics for all types.

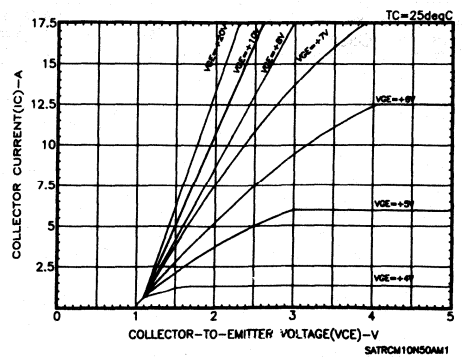


Fig. 6 - Typical saturation characteristics for all types.

IGTH10N40 IGTH10N40A IGTH10N50 IGTH10N50A
IGTM10N40 IGTM10N40A IGTM10N50 IGTM10N50A
IGTP10N40 IGTP10N40A IGTP10N50 IGTP10N50A

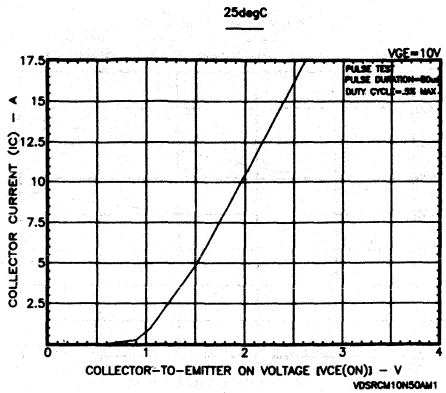


Fig. 7 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

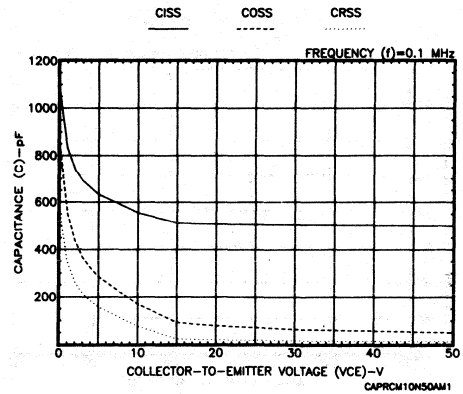


Fig. 8 - Capacitance as a function of collector-to-emitter voltage for all types.

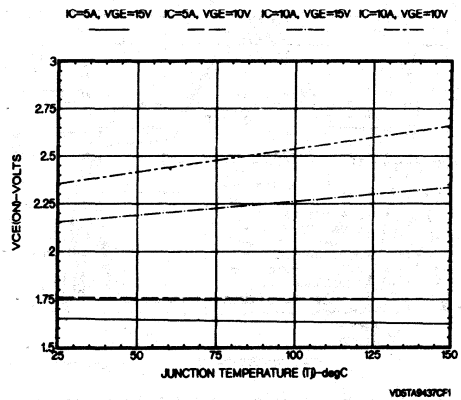


Fig. 9 - Typical $V_{CE}(on)$ vs. temperature for all types.

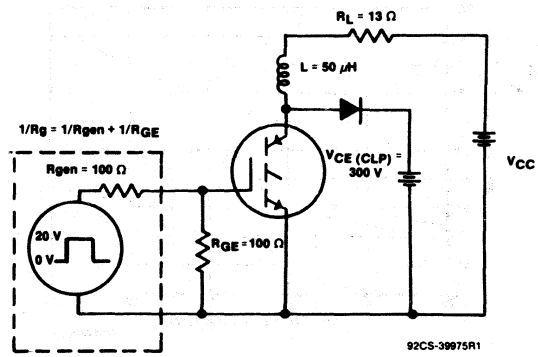


Fig. 10 - Inductive switching test circuit.

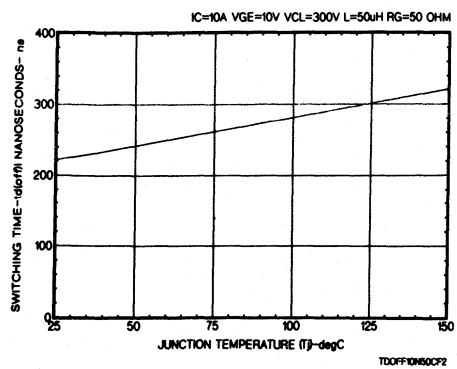


Fig. 11 - Typical turn-off delay time for all types.

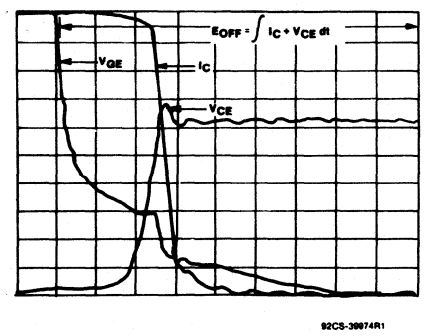


Fig. 12 - Typical inductive switching waveforms.

IGTH10N40 IGTH10N40A IGTH10N50 IGTH10N50A
IGTM10N40 IGTM10N40A IGTM10N50 IGTM10N50A
IGTP10N40 IGTP10N40A IGTP10N50 IGTP10N50A

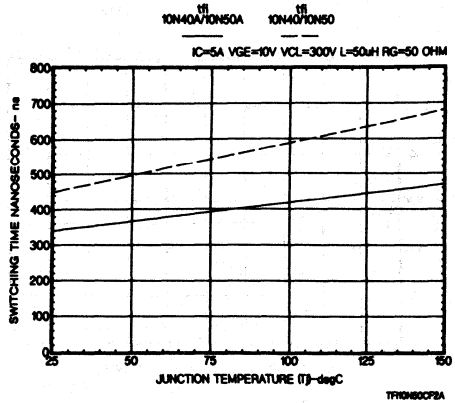


Fig. 13 - Typical fall time for all types (I_C = 5 A).

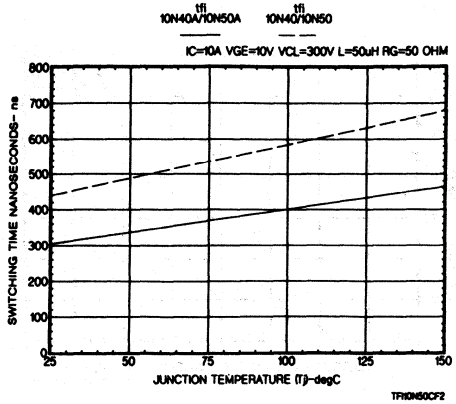


Fig. 14 - Typical fall time for all types (I_C = 10 A).

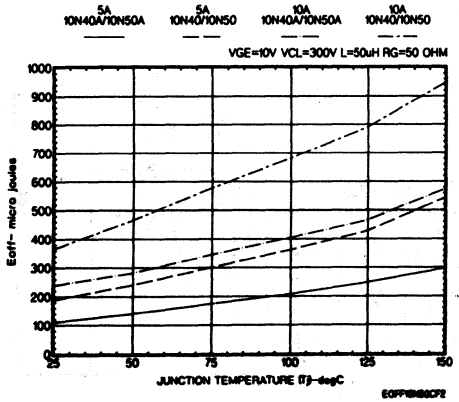
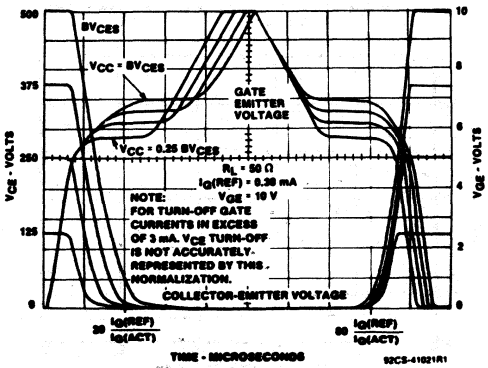


Fig. 15 - Typical clamped inductive turn-off switching loss/cycle.



Refer to RCA application notes AN-7254 and AN-7260 on the use of normalized switching waveforms.

Fig. 16 - Normalized switching waveforms at constant gate current.

File Number **2273**

IGTH10N40D, IGTH10N40AD, IGTH10N50D, IGTH10N50AD

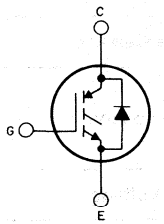
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) With Anti-Parallel Ultra-Fast Diode

10 A, 400 V and 500 V
V_{CE}(on): 2.5 V Maximum
T_{fall}: 1 μs, 0.5 μs

Features:
- *Low on-state voltage*
- *Fast switching speeds*
- *High input impedance*
- *Anti-parallel diode*

Applications:
- *Power supplies*
- *Motor drives*
- *Protective circuits*

N-CHANNEL ENHANCEMENT MODE

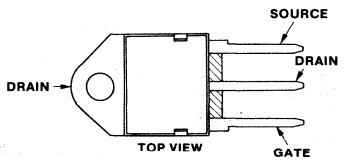


92CS-43516

TERMINAL DIAGRAM

The IGTH10N40D, IGTH10N40AD, IGTH10N50D, and IGTH10N50AD are n-channel enhancement-mode conductivity modulated field-effect transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits. They are supplied in the JEDEC TO-218AC plastic package and are fabricated using the TA9573 and TA9616 dies.

TERMINAL DESIGNATION



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

		IGTH10N40D IGTH10N40AD	IGTH10N50D IGTH10N50AD	
COLLECTOR-EMITTER VOLTAGE	V_{CES}	400	500	V
COLLECTOR-GATE VOLTAGE (R_{ge} = 1 MΩ)	V_{CGR}	400	500	V
GATE-EMITTER VOLTAGE	V_{GE}	±20		V
COLLECTOR CURRENT, RMS Continuous	I_C	10		A
Pulsed	I_{CM}	17.5		A
POWER DISSIPATION at T_C = 25° C	P_T	75		W
Derate above T_C = 25° C		0.6		W/° C
OPERATING AND STORAGE TEMPERATURE	T_J, T_S	-55 to +150		°C

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

IGTH10N40D, IGTH10N40AD, IGTH10N50D, IGTH10N50AD

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			IGTH10N40D IGTH10N40AD		IGTH10N50D IGTH10N50AD		
			MIN.	MAX.	MIN.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	V_{GE}(th)	V_{GE} = V_{CE} I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V	—	250	—	—	μA
		V_{CE} = 500 V	—	—	—	250	
		T_C = 125° C	—	—	—	—	
		V_{CE} = 400 V	—	1000	—	—	
		V_{CE} = 500 V	—	—	—	1000	
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On-Voltage	V_{CE}(on)	I_C = 10 A V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 17.5 A V_{GE} = 20 V	—	3.2	—	3.2	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5 A V_{CE} = 10 V	—	6 (typ)	—	6 (typ)	
On-State Gate Charge	Q_G(on)	I_C = 5 A V_{CE} = 10 V	—	19(typ)	—	19(typ)	nC
Turn-On Delay Time	t_d(on)	I_C = 10 A V_{CE}(clp) = 300 V L = 50 μH T_J = 100° C V_{GE} = 10 V R_g = 50 Ω	—	50	—	50	ns
Rise Time	t_r		—	50	—	50	
Turn-Off Delay Time	t_d(off)		—	400	—	400	
Fall Time	t_{fi}						
	10N40D		TYP		TYP		
	10N50D		680	1000	680	1000	
	10N40AD		TYP		TYP		
	10N50AD		400	500	400	500	
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off}	I_C = 10 A V_{CE}(clp) = 300 V L = 50 μH T_J = 100° C V_{GE} = 10 V R_g = 50 Ω					μJ
	10N40D 20N50D		1810 (typ)				
	10N40AD 10N50AD		1070 (typ)				
Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	—	1.67	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 10 A	—	2	—	2	V
Diode Reverse Recovery Time	T_{rr}	I_{EC} = 10 A di/dt = 100 A/μs	—	100	—	100	ns

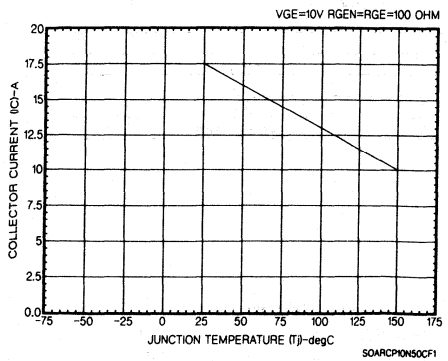


Fig. 1 - Maximum switching current level for all types. Minimum allowable values are R_g = 50 Ω, V_{GE} = 0 V.

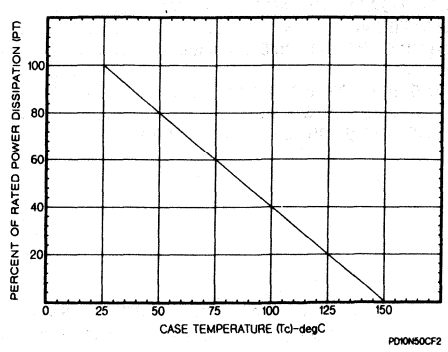


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

IGTH10N40D, IGTH10N40AD, IGTH10N50D, IGTH10N50AD

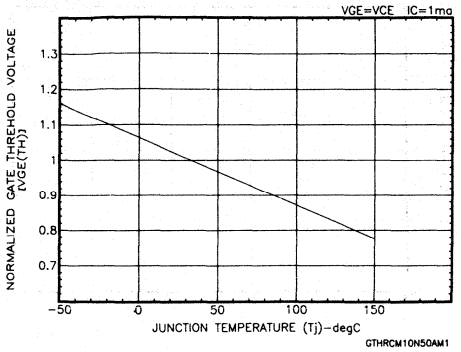


Fig. 3 - Typical normalized gate-threshold voltage as a function of junction temperature for all types.

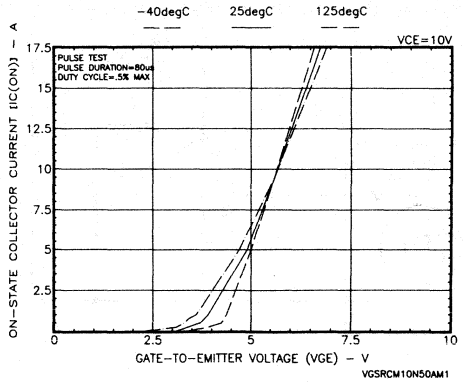


Fig. 4 - Typical transfer characteristics for all types.

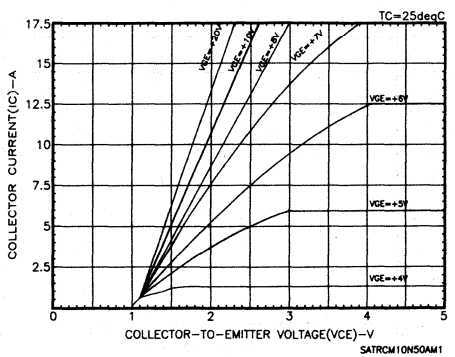


Fig. 5 - Typical saturation characteristics for all types.

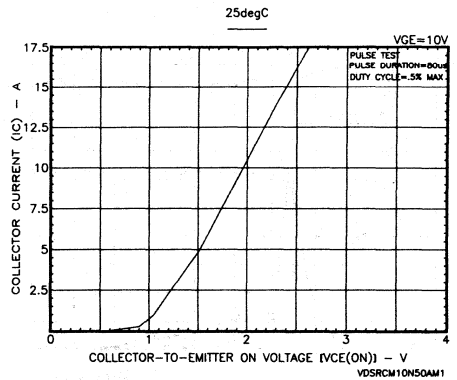


Fig. 6 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

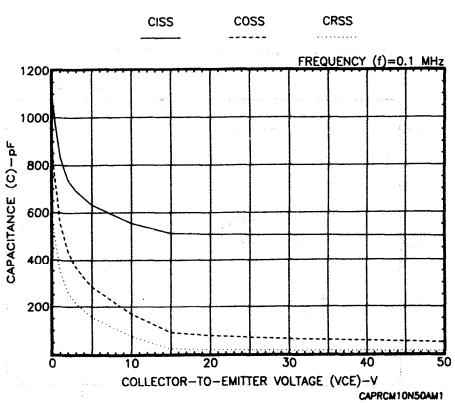


Fig. 7 - Capacitance as a function of collector-to-emitter voltage for all types.

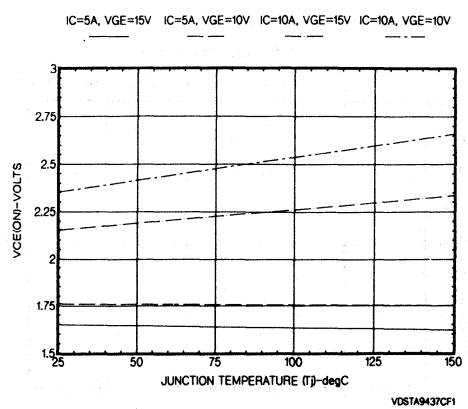


Fig. 8 - Typical $V_{CE}(on)$ vs. temperature for all types.

IGTH10N40D, IGTH10N40AD, IGTH10N50D, IGTH10N50AD

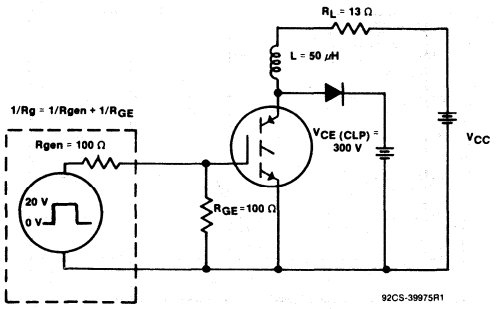


Fig. 9 - Inductive switching test circuit.

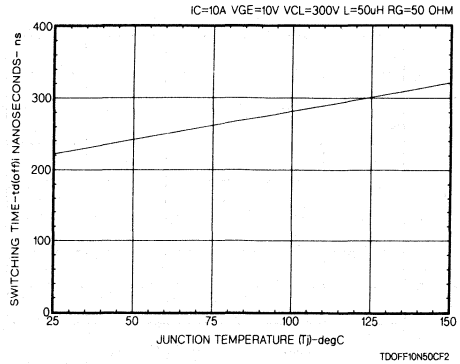


Fig. 10 - Typical turn-off delay time for all types.

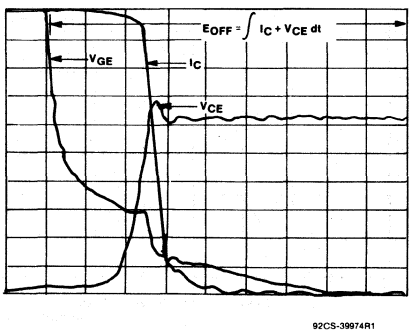


Fig. 11 - Typical inductive switching waveforms.

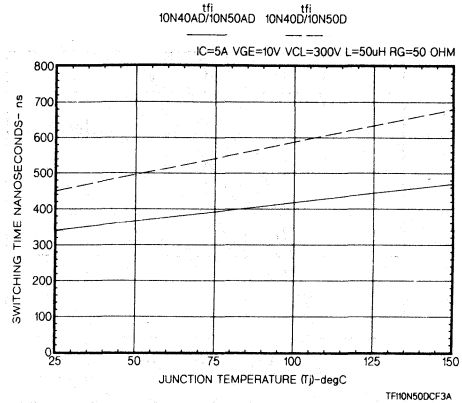


Fig. 12 - Typical fall time for all types (I_C = 5 A).

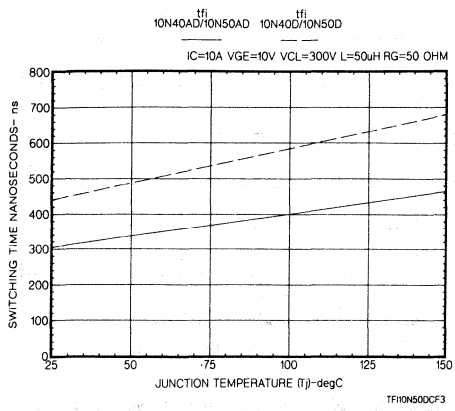


Fig. 13 - Typical fall time for all types (I_C = 10 A).

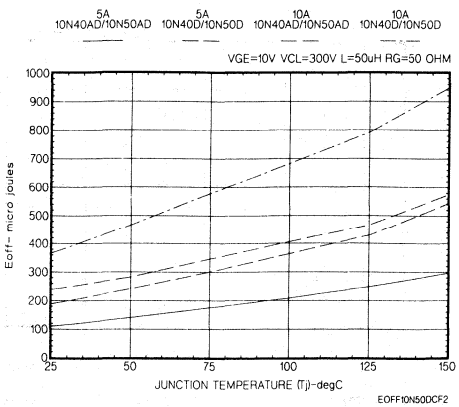


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.

IGTH10N40D, IGTH10N40AD, IGTH10N50D, IGTH10N50AD

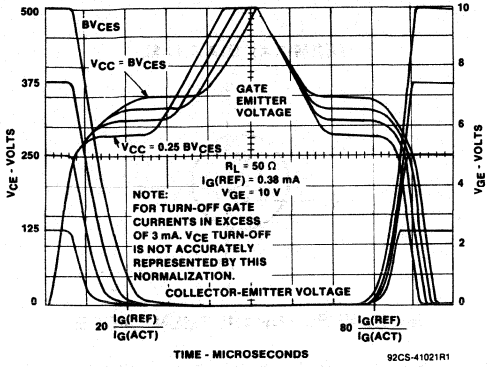


Fig. 15 - Normalized switching waveforms at constant gate current. (Refer to RCA application notes AN7254 and AN7260.)

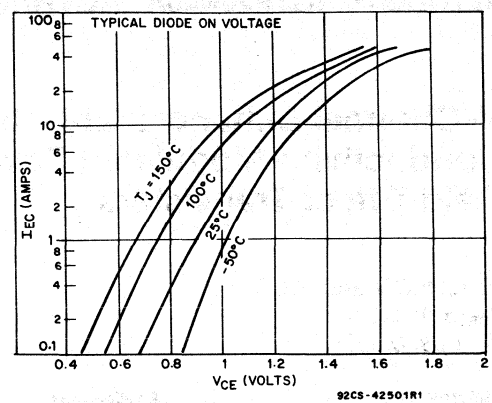


Fig. 16 - Typical diode collector-to-emitter voltage vs. current for all types.

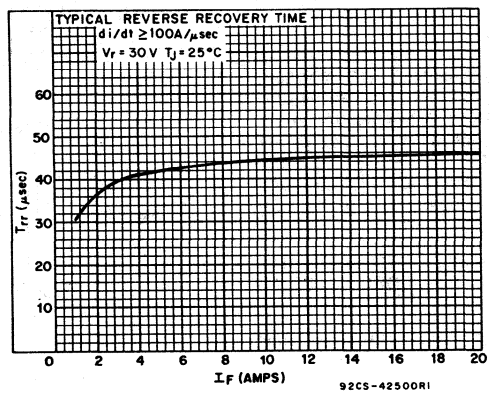


Fig. 17 - Typical diode reverse-recovery time for all types.

IGTH/IGTM/IGTP20N40 IGTH/IGTM/IGTP20N50
IGTH/IGTM/IGTP20N40A IGTH/IGTM/IGTP20N50A

File Number **2174**

N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

20 A, 400 V and 500 V
$V_{CE}(on)$: 2.5 V
T_{fi}: 1 μs, 0.5 μs

Features:
- *Low on-state voltage*
- *Fast switching speeds*
- *High input impedance*
- *No anti-parallel diode*

Applications:
- *Power supplies*
- *Motor drives*
- *Protection circuits*

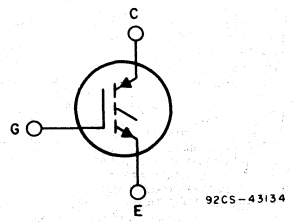
The RCH20N40, RCH20N40A, RCH20N50, RCH20N50A, RCP20N40, RCP20N40A, RCP20N50, RCP20N50A, RCM20N40, RCM20N40A, RCM20N50, RCM20N50A* are n-channel enhancement-mode conductivity-modulated power field-effect transistors designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

The RCH-types are supplied in the JEDEC TO-218AC plastic package and the RCP-types in the JEDEC TO-220AB plastic package.

The RCM-types are supplied in the JEDEC TO-204AA steel package.

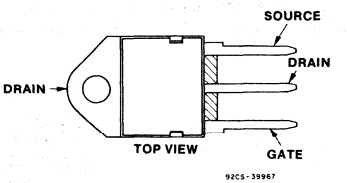
*The RCH and RCP series were formerly RCA Development Type Nos. TA9573XD and TA9573XV, respectively. The RCM series was formerly RCA Development Type No. TA9573XG.

TERMINAL DIAGRAM

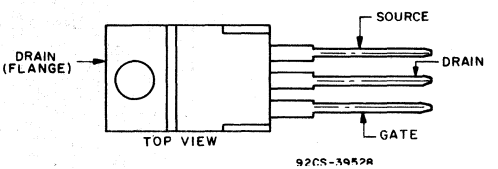


N-CHANNEL ENHANCEMENT MODE

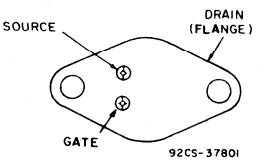
TERMINAL DESIGNATION



JEDEC TO-218AC



JEDEC TO-220AB



JEDEC TO-204AA

MAXIMUM RATINGS,
Absolute-Maximum Values ($T_C = 25°C$):

	IGTH20N40 IGTH20N40A IGTH20N50 IGTH20N50A	IGTM20N40 IGTM20N40A IGTM20N50 IGTM20N50A	IGTP20N40 IGTP20N40A	IGTP20N50 IGTP20N50A	
COLLECTOR-EMITTER VOLTAGE, V_{CES}	400	500	400	500	V
COLLECTOR-GATE VOLTAGE ($R_{ge} = 1$ MΩ), V_{CGR}	400	500	400	500	V
REVERSE COLLECTOR-EMITTER VOLTAGE, $V_{CES}(rev)$		-5			V
GATE-EMITTER VOLTAGE, V_{GE}		±20			V
COLLECTOR CURRENT, RMS Continuous, I_C		20			A
Pulsed, I_{CM}		35			A
POWER DISSIPATION @ $T_C = 25°$, P_T	100	100	75	75	W
Derate above $T_C = 25°C$	0.8	0.8	0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}		-55 to +150			°C

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

IGTH/IGTM/IGTP20N40 IGTH/IGTM/IGTP20N50
IGTH/IGTM/IGTP20N40A IGTH/IGTM/IGTP20N50A

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C = 25° C) unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RCH20N40 RCM20N40 RCP20N40	RCH20N40A RCM20N40A RCP20N40A	RCH20N50 RCM20N50 RCP20N50	RCH20N50A RCM20N50A RCP20N50A	
			Min.	Max.	Min.	Max.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA, V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE}, I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V	—	250	—	—	μA
		V_{CE} = 500 V	—	—	—	250	
		T_C = 125° C, V_{CE} = 400 V	—	—	—	—	
		T_C = 125° C, V_{CE} = 500 V	—	1000	—	—	
			—	—	—	1000	
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V, V_{CE} = 0	—	100	—	100	nA
Reverse Collector-Emitter Leakage Current	I_{CE}	R_{GE} = 0 Ω, V_{EC} = 5 V	—	-5	—	-5	mA
Collector-Emitter On Voltage	$V_{CE}(on)$	I_C = 20 A, V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 35 A, V_{GE} = 20 V	—	3.2	—	3.2	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10 A, V_{CE} = 10 V	—	6 (typ.)	—	6 (typ.)	V
On-State Gate Charge	$Q_g(on)$	I_C = 10 A, V_{CE} = 10 V	—	33 (typ.)	—	33 (typ.)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 20 A	—	50	—	50	ns
Rise Time	t_r	$V_{CE(CLP)}$ = 300 V	—	50	—	50	
Turn-Off Delay Time	$t_d(off)$	L = 25 μH	—	400	—	400	
Fall Time	t_{fi} 20N40 20N50	T_J = 100° C, V_{GE} = 10 V, R_g = 25 Ω	Typ. 680	1000	Typ. 680	1000	
	20N40A 20N50A		400	500	400	500	
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off} 20N40 20N50	I_C =10 A, $V_{CE(CLP)}$ = 300 V, L = 25 μH, T_J = 100° C, V_{GE} = 10 V, R_g = 25 Ω	1810 (typ.)				μJ
	20N40A 20N50A		1070 (typ.)				
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	IGTH/IGTM	—	1.25	—	1.25	°C/W
		IGTP	—	1.67	—	1.67	

IGTH/IGTM/IGTP20N40 IGTH/IGTM/IGTP20N50
IGTH/IGTM/IGTP20N40A IGTH/IGTM/IGTP20N50A

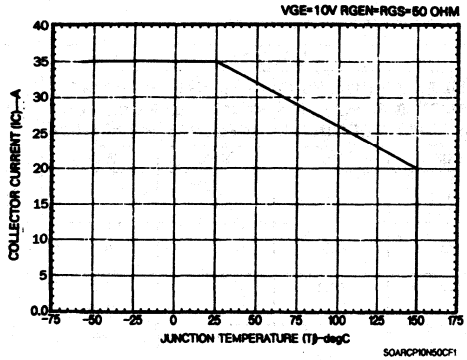


Fig. 1 - Maximum switching current level for all types. R_g = 25 Ω, V_{GE} = 0 V are the minimum allowable values.

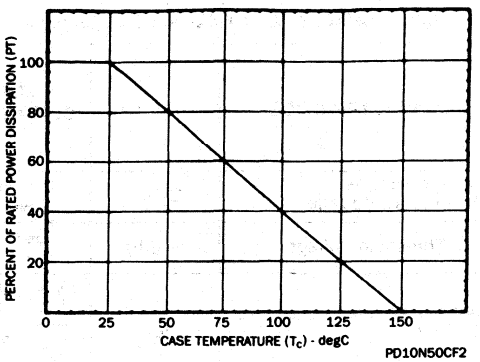


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

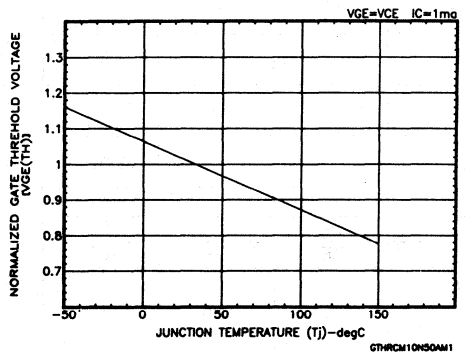


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

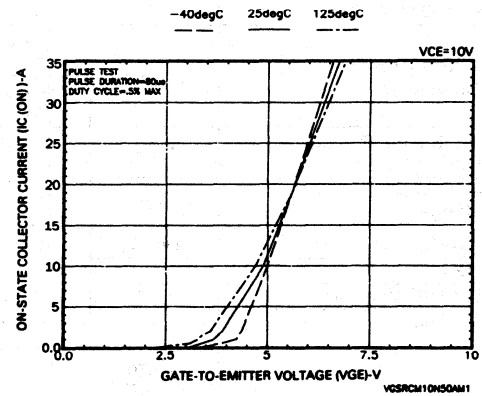


Fig. 4 - Typical transfer characteristics for all types.

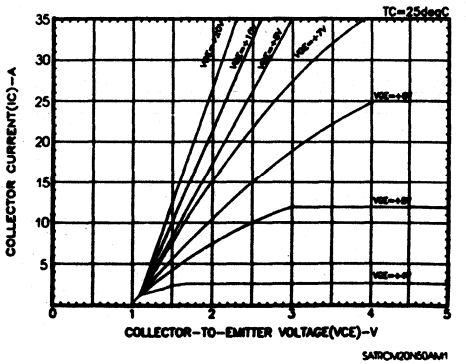


Fig. 5 - Typical saturation characteristics for all types.

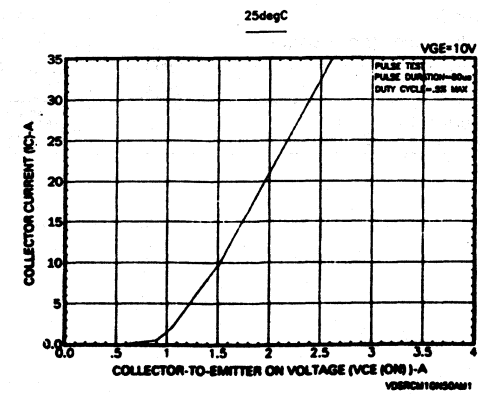


Fig. 6 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

IGTH/IGTM/IGTP20N40 IGTH/IGTM/IGTP20N50
IGTH/IGTM/IGTP20N40A IGTH/IGTM/IGTP20N50A

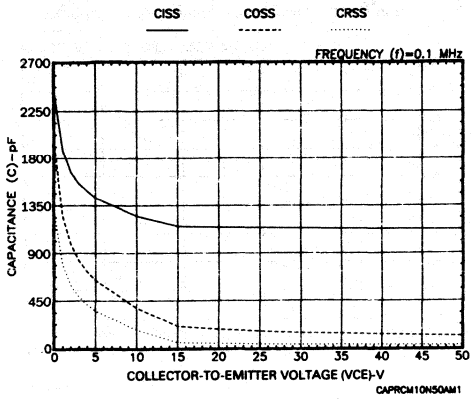


Fig. 7 - Capacitance as a function of collector-to-emitter voltage for all types.

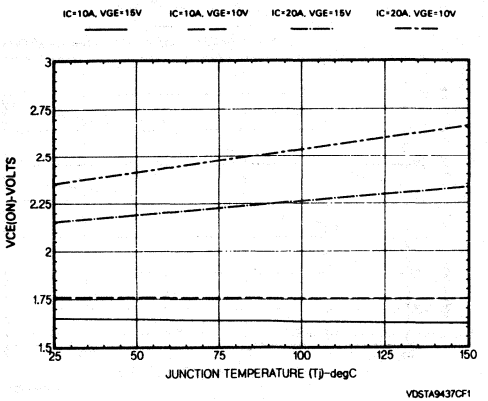


Fig. 8 - Typical V_{CE} (on) vs. temperature for all types.

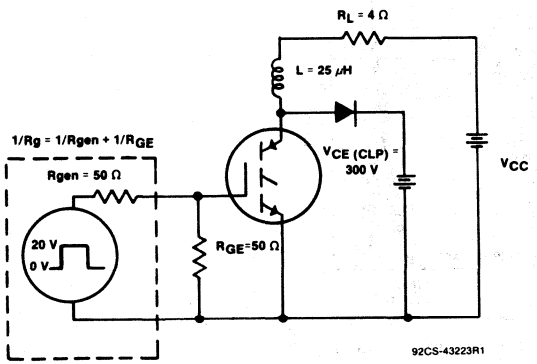


Fig. 9 - Inductive switching test circuit.

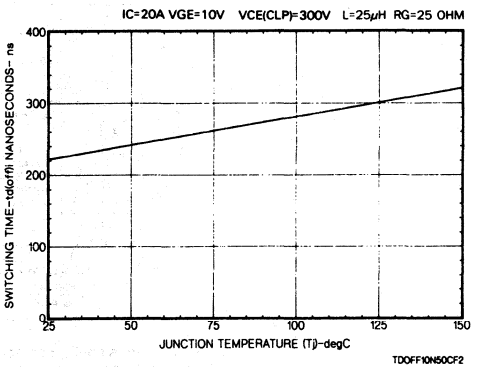


Fig. 10 - Typical turn-off delay time for all types.

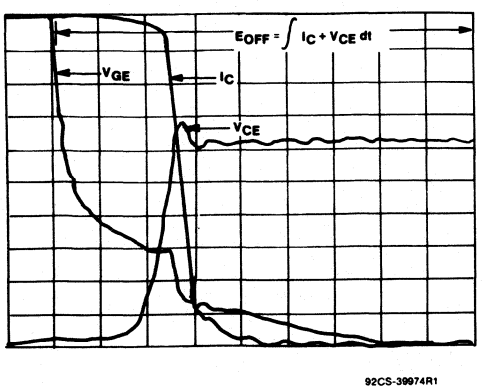


Fig. 11 - Typical inductive switching waveforms.

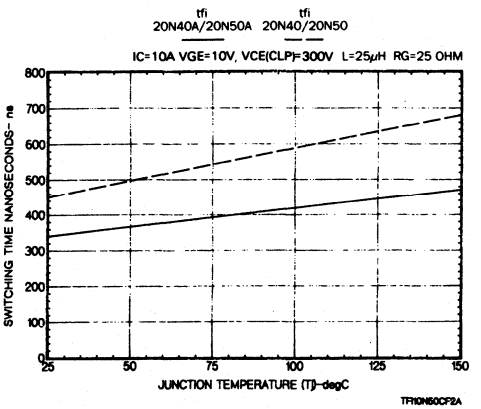


Fig. 12 - Typical fall time for all types.

IGTH/IGTM/IGTP20N40 IGTH/IGTM/IGTP20N50
IGTH/IGTM/IGTP20N40A IGTH/IGTM/IGTP20N50A

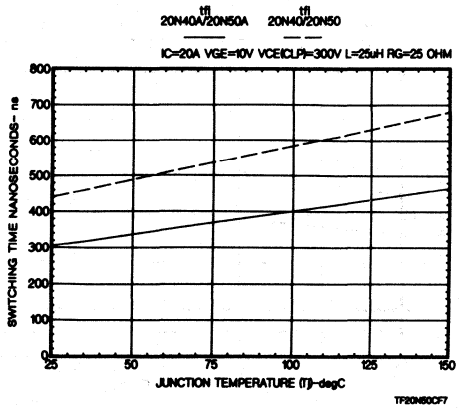


Fig. 13 - Typical fall time for all types (I_C = 20 A).

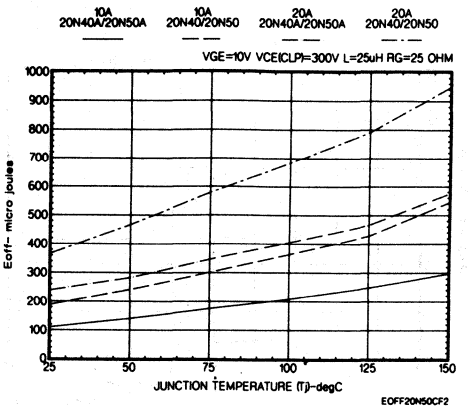
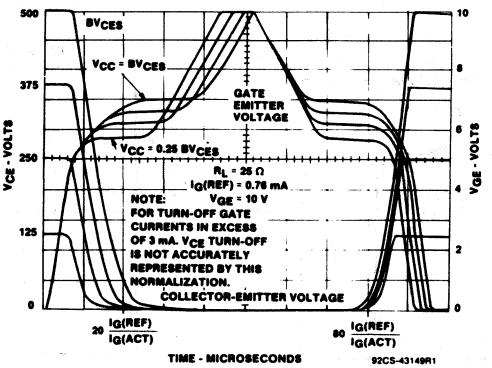


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.



Refer to RCA application notes AN-7254 and AN-7260 on the use of normalized switching waveforms.

Fig. 15 - Normalized switching waveforms at constant gate current.

File Number **2271**

IGTH20N40D, IGTH20N40AD, IGTH20N50D, IGTH20N50AD

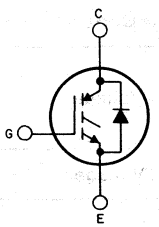
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) With Anti-Parallel Ultra-Fast Diode

20 A, 400 V and 500 V
$V_{CE}(on)$: 2.5 V Maximum
T_{fall}: 1 μs, 0.5 μs

Features:
- *Low on-state voltage*
- *Fast switching speeds*
- *High input impedance*
- *Anti-parallel diode*

Applications:
- *Power supplies*
- *Motor drives*
- *Protective circuits*

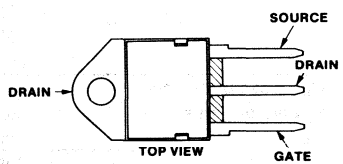
N-CHANNEL ENHANCEMENT MODE



92CS-43516

TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-218AC

The IGTH20N40D, IGTH20N40AD, IGTH20N50D, and IGTH20N50AD are n-channel enhancement-mode conductivity modulated field-effect transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits. They are supplied in the JEDEC TO-218AC plastic package and are fabricated using the TA9573 and TA9616 dies.

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

	IGTH20N40D IGTH20N40AD	IGTH20N50D IGTH20N50AD	
COLLECTOR-EMITTER VOLTAGE ..... V_{CES}	400	500	V
COLLECTOR-GATE VOLTAGE (R_{ge} = 1 MΩ) ..... V_{CGR}	400	500	V
GATE-EMITTER VOLTAGE ..... V_{GE}	±20		V
COLLECTOR CURRENT, RMS Continuous ..... I_C	20		A
Pulsed ..... I_{CM}	35		A
POWER DISSIPATION at T_C = 25° C ..... P_T	100		W
Derate above T_C = 25° C	0.8		W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_S	−55 to +150		°C

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

IGTH20N40D, IGTH20N40AD, IGTH20N50D, IGTH20N50AD

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			IGTH20N40D IGTH20N40AD		IGTH20N50D IGTH20N50AD		
			MIN.	MAX.	MIN.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V	—	250	—	—	μA
		V_{CE} = 500 V	—	—	—	250	μA
		T_C = 125° C V_{CE} = 400 V	—	—	—	—	μA
		V_{CE} = 400 V	—	1000	—	—	μA
		V_{CE} = 500 V	—	—	—	1000	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On-Voltage	$V_{CE}(on)$	I_C = 20 A V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 35 A V_{GE} = 20 V	—	3.2	—	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10 A V_{CE} = 10 V	—	6 (typ)	—	6 (typ)	V
On-State Gate Charge	$Q_G(on)$	I_C = 10 A V_{CE} = 10 V	—	33(typ)	—	33(typ)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 20 A $V_{CE}(clp)$ = 300 V L = 25 μH T_J = 100° C V_{GE} = 10 V R_g = 25 Ω	—	50	—	50	ns
Rise Time	t_r		—	50	—	50	ns
Turn-Off Delay Time	$t_d(off)$		—	400	—	400	ns
Fall Time	t_{fi}						ns
	20N40D 20N50D		TYP 680	1000	TYP 680	1000	ns
	20N40AD 20N50AD		TYP 400	500	TYP 400	500	ns
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off}	I_C = 20 A $V_{CE}(clp)$ = 300 V L = 25 μH T_J = 100° C V_{GE} = 10 V R_g = 25 Ω					μJ
	20N40D 20N50D		1810 (typ)				μJ
	20N40AD 20N50AD		1070 (typ)				μJ
Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.25	—	1.25	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 20 A	—	2	—	2	V
Diode Reverse Recovery Time	T_{rr}	I_{EC} = 20 A di/dt = 100 A/μs	—	100	—	100	ns

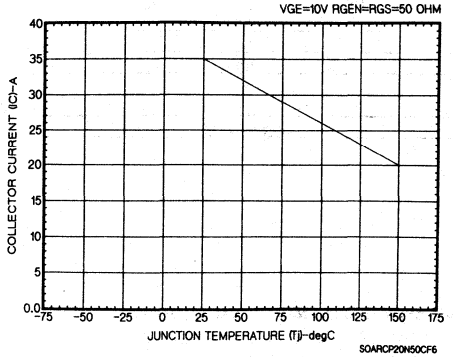


Fig. 1 - Maximum switching current level for all types. Minimum allowable values are R_g = 50 Ω, V_{GE} = 0 V.

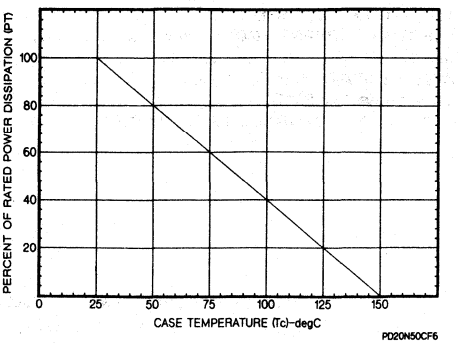


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

IGTH20N40D, IGTH20N40AD, IGTH20N50D, IGTH20N50AD

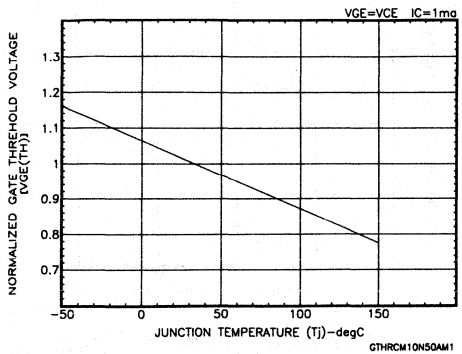


Fig. 3 - Typical normalized gate-threshold voltage as a function of junction temperature for all types.

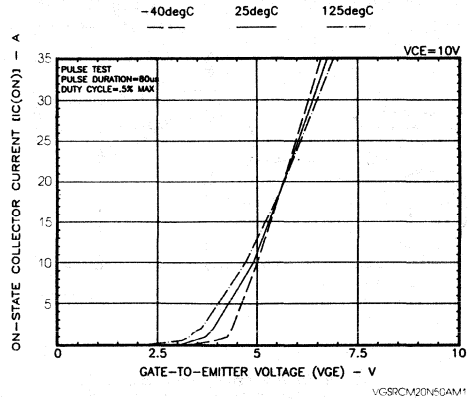


Fig. 4 - Typical transfer characteristics for all types.

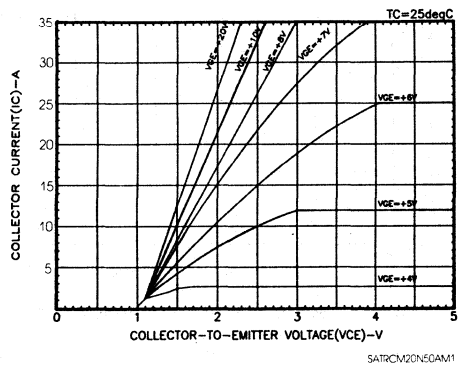


Fig. 5 - Typical saturation characteristics for all types.

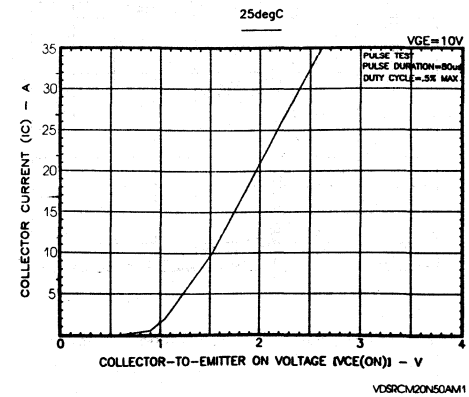


Fig. 6 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

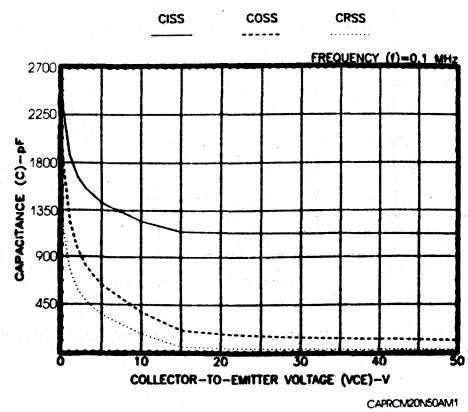


Fig. 7 - Capacitance as a function of collector-to-emitter voltage for all types.

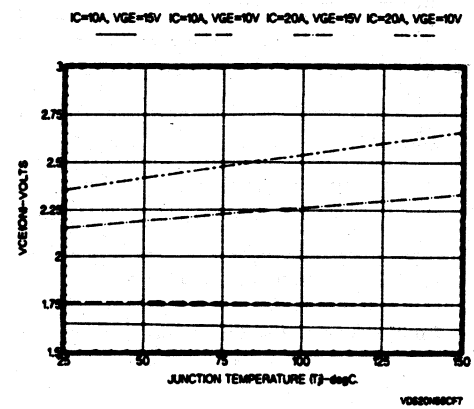


Fig. 8 - Typical $V_{CE}(on)$ vs. temperature for all types.

IGTH20N40D, IGTH20N40AD, IGTH20N50D, IGTH20N50AD

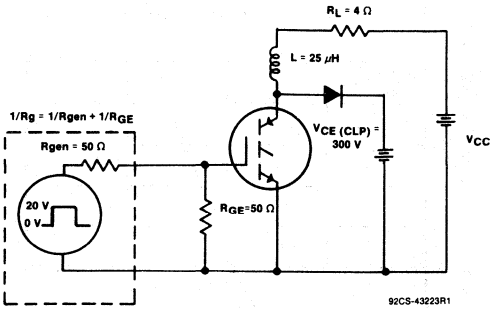


Fig. 9 - Inductive switching test circuit.

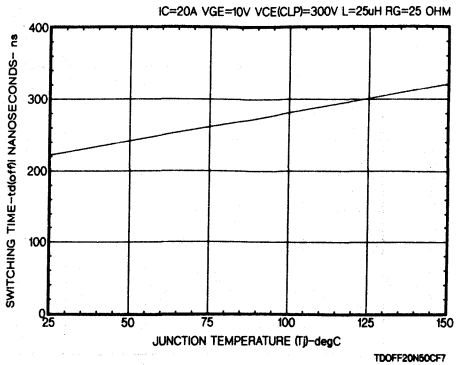


Fig. 10 - Typical turn-off delay time for all types.

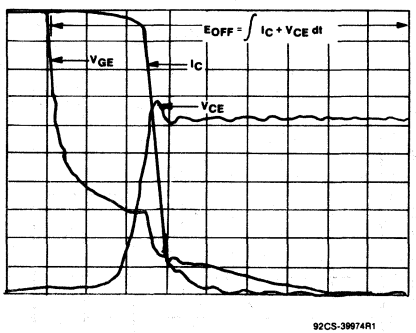


Fig. 11 - Typical inductive switching waveforms.

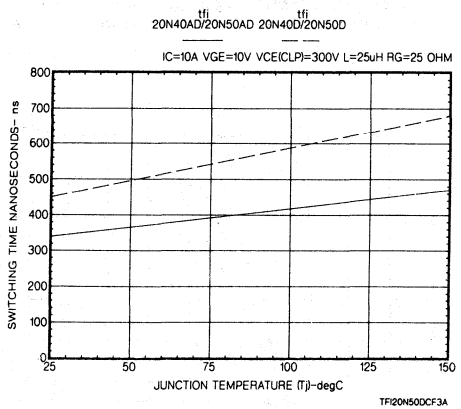


Fig. 12 - Typical fall time for all types (I_C = 10 A).

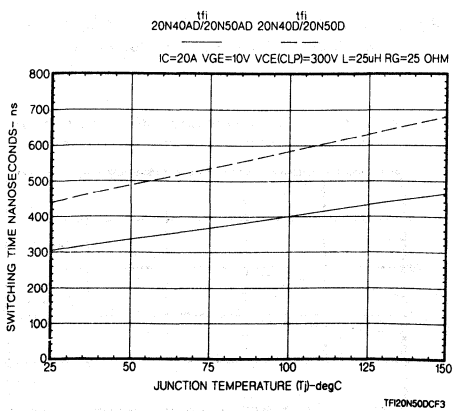


Fig. 13 - Typical fall time for all types (I_C = 20 A).

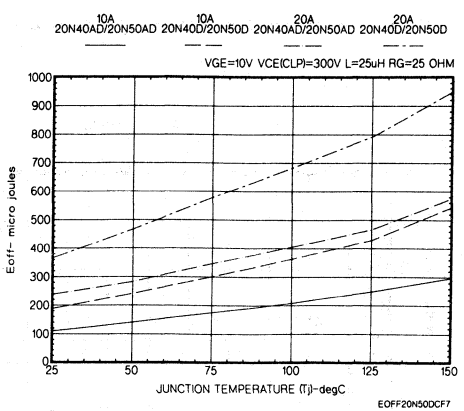


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.

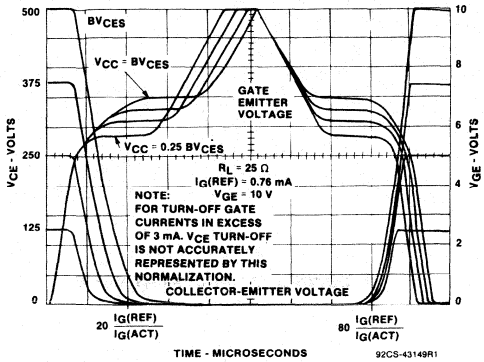


Fig. 15 - Normalized switching waveforms at constant gate current. (Refer to RCA application notes AN7254 and AN7260.)

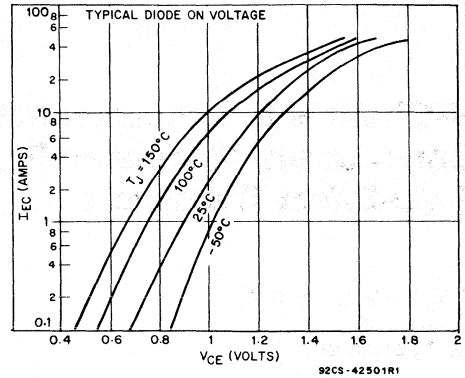


Fig. 16 - Typical diode collector-to-emitter voltage vs. current for all types.

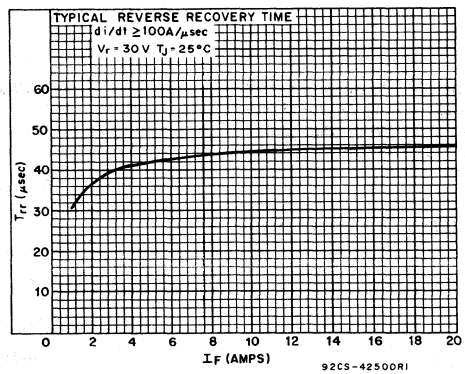


Fig. 17 - Typical diode reverse-recovery time for all types.

2N6975, 2N6976, 2N6977, 2N6978

File Number **2297**

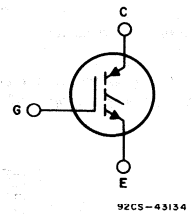
N-Channel Enhancement-Mode Conductivity-Modulated Power Field-Effect Transistors

5 A, 400 V and 500 V
$V_{CE(on)}$: 2 V
T_{fi}: 1 μs, 0.5 μs

Features:
- *Low on-state voltage*
- *Fast switching speeds*
- *High input impedance*

Applications:
- *Power supplies*
- *Motor drives*
- *Protection circuits*

N-CHANNEL ENHANCEMENT MODE

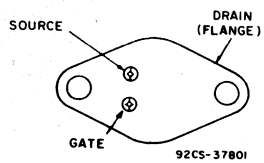


TERMINAL DIAGRAM

The 2N6975, 2N6976, 2N6977 and the 2N6978 are n-channel enhancement-mode conductivity-modulated power field-effect transistors designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

	2N6975 2N6977		2N6976 2N6978	
COLLECTOR-EMITTER VOLTAGE, V_{CES}	400*		500*	V
COLLECTOR-GATE VOLTAGE (R_{GE} = 1 MΩ), V_{CGR}	400*		500*	V
REVERSE COLLECTOR-EMITTER VOLTAGE, $V_{CES(rev.)}$		5*		V
GATE-EMITTER VOLTAGE, V_{GE}		±20*		V
COLLECTOR CURRENT, RMS Continuous, I_C		5*		A
Pulsed, I_{CM}		10*		A
POWER DISSIPATION @ T_C = 25°C, P_T		100*		W
Derate above T_C = 25°C		0.8*		W/°C
OPERATING AND STORAGE TEMPERATURE, T_J, T_{stg}		-55 to +150*		°C

*JEDEC registered value.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			2N6975 2N6977		2N6976 2N6978		
			Min.	Max.	Min.	Max.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400*	—	500*	—	V
Gate Threshold Voltage	$V_{GE(th)}$	$V_{GE} = V_{CE}$ I_C = 1 mA	2*	4.5*	2*	4.5*	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V V_{CE} = 500 V	— —	250* —	— —	— 250*	μA
		T_C = 125° C V_{CE} = 400 V V_{CE} = 500 V	— — —	— 1000* —	— — —	— — 1000*	
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100*	—	100*	nA
Reverse Collector-Emitter Leakage Current	I_{ECS}	R_{GE} = 0 Ω V_{EC} = 5 V	—	5*	—	5*	mA
Collector-Emitter On Voltage	$V_{CE(on)}$	I_C = 5 A V_{GE} = 10 V	—	2*	—	2*	V
		I_C = 10 A V_{GE} = 20V	—	2.5	—	2.5	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5 A V_{CE} = 10 V	3.4*	6.8*	3.4*	6.8*	V
On-State Gate Charge	$Q_{g(on)}$	I_C = 5 A V_{CE} = 10 V	12*	25*	12*	25*	nC
Turn-On Delay Time	$t_{d(on)}$	I_C = 5 A $V_{CE(CLP)}$ = 300 V L = 50 μH T_J = 125° C V_{GE} = 10 V R_G = 50 Ω	50 max				ns
Rise Time	t_r		50 max				
Turn-Off Delay Time	$t_{d(off)}$		400 max *				
Fall Time	t_{fi}		2N6975 2N6976	1000 max*			
			2N6977 2N6978	500 max *			
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off}	I_C = 5 A $V_{CE(CLP)}$ = 300 V L = 50 μH T_J = 125° C V_{GE} = 10 V R_G = 50 Ω	2N6975 2N6977	1000 max*			μJ
			2N6976 2N6978	500 max*			
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		1.25*				°C/W

*JEDEC registered value.

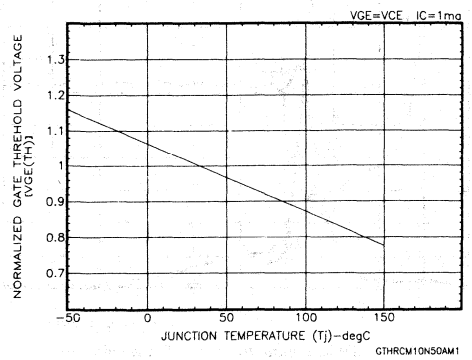


Fig. 1 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

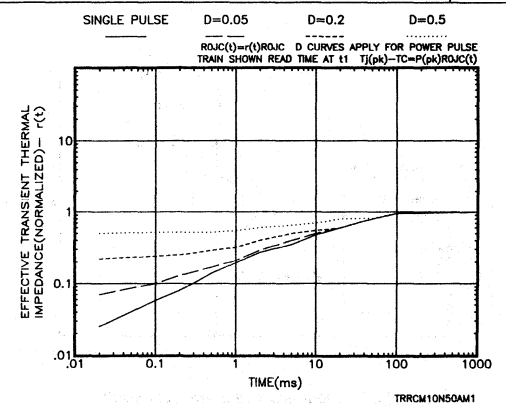


Fig. 2 - Normalized thermal response characteristics for all types.

2N6975, 2N6976, 2N6977, 2N6978

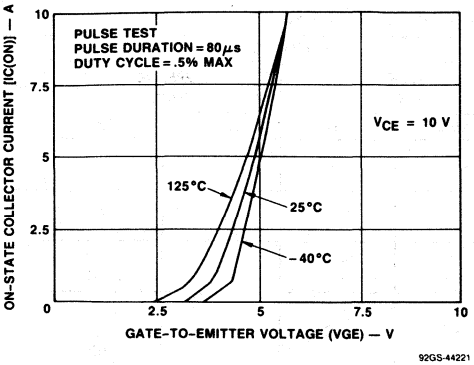


Fig. 3 - Typical transfer characteristics for all types.

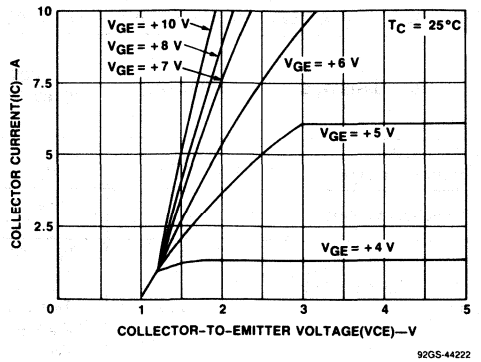


Fig. 4 - Typical saturation characteristics for all types.

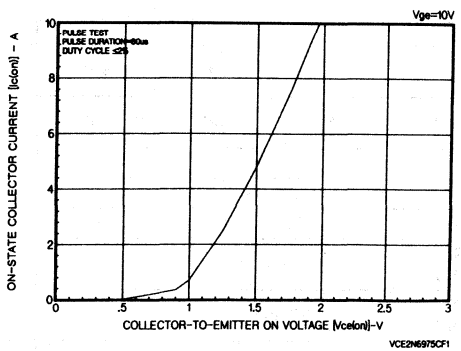


Fig. 5 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

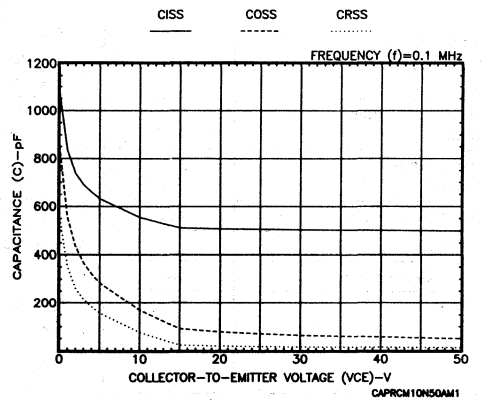


Fig. 6 - Capacitance as a function of collector-to-emitter voltage for all types.

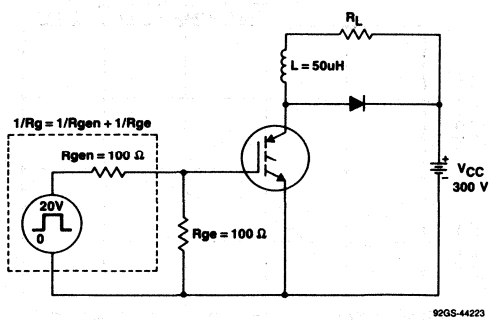


Fig. 7 - Inductive switching test circuit.

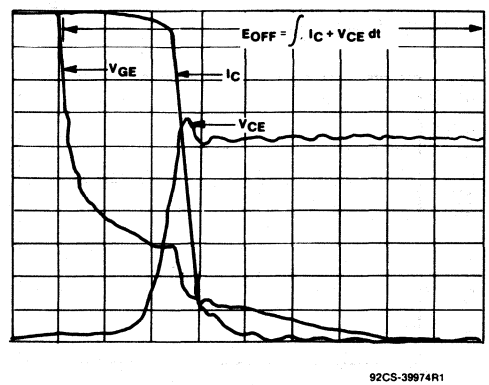


Fig. 8 - Typical inductive switching waveforms.

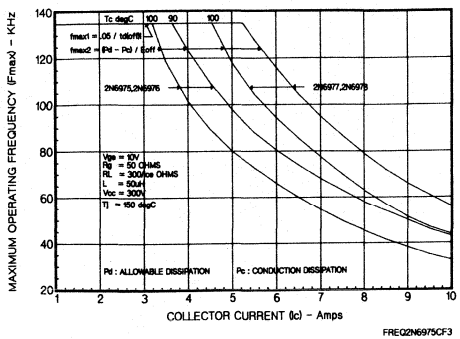


Fig. 9 - Maximum operating frequency vs collector current (typical).

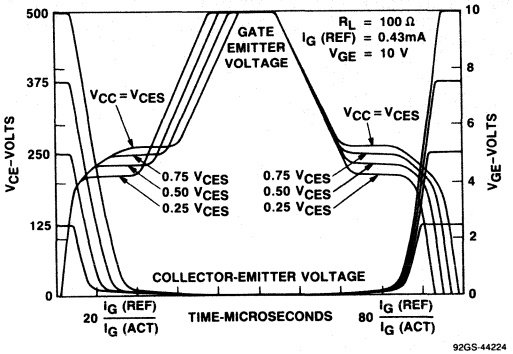


Fig. 10 - Normalized switching waveforms at constant gate current. (Refer to RCA application notes AN-7254 and AN7260.)

Advanced Discrete

RLP1N08L

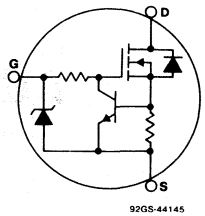
File Number **2252**

Current Limited - ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

1 A, 80 V
$r_{DS}(on)$: 0.75 Ω
I_{limit} = 1.5 A Maximum at 150° C

Features:
- *Built-in current limiting*
- *ESD protected*
- *Controlled switching limits EMI and RFI*
- *Specified for 150° C operation*

N-CHANNEL ENHANCEMENT MODE



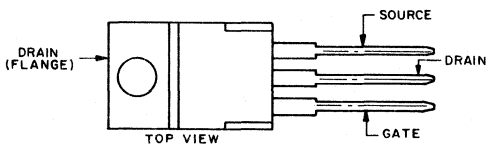
92GS-44145

TERMINAL DIAGRAM

The RLP1N08L is a semi-smart monolithic power circuit which incorporates a lateral bipolar transistor, two resistors, a zener diode, and a PowerMOS transistor. Good control of the current-limiting levels allows use of these devices where a shorted load condition may be encountered. "Logic level" gates allow this device to be fully biased on with only 5 volts from gate to source. The zener diode provides ESD protection up to 2 kV. These devices can be produced on the standard PowerMOS production line.

The RLP-series types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

DRAIN-SOURCE VOLTAGE	V_{DSS}	80	V
DRAIN-GATE VOLTAGE	V_{DGR}	80	V
• GATE-SOURCE VOLTAGE	V_{GS}	5.5	V
- Reverse voltage gate bias not allowed			
ELECTROSTATIC VOLTAGE at 100 pF, 1500 Ω	ESD	2	kV
DRAIN CURRENT, RMS Continuous	I_D	Self Limited	
POWER DISSIPATION at T_C = 25° C	P_T	75	W
Derate above 25° C		0.24	W/° C
OPERATING AND STORAGE TEMPERATURE	T_S, T_J	-55 to +150	°C

•May be exceeded if current is limited to 10 mA.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V	80	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V, V_{GS} = 0 V	—	1	μA
		T_C = 150° C	—	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 5 V, T_C = 150° C	—	50	μA
On Resistance	$r_{DS}(on)$	I_D = 1 A, V_{GS} = 5 V	—	0.75	Ω
		T_C = 150° C	—	1.5	Ω
Limiting Current	$I_{DS}(Lim)$	V_{DS} = 15 V, V_{GS} = 5 V	1.8	3	A
		T_C = 150° C	1.1	1.5	A
Turn-On Time	t(on)	V_{DD} = 30 V, I_D = 1 A	—	6.5	μs
Turn-On Delay Time	$t_d(on)$	V_{GS} = 5 V, R_{GS} = 25 Ω	—	1.5	μs
Rise Time	t_r	R1 = 30 Ω	1	5	μs
Turn-Off Delay Time	$t_d(off)$		—	7.5	μs
Fall Time	t_f		1	5	μs
Turn-Off Time	t(off)		—	12.5	μs
Plateau Voltage	V(plateau)	I_D = 1 A, V_{DS} = 15 V	—	5	V
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$		—	4.17	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$		—	80	°C/W
Electrostatic Voltage	ESD	Human Model (100 pF, 1.5 kΩ)	2000	—	V

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 1 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 1 A	—	1	ms

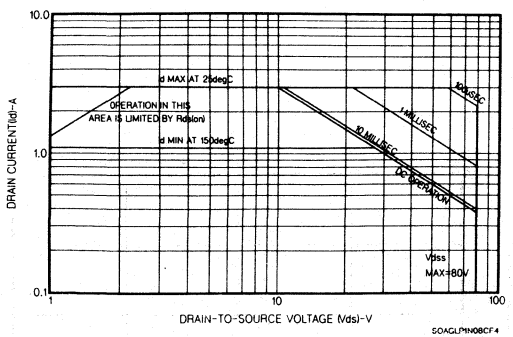


Fig. 1 - Safe-operating-area curve.

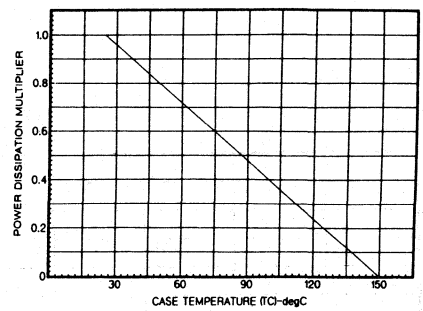


Fig. 2 - Normalized power dissipation vs. temperature derating curve.

RLP1N08L

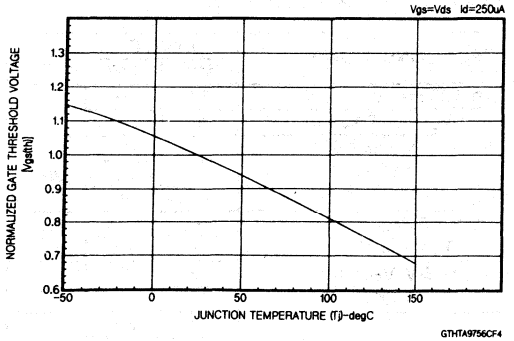


Fig. 3 - Typical normalized gate-threshold voltage.

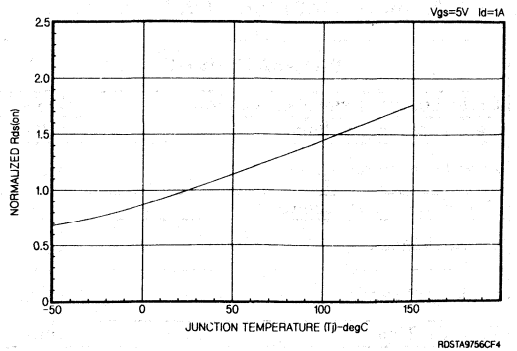


Fig. 4 - Normalized $r_{DS}(on)$ vs. junction temperature.

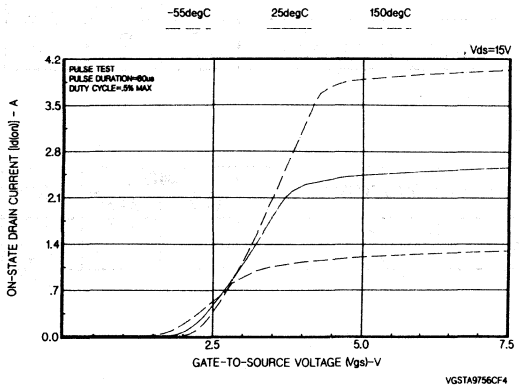


Fig. 5 - Typical transfer characteristics.

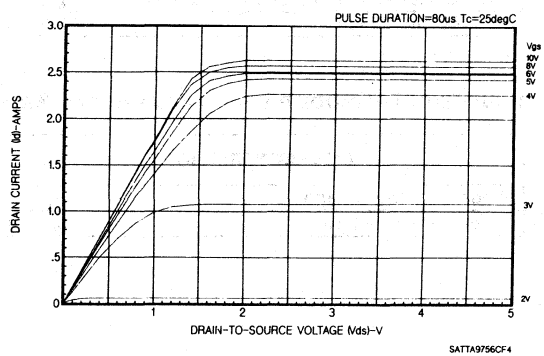


Fig. 6 - Typical saturation characteristics.

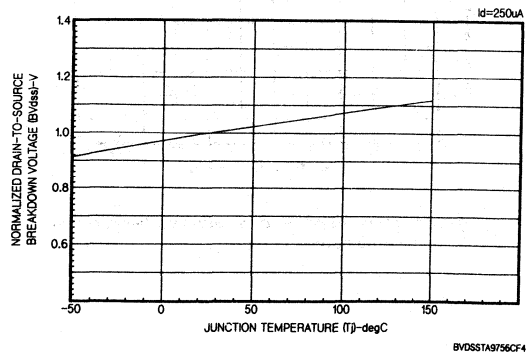


Fig. 7 - Drain-source breakdown voltage vs. temperature.

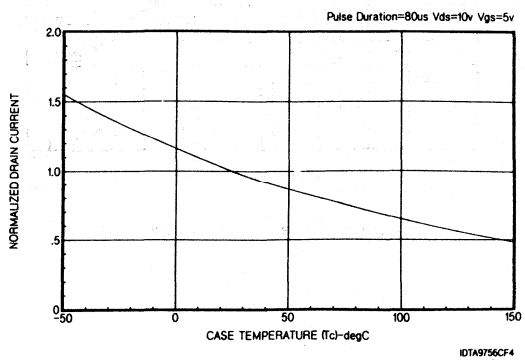


Fig. 8 - Normalized current limit vs. temperature.

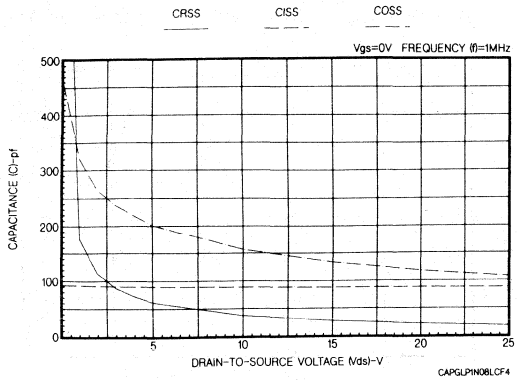


Fig. 9 - Typical capacitance vs. voltage.

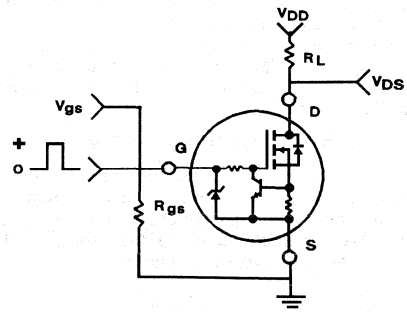


Fig. 10 - Switching test circuit.

Temperature Dependence of Current Limiting and Switching Speed

The RLP1N08L is a monolithic power device which incorporates a Logic Level PowerMOS transistor with a resistor in series with the source. The base and emitter of a lateral bipolar transistor is connected across this resistor, and the collector of the bipolar transistor is connected to the gate of the PowerMOS transistor. When the voltage across the resistor reaches the value required to forward bias the emitter base junction of the bipolar transistor, the bipolar transistor "turns on". A series resistor is incorporated in series with the gate of the PowerMOS transistor allowing the bipolar transistor to drive the gate of the PowerMOS transistor to a voltage which just maintains a constant current in the PowerMOS transistor. Since both the resistance of the resistor in series with the PowerMOS transistor source and the voltage required to forward bias the base emitter junction of the bipolar transistor vary with the temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 8.

The resistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP1N08L

The limit on drain-to-source voltage for operation in current limiting on a steady state (dc) basis is shown as Figure A. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOS devices today, is limited to 150°C. The maximum voltage allowable can, therefore, be expressed as:

$$V_s = \frac{(150 - T_{ambient})}{I_{lim}\,(R_{\theta JC} + R_{\theta})}$$

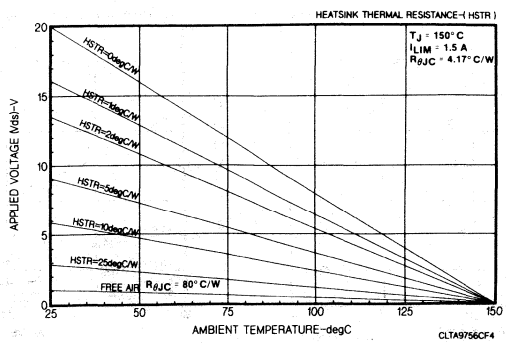


Fig. A - DC operation in current limiting.

RLP1N08L

Duty Cycle Operation of the RLP1N08L

In many applications either the drain-to-source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N08L is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_c = (V_{SD} * I_D * D * R_{\theta CA}) + \text{Tambient}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 150°C and using the T_C calculated above, the expression for maximum V_{SD} under duty cycle operation is:

$$V_{SD} = \frac{150 - T_c}{I_{lim} * D * R_{\theta JC}}$$

These values are plotted as Figures B1 - B5 for various heat sink thermal resistances.

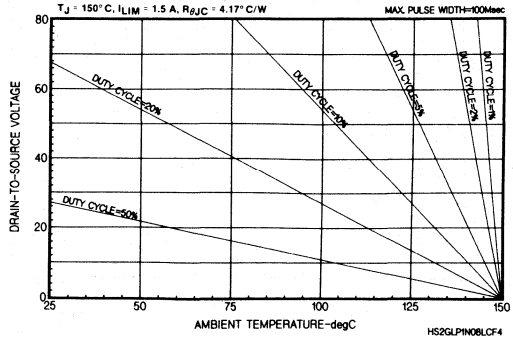


Fig. B1 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 2° C/W)

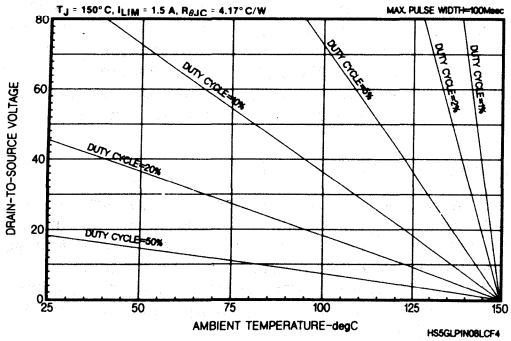


Fig. B2 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 5° C/W)

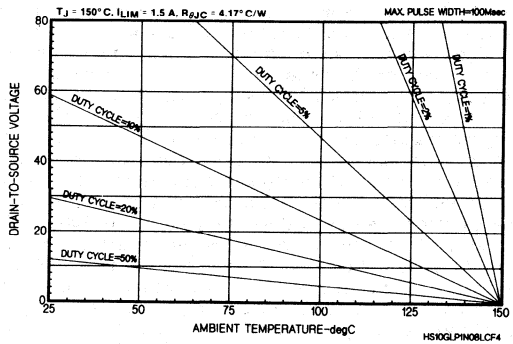


Fig. B3 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 10° C/W)

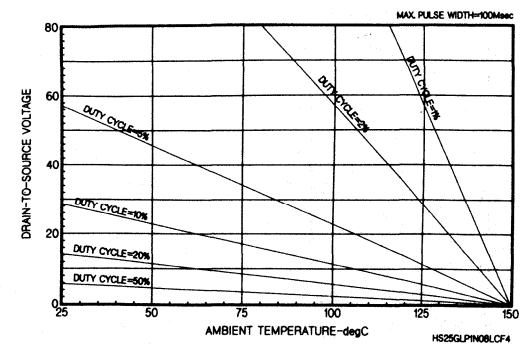


Fig. B4 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 25° C/W)

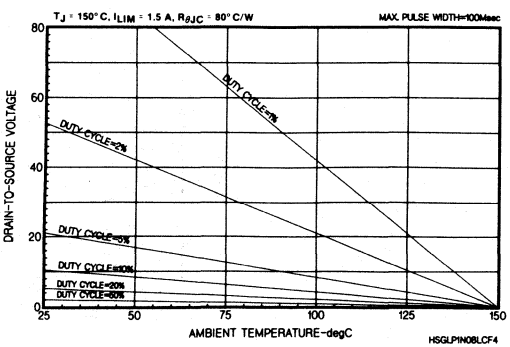


Fig. B5 - Maximum V_{DS} vs. ambient temperature in current limiting. (No external heatsink)

Limited Time Operations of the RLP1N08L

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1 - C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 150°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

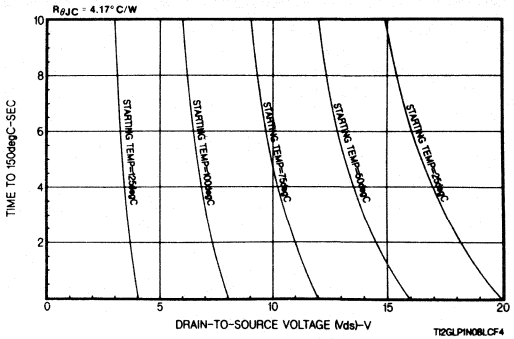


Fig. C1 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 2° C/W
Heatsink thermal capacitance = 4 j/° C)

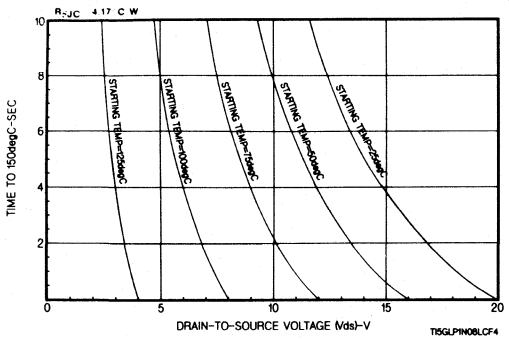


Fig. C2 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 5° C/W
Heatsink thermal capacitance = 2 j/° C)

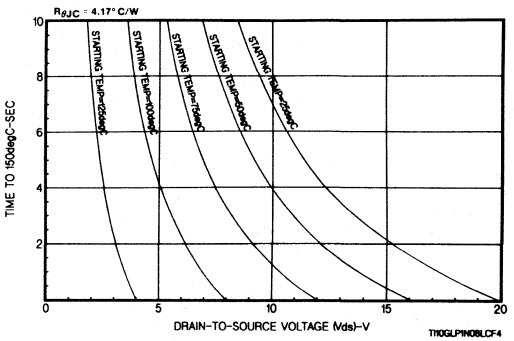


Fig. C3 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 10° C/W
Heatsink thermal capacitance = 1 j/° C)

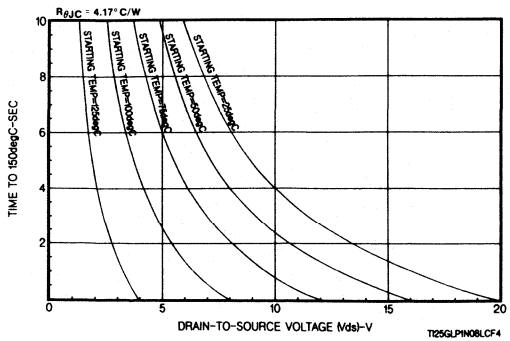


Fig. C4 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 25° C/W
Heatsink thermal capacitance = 5 j/° C)

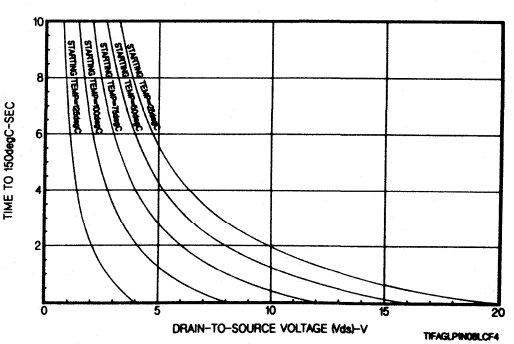


Fig. C5 - Time to 150° C in current limiting.
(No external heatsink)

High Reliability Power MOSFETs

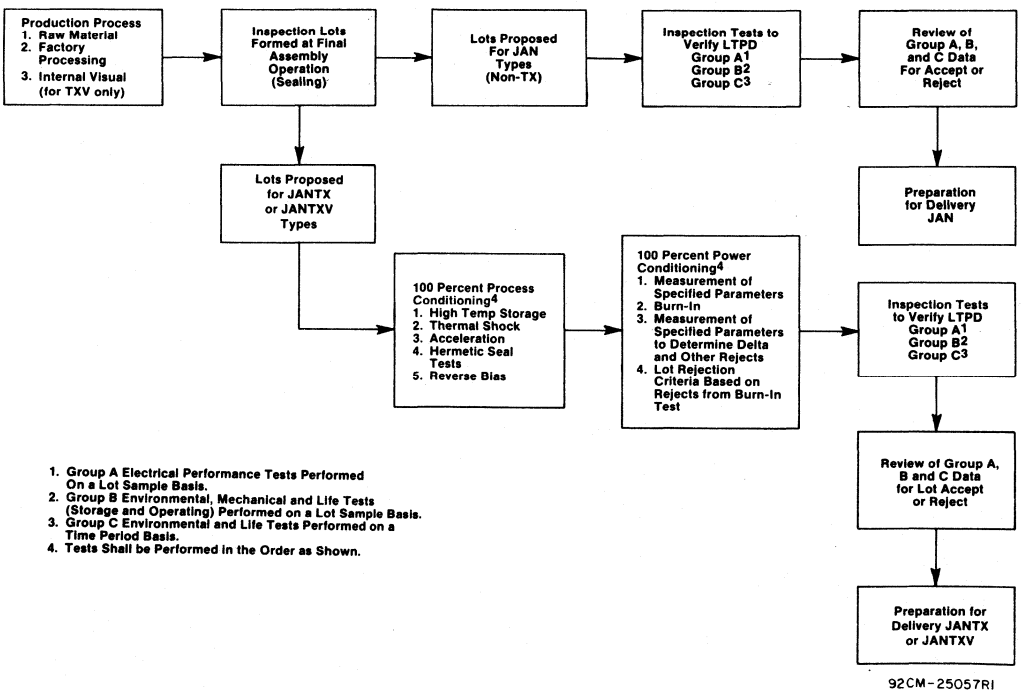
JAN, JANTX and JANTXV Types **9-3**
Harris Added Value Screening **9-4**

High-Reliability Power Products

Solid-state devices classified as high-reliability types have come to be primarily associated with military and aerospace applications. In many ways, this association is misleading because the commerical equipment market is probably the largest user of high-reliability products, but not necessarily by that label. Military and aerospace agencies, however, have been largely responsible for establishment of comprehensive published reliability specifications and standards which have been accepted by the solid-state industry. MIL standards dominate the procedures used to specify high-reliability solid-state devices and represent a common reference point frequently used by commerical users to define their requirements.

Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured: rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed those required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment. These standards also cover a wide range of requirements for the manufacturer on such things as:

(a) The procedure and requirements for a manufacturer to become certified to manufacture MIL-spec parts.
(b) The requirements for qualifying parts.
(c) Product-assurance provisions in such areas as quality control, inspection procedures, personnel training, cleanliness, failure analysis, and documentation.
(d) Test methods and procedures.
(e) Marking and identification of product.
(f) Preservation and packing.



Order of procedure diagram for JAN, JANTX, and JANTXV solid-state devices.

JAN, JANTX, and JANTXV Solid-State Power Devices

The major military specification used for the procurement of standard solid-state devices by the military is MIL-S-19500, which covers the devices such as discrete transistors, thyristors, and diodes.

MIL-S-19500 is the specification for the familiar "JAN" type solid state devices. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center (DESC).

Levels of reliability are defined by MIL-S-19500. JAN types receive Group A, Group B, and Group C lot sampling only, and are the least expensive. JANTX types receive 100 percent process conditioning, and power conditioning, and are subjected to lot rejection based on delta parameter criteria in addition to Group A, Group B, and Group C lot sampling. JANTXV types are subjected to 100 percent (JTXV) internal visual inspection in addition to all of the JANTX tests in accordance with MIL-STD-750 test methods and MIL-S-19500.

DESC publishes "QPL-19500", a Qualified Products List of all types and suppliers approved to produce and brand devices in accordance with MIL-S-19500.

The following tables list approved "QPL" types and types that are process of testing preliminary to QPL approval by DESC, respectively.

Custom high-reliability selections of Harris Power MOSFETs can also be supplied with similar process and power conditioning tests and delta criteria.

QPL Approved Types

Harris is presently qualified on the following devices. Prices and delivery quotations may be obtained from your local sales representative.

JAN and JANTX Power MOSFETs

N-Channel Types	MIL-S-19500/	Package	Channel	P_T (W)	I_D (A)	BV_{DSS} (V)	r_{DS} (on) Ω
2N6756	542	TO-204AA	N	75	14	100	0.18
2N6758	542	TO-204AA	N	75	9	200	0.4
2N6760	542	TO-204AA	N	75	5.5	400	1
2N6762	542	TO-204AA	N	75	4.5	500	1.5
2N6764	543	TO-204AE	N	150	38	100	0.055
2N6766	543	TO-204AE	N	150	30	200	0.085
2N6768	543	TO-204AA	N	150	14	400	0.3
2N6770	543	TO-204AA	N	150	12	500	0.4
2N6782	556	TO-205AF	N	15	3.5	100	0.6
2N6784	556	TO-205AF	N	15	2.25	200	1.5
2N6788	555	TO-205AF	N	20	6	100	0.3
2N6790	555	TO-205AF	N	20	3.5	200	0.8
2N6792	555	TO-205AF	N	20	2	400	1.8
2N6794	555	TO-205AF	N	20	1.5	500	3
2N6796	557	TO-205AF	N	25	8	100	0.18
2N6798	557	TO-205AF	N	25	5.5	100	0.4
2N6800	557	TO-205AF	N	25	3	400	1
2N6802	557	TO-205AF	N	25	2.5	500	1.5
P-Channel Types	**MIL-S-19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**r_{DS} (on) Ω**
2N6895	565	TO-205AF	P	8.33	-1.5	-100	3.65
2N6896	565	TO-204AA	P	60	-6	-100	0.6
2N6897	565	TO-204AA	P	100	-12	-100	0.3
2N6898	565	TO-204AA	P	150	-25	-100	0.2
2N6849	564	TO-205AF	P	25	-6.5	-100	0.3
2N6851	564	TO-205AF	P	25	-4.0	-200	0.8
N-Channel Logic-Level Types	**MIL-S-19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**r_{DS} (on) Ω**
2N6901	566	TO-205AF	N	8.33	1.5	100	1.4
2N6902	566	TO-204AA	N	75	12	100	0.2
2N6903	566	TO-205AF	N	8.33	1.5	200	3.65
2N6904	566	TO-204AA	N	75	8	200	0.65

Added Value Screening

Harris Added Value Screening for Power MOSFETs and Chips

Many solid-state devices not yet covered by military specifications, because they are too new, offer the most recent technological advances or have special performance characteristics which offer advantages to the designer of high-reliability equipment. Harris cooperates with the users of such devices in establishment of high-reliability specifications patterned after MIL standards, which allow these designs to be approved for use in military and aerospace systems, as well as commercial equipment.

Most procurements of solid-state devices for military systems are made by the equipment contractor from the MIL-STD parts list as awards are received for electronic equipment. Some military and aerospace programs, because of their size, duration, or special requirements (Minuteman and Peacekepper are two examples), require that special specifications and process methods, or even special production lines, be established and tailored to the particular functional, reliability, and economic needs of the program. Harris has frequently used the resources of its laboratories, production facilities, and expert technical staff to contribute to the success of such programs.

All Harris high-reliability power MOSFETs are processed in accordance with provisions of MIL-S-19500. The desired screening test sequence can be chosen from the models shown in the screening table.

Class S devices provide wafer lot control traceability from wafer diffusion through screening.

Class S chips also provide wafer lot control traceability from wafer diffusion through screening. A sample of 22 devices taken from this lot is assembled in a suitable package. The assembled sample devices are subjected to the Class S screening sequence in the table below. Class S chips are released for shipment when the assembled sample devices successfully pass the screen.

Group B and Group C tests will be performed when requested in accordance with MIL-S-19500.

ADDED VALUE HIGH-RELIABILITY SCREENING

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
1. Internal Visual	2072	For transistors.	100%	100%	—
2. High Temp Life (LTPD) (stabilization bake)	1032	24 hrs min at max rated storage temp.	100%	100%	100%
3. Thermal shock (temp cycling)	1051	No dwell is required at 25° C. Test condition C, 20 cycles, t (extremes) > 10 min.	100%	100%	100%
4. Constant acceleration 1/	2006	Y_1 direction at 20,000 G min except at 10,000 G min for devices with power rating of > 10 watts at T_C = 25° C. The 1 min hold time requirement shall not apply.	100%	100%	100%

Added Value Screening

ADDED VALUE HIGH-RELIABILITY SCREENING (Continued)

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
5. Hermetic Seal Fine 1/	1071	Test condition G or H, max leak rate = $5x10^{-8}$ atm cc/s except $5x10^{-7}$ atm cc/s for devices with internal cavity > 0.3 cc.	Optional if done in screen 14.	100% 4/	100% 4/
Gross		Test condition A, C, D, E, or F.	Optional	100% 4/	100% 4/
6. Serialization		See 3.7.9.	100%		
7. Interim Electrical Parameters		As specified.	100% (Read and record)		
8. High Temp Reverse Bias (HTRB)		48 hrs min at T_A = 150° C (min) and minimum applied voltage as follows:			
Burn-in (for transistors)	1039	Transistors - 80% (min) of rated V_{CB} (bipolar), $V_{GS(FET)}$, or $V_{DS(FET)}$ as applicable. Test condition A.	100%	100%	100%
9. Interim electrical and delta parameters		As specified but including all delta parameters as a minimum. Leakage current shall be measured on each device before any other test is made.	100% (Measure all specified parameters within 16 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)

Added Value Screening

ADDED VALUE HIGH-RELIABILITY SCREENING (Continued)

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
10. Power Burn-In		As specified.	100%	100%	100%
Burn-In (Transistors)		Transistors. Test condition B.	240 hrs (min)	160 hrs (min)	160 hrs (min)
Burn-In (Thyristors) 3/	1040	Thyristors.	240 hrs (min)	96 hrs (min)	96 hrs (min)
11. Final Electrical Test		As specified.	100%	100%	100%
Interim Electrical		All interim and delta parameter measurements must be completed within 96 hrs after removal from burn-in conditions.	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)
Other Electrical Parameters			Group A, sub-groups 2 and 3.	Group A, sub-groups 2 and 3.	Group A, sub-roups 2 and 3.
12. Hermetic Seal	1071	(Same as 5 on previous page) 2/	100%	Optional 4/	Optional 4/
Fine 1/					
Gross					
13. Radiography	2076	2/	100%	—	—
14. External Visual Examination	2071	To be performed after complete marking.	100%	—	—

*1/ Omit fine leak seal test and constant acceleration test for double plug, non-internal cavity diode construction.
*2/ The radiographic and seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 5 it does not have to be performed again in screen 12 for double plug, non-internal cavity diode construction.
*3/ Reverse-blocking test shall replace power burn-in for power rectifiers at $\geq$ 10 amp rating at $T_C \geq 100°$ C and all thyristors.
4/ Fine and gross seal leak test for JANTX and JANTXV shall be performed in either block 5 or block 12.

Radiation-Hardened MOSFETs

FRF6764M, FRF6764D, FRF6764R, FRF6764H

File Number **2323**

Radiation-Hardened N-Channel Power MOSFETs

Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

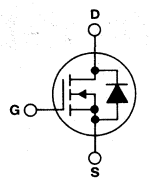
30 A, 100 V

$r_{DS(on)}$ = 0.055 Ω

Features:

- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *Isolated case*
- *FRF6764M rated to 3k rads*
- *FRF6764D rated to 10K rads*
- *FRF6764R rated to 100K rads*
- *FRF6764H rated to 1000K rads*

TERMINAL DIAGRAM



92CS-43357

N-CHANNEL ENHANCEMENT MODE

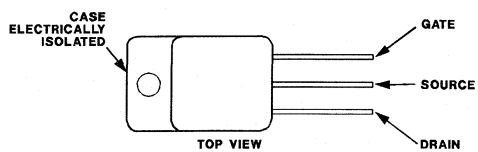
The FRF6764M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRF6764 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRF6764 family is supplied in the JEDEC TO-254AA metal package with the case electrically isolated. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

The FRF6764 family was formerly developmental type TA9798.

TERMINAL DESIGNATION



JEDEC TO-254AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DS}	100	V
DRAIN-GATE VOLTAGE (R_{gs} = 20 KΩ)	V_{DGR}	100	V
CONTINUOUS DRAIN CURRENT:	I_D		
At T_c = 25° C		30	A
At T_c = 100° C		24	A
PULSED DRAIN CURRENT	I_{DM}	70	A
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
POWER DISSIPATION:	P_T		
At T_c = 25° C		125 (See Fig. 9)	W
At T_c = 100° C		50 (See Fig. 9)	W
Derate linearly above T_c = 25° C		1.2 (See Fig. 9)	W/° C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH	I_{LM}	70 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering):	T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.		300	°C

FRF6764M, FRF6764D, FRF6764R, FRF6764H

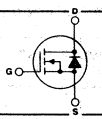
PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	—	25	μA
		V_{DS} = 80 V, V_{GS} = 0, T_c = 125°C	—	—	250	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A	—	—	1.80	V
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 24 A	—	0.040	0.055	Ω
		V_{GS} = 10 V, I_D = 24 A, T_c = 125°C	—	—	0.094	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 24 A	9	—	27	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	4000	—	pF
Output Capacitance	C_{oss}		—	1000	—	
Reverse-Transfer Capacitance	C_{rss}		—	600	—	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 24 A, Z_o = 4.7 Ω (See Figs. 11 & 12)	—	—	35	ns
Rise Time	t_r		—	—	250	
Turn-Off Delay Time	$t_{d(off)}$		—	—	125	
Fall Time	t_f		—	—	100	
Gate-Charge Threshold	Q_{gth}	V_{DD} = 50 V, I_D = 30 A Method 3471 from Mil-Std-750, Cond. A (See Fig. 13)	3	7.5	11	nC
Gate Charge	Q_g		48	110	160	
Gate-Charge Total	Q_{gm}		92	250	350	
Gate-Plateau Voltage	V_{gp}		4.5	9	13	V
Gate-Source Charge	Q_{gs}		6.4	35	50	nC
Gate-Drain ("Miller") Charge	Q_{gd}		24	70	100	

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Junction-to-Case	$R_{\theta JC}$		—	—	1	°C/W
Case-to-Sink	$R_{\theta JC}$	Mounting surface flat, smooth and greased	—	0.21	—	
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	48	

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Source current (Body Diode)	I_s	MOSFET symbol showing the integral reverse P-N junction rectifier 	—	—	30	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	70	
Diode Forward Voltage[1]	V_{SD}	T_c = 25°C, I_F = 30 A, V_{GS} = 0	0.85	—	1.9	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	225	500	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

FRF6764M, FRF6764D, FRF6764R, FRF6764H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = 1 mA[2,3,4,5] (See Fig. 14)	100	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRF6764M	$V_{GS} = V_{DS}$, I_D = 1 mA[3,4,5] (See Fig. 15)	2	4	V
		FRF6764D		1.5	4.2	
		FRF6764R		1	4.5	
		FRF6764H		0.5	5	
		All	$V_{GS} = V_{DS}$, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRF6764M	V_{GS} = 0, V_{DS} = 80 V[3,4,5]	—	25	μA
		FRF6764D		—	50	
		FRF6764R		—	100	
		FRF6764H		—	250	
		All	V_{GS} = 0, V_{DS} = 80 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRF6764M	V_{GS} = 10 V, I_D = 24 A[3,4,5]	—	0.055	Ω
		FRF6764D	V_{GS} = 10 V, I_D = 24 A[3,4,5]	—	0.055	
		FRF6764R	V_{GS} = 12 V, I_D = 24 A[3,4,5]	—	0.060	
		FRF6764H	V_{GS} = 16 V, I_D = 12 A[3,4,5]	—	0.125	
		All	V_{GS} = 10 V, I_D = 24 A[2]	—	0.060	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRF6764M	V_{GS} = 10 V, I_D = 30 A[3,4,5]	—	1.8	V
		FRF6764D	V_{GS} = 10 V, I_D = 30 A[3,4,5]	—	2	
		FRF6764R	V_{GS} = 12 V, I_D = 30 A[3,4,5]	—	2.4	
		FRF6764H	V_{GS} = 16 V, I_D = 16 A[3,4,5]	—	3	
		All	V_{GS} = 10 V, I_D = 30 A[2]	—	1.95	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 2 x 10^{12} n°/cm^2, $V_{GS} = V_{DS} = 0$.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 80 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRF6764M, D, R, and H, respectively.

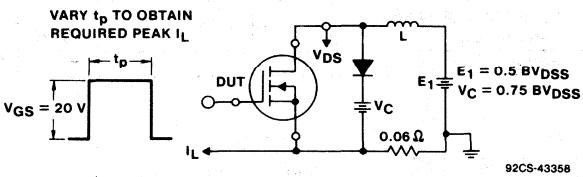


Fig. 1 - Clamped inductive test circuit.

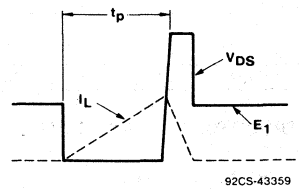


Fig. 2 - Clamped inductive waveforms.

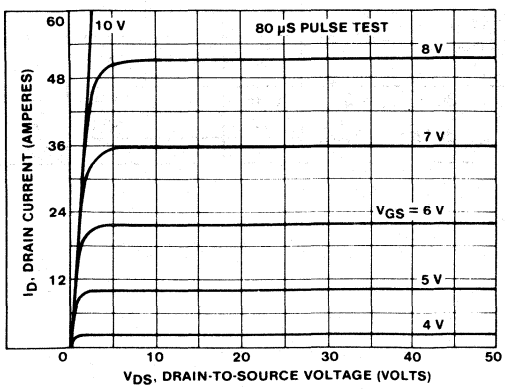


Fig. 3 - Typical output characteristics.

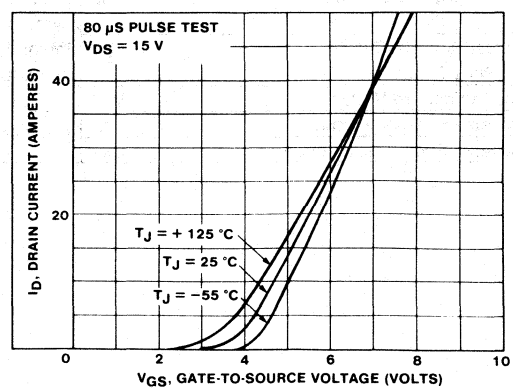


Fig. 4 - Typical transfer characteristics.

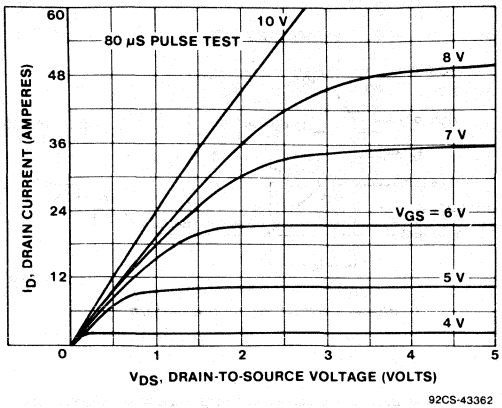


Fig. 5 - Typical saturation characteristics.

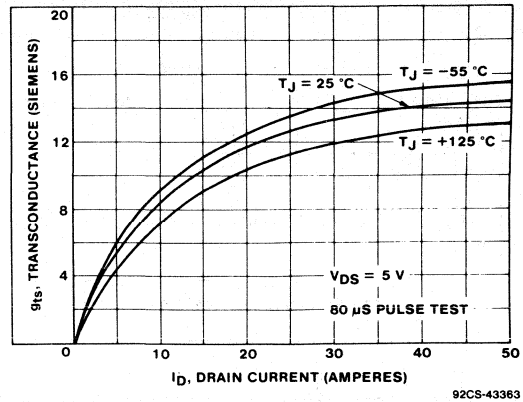


Fig. 6 - Typical transconductance vs. drain current.

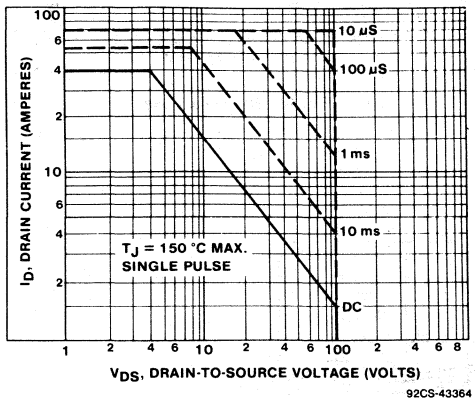


Fig. 7 - Maximum safe operating area.

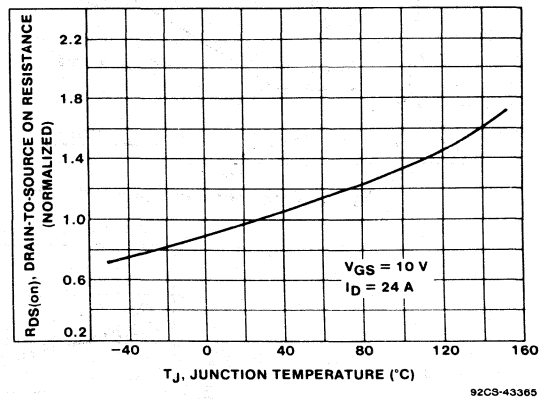


Fig. 8 - Normalized typical on-resistance vs. temperature.

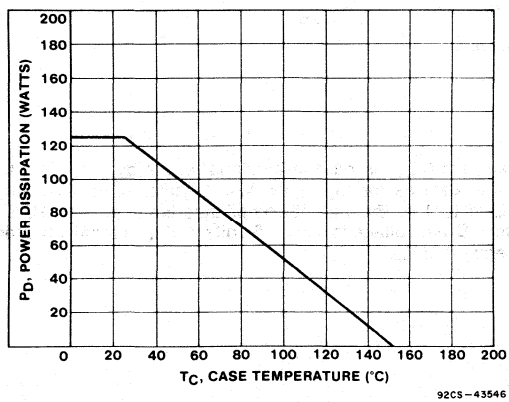


Fig. 9 - Power vs. temperature derating curve.

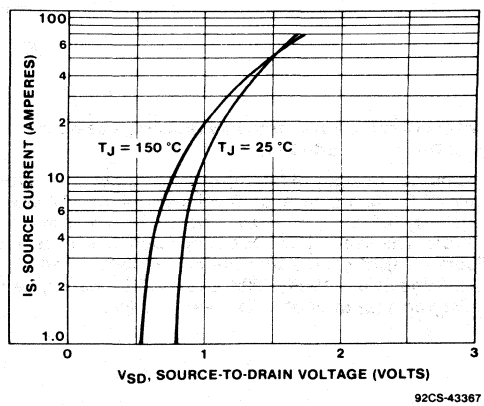


Fig. 10 - Typical body-drain diode forward voltage.

FRF6764M, FRF6764D, FRF6764R, FRF6764H

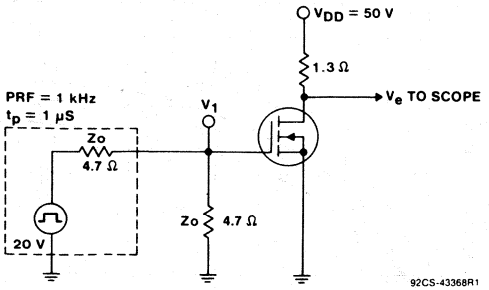


Fig. 11 - Switching time test circuit.

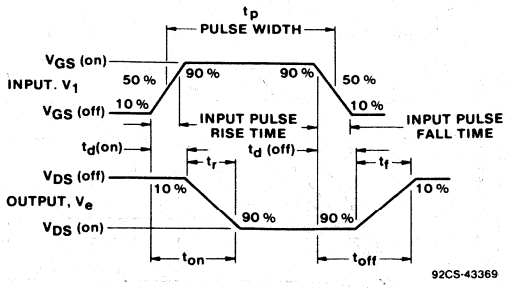


Fig. 12 - Switching time waveforms.

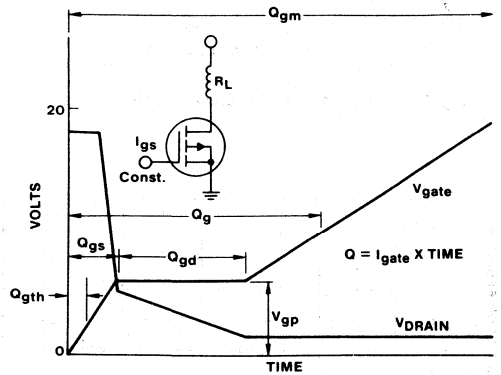


Fig. 13 - Gate charge waveforms.

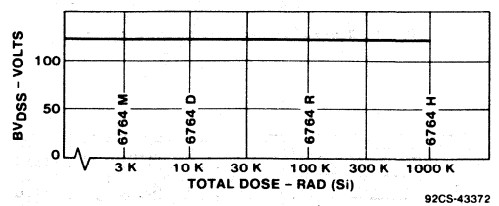


Fig. 14 - BV_{DSS} vs. dose.

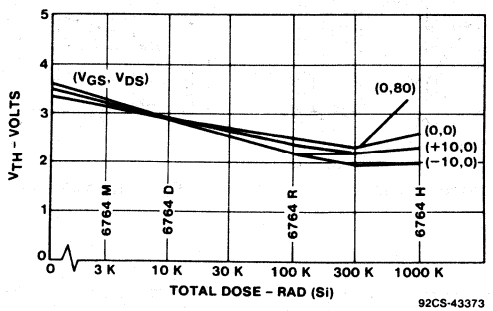


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Figs. 16 through 19 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of I_D = 5 A/div. and horizontal sensitivity of ½ V/div. The five FRF6764H devices were biased as noted in diagram (e) of each figure during irradiation and removed for testing at 0K, 100K, 300K and 1000K rads (Si) as noted in diagrams (a) through (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log I_D vs. V_{GS}. Vertical scale is I_D from 1E-11 to 1 A. Equipment compliance limits data to 1E-1 A max. Drain voltage is set at +5 volts, but I_D is relatively independent of V_{DS}.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = -10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

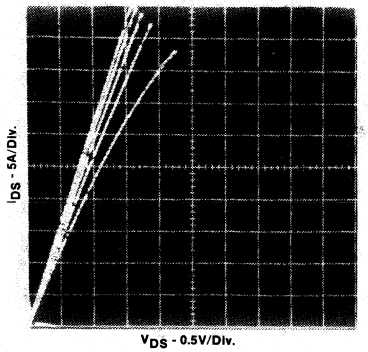


Fig. 16(a) - Typical output characteristics at pre-radiation.

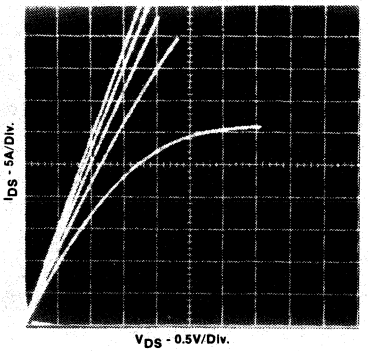


Fig. 16(b) - Typical output characteristics at 100K rads (Si).

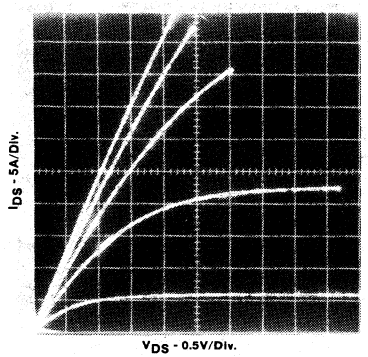


Fig. 16(c) - Typical output characteristics at 300K rads (Si).

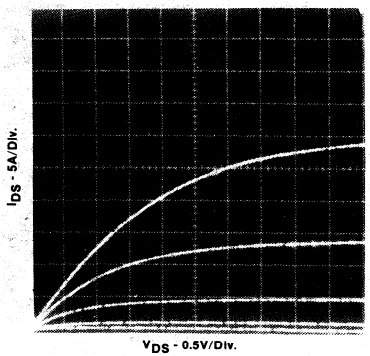


Fig. 16(d) - Typical output characteristics at 1M rad (Si).

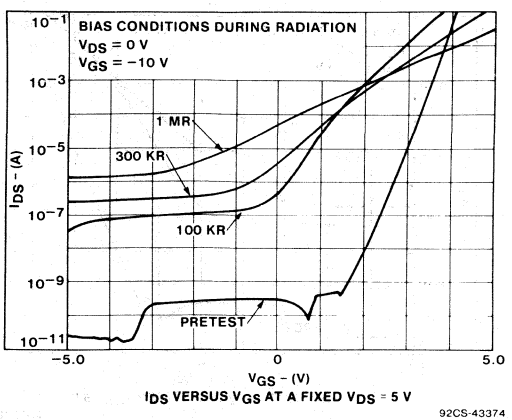


Fig. 16(e) - Drain source current as a function of gate bias.

FRF6764M, FRF6764D, FRF6764R, FRF6764H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = +10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

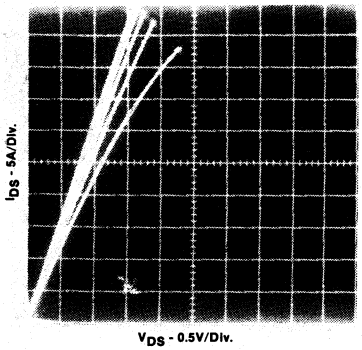


Fig. 17(a) - Typical output characteristics at pre-radiation.

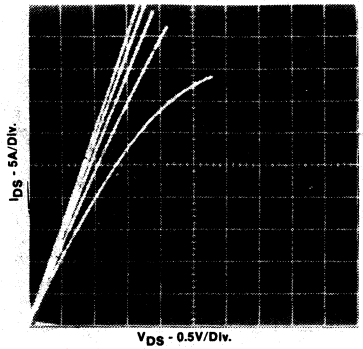


Fig. 17(b) - Typical output characteristics at 100K rads (Si).

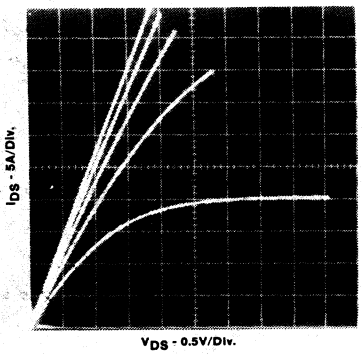


Fig. 17(c) - Typical output characteristics at 300K rads (Si).

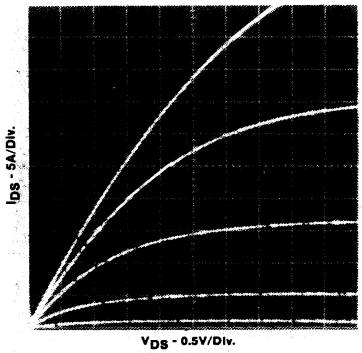


Fig. 17 (d)- Typical output characteristics at 1M rad (Si).

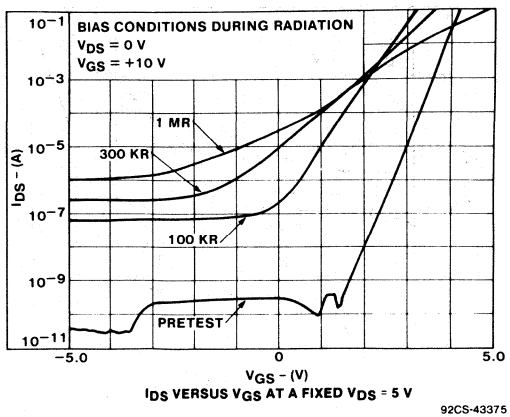


Fig. 17(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

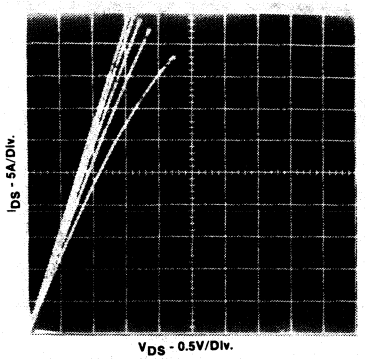


Fig. 18(a) - Typical output characteristics at pre-radiation.

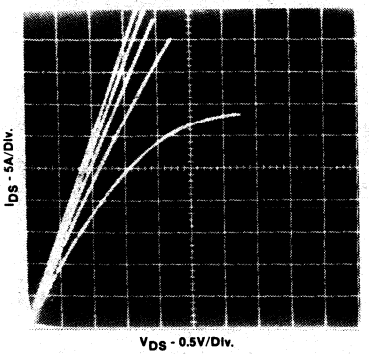


Fig. 18(b) - Typical output characteristics at 100K rads (Si).

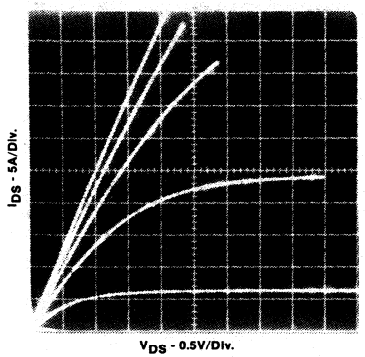


Fig. 18(c) - Typical output characteristics at 300K rads (Si).

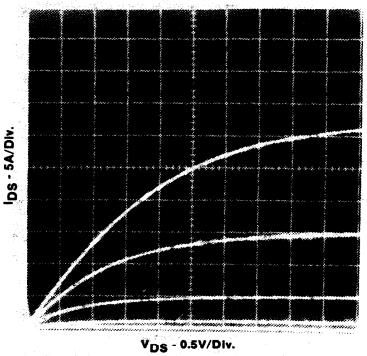


Fig. 18(d) - Typical output characteristics at 1M rad (Si).

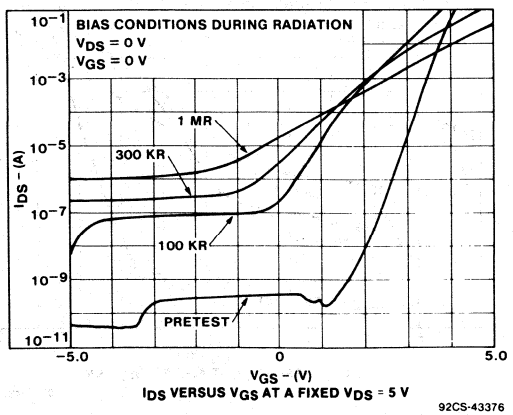


Fig. 18(e) - Drain source current as a function of gate bias.

FRF6764M, FRF6764D, FRF6764R, FRF6764H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 80 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

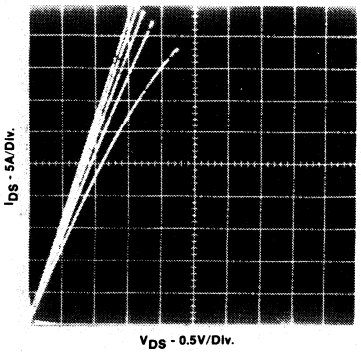


Fig. 19(a) - Typical output characteristics at pre-radiation.

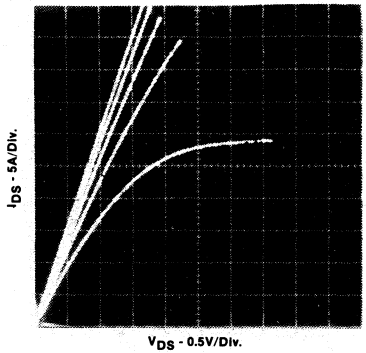


Fig. 19(b) - Typical output characteristics at 100K rads (Si).

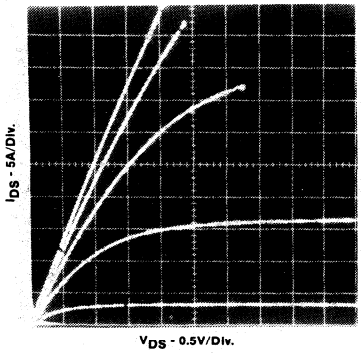


Fig. 19(c) - Typical output characteristics at 300K rads (Si).

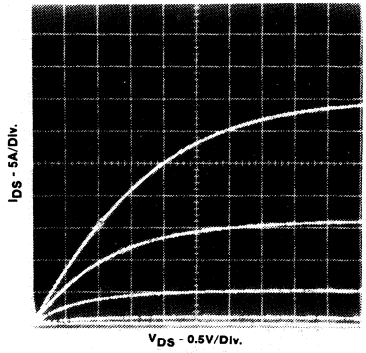


Fig. 19(d) - Typical output characteristics at 1M rad (Si).

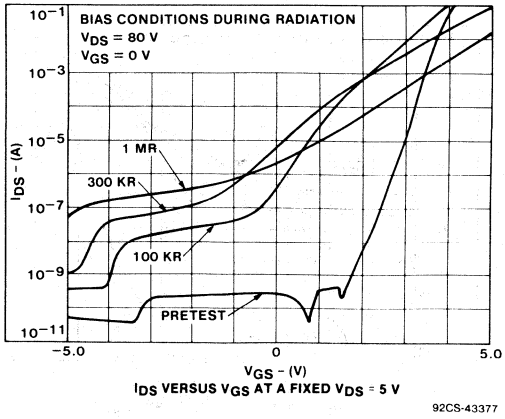


Fig. 19(e) - Drain source current as a function of gate bias.

File Number **2322**

FRF6766M, FRF6766D, FRF6766R, FRF6766H

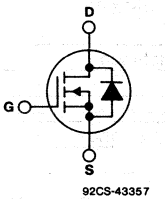
Radiation-Hardened N-Channel Power MOSFETs

Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

30 A, 200 V
$r_{DS(on)}$ = 0.85 Ω

Features:
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *Isolated case*
- *FRF6766M rated to 3k rads*
- *FRF6766D rated to 10K rads*
- *FRF6766R rated to 100K rads*
- *FRF6766H rated to 1000K rads*

TERMINAL DIAGRAM



92CS-43357

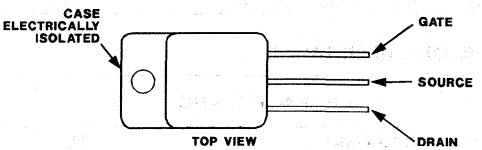
N-CHANNEL ENHANCEMENT MODE

The FRF6766M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRF6766 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRF6766 family is supplied in the JEDEC TO-254AA metal package with the case electrically isolated. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

TERMINAL DESIGNATION



JEDEC TO-254AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DS}	200	V
DRAIN-GATE VOLTAGE (R_{gs} = 20 KΩ)	V_{DGR}	200	V
CONTINUOUS DRAIN CURRENT:	I_D		
At T_c = 25°C		30	A
At T_c = 100°C		19	A
PULSED DRAIN CURRENT	I_{DM}	60	A
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
POWER DISSIPATION:	P_T		
At T_c = 25°C		125 (See Fig. 9)	W
At T_c = 100°C		50 (See Fig. 9)	W
Derate linearly above T_c = 25°C		1.2 (See Fig. 9)	W/°C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH	I_{LM}	60 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering):	T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.		300	°C

FRF6766M, FRF6766D, FRF6766R, FRF6766H

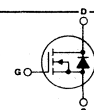
PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA	200	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	—	25	μA
		V_{DS} = 160 V, V_{GS} = 0, T_c = 125° C	—	—	250	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A	—	—	2.8	V
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 19 A	—	0.070	0.085	Ω
		V_{GS} = 10 V, I_D = 19 A, T_c = 125° C	—	—	0.153	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 19 A	—	15	—	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	4000	—	pF
Output Capacitance	C_{oss}		—	750	—	
Reverse-Transfer Capacitance	C_{rss}		—	250	—	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 19 A, Z_o = 4.7 Ω (See Figs. 11 & 12)	—	—	35	ns
Rise Time	t_r		—	—	100	
Turn-Off Delay Time	$t_{d(off)}$		—	—	125	
Fall Time	t_f		—	—	100	
Gate-Charge Threshold	Q_{gth}	V_{DD} = 100 V, I_D = 30 A Method 3471 from Mil-Std-750, Cond. A (See Fig. 13)	3	7.2	11	nC
Gate Charge	Q_g		48	115	165	
Gate-Charge Total	Q_{gm}		88	230	330	
Gate-Plateau Voltage	V_{gp}		4.5	7.5	11	V
Gate-Source Charge	Q_{gs}		6.1	27	40	nC
Gate-Drain ("Miller") Charge	Q_{gd}		24	58	85	

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Junction-to-Case	$R_{\theta JC}$		—	—	1	°C/W
Case-to-Sink	$R_{\theta JC}$	Mounting surface flat, smooth and greased	—	0.21	—	
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	48	

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Source current (Body Diode)	I_s	MOSFET symbol showing the integral reverse P-N junction rectifier 	—	—	30	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	60	
Diode Forward Voltage[1]	V_{SD}	T_c = 25° C, I_F = 30 A, V_{GS} = 0	0.85	—	1.8	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	325	950	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

FRF6766M, FRF6766D, FRF6766R, FRF6766H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = mA[2,3,4,5] (See Fig. 14)	180	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRF6766M	$V_{GS} = V_{DS}$, I_D = 0.25 mA[3,4,5] (See Fig. 15)	2	4	V
		FRF6766D		1.5	4.2	
		FRF6766R		1	4.5	
		FRF6766H		0.5	5	
		All	$V_{GS} = V_{DS}$, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRF6766M	V_{GS} = 0, V_{DS} = 160 V[3,4,5]	—	25	μA
		FRF6766D		—	50	
		FRF6766R		—	50	
		FRF6766H		—	100	
		All	V_{GS} = 0, V_{DS} = 160 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRF6766M	V_{GS} = 10 V, I_D = 19 A[3,4,5]	—	0.085	Ω
		FRF6766D	V_{GS} = 10 V, I_D = 19 A[3,4,5]	—	0.100	
		FRF6766R	V_{GS} = 10 V, I_D = 19 A[3,4,5]	—	0.125	
		FRF6766H	V_{GS} = 16 V, I_D = 6 A[3,4,5]	—	0.250	
		All	V_{GS} = 10 V, I_D = 19 A[2]	—	0.100	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRF6766M	V_{GS} = 10 V, I_D = 30 A[3,4,5]	—	2.8	V
		FRF6766D	V_{GS} = 10 V, I_D = 30 A[3,4,5]	—	3	
		FRF6766R	V_{GS} = 12 V, I_D = 25 A[3,4,5]	—	3.5	
		FRF6766H	V_{GS} = 16 V, I_D = 8 A[3,4,5]	—	3	
		All	V_{GS} = 10 V, I_D = 30 A[2]	—	3	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 2 x 10^{12} n°/cm^2, $V_{GS} = V_{DS}$ = 0.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 160 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRF6766M, D, R and H, respectively.

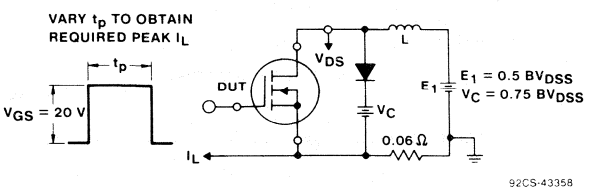


Fig. 1 - Clamped inductive test circuit.

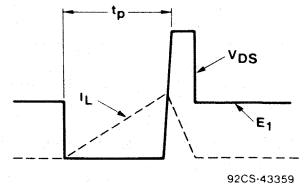


Fig. 2 - Clamped inductive waveforms.

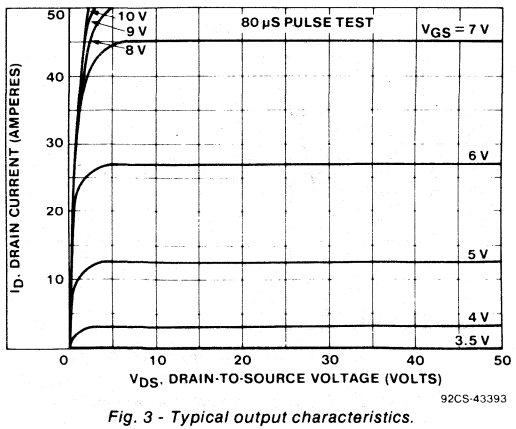


Fig. 3 - Typical output characteristics.

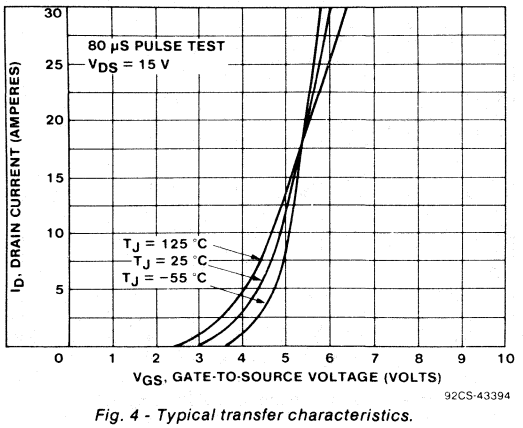


Fig. 4 - Typical transfer characteristics.

FRF6766M, FRF6766D, FRF6766R, FRF6766H

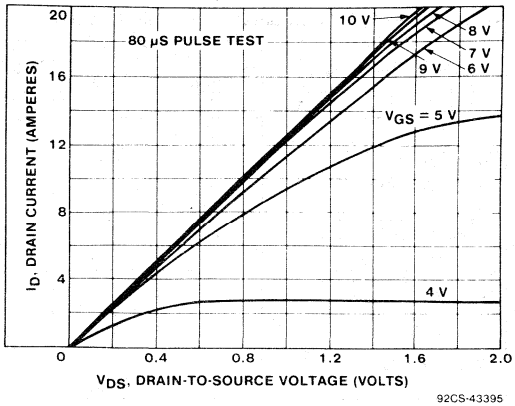


Fig. 5 - Typical saturation characteristics.

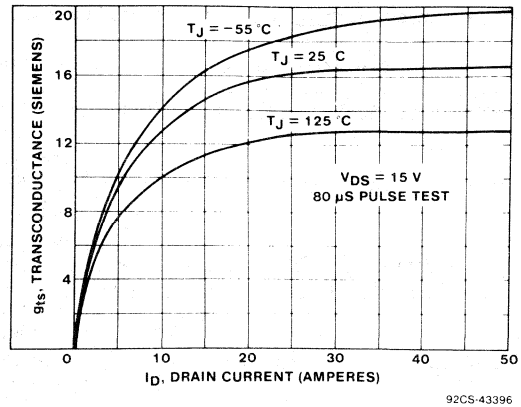


Fig. 6 - Typical transconductance vs. drain current.

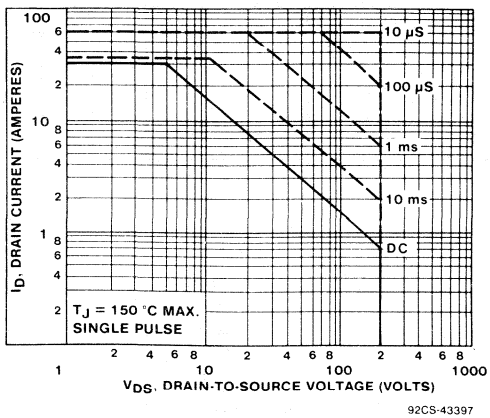


Fig. 7 - Maximum safe operating area.

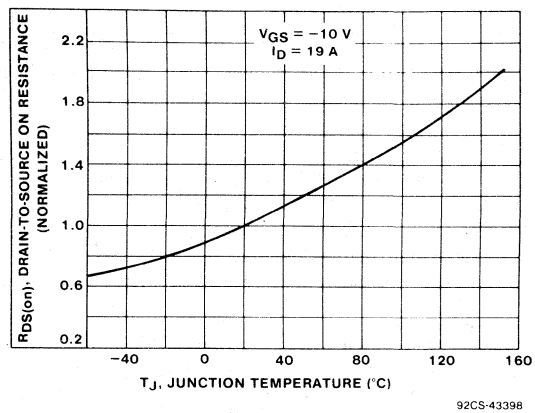


Fig. 8 - Normalized typical on-resistance vs. temperature.

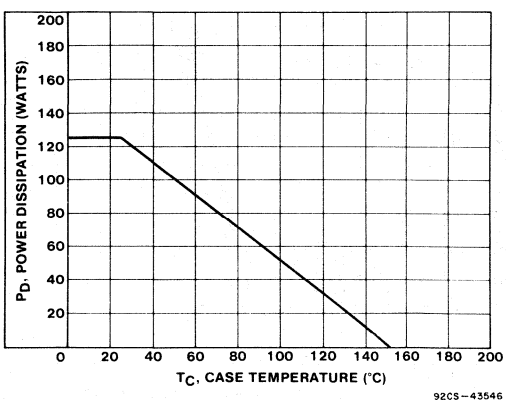


Fig. 9 - Power vs. temperature derating curve.

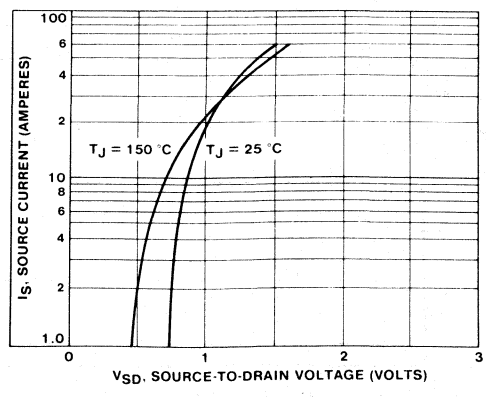


Fig. 10 - Typical body-drain diode forward voltage.

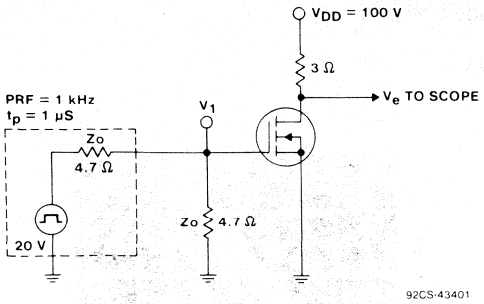


Fig. 11 - Switching time test circuit.

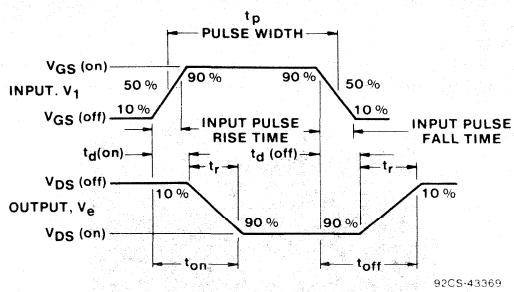


Fig. 12 - Switching time waveforms.

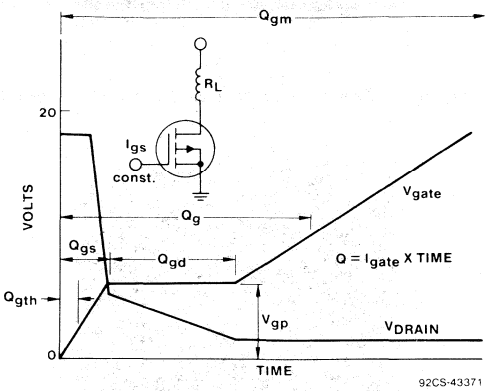


Fig. 13 - Gate charge waveforms.

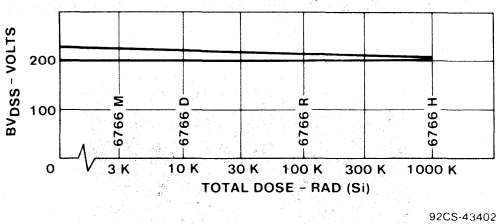


Fig. 14 - BV_{DSS} vs. dose.

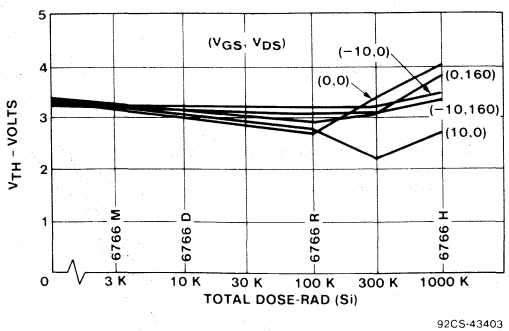


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Figs. 16 through 19 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of I_D = 5 A/div. and horizontal sensitivity of ½V/div. The five FRF6766H devices were biased as noted in diagram (e) of each figure during irradiation and removed for testing at 0K, 100K, 300K and 1000K rads (Si) as noted in diagrams (a) through (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log I_D vs. V_{GS}. Vertical scale is I_D from 1E-11 to 1 A. Equipment compliance limits data to 1E-1 A max. Drain voltage is set at +5 volts, but I_D is relatively independent of V_{DS}.

FRF6766M, FRF6766D, FRF6766R, FRF6766H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = -10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

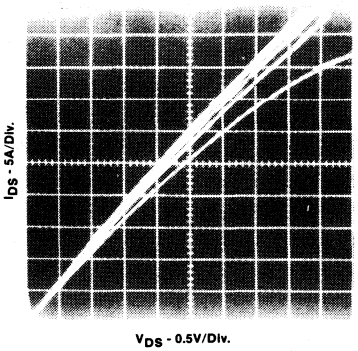


Fig. 16(a) - Typical output characteristics at pre-radiation.

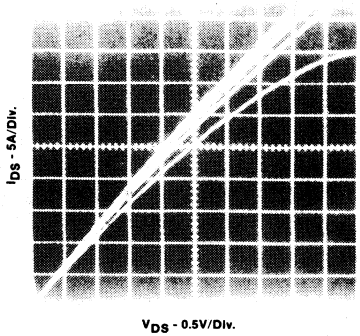


Fig. 16(b) - Typical output characteristics at 100K rads (Si).

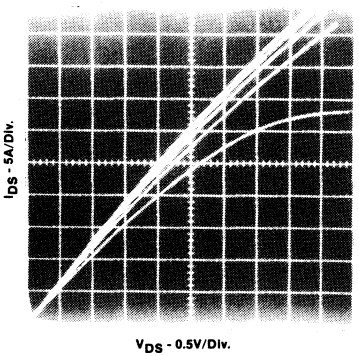


Fig. 16(c) - Typical output characteristics at 300K rads (Si).

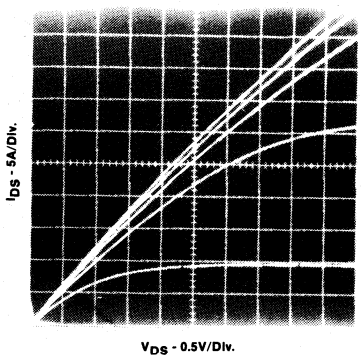


Fig. 16(d) - Typical output characteristics at 1M rad (Si).

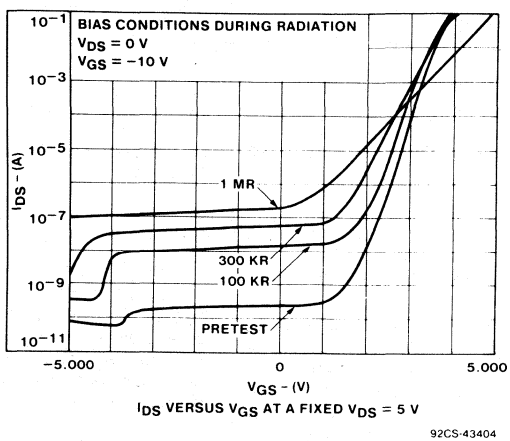


Fig. 16(e) - Drain source current as a function of gate bias.

FRF6766M, FRF6766D, FRF6766R, FRF6766H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

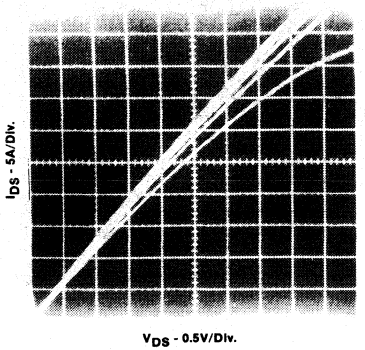


Fig. 17(a) - Typical output characteristics at pre-radiation.

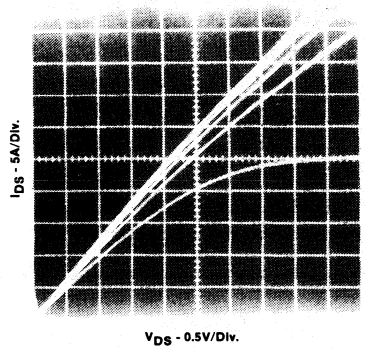


Fig. 17(b) - Typical output characteristics at 100K rads (Si).

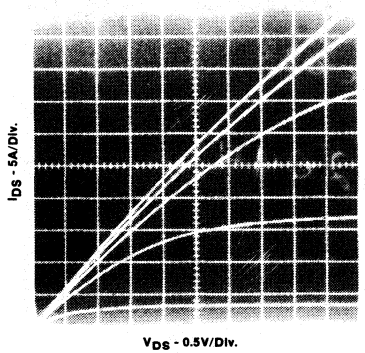


Fig. 17(c) - Typical output characteristics at 300K rads (Si).

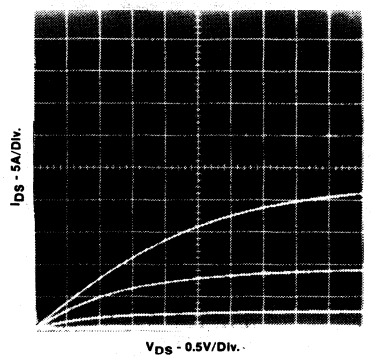
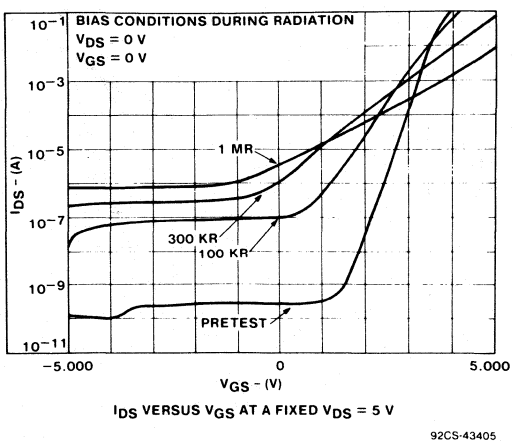


Fig. 17(d) - Typical output characteristics at 1M rad (Si).



I_{DS} VERSUS V_{GS} AT A FIXED V_{DS} = 5 V

92CS-43405

Fig. 17(e) - Drain source current as a function of gate bias.

FRF6766M, FRF6766D, FRF6766R, FRF6766H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = +10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

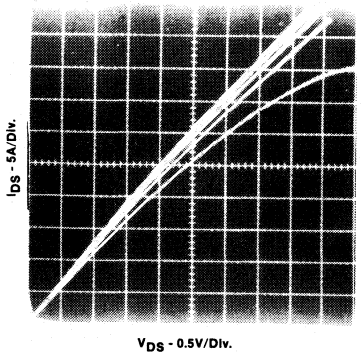


Fig. 18(a) - Typical output characteristics at pre-radiation.

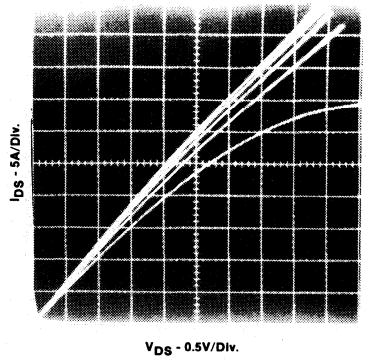


Fig. 18(b) - Typical output characteristics at 100K rads (Si).

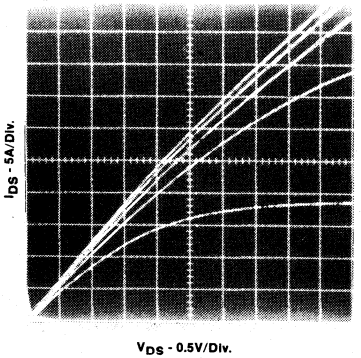


Fig. 18(c) - Typical output characteristics at 300K rads (Si).

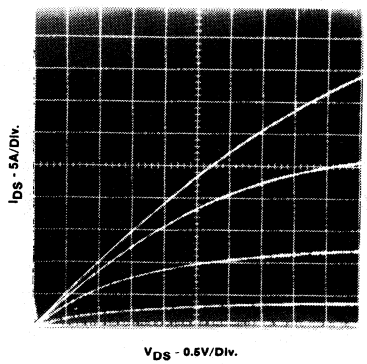


Fig. 18(d) - Typical output characteristics at 1M rad (Si).

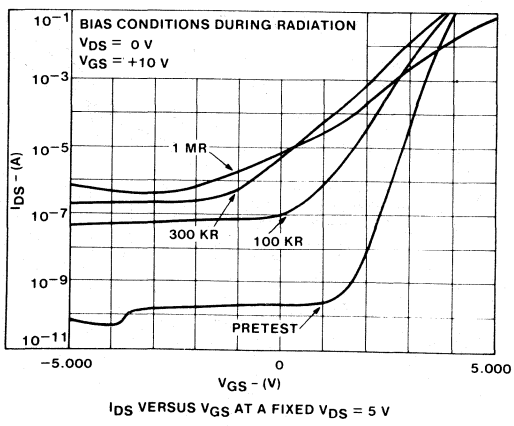


Fig. 18(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 160 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

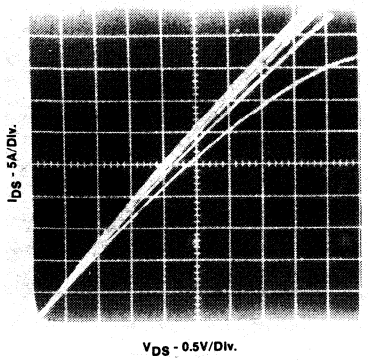


Fig. 19(a) - Typical output characteristics at pre-radiation.

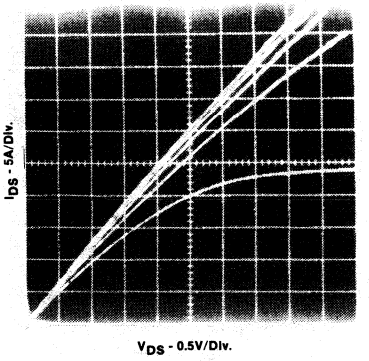


Fig. 19(b) - Typical output characteristics at 100K rads (Si).

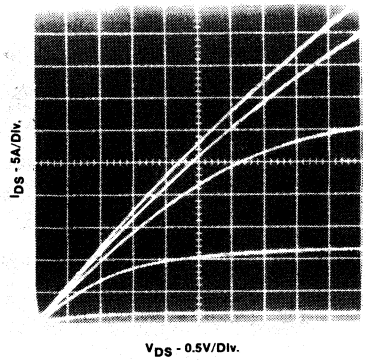


Fig. 19(c) - Typical output characteristics at 300K rads (Si).

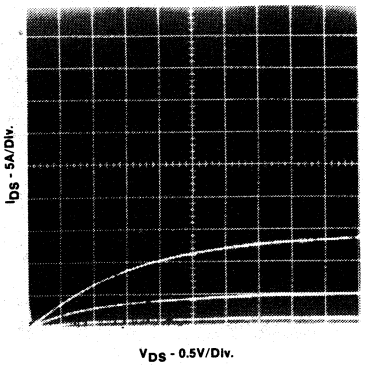


Fig. 19(d) - Typical output characteristics at 1M rad (Si).

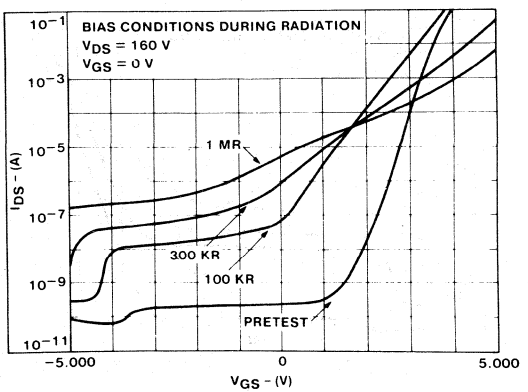


Fig. 19(e) - Drain source current as a function of gate bias.

FRF6766M, FRF6766D, FRF6766R, FRF6766H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = -10 V and V_{DS} = 160 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

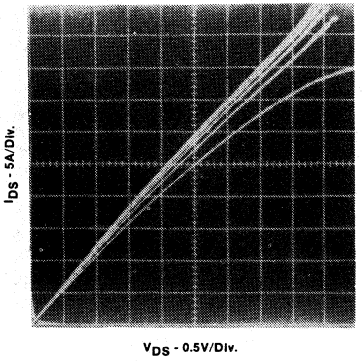


Fig. 20(a) - Typical output characteristics at pre-radiation.

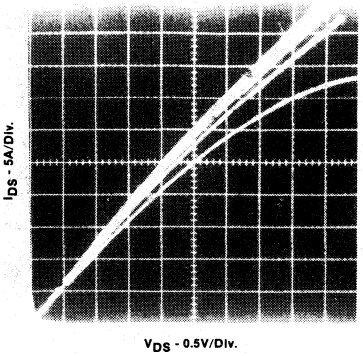


Fig. 20(b) - Typical output characteristics at 100K rads (Si).

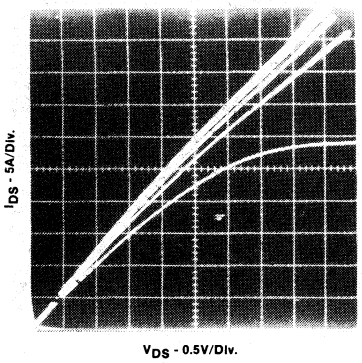


Fig. 20(c) - Typical output characteristics at 300K rads (Si).

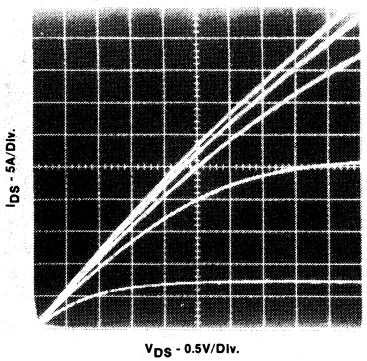


Fig. 20(d) - Typical output characteristics at 1M rad (Si).

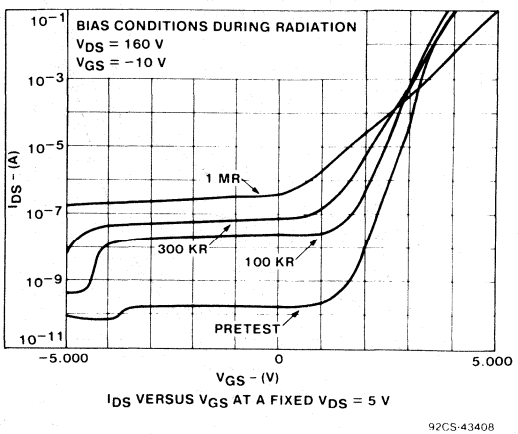


Fig. 20(e) - Drain source current as a function of gate bias.

File Number **2170**

FRK6764M, FRK6764D
FRK6764R, FRK6764H

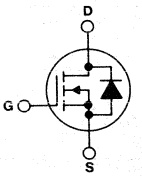
Radiation-Hardened N-Channel Power MOSFETs

Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

38 A, 100 V
$r_{DS}(on)$ = 0.055 Ω

Features:
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *FRK6764M rated to 3K rads*
- *FRK6764D rated to 10K rads*
- *FRK6764R rated to 100K rads*
- *FRK6764H rated to 1000K rads*

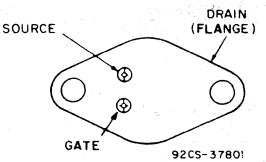
N-CHANNEL ENHANCEMENT MODE



92CS-43357

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

The FRK6764M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRK6764 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRK6764 family is supplied in the JEDEC TO-204AE steel package. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

The FRK6764 family was formerly developmental type TA9798.

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

DRAIN-SOURCE VOLTAGE, V_{DS}	100	V
DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ) V_{DGR}	100	V
CONTINUOUS DRAIN CURRENT: I_D		
At T_C = 25°C	38	A
At T_C = 100°C	24	A
PULSED DRAIN CURRENT I_{DM}	70	A
GATE-SOURCE VOLTAGE V_{GS}	±20	V
POWER DISSIPATION: P_T		
At T_C = 25°C	150 (See Fig. 9)	W
At T_C = 100°C	60 (See Fig. 9)	W
Derate linearly above T_C = 25°C	1.2 (See Fig. 9)	W/°C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH I_{LM}	70 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering): T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.	300	°C

FRK6764M, FRK6764D, FRK6764R, FRK6764H

PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless other specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0, I_D = 1 mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	0.1	1	mA
		V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C	—	0.2	4	
Static Drain-Source On-State Voltage[1]	$V_{DS}(on)$	V_{GS} = 10 V, I_D = 38 A	—	—	2.09	V
Static Drain-Source On-State Resistance[1]	$r_{DS}(on)$	V_{GS} = 10 V, I_D = 24 A	—	0.038	0.055	Ω
		V_{GS} = 10 V, I_D = 24 A, T_C = 125°C	—	—	0.094	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 24 A	—	15	—	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	3000	—	pF
Output Capacitance	C_{oss}		—	1000	—	
Reverse-Transfer Capacitance	C_{rss}		—	250	—	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V, I_D = 24 A, Z_O = 4.7 Ω (See Figs. 11 & 12)	—	—	35	ns
Rise Time	t_r		—	—	250	
Turn-Off Delay Time	$t_d(off)$		—	—	125	
Fall Time	t_f		—	—	100	
Gate-Charge Threshold	Q_{gth}	V_{DD} = 50 V, I_D = 38 A Method 3471 from Mil-Std-750,Cond.A (See Fig. 13)	3	5.5	8	nC
Gate Charge	Q_g		48	80	125	
Gate-Charge Total	Q_{gm}		92	150	215	
Gate-Plateau Voltage	V_{gp}		4.5	7	8.2	V
Gate-Source Charge	Q_{gs}		6.4	19	30	nC
Gate-Drain ("Miller") Charge	Q_{gd}		24	44	75	

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Junction-to-Case	$R_{\theta JC}$		—	—	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	—	0.1	—	
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	30	

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse P-N junction rectifier 	—	—	38	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	70	
Diode Forward Voltage[1]	V_{SD}	T_C = 25°C, I_F = 38 A, V_{GS} = 0	0.8	—	1.9	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	225	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

FRK6764M, FRK6764D, FRK6764R, FRK6764H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = 1 mA[2,3,4,5] (See Fig. 14)	100	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRK6764M	$V_{GS} = V_{DS}$, I_D = 1 mA[3,4,5] (See Fig. 15)	2	4	V
		FRK6764D		1.5	4.2	
		FRK6764R		1	4.5	
		FRK6764H		0.5	5	
		All	$V_{GS} = V_{DS}$, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRK6764M	V_{GS} = 0, V_{DS} = 80 V[3,4,5]	—	25	μA
		FRK6764D		—	50	
		FRK6764R		—	100	
		FRK6764H		—	250	
		All	V_{GS} = 0, V_{DS} = 80 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRK6764M	V_{GS} = 10 V, I_D = 24 A[3,4,5]	—	0.055	Ω
		FRK6764D	V_{GS} = 10 V, I_D = 24 A[3,4,5]	—	0.055	
		FRK6764R	V_{GS} = 12 V, I_D = 24 A[3,4,5]	—	0.060	
		FRK6764H	V_{GS} = 16 V, I_D = 12 A[3,4,5]	—	0.125	
		All	V_{GS} = 10 V, I_D = 24 A[2]	—	0.060	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRK6764M	V_{GS} = 10 V, I_D = 38 A[3,4,5]	—	2.49	V
		FRK6764D	V_{GS} = 10 V, I_D = 38 A[3,4,5]	—	2.49	
		FRK6764R	V_{GS} = 12 V, I_D = 38 A[3,4,5]	—	3	
		FRK6764H	V_{GS} = 16 V, I_D = 16 A[3,4,5]	—	3	
		All	V_{GS} = 10 V, I_D = 38 A[2]	—	2.7	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 1 x 10^{12} n°/cm^2, $V_{GS} = V_{DS}$ = 0.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 80 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRK6764M,D,R and H, respectively.

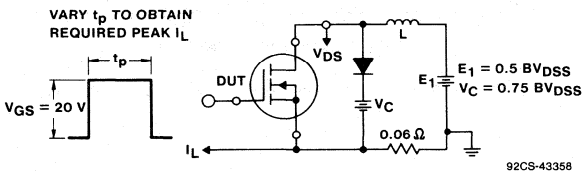


Fig. 1 - Clamped inductive test circuit.

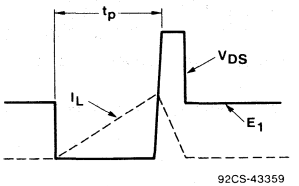


Fig. 2 - Clamped inductive waveforms.

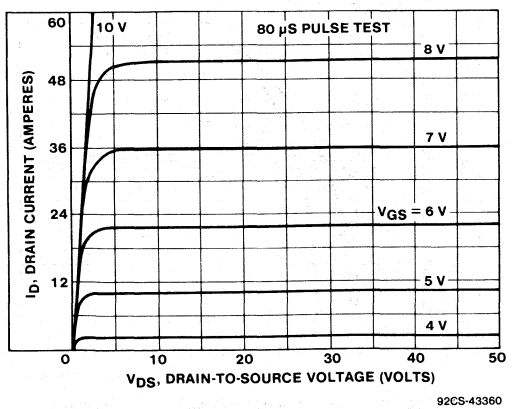


Fig. 3 - Typical output characteristics.

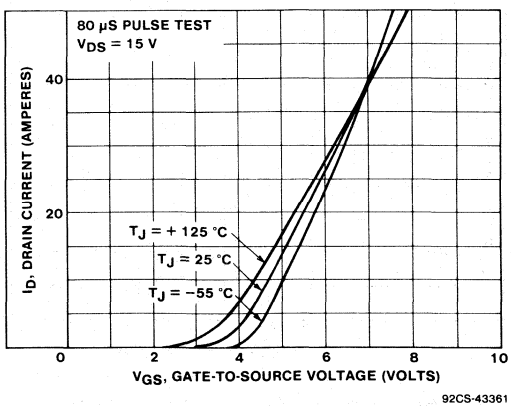


Fig. 4 - Typical transfer characteristics.

FRK6764M, FRK6764D, FRK6764R, FRK6764H

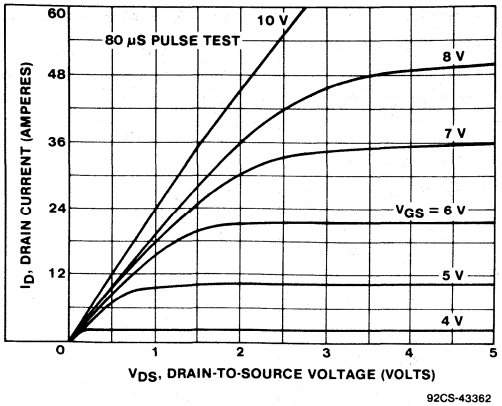


Fig. 5 - Typical saturation characteristics.

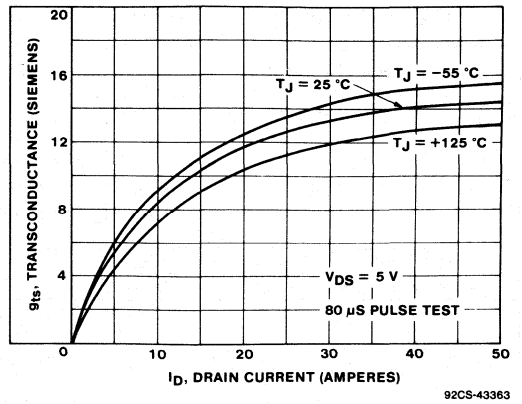


Fig. 6 - Typical transconductance vs. drain current.

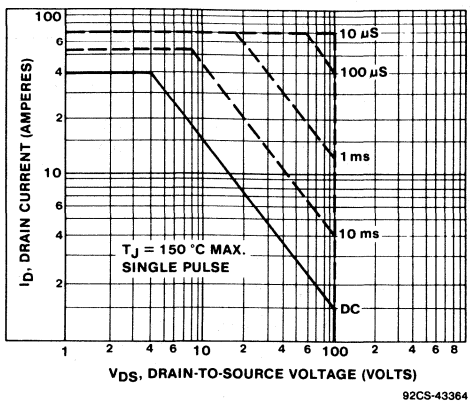


Fig. 7 - Maximum safe operating area.

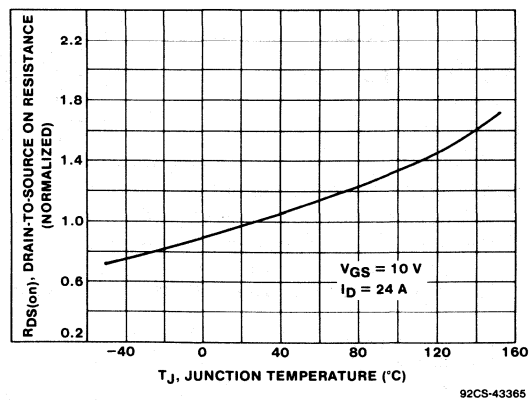


Fig. 8 - Normalized typical on-resistance vs. temperature.

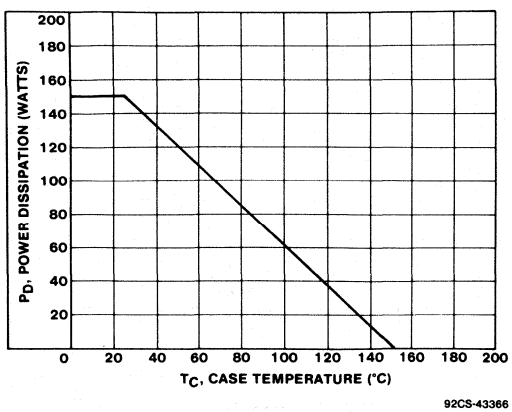


Fig. 9 - Power vs. temperature derating curve.

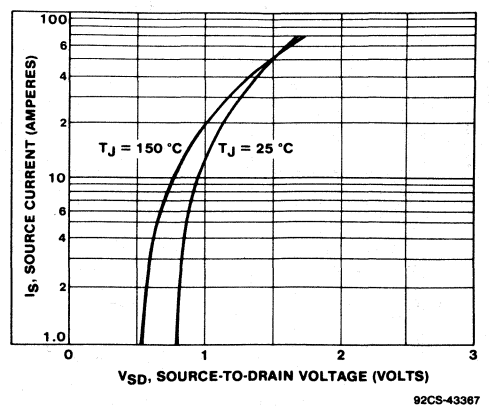


Fig. 10 - Typical body-drain diode forward voltage.

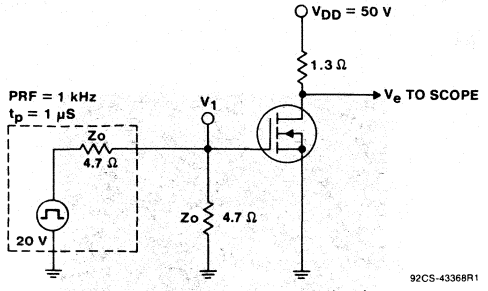


Fig. 11 - Switching time test circuit.

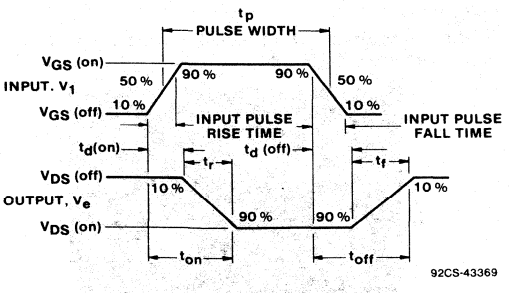


Fig. 12 - Switching time waveforms.

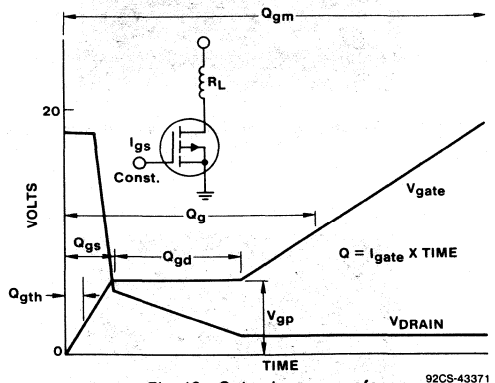


Fig. 13 - Gate charge waveforms.

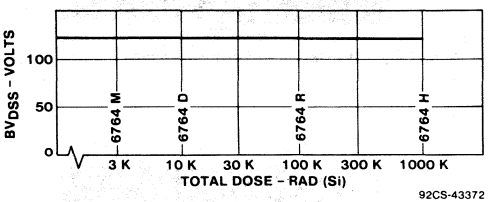


Fig. 14 - BV_{DSS} vs. dose.

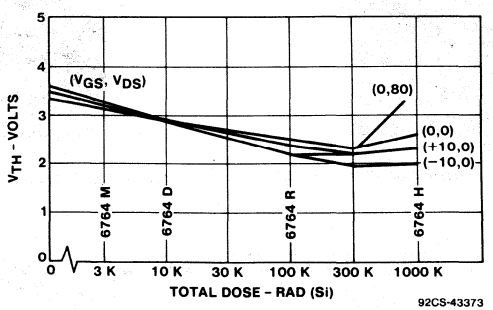


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Figs.16 through 19 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of I_D = 5 A/div. and horizontal sensitivity of ½V/div. The four FRK6764H devices were biased as noted in diagram (e) of each figure during irradiation and removed for testing at 0K, 100K, 300K and 1000K rads (Si) as noted in diagrams (a) through (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log I_D vs. V_{GS}. Vertical scale is I_D from 1E-11 to 1A. Equipment compliance limits data to 1E-1A max. Drain voltage is set at +5 volts, but I_D is relatively independent of V_{DS}.

FRK6764M, FRK6764D, FRK6764R, FRK6764H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = -10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

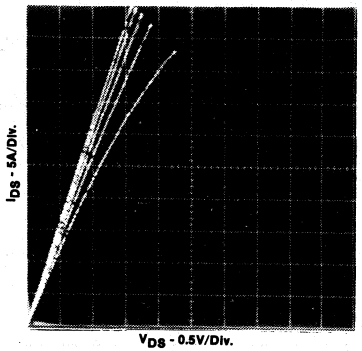


Fig. 16(a) - Typical output characteristics at pre-radiation.

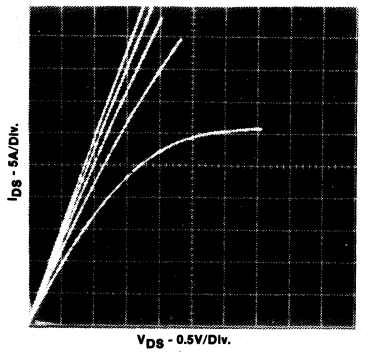


Fig. 16(b) - Typical output characteristics at 100K rads (Si).

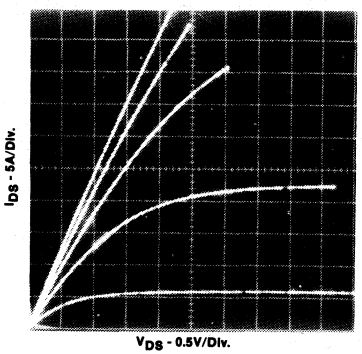


Fig. 16(c) - Typical output characteristics at 300K rads (Si).

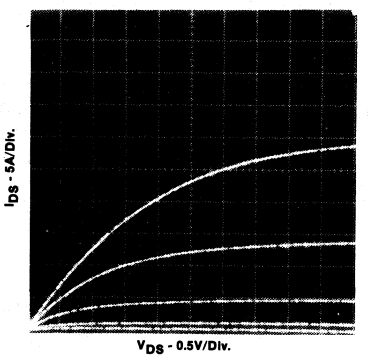


Fig. 16(d) - Typical output characteristics at 1M rad (Si).

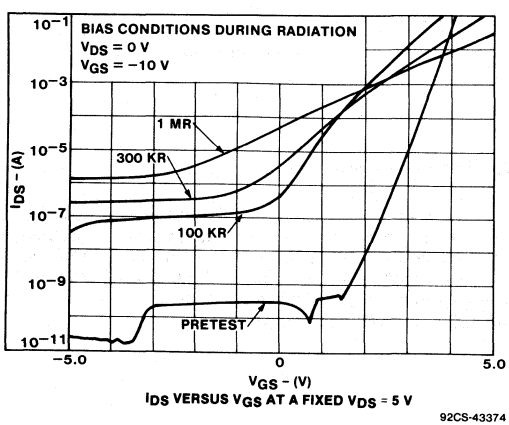


Fig. 16(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = +10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

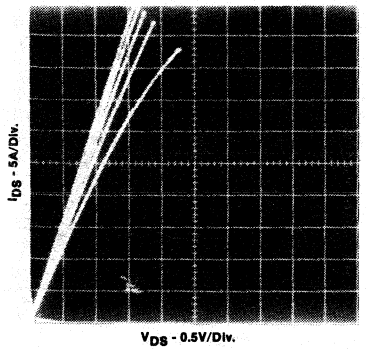


Fig. 17(a) - Typical output characteristics at pre-radiation.

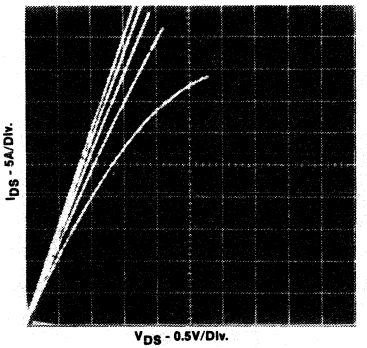


Fig. 17(b) - Typical output characteristics at 100K rads (Si).

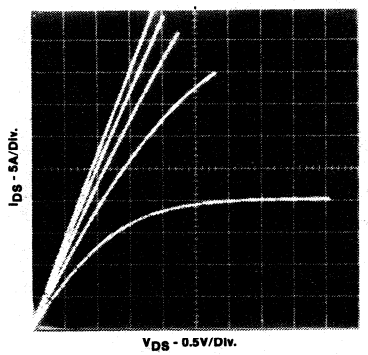


Fig. 17(c) - Typical output characteristics at 300K rads (Si).

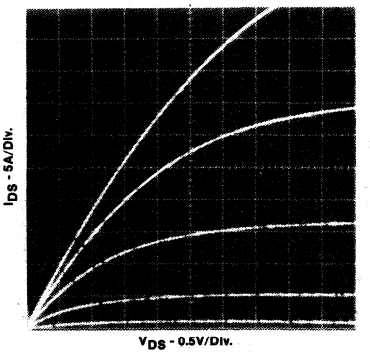


Fig. 17 (d)- Typical output characteristics at 1M rad (Si).

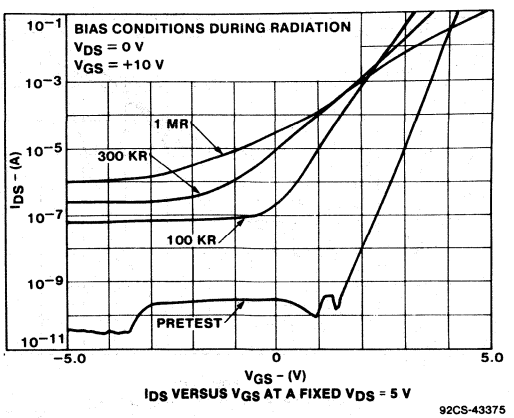


Fig. 17(e) - Drain source current as a function of gate bias.

FRK6764M, FRK6764D, FRK6764R, FRK6764H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

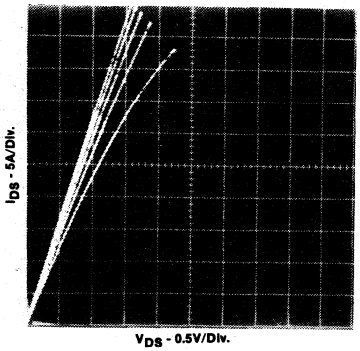


Fig. 18(a) - Typical output characteristics at pre-radiation.

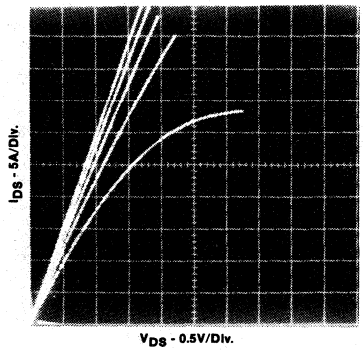


Fig. 18(b) - Typical output characteristics at 100K rads (Si).

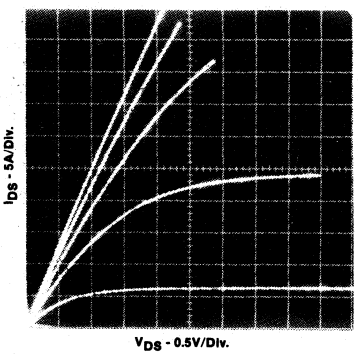


Fig. 18(c) - Typical output characteristics at 300K rads (Si).

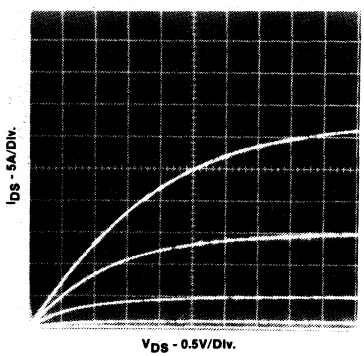


Fig. 18(d) - Typical output characteristics at 1M rad (Si).

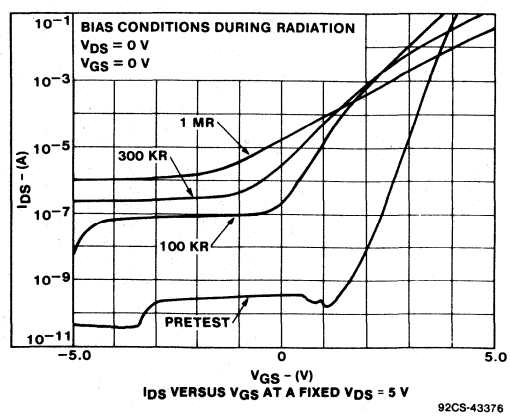


Fig. 18(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 80 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

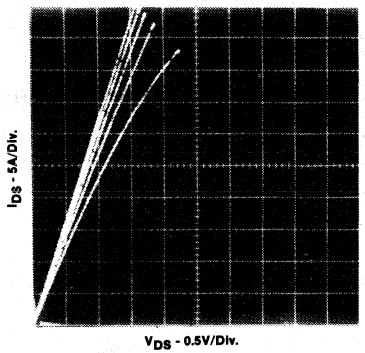


Fig. 19(a) - Typical output characteristics at pre-radiation.

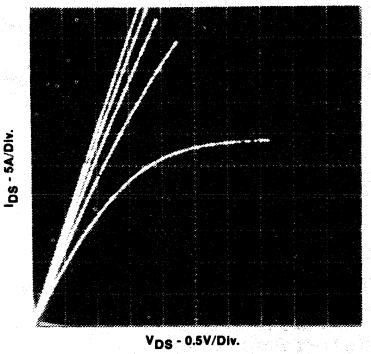


Fig. 19(b) - Typical output characteristics at 100K rads (Si).

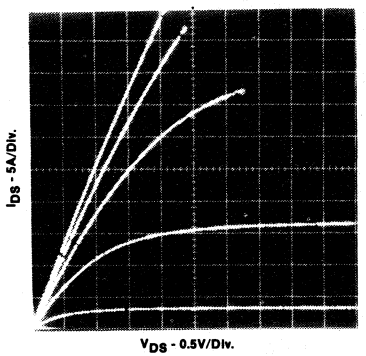


Fig. 19(c) - Typical output characteristics at 300K rads (Si).

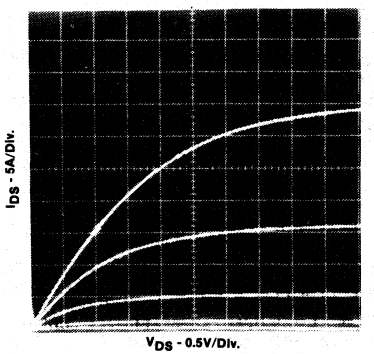


Fig. 19(d) - Typical output characteristics at 1M rad (Si).

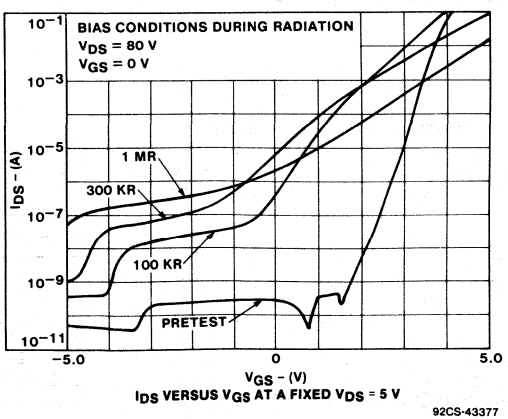


Fig. 19(e) - Drain source current as a function of gate bias.

FRK6766M, FRK6766D
FRK6766R, FRK6766H

File Number **2172**

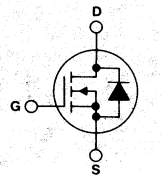
Radiation-Hardened N-Channel Power MOSFETs

Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

30 A, 200 V
$r_{DS}(on)$ = 0.085 Ω

Features:
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *FRK6766M rated to 3K rads*
- *FRK6766D rated to 10K rads*
- *FRK6766R rated to 100K rads*
- *FRK6766H rated to 1000K rads*

N-CHANNEL ENHANCEMENT MODE



92CS-43357

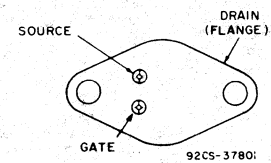
TERMINAL DIAGRAM

The FRK6766M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRK6766 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRK6766 family is supplied in the JEDEC TO-204AE steel package. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

DRAIN-SOURCE VOLTAGE, V_{DS}	200	V
DRAIN-GATE VOLTAGE (R_{gs} = 20 KΩ) V_{DGR}	200	V
CONTINUOUS DRAIN CURRENT: I_D		
At T_C = 25°C	30	A
At T_C = 100°C	19	A
PULSED DRAIN CURRENT I_{DM}	60	A
GATE-SOURCE VOLTAGE V_{GS}	±20	V
POWER DISSIPATION: P_T		
At T_C = 25°C	150 (See Fig. 9)	W
At T_C = 100°C	60 (See Fig. 9)	W
Derate linearly above T_C = 25°C	1.2 (See Fig. 9)	W/°C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH I_{LM}	60 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering): T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.	300	°C

FRK6766M, FRK6766D, FRK6766R, FRK6766H

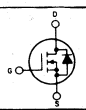
PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless other specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0, I_D = 1 mA	200	—	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	V
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	0.1	1	mA
		V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125° C	—	0.2	4	mA
Static Drain-Source On-State Voltage[1]	$V_{DS}(on)$	V_{GS} = 10 V, I_D = 30 A	—	—	2.7	V
Static Drain-Source On-State Resistance[1]	$r_{DS}(on)$	V_{GS} = 10 V, I_D = 19 A	—	0.070	0.085	Ω
		V_{GS} = 10 V, I_D = 19 A, T_C = 125° C	—	—	0.153	Ω
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 19 A	—	15	—	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	3000	—	pF
Output Capacitance	C_{oss}		—	600	—	pF
Reverse-Transfer Capacitance	C_{rss}		—	150	—	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V, I_D = 19 A, Z_o = 4.7 Ω (See Figs. 11 & 12)	—	—	35	ns
Rise Time	t_r		—	—	100	ns
Turn-Off Delay Time	$t_d(off)$		—	—	125	ns
Fall Time	t_f		—	—	100	ns
Gate-Charge Threshold	Q_{gth}	V_{DD} = 100 V, I_D = 30 A Method 3471 from Mil-Std-750,Cond.A (See Fig. 13)	3	5.5	8	nC
Gate Charge	Q_g		48	90	125	nC
Gate-Charge Total	Q_{gm}		88	160	215	nC
Gate-Plateau Voltage	V_{gp}		4.5	6.4	7.5	V
Gate-Source Charge	Q_{gs}		6.1	18	27	nC
Gate-Drain ("Miller") Charge	Q_{gd}		24	45	75	nC

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Junction-to-Case	$R_{\theta JC}$		—	—	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	—	0.1	—	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	30	°C/W

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse P-N junction rectifier 	—	—	30	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	60	A
Diode Forward Voltage[1]	V_{SD}	T_C = 25° C, I_F = 30 A, V_{GS} = 0	0.8	—	1.6	V
Reverse Recovery Time	t_{rr}	T_J = 25° C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	325	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

FRK6766M, FRK6766D, FRK6766R, FRK6766H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = 1 mA[2,3,4,5] (See Fig. 14)	180	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRK6766M	$V_{GS} = V_{DS}$, I_D = 1 mA[3,4,5] (See Fig. 15)	2	4	V
		FRK6766D		1.5	4.2	
		FRK6766R		1	4.5	
		FRK6766H		0.5	5	
		All	$V_{GS} = V_{DS}$, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRK6766M	V_{GS} = 0, V_{DS} = 160 V[3,4,5]	—	25	μA
		FRK6766D		—	50	
		FRK6766R		—	100	
		FRK6766H		—	250	
		All	V_{GS} = 0, V_{DS} = 160 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRK6766M	V_{GS} = 10 V, I_D = 19 A[3,4,5]	—	0.085	Ω
		FRK6766D	V_{GS} = 10 V, I_D = 19 A[3,4,5]	—	0.100	
		FRK6766R	V_{GS} = 10 V, I_D = 19 A[3,4,5]	—	0.125	
		FRK6766H	V_{GS} = 16 V, I_D = 6 A[3,4,5]	—	0.250	
		All	V_{GS} = 10 V, I_D = 19 A[2]	—	0.100	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRK6766M	V_{GS} = 10 V, I_D = 30 A[3,4,5]	—	2.7	V
		FRK6766D	V_{GS} = 10 V, I_D = 30 A[3,4,5]	—	3	
		FRK6766R	V_{GS} = 12 V, I_D = 25 A[3,4,5]	—	3.5	
		FRK6766H	V_{GS} = 16 V, I_D = 8 A[3,4,5]	—	3	
		All	V_{GS} = 10 V, I_D = 30 A[2]	—	3	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 1 x 10^{12} n°/cm^2, $V_{GS} = V_{DS}$ = 0.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 160 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRK6766M,D,R and H, respectively.

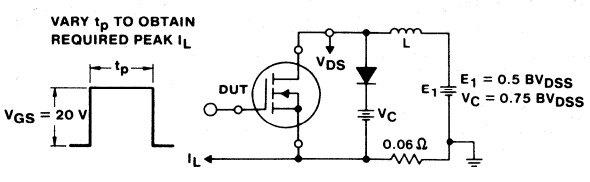


Fig. 1 - Clamped inductive test circuit.

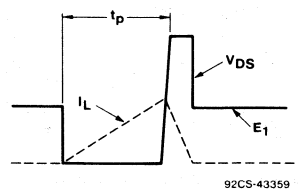


Fig. 2 - Clamped inductive waveforms.

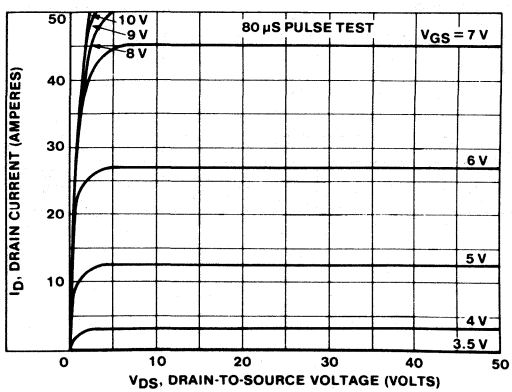


Fig. 3 - Typical output characteristics.

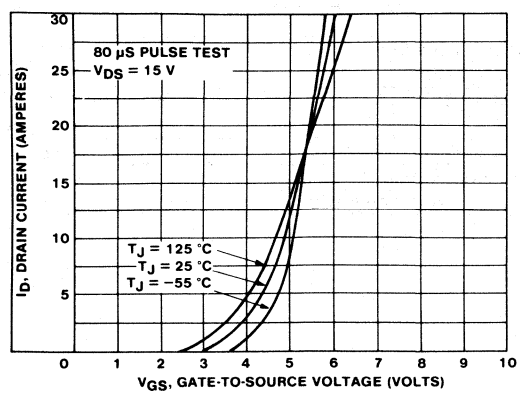


Fig. 4 - Typical transfer characteristics.

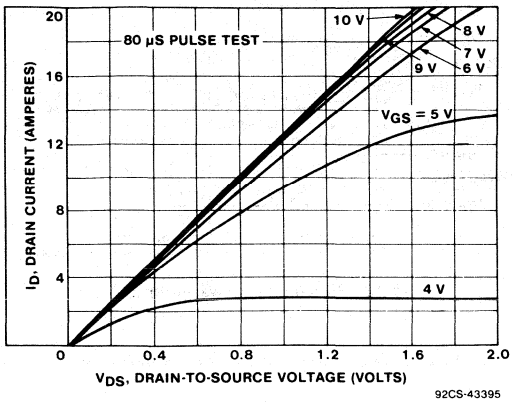


Fig. 5 - Typical saturation characteristics.

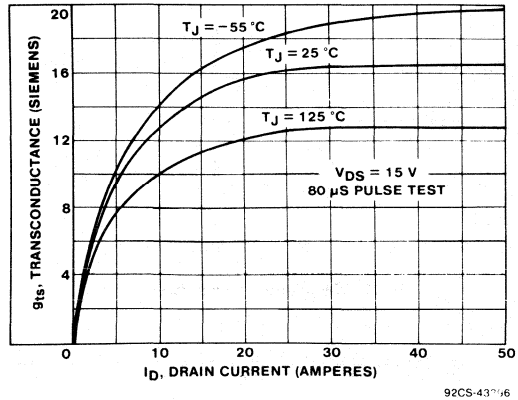


Fig. 6 - Typical transconductance vs. drain current.

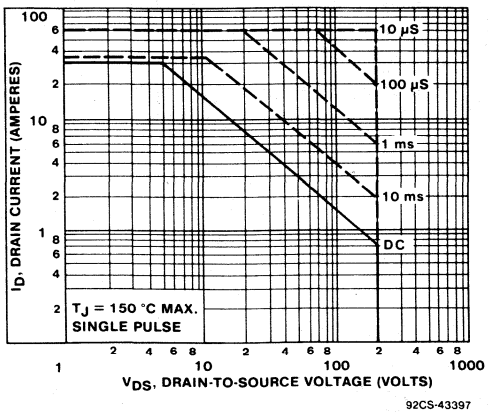


Fig. 7 - Maximum safe operating area.

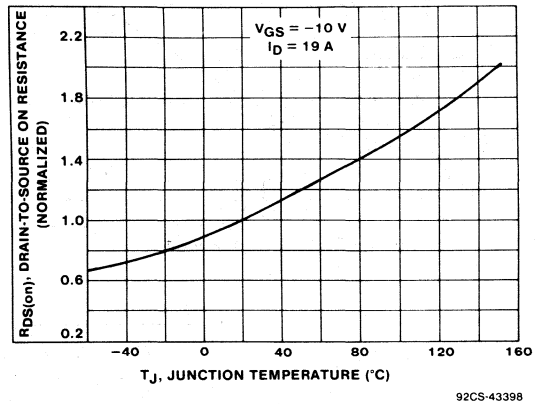


Fig. 8 - Normalized typical on-resistance vs. temperature.

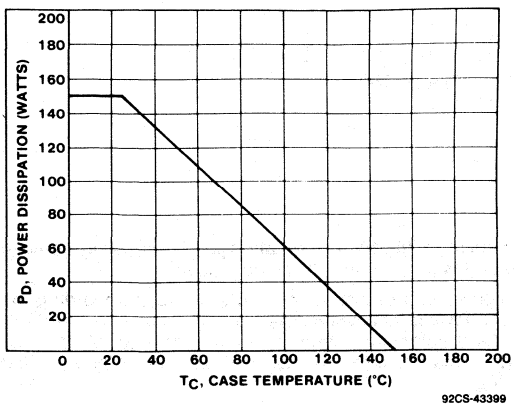


Fig. 9 - Power vs. temperature derating curve.

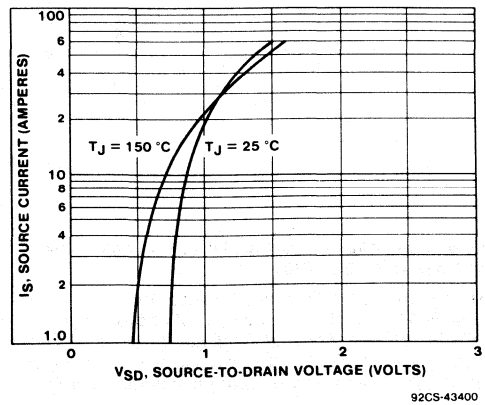


Fig. 10 - Typical body-drain diode forward voltage.

FRK6766M, FRK6766D, FRK6766R, FRK6766H

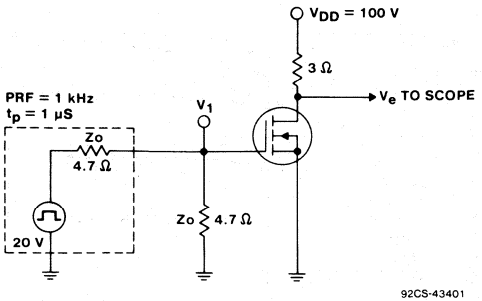


Fig. 11 - Switching time test circuit.

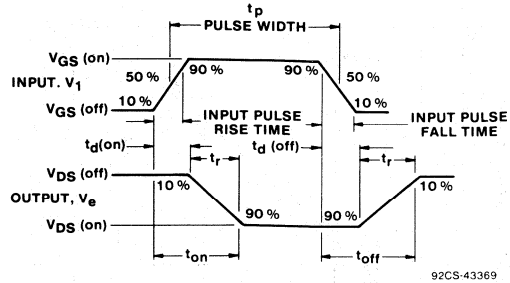


Fig. 12 - Switching time waveforms.

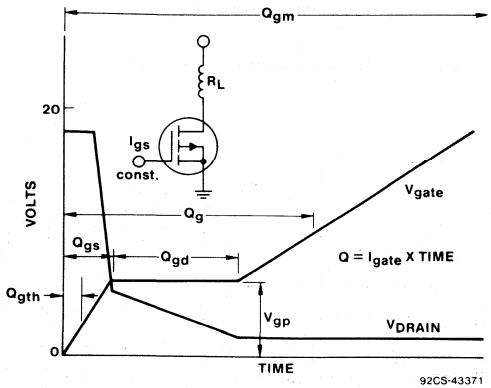


Fig. 13 - Gate charge waveforms.

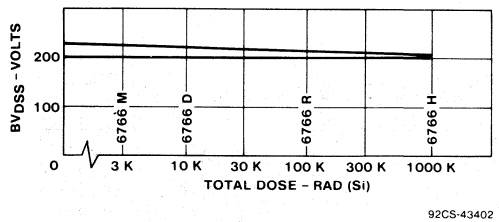


Fig. 14 - BV_{DSS} vs. dose.

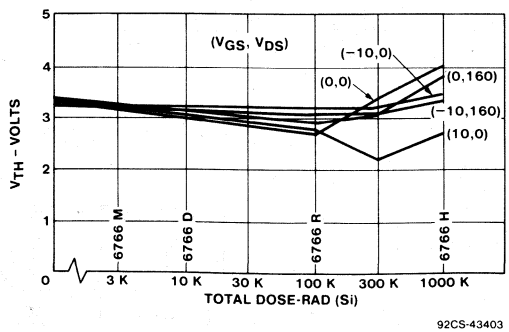


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Figs. 16 through 20 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of I_D = 5 A/div. and horizontal sensitivity of ½V/div. The five FRK6766H devices were biased as noted in diagram (e) of each figure during irradiation and removed for testing at 0K, 100K, 300K and 1000K rads (Si) as noted in diagrams (a) through (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log I_D vs. V_{as}. Vertical scale is I_D from 1E-11 to 1A. Equipment compliance limits data to 1E-1A max. Drain voltage is set at +5 volts, but I_D is relatively independent of V_{DS}.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = -10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

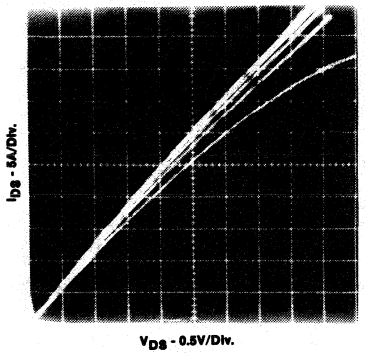


Fig. 16(a) - Typical output characteristics at pre-radiation.

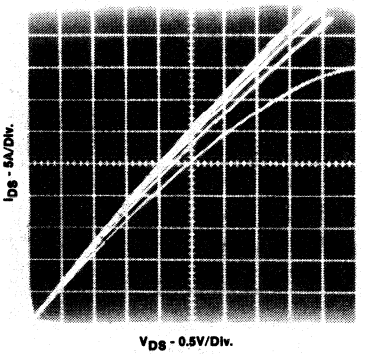


Fig. 16(b) - Typical output characteristics at 100K rads (Si).

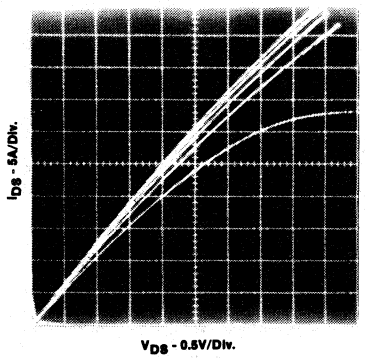


Fig. 16(c) - Typical output characteristics at 300K rads (Si).

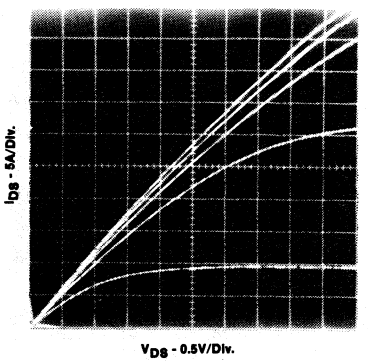


Fig. 16(d) - Typical output characteristics at 1M rad (Si).

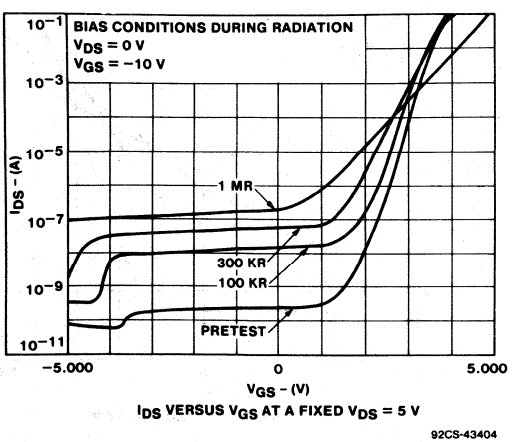


Fig. 16(e) - Drain source current as a function of gate bias.

FRK6766M, FRK6766D, FRK6766R, FRK6766H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

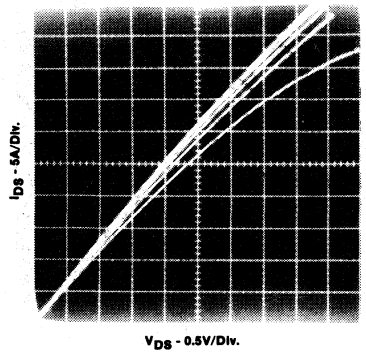


Fig. 17(a) - Typical output characteristics at pre-radiation.

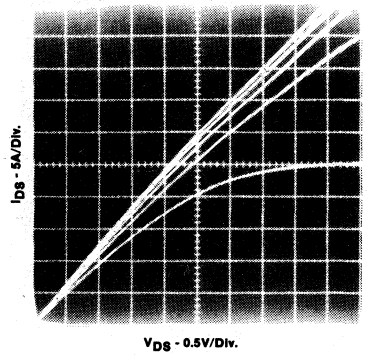


Fig. 17(b) - Typical output characteristics at 100K rads (Si).

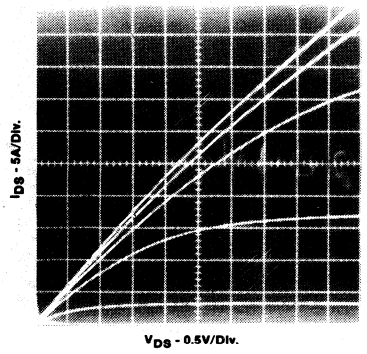


Fig. 17(c) - Typical output characteristics at 300K rads (Si).

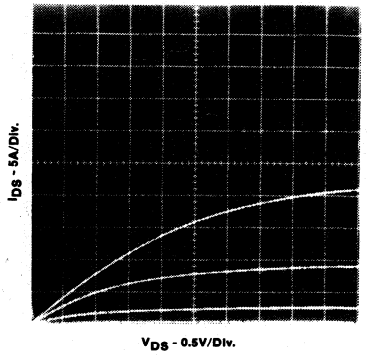


Fig. 17(d) - Typical output characteristics at 1M rad (Si).

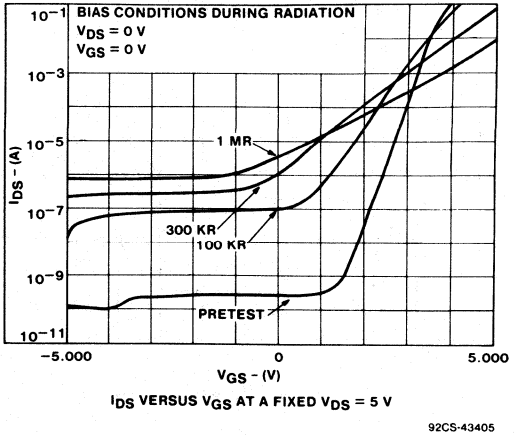


Fig. 17(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = +10 V and V_{DS} = 0 V.
2. Curves are for V_{GC} = 8 V, 10 V, 12 V, 14 V and 16 V.

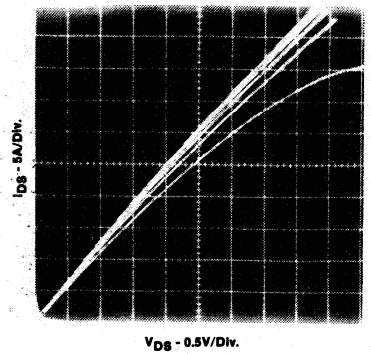


Fig. 18(a) - Typical output characteristics at pre-radiation.

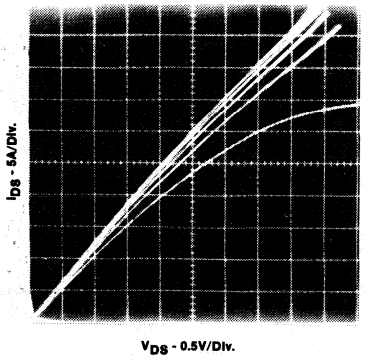


Fig. 18(b) - Typical output characteristics at 100K rads (Si).

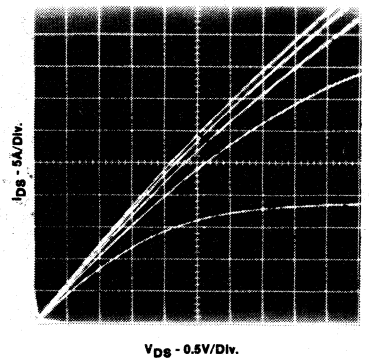


Fig. 18(c) - Typical output characteristics at 300K rads (Si).

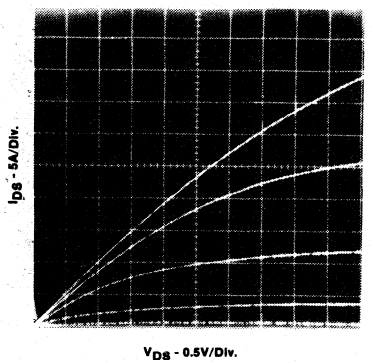
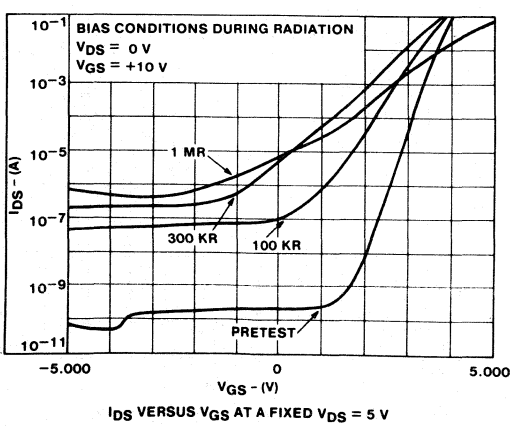


Fig. 18(d) - Typical output characteristics at 1M rad (Si).



IDS VERSUS VGS AT A FIXED VDS = 5 V

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Fig. 18(e) - Drain source current as a function of gate bias.

FRK6766M, FRK6766D, FRK6766R, FRK6766H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 160 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

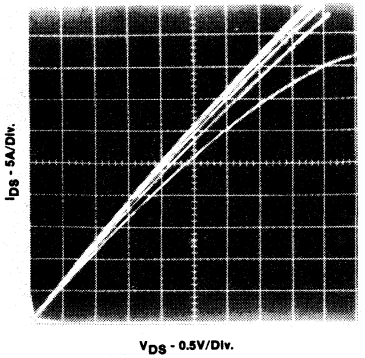


Fig. 19(a) - Typical output characteristics at pre-radiation.

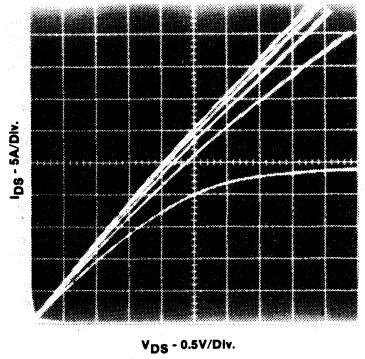


Fig. 19(b) - Typical output characteristics at 100K rads (Si).

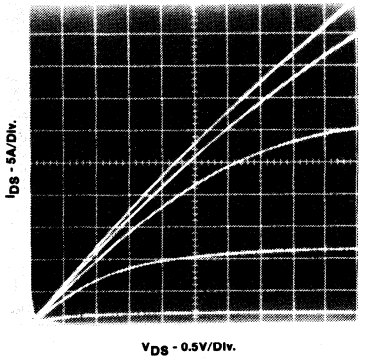


Fig. 19(c) - Typical output characteristics at 300K rads (Si).

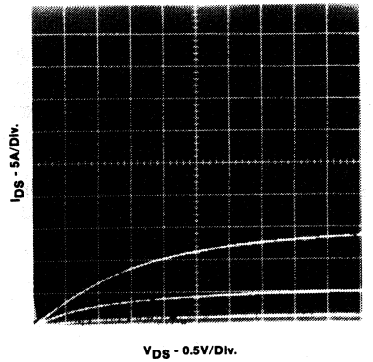
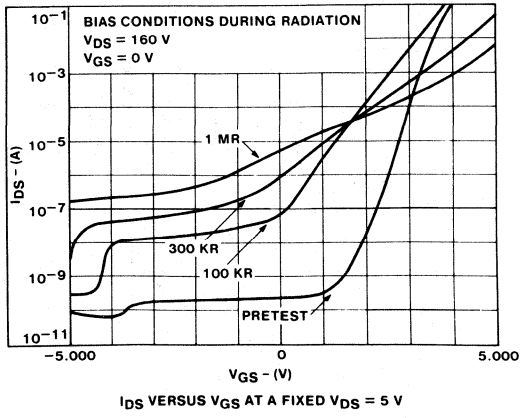


Fig. 19(d) - Typical output characteristics at 1M rad (Si).



I_{DS} VERSUS V_{GS} AT A FIXED V_{DS} = 5 V

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Fig. 19(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = −10 V and V_{DS} = 160 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

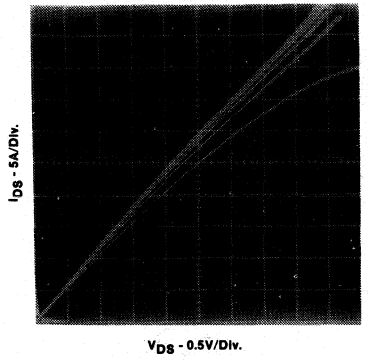


Fig. 20(a) - Typical output characteristics at pre-radiation.

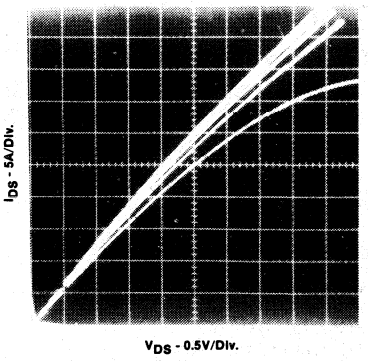


Fig. 20(b) - Typical output characteristics at 100K rads (Si).

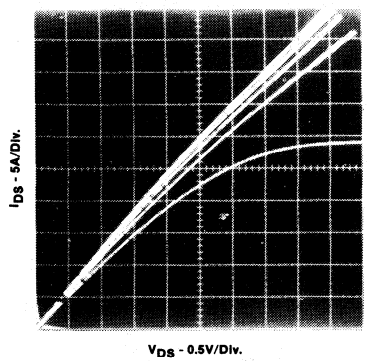


Fig. 20(c) - Typical output characteristics at 300K rads (Si).

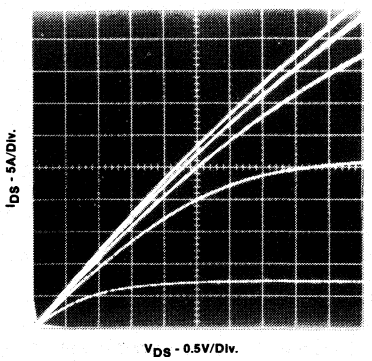


Fig. 20(d) - Typical output characteristics at 1M rad (Si).

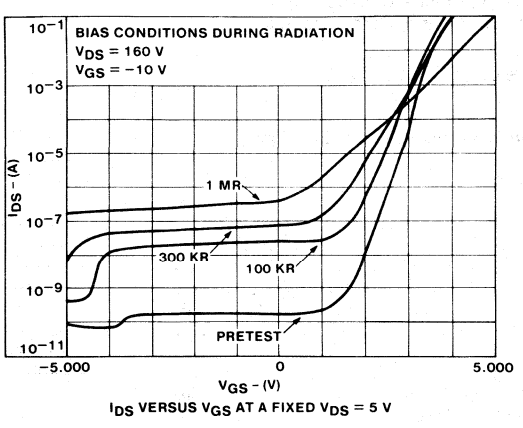


Fig. 20(e) - Drain source current as a function of gate bias.

FRL6796M, FRL6796D, FRL6796R, FRL6796H

File Number **2320**

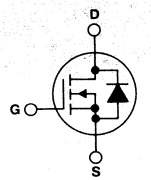
Radiation-Hardened N-Channel Power MOSFETs

Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

8 A, 100 V
$r_{DS(on)}$ = 0.18 Ω

Features:
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *FRL6796M rated to 3k rads*
- *FRL6796D rated to 10K rads*
- *FRL6796R rated to 100K rads*
- *FRL6796H rated to 1000K rads*

TERMINAL DIAGRAM



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N-CHANNEL ENHANCEMENT MODE

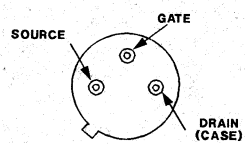
The FRL6796M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRL6796 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRL6796 family is supplied in the JEDEC TO-205AF metal package. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

The FRL6796 was formerly developmental type TA9799.

TERMINAL DESIGNATION



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DS}	100	V
DRAIN-GATE VOLTAGE (R_{gs} = 20 KΩ)	V_{DGR}	100	V
CONTINUOUS DRAIN CURRENT:	I_D		
At T_c = 25°C		8	A
At T_c = 100°C		5	A
PULSED DRAIN CURRENT	I_{DM}	30	A
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
POWER DISSIPATION:	P_T		
At T_c = 25°C		25 (See Fig. 9)	W
At T_c = 100°C		10 (See Fig. 9)	W
Derate linearly above T_c = 25°C		0.2 (See Fig. 9)	W/°C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH	I_{LM}	32 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering):	T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.		300	°C

FRL6796M, FRL6796D, FRL6796R, FRL6796H

PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	—	25	μA
		V_{DS} = 80 V, V_{GS} = 0, T_c = 125°C	—	—	250	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 8 A	—	—	1.56	V
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	—	0.14	0.18	Ω
		V_{GS} = 10 V, I_D = 5 A, T_c = 125°C	—	—	0.35	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 5 A	—	5.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	900	—	pF
Output Capacitance	C_{oss}		—	300	—	
Reverse-Transfer Capacitance	C_{rss}		—	100	—	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 5 A, Z_o = 15 Ω (See Figs. 11 & 12)	—	—	30	ns
Rise Time	t_r		—	—	75	
Turn-Off Delay Time	$t_{d(off)}$		—	—	40	
Fall Time	t_f		—	—	45	
Gate-Charge Threshold	Q_{gth}	V_{DD} = 50 V, I_D = 8 A Method 3471 from Mil-Std-750, Cond. A (See Fig. 13)	1.2	1.8	2.5	nC
Gate Charge	Q_g		13	25	40	
Gate-Charge Total	Q_{gm}		24	45	80	
Gate-Plateau Voltage	V_{gp}		5.2	7.5	10.2	V
Gate-Source Charge	Q_{gs}		2.1	6	9	nC
Gate-Drain ("Miller") Charge	Q_{gd}		6.7	11	21	

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Junction-to-Case	$R_{\theta JC}$		—	—	5	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	175	

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Source current (Body Diode)	I_s		—	—	8	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	30	
Diode Forward Voltage[1]	V_{SD}	T_c = 25°C, I_F = 8 A, V_{GS} = 0	0.75	—	1.5	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	150	—	ns
Reverse Recovered Charge	Q_{RR}		—	—	—	μC

FRL6796M, FRL6796D, FRL6796R, FRL6796H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = 1 mA[2,3,4,5] (See Fig. 14)	100	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRL6796M	$V_{GS} = V_{DS}$, I_D = 1 mA[3,4,5] (See Fig. 15)	2	4	V
		FRL6796D		1.5	4.2	
		FRL6796R		1	4.5	
		FRL6796H		0.5	5	
		All	$V_{GS} = V_{DS}$, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRL6796M	V_{GS} = 0, V_{DS} = 80 V[3,4,5]	—	25	μA
		FRL6796D		—	30	
		FRL6796R		—	50	
		FRL6796H		—	100	
		All	V_{GS} = 0, V_{DS} = 80 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRL6796M	V_{GS} = 10 V, I_D = 5 A[3,4,5]	—	0.18	Ω
		FRL6796D	V_{GS} = 10 V, I_D = 5 A[3,4,5]	—	0.18	
		FRL6796R	V_{GS} = 12 V, I_D = 5 A[3,4,5]	—	0.20	
		FRL6796H	V_{GS} = 16 V, I_D = 4 A[3,4,5]	—	0.30	
		All	V_{GS} = 10 V, I_D = 5 A[2]	—	0.20	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRL6796M	V_{GS} = 10 V, I_D = 8 A[3,4,5]	—	1.6	V
		FRL6796D	V_{GS} = 10 V, I_D = 8 A[3,4,5]	—	1.6	
		FRL6796R	V_{GS} = 12 V, I_D = 8 A[3,4,5]	—	2	
		FRL6796H	V_{GS} = 16 V, I_D = 5 A[3,4,5]	—	3	
		All	V_{GS} = 10 V, I_D = 8 A[2]	—	1.6	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 2 x 10^{12} n°/cm^2, $V_{GS} = V_{DS} = 0$.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 80 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRL6796M, D, R, and H, respectively.

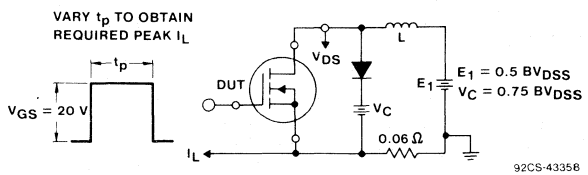


Fig. 1 - Clamped inductive test circuit.

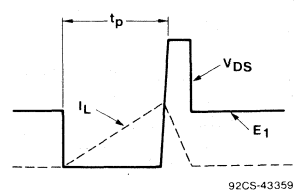


Fig. 2 - Clamped inductive waveforms.

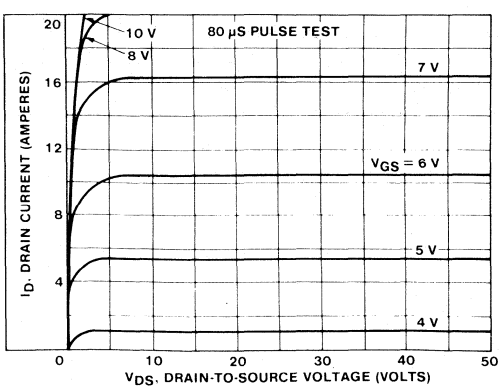


Fig. 3 - Typical output characteristics.

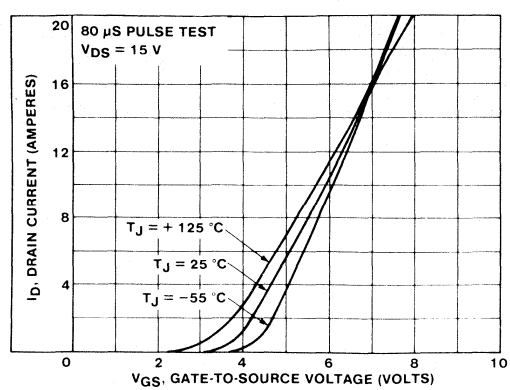


Fig. 4 - Typical transfer characteristics.

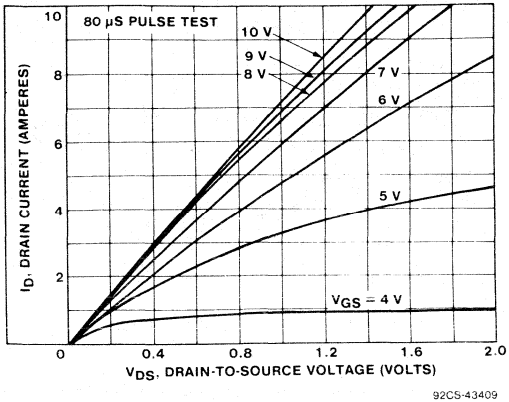


Fig. 5 - Typical saturation characteristics.

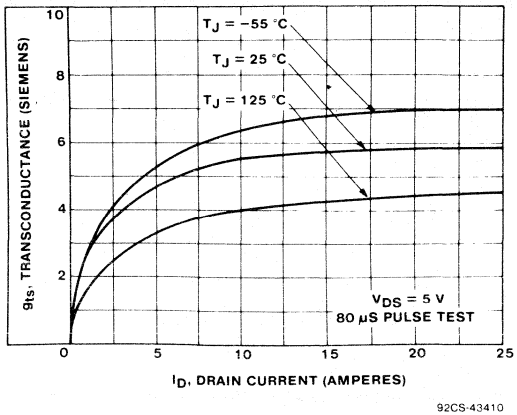


Fig. 6 - Typical transconductance vs. drain current.

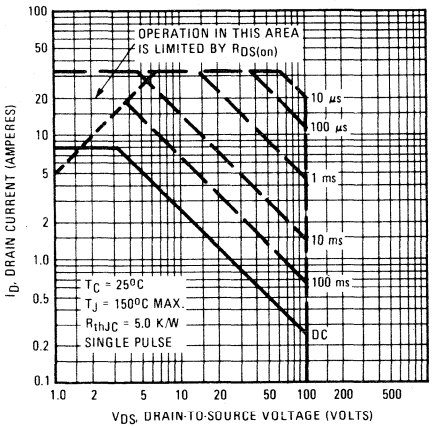


Fig. 7 - Maximum safe operating area.

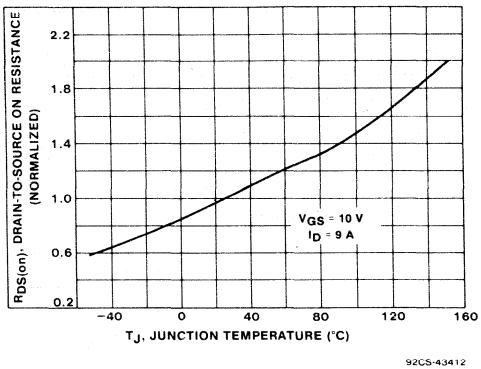


Fig. 8 - Normalized typical on-resistance vs. temperature.

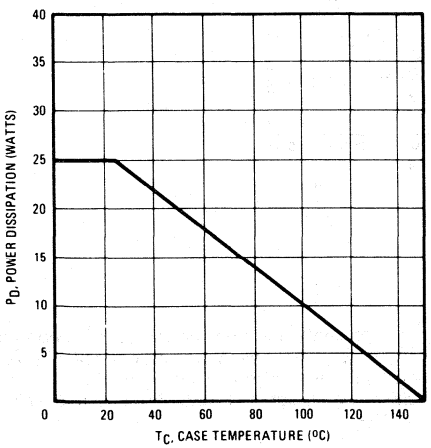


Fig. 9 - Power vs. temperature derating curve.

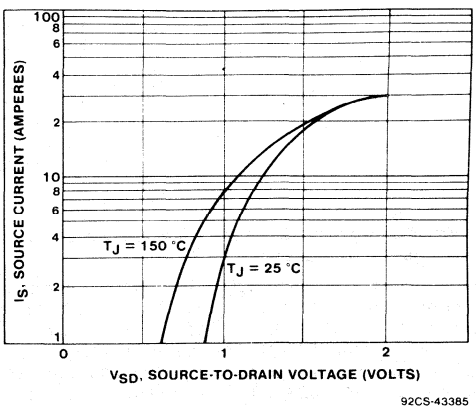


Fig. 10 - Typical body-drain diode forward voltage.

FRL6796M, FRL6796D, FRL6796R, FRL6796H

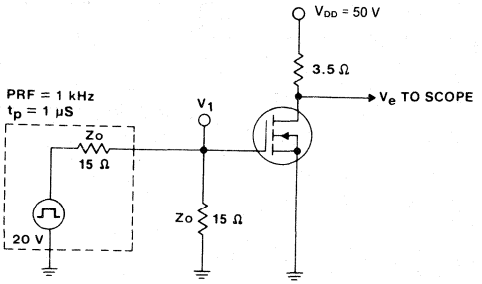


Fig. 11 - Switching time test circuit.

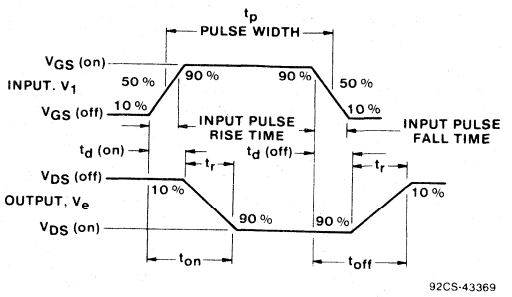


Fig. 12 - Switching time waveforms.

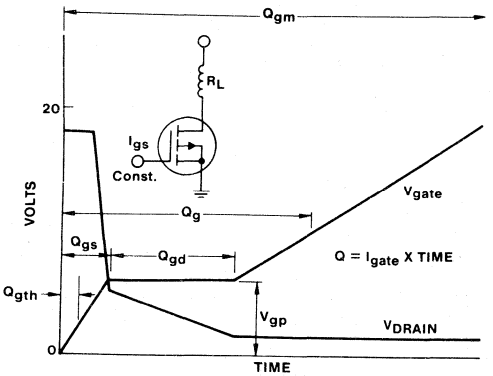


Fig. 13 - Gate change waveforms.

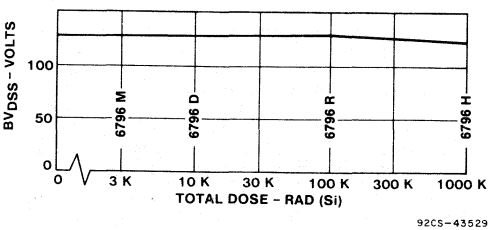


Fig. 14 - BV_{DSS} vs. dose.

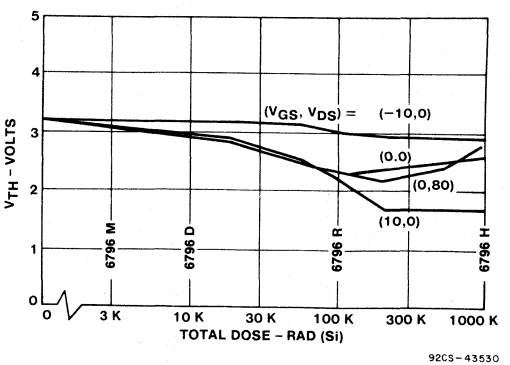


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Figs. 16 through 19 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of I_D = 2 A/div. and horizontal sensitivity of 1/2v/div. The four FRL6796H devices were biased as noted in diagram (e) of each figure during irradiation and removed for testing at 0K, 100K, 300K and 1000K rads (Si) as noted in diagrams (a) through (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log I_D vs. V_{GS}. Vertical scale is I_D from 1E-11 to 1 A. Equipment compliance limits data to 1E-1 A max. Drain voltage is set at +5 volts, but I_D is relatively independent of V_{DS}.

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = -10V and V_{DS} = 0V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

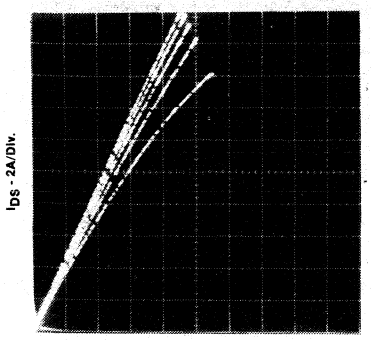


Fig. 16a - Typical output characteristics at pre-radiation.

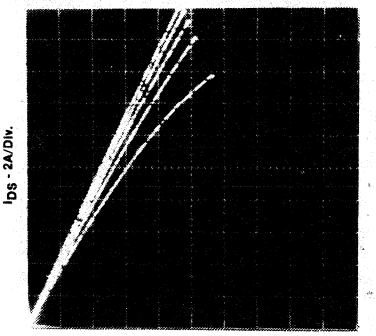


Fig. 16b - Typical output characteristic at 100K rads(Si).

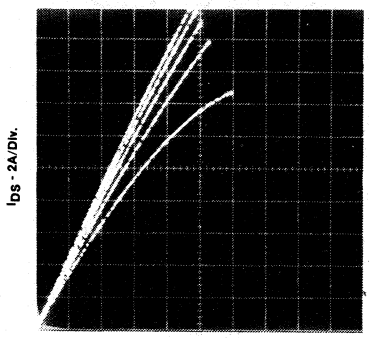


Fig. 16c - Typical output characteristic at 300K rads(Si).

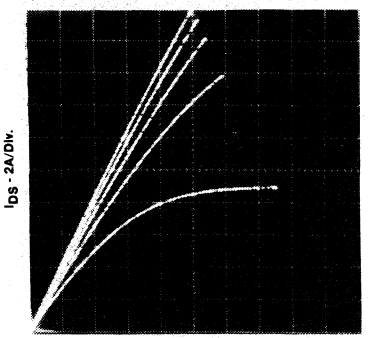


Fig. 16d - Typical output characteristic at 1M rad(Si).

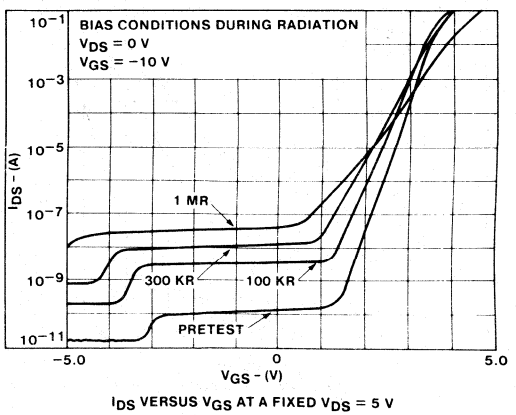


Fig. 16e - Drain source current as a function of gate bias.

FRL6796M, FRL6796D, FRL6796R, FRL6796H

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = +10V and V_{DS} = 0V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

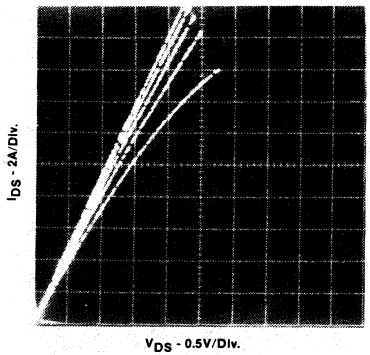


Fig. 17a - Typical output characteristics at pre-radiation.

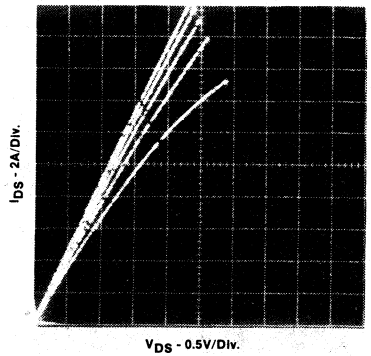


Fig. 17b - Typical output characteristic at 100K rads(Si).

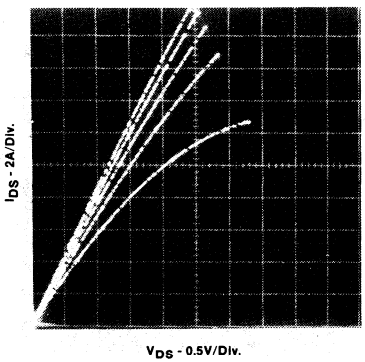


Fig. 17c - Typical output characteristic at 300K rads(Si).

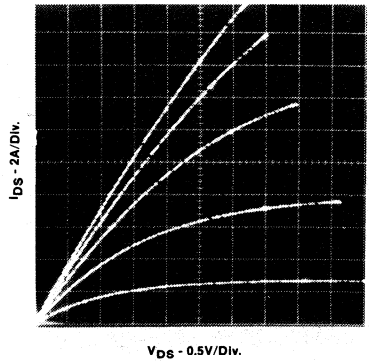


Fig. 17d - Typical output characteristic at 1M rad(Si).

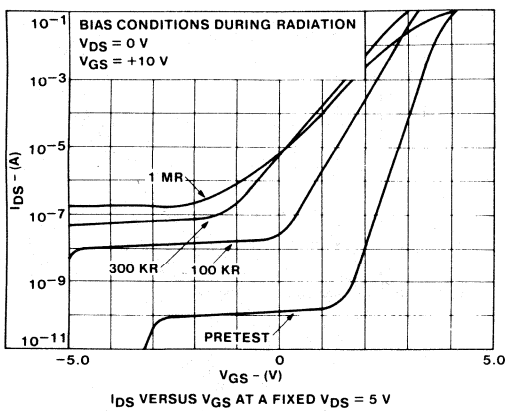


Fig. 17e - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = 0V and V_{DS} = 0V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

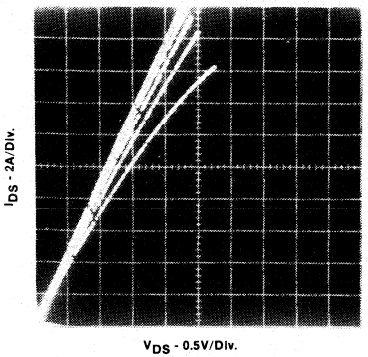


Fig. 18a - Typical output characteristics at pre-radiation.

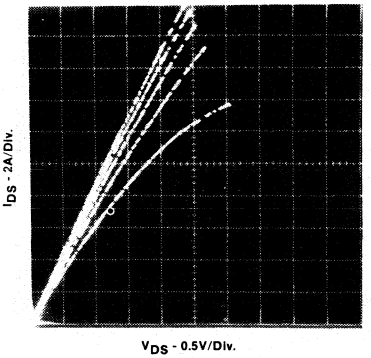


Fig. 18b - Typical output characteristic at 100K rads(Si).

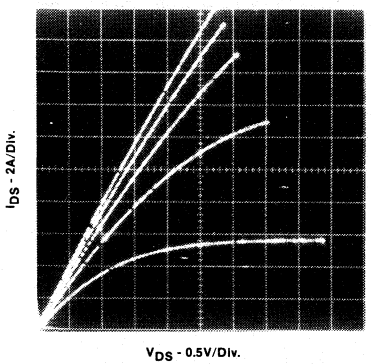


Fig. 18c - Typical output characteristic at 300K rads(Si).

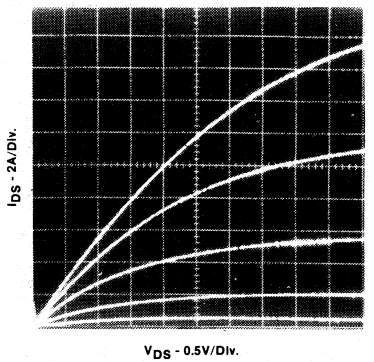


Fig. 18d - Typical output characteristic at 1M rad(Si).

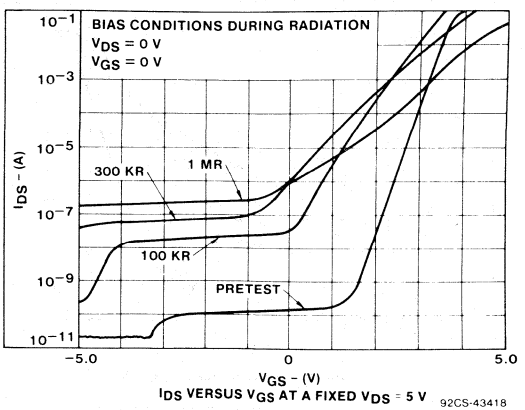


Fig. 18e - Drain source current as a function of gate bias.

FRL6796M, FRL6796D, FRL6796R, FRL6796H

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = 0V and V_{DS} = 80V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

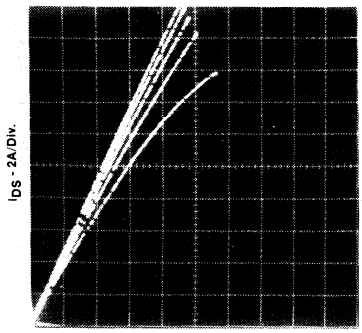


Fig. 19a - Typical output characteristics at pre-radiation.

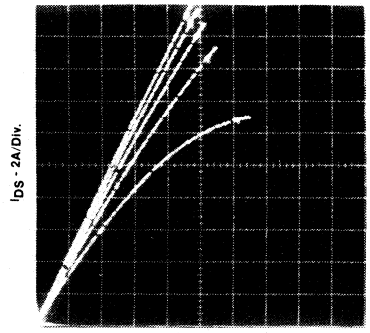


Fig. 19b - Typical output characteristic at 100K rads(Si).

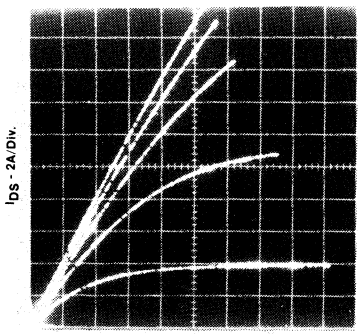


Fig. 19c - Typical output characteristic at 300K rads(Si).

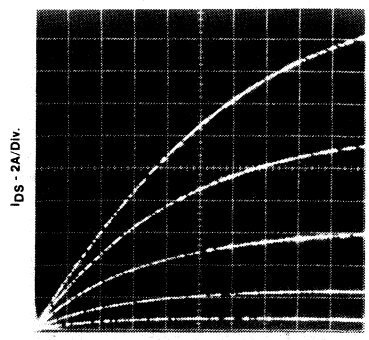
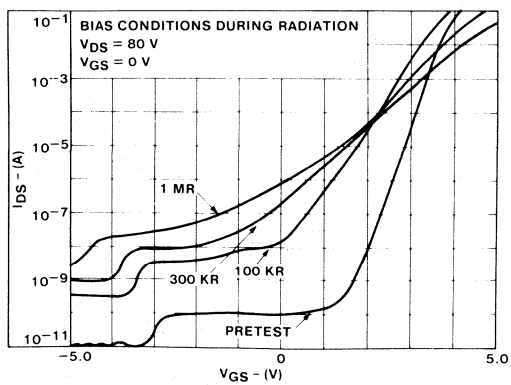


Fig. 19d - Typical output characteristic at 1M rad(Si).



IDS VERSUS VGS AT A FIXED VDS = 5 V

92CS-43419

Fig. 19e - Drain source current as a function of gate bias.

File Number **2321**

FRL6798M, FRL6798D, FRL6798R, FRL6798H

Radiation-Hardened N-Channel Power MOSFETs

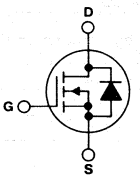
Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

5.5 A, 200 V
$r_{DS(on)}$ = 0.4 Ω

Features:

- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *FRL6798M rated to 3k rads*
- *FRL6798D rated to 10K rads*
- *FRL6798R rated to 100K rads*
- *FRL6798H rated to 1000K rads*

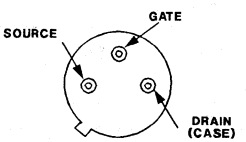
TERMINAL DIAGRAM



92CS-43357

N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-205AF

The FRL6798M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRL6798 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRL6798 family is supplied in the JEDEC TO-205AF metal package. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

The FRL6798 was formerly developmental type TA9799.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c = 25° C):*

DRAIN-SOURCE VOLTAGE ..... V_{DS}	200	V
DRAIN-GATE VOLTAGE (R_{gs} = 20 KΩ) ..... V_{DGR}	200	V
CONTINUOUS DRAIN CURRENT: ..... I_D		
At T_c = 25° C	5.5	A
At T_c = 100° C	3.5	A
PULSED DRAIN CURRENT ..... I_{DM}	15	A
GATE-SOURCE VOLTAGE ..... V_{GS}	±20	V
POWER DISSIPATION: ..... P_T		
At T_C = 25° C	25 (See Fig. 9)	W
At T_C = 100° C	10 (See Fig. 9)	W
Derate linearly above T_C = 25° C	0.2 (See Fig. 9)	W/° C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH ..... I_{LM}	22 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering): ..... T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.	300	°C

FRL6798M, FRL6798D, FRL6798R, FRL6798H

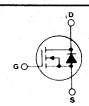
PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA	200	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	—	25	μA
		V_{DS} = 160 V, V_{GS} = 0, T_c = 125°C	—	—	250	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 5.5 A	—	—	2.3	V
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.5 A	—	—	0.4	Ω
		V_{GS} = 10 V, I_D = 3.5 A, T_c = 125°C	—	—	0.75	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5 V, I_D = 3.5 A	—	4.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	900	—	pF
Output Capacitance	C_{oss}		—	250	—	
Reverse-Transfer Capacitance	C_{rss}		—	80	—	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 3.5 A, Z_o = 15 Ω (See Figs. 11 & 12)	—	—	30	ns
Rise Time	t_r		—	—	50	
Turn-Off Delay Time	$t_{d(off)}$		—	—	50	
Fall Time	t_f		—	—	40	
Gate-Charge Threshold	Q_{gth}	V_{DD} = 100 V, I_D = 5.5 A Method 3471 from Mil-Std-750, Cond. A (See Fig. 13)	1.2	1.8	3	nC
Gate Charge	Q_g		15	24	40	
Gate-Charge Total	Q_{gm}		26	48	80	
Gate-Plateau Voltage	V_{gp}		4.7	6	9.7	V
Gate-Source Charge	Q_{gs}		2	6	9	nC
Gate-Drain ("Miller") Charge	Q_{gd}		8.3	12	20	

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Junction-to-Case	$R_{\theta JC}$		—	—	5	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	175	

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Source current (Body Diode)	I_s	MOSFET symbol showing the integral reverse P-N junction rectifier 	—	—	5.5	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	15	
Diode Forward Voltage[1]	V_{SD}	T_c = 25°C, I_F = 5.5 A, V_{GS} = 0	0.7	—	1.4	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	250	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

FRL6798M, FRL6798D, FRL6798R, FRL6798H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = 1 mA[2,3,4,5] (See Fig. 14)	180	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRL6798M	$V_{GS} = V_{DS}$, I_D = 1 mA[3,4,5] (See Fig. 15)	2	4	V
		FRL6798D		1.5	4.2	
		FRL6798R		1	4.5	
		FRL6798H		0.5	5	
		All	$V_{GS} = V_{DS}$, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRL6798M	V_{GS} = 0, V_{DS} = 160 V[3,4,5]	—	25	μA
		FRL6798D		—	30	
		FRL6798R		—	50	
		FRL6798H		—	100	
		All	V_{GS} = 0, V_{DS} = 160 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRL6798M	V_{GS} = 10 V, I_D = 3.5 A[3,4,5]	—	0.40	Ω
		FRL6798D	V_{GS} = 10 V, I_D = 3.5A[3,4,5]	—	0.40	
		FRL6798R	V_{GS} = 12 V, I_D = 3.5A[3,4,5]	—	0.50	
		FRL6798H	V_{GS} = 16 V, I_D = 3 A[3,4,5]	—	0.75	
		All	V_{GS} = 10 V, I_D = 3.5 A[2]	—	0.45	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRL6798M	V_{GS} = 10 V, I_D = 5.5 A[3,4,5]	—	2.3	V
		FRL6798D	V_{GS} = 10 V, I_D = 5.5 A[3,4,5]	—	2.3	
		FRL6798R	V_{GS} = 12 V, I_D = 5.5 A[3,4,5]	—	2.3	
		FRL6798H	V_{GS} = 16 V, I_D = 4 A[3,4,5]	—	3.6	
		All	V_{GS} = 10 V, I_D = 5.5 A[2]	—	2.3	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 2 x 10^{12} n°/cm^2, $V_{GS} = V_{DS} = 0$.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 160 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRL6798M, D, R, and H, respectively.

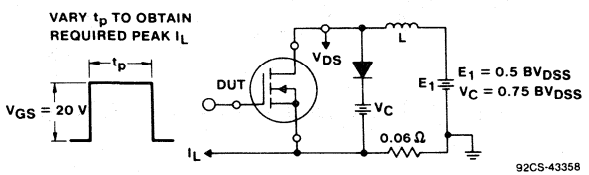


Fig. 1 - Clamped inductive test circuit.

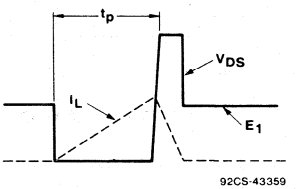


Fig. 2 - Clamped inductive waveforms.

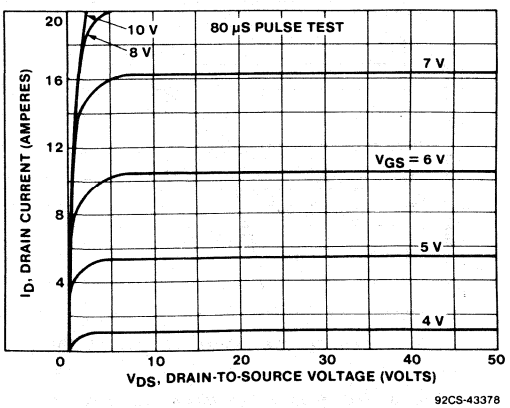


Fig. 3 - Typical output characteristics.

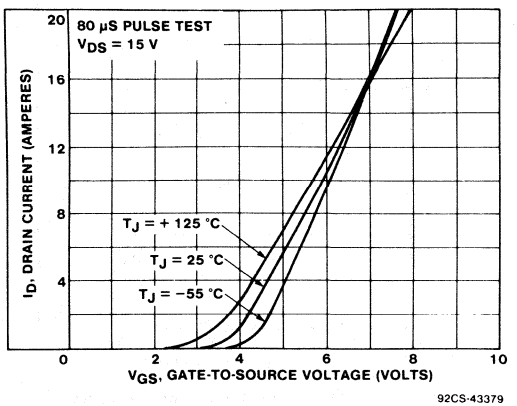


Fig. 4 - Typical transfer characteristics.

FRL6798M, FRL6798D, FRL6798R, FRL6798H

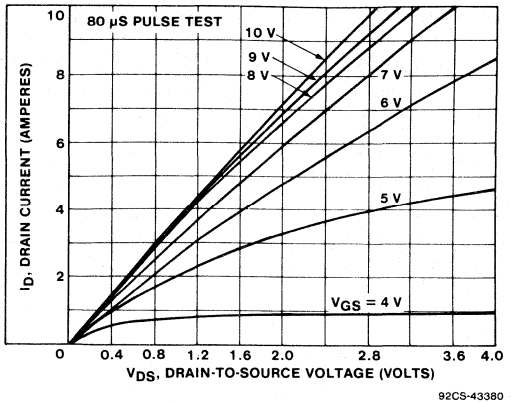


Fig. 5 - Typical saturation characteristics.

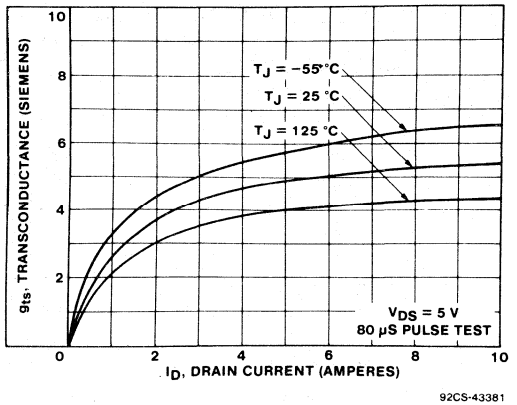


Fig. 6 - Typical transconductance vs. drain current.

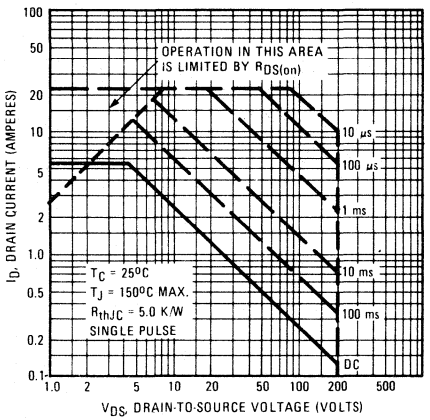


Fig. 7 - Maximum safe operating area.

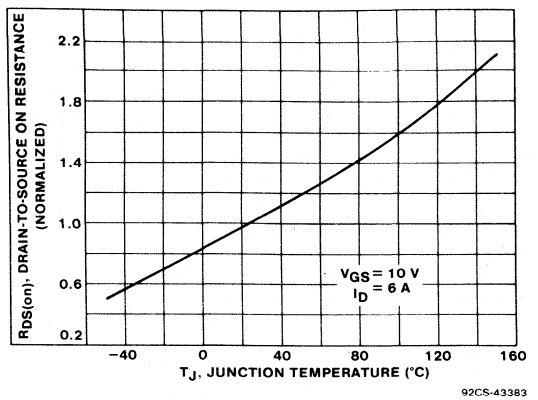


Fig. 8 - Normalized typical on-resistance vs. temperature.

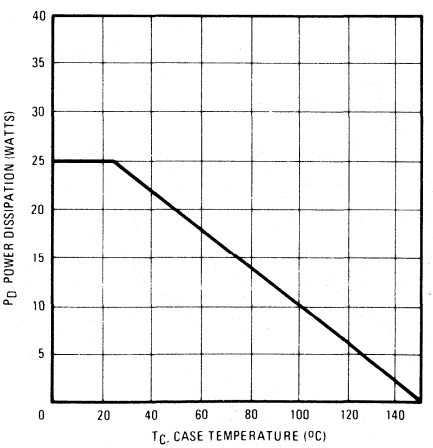


Fig. 9 - Power vs. temperature derating curve.

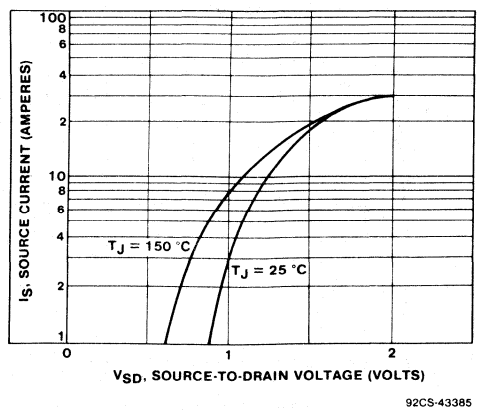


Fig. 10 - Typical body-drain diode forward voltage.

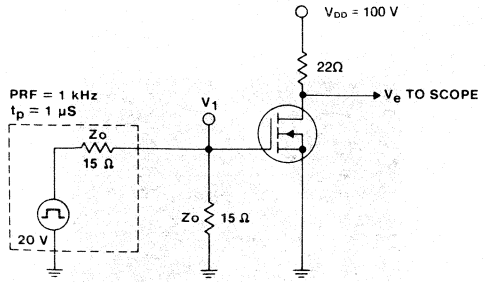


Fig. 11 - Switching time test circuit.

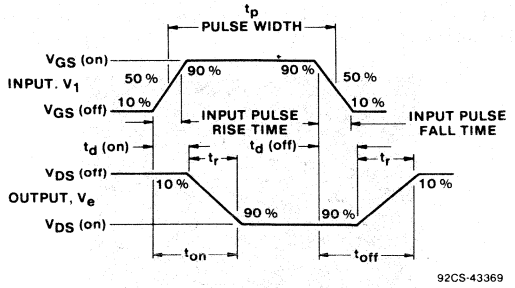


Fig. 12 - Switching time waveforms.

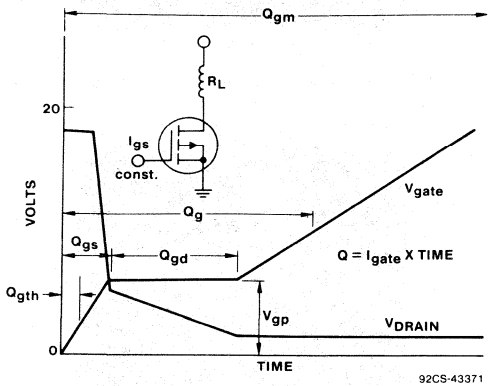


Fig. 13 - Gate charge waveforms.

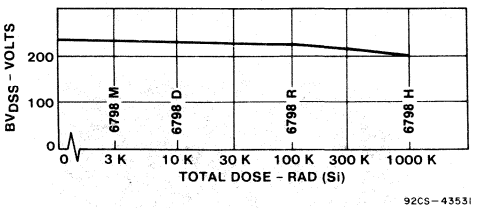


Fig. 14 - BV_{DSS} vs. dose.

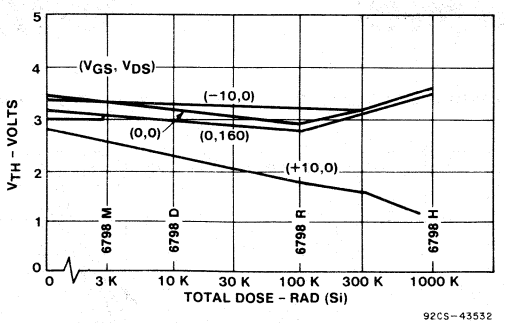


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Figs. 16 through 19 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of I_D = 1 A/div. and horizontal sensitivity of ½ V/div. The four FRL6798H devices were biased as noted in diagram (e) of each figure during irradiation and removed for testing at 0K, 100K, 300K and 1000K rads (Si) as noted in diagrams (a) through (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log I_D vs. V_{GS}. Vertical scale is I_D from 1E-11 to 1A. Equipment compliance limits data to 1E-1A max. Drain voltage is set at +5 volts, but I_D is relatively independent of V_{DS}.

FRL6798M, FRL6798D, FRL6798R, FRL6798H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = −10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

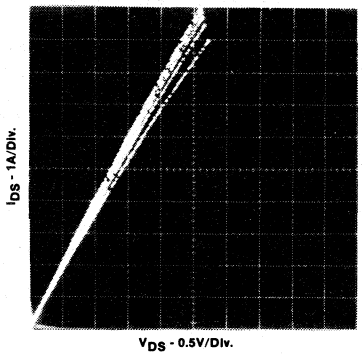


Fig. 16(a) - Typical output characteristics at pre-radiation.

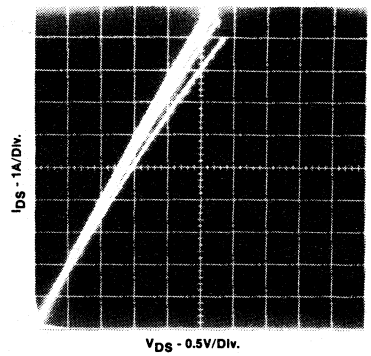


Fig. 16(b) - Typical output characteristics at 100K rads (Si).

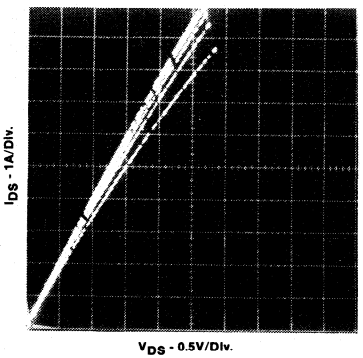


Fig. 16(c) - Typical output characteristics at 300K rads (Si).

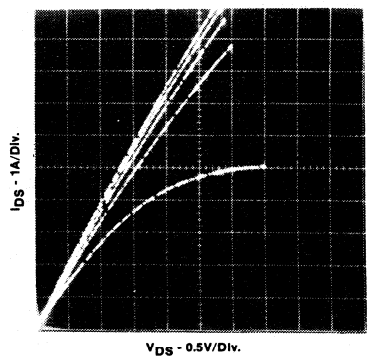


Fig. 16(d) - Typical output characteristics at 1M rad (Si).

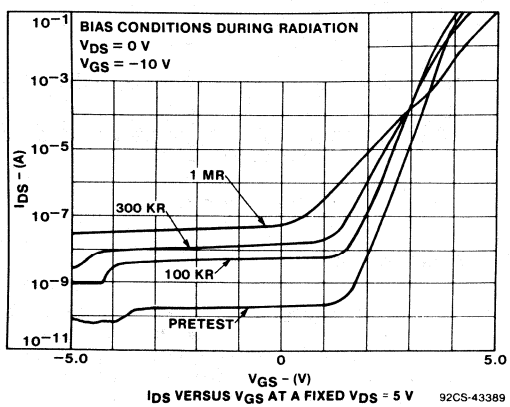


Fig. 16(e) - Drain source current as a function of gate bias.

FRL6798M, FRL6798D, FRL6798R, FRL6798H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = +10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

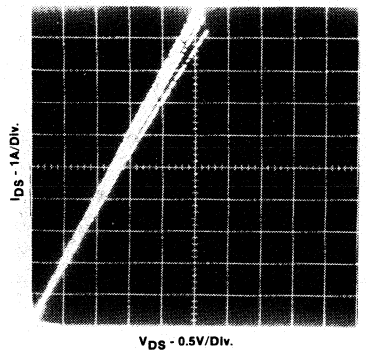


Fig. 17(a) - Typical output characteristics at pre-radiation.

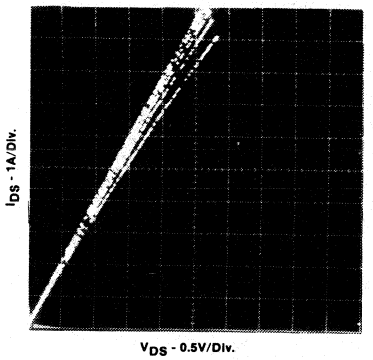


Fig. 17(b) - Typical output characteristics at 100K rads (Si).

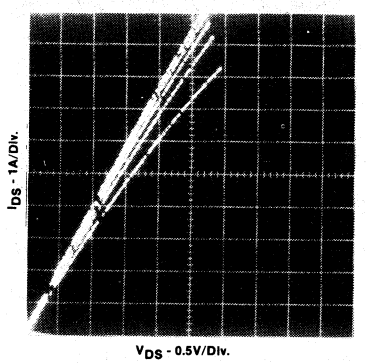


Fig. 17(c) - Typical output characteristics at 300K rads (Si).

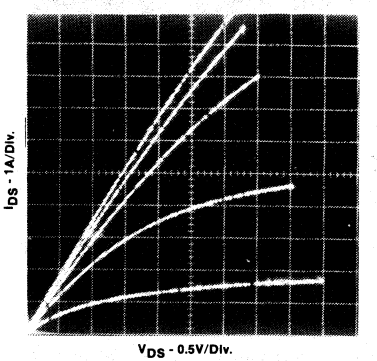


Fig. 17(d) - Typical output characteristics at 1M rad (Si).

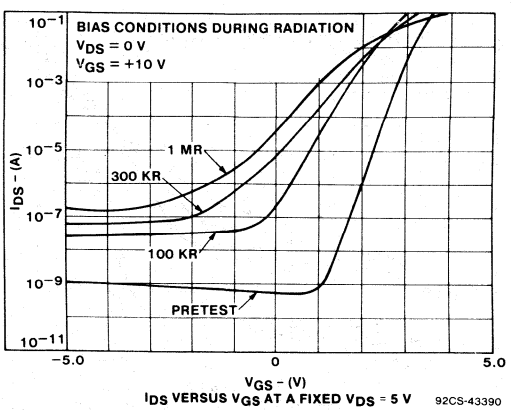


Fig. 17(e) - Drain source current as a function of gate bias.

FRL6798M, FRL6798D, FRL6798R, FRL6798H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

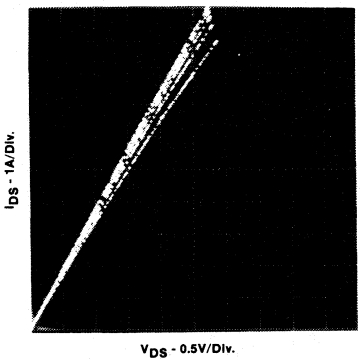


Fig. 18(a) - Typical output characteristics at pre-radiation.

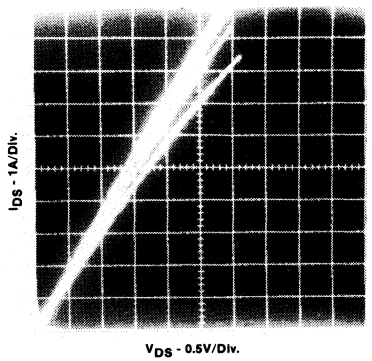


Fig. 18(b) - Typical output characteristics at 100K rads (Si).

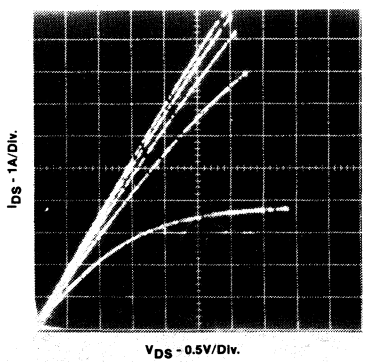


Fig. 18(c) - Typical output characteristics at 300K rads (Si).

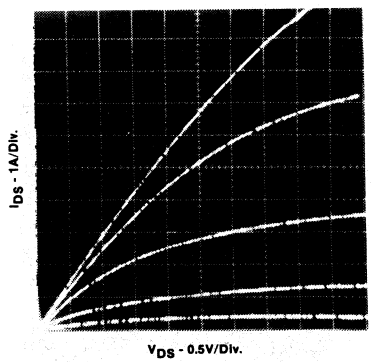


Fig. 18(d) - Typical output characteristics at 1M rad (Si).

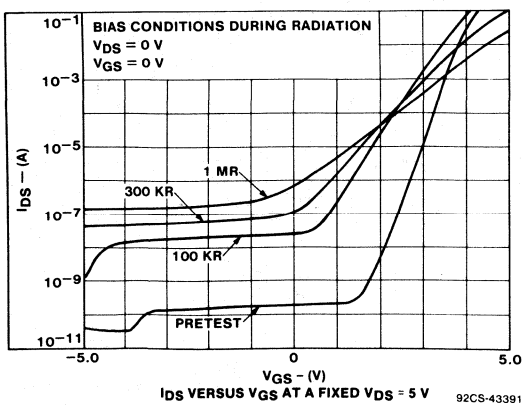


Fig. 18(e) - Drain source current as a function of gate bias.

FRL6798M, FRL6798D, FRL6798R, FRL6798H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 160 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

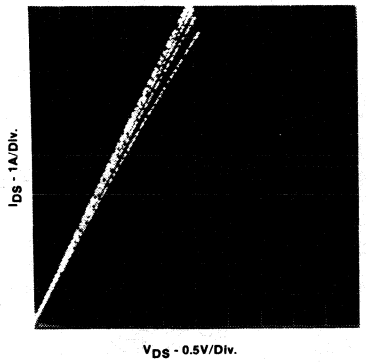


Fig. 19(a) - Typical output characteristics at pre-radiation.

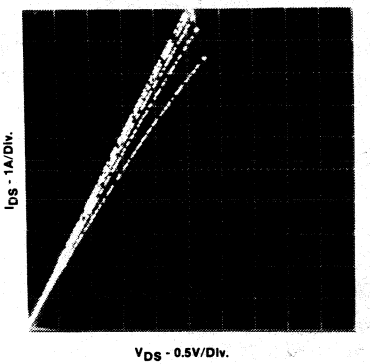


Fig. 19(b) - Typical output characteristics at 100K rads (Si).

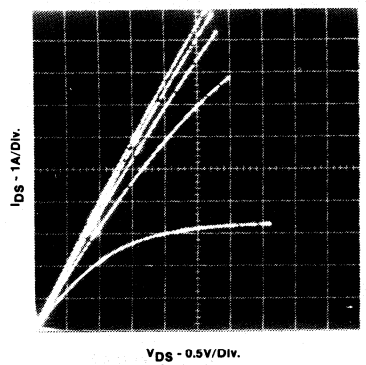


Fig. 19(c) - Typical output characteristics at 300K rads (Si).

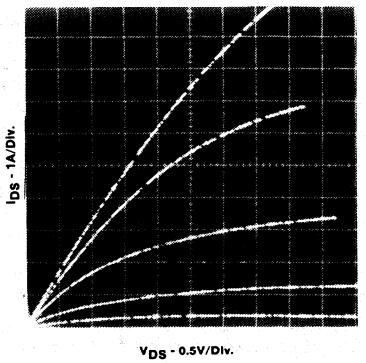


Fig. 19(d) - Typical output characteristics at 1M rad (Si).

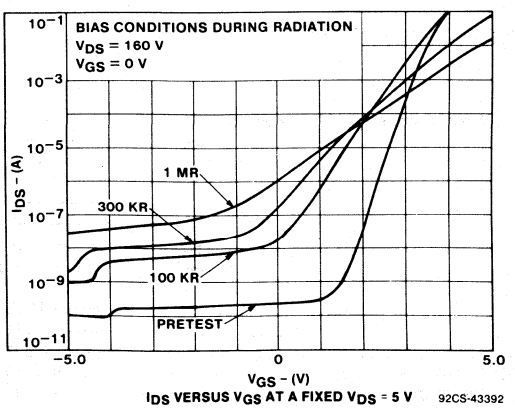


Fig. 19(e) - Drain source current as a function of gate bias.

FRM6756M, FRM6756D
FRM6756R, FRM6756H

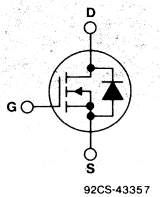
File Number **2173**

Radiation-Hardened N-Channel Power MOSFETs

Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

14 A, 100 V
$r_{DS}(on)$ = 0.18 Ω

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

Features:
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *FRM6756M rated to 3K rads*
- *FRM6756D rated to 10K rads*
- *FRM6756R rated to 100K rads*
- *FRM6756H rated to 1000K rads*

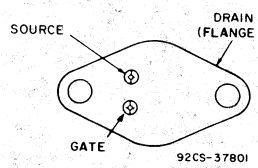
The FRM6756M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRM6756 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRM6756 family is supplied in the JEDEC TO-204AA steel package. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

The FRM6756 was formerly developmental type TA9797.

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

DRAIN-SOURCE VOLTAGE	V_{DS}	100	V
DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ)	V_{DGR}	100	V
CONTINUOUS DRAIN CURRENT:	I_D		
At T_C = 25°C		14	A
At T_C = 100°C		9	A
PULSED DRAIN CURRENT	I_{DM}	30	A
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
POWER DISSIPATION:	P_T		
At T_C = 25°C		75 (See Fig. 9)	W
At T_C = 100°C		30 (See Fig. 9)	W
Derate linearly above T_C = 25°C		0.6 (See Fig. 9)	W/°C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH	I_{LM}	30 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering):	T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.		300	°C

PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless other specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0, I_D = 1 mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	V
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	0.1	1	mA
		V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C	—	0.2	4	mA
Static Drain-Source On-State Voltage[1]	$V_{DS}(on)$	V_{GS} = 10 V, I_D = 14 A	—	—	2.52	V
Static Drain-Source On-State Resistance[1]	$r_{DS}(on)$	V_{GS} = 10 V, I_D = 9 A	—	0.14	0.18	Ω
		V_{GS} = 10 V, I_D = 9 A, T_C = 125°C	—	—	0.33	Ω
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 9 A	—	5.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	900	—	pF
Output Capacitance	C_{oss}		—	300	—	pF
Reverse-Transfer Capacitance	C_{rss}		—	100	—	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50V, I_D = 9 A, Z_O = 15 Ω (See Figs. 11 & 12)	—	—	30	ns
Rise Time	t_r		—	—	75	ns
Turn-Off Delay Time	$t_d(off)$		—	—	40	ns
Fall Time	t_f		—	—	45	ns
Gate-Charge Threshold	Q_{gth}	V_{DD} = 50V, I_D = 14A Method 3471 from Mil-Std-750,Cond.A (See Fig. 13)	1.1	1.8	3.5	nC
Gate Charge	Q_g		12	25	38	nC
Gate-Charge Total	Q_{gm}		23	45	62	nC
Gate-Plateau Voltage	V_{gp}		4.5	6	8.2	V
Gate-Source Charge	Q_{gs}		2.5	5	6.3	nC
Gate-Drain ("Miller") Charge	Q_{gd}		7	11	21	nC

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Junction-to-Case	$R_{\theta JC}$		—	—	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	—	0.1	—	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	30	°C/W

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Source Current (Body Diode)	I_S		—	—	14	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	30	A
Diode Forward Voltage[1]	V_{SD}	T_C = 25°C, I_F = 14 A, V_{GS} = 0	0.9	—	1.8	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	150	—	ns
Reverse Recovered Charge	Q_{RR}		—	—	—	μC

FRM6756M, FRM6756D, FRM6756R, FRM6756H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = 1 mA[2,3,4,5] (See Fig. 14)	100	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRM6756M	$V_{GS} = V_{DS}$, I_D = 1 mA[3,4,5] (See Fig. 15)	2	4	V
		FRM6756D		1.5	4.2	
		FRM6756R		1	4.5	
		FRM6756H		0.5	5	
		All	$V_{GS} = V_{DS}$, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRM6756M	V_{GS} = 0, V_{DS} = 80 V[3,4,5]	—	25	μA
		FRM6756D		—	30	
		FRM6756R		—	50	
		FRM6756H		—	100	
		All	V_{GS} = 0, V_{DS} = 80 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRM6756M	V_{GS} = 10 V, I_D = 9 A[3,4,5]	—	0.18	Ω
		FRM6756D	V_{GS} = 10 V, I_D = 9 A[3,4,5]	—	0.18	
		FRM6756R	V_{GS} = 12 V, I_D = 9 A[3,4,5]	—	0.20	
		FRM6756H	V_{GS} = 16 V, I_D = 6 A[3,4,5]	—	0.30	
		All	V_{GS} = 10 V, I_D = 9 A[2]	—	0.20	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRM6756M	V_{GS} = 10 V, I_D = 14 A[3,4,5]	—	2.52	V
		FRM6756D	V_{GS} = 10 V, I_D = 14 A[3,4,5]	—	2.52	
		FRM6756R	V_{GS} = 12 V, I_D = 14 A[3,4,5]	—	3	
		FRM6756H	V_{GS} = 16 V, I_D = 8 A[3,4,5]	—	4	
		All	V_{GS} = 10 V, I_D = 14 A[2]	—	2.7	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 2 x 10^{12} n°/cm^2, $V_{GS} = V_{DS}$ = 0.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 80 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRM6756M,D,R and H, respectively.

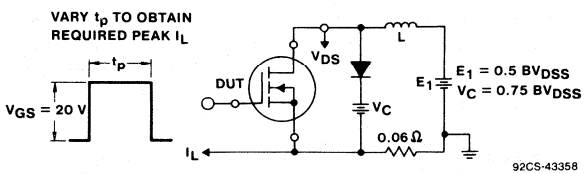


Fig. 1 - Clamped inductive test circuit.

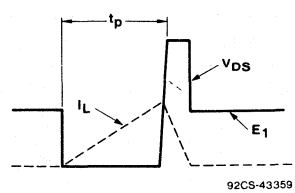


Fig. 2 - Clamped inductive waveforms.

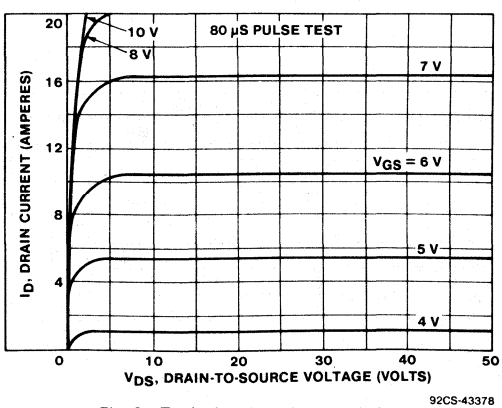


Fig. 3 - Typical output characteristics.

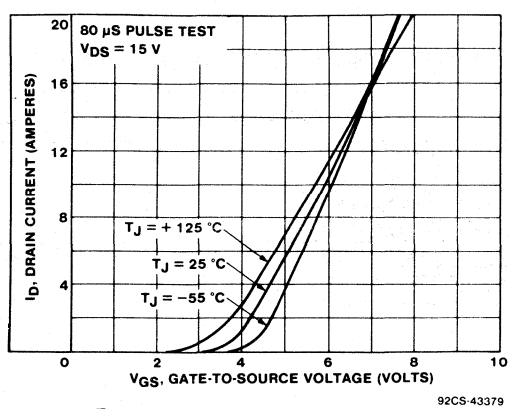


Fig. 4 - Typical transfer characteristics.

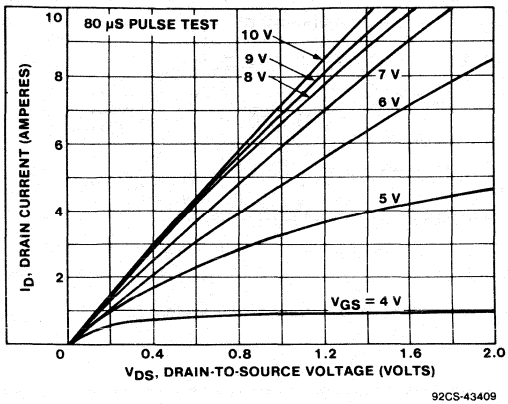


Fig. 5 - Typical saturation characteristics.

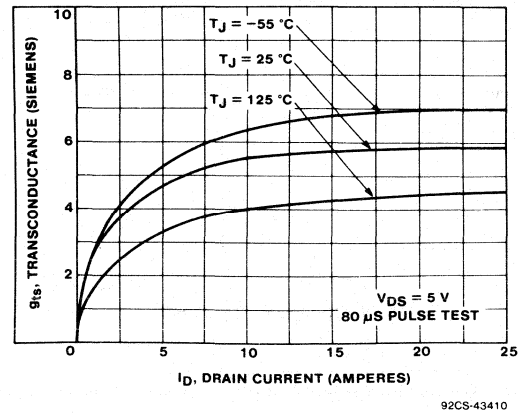


Fig. 6 - Typical transconductance vs. drain current.

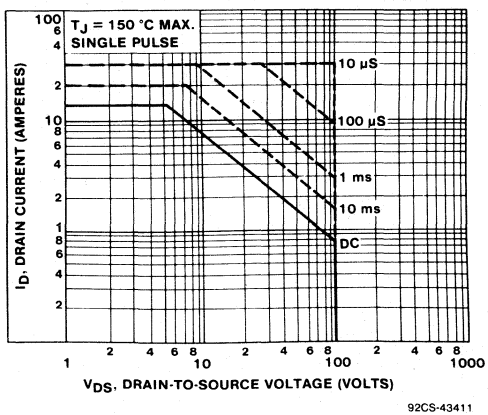


Fig. 7 - Maximum safe operating area.

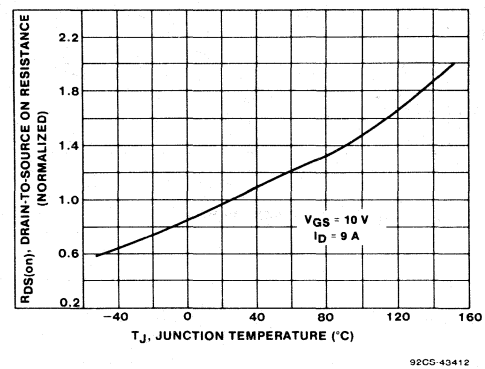


Fig. 8 - Normalized typical on-resistance vs. temperature.

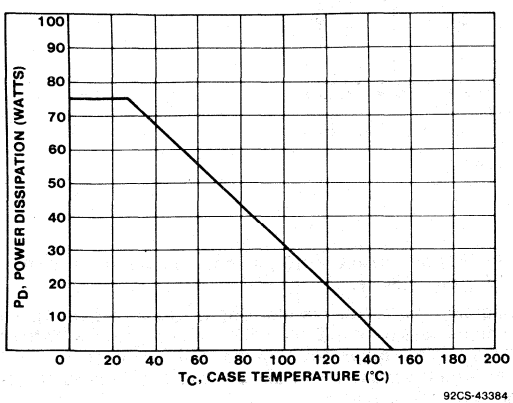


Fig. 9 - Power vs. temperature derating curve.

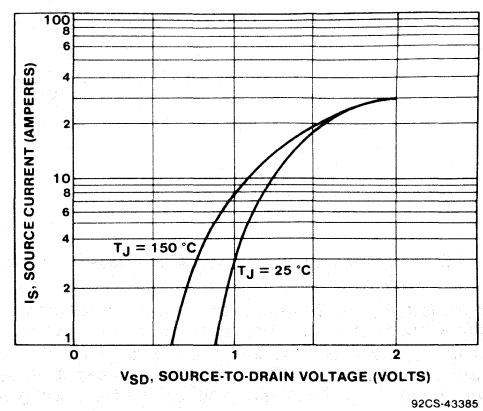


Fig. 10 - Typical body-drain diode forward voltage.

FRM6756M, FRM6756D, FRM6756R, FRM6756H

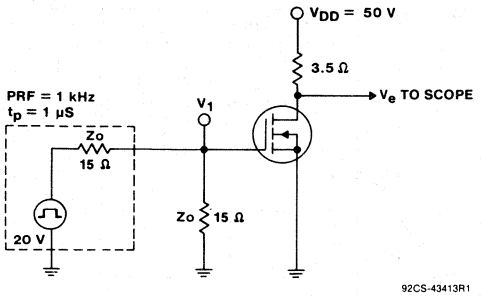


Fig. 11 - Switching time test circuit.

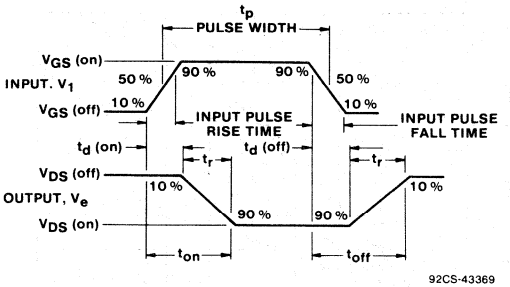


Fig. 12 - Switching time waveforms.

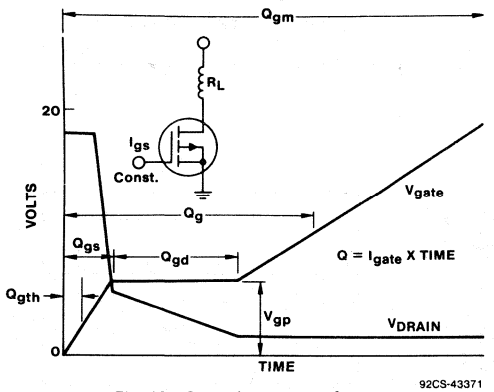


Fig. 13 - Gate change waveforms.

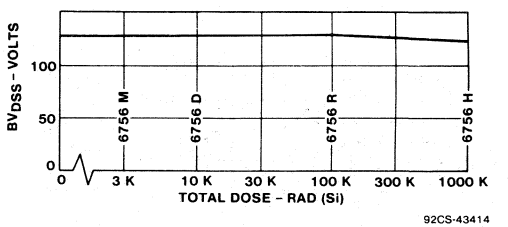


Fig. 14 - BV_{DSS} vs. dose.

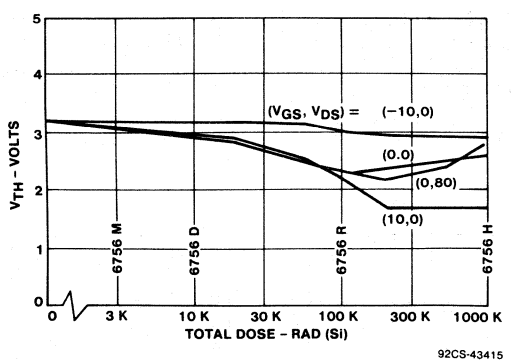


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Fig. 16 through 19 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of ID = 2A/div. and horizontal sensitivity of 1/2v/div. The four FRM6756H devices were biased as noted in diagram (e) during irradiation and removed for testing at 0,100,300 and 1000K rad(Si) as noted in diagrams (a) thru (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log ID vs. VGS. Vertical scale is ID from 1E-11 to 1A. Equipment compliance limits data to 1E-1A max. Drain voltage is set at +5 volts, but ID is relatively independent of VDS.

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = -10V and V_{DS} = 0V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

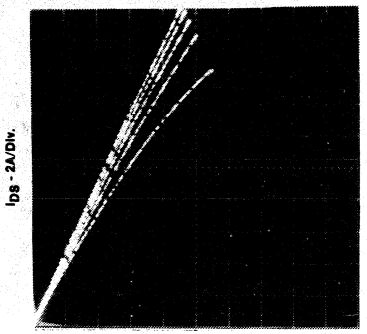


Fig. 16a - Typical output characteristics at pre-radiation.

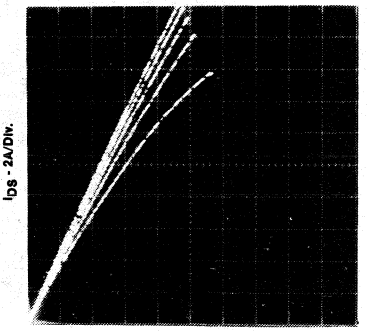


Fig. 16b - Typical output characteristic at 100K rads(Si).

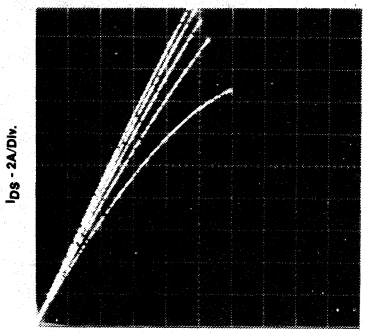


Fig. 16c - Typical output characteristic at 300K rads(Si).

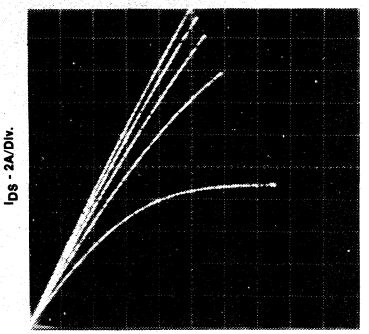


Fig. 16d - Typical output characteristic at 1M rad(Si).

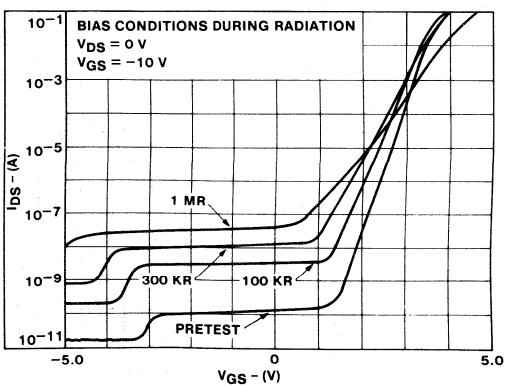


Fig. 16e - Drain source current as a function of gate bias.

FRM6756M, FRM6756D, FRM6756R, FRM6756H

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = +10V and V_{DS} = 0V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

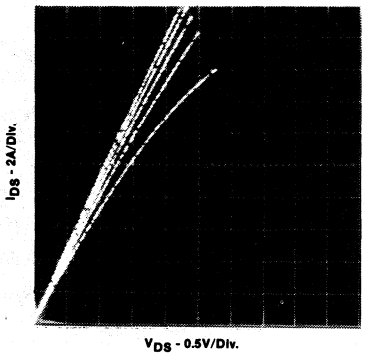


Fig. 17a - Typical output characteristics at pre-radiation.

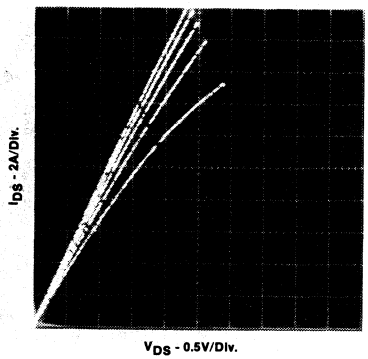


Fig. 17b - Typical output characteristic at 100K rads(Si).

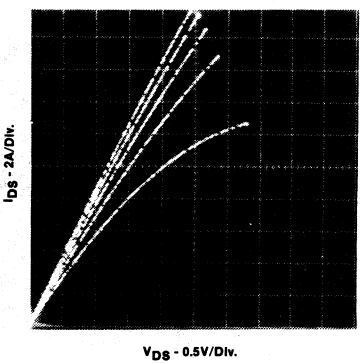


Fig. 17c - Typical output characteristic at 300K rads(Si).

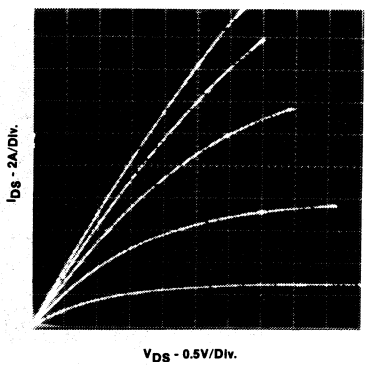


Fig. 17d - Typical output characteristic at 1M rad(Si).

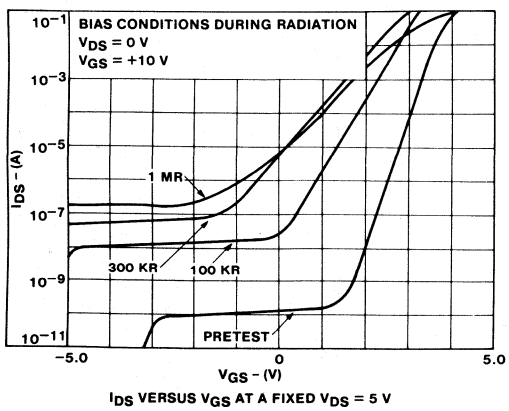


Fig. 17e - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = 0V and V_{DS} = 0V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

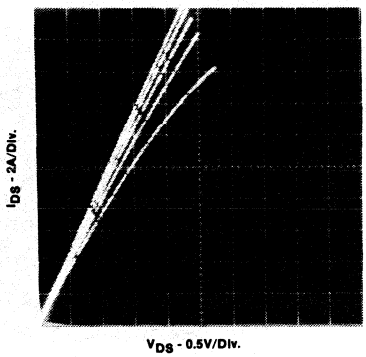


Fig. 18a - Typical output characteristics at pre-radiation.

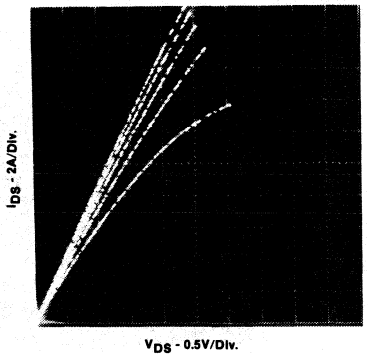


Fig. 18b - Typical output characteristic at 100K rads(Si).

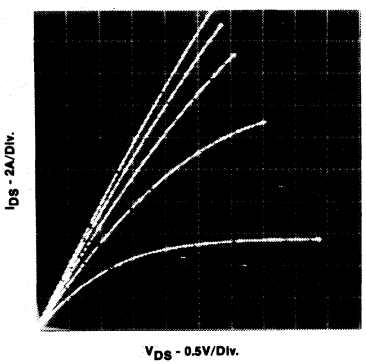


Fig. 18c - Typical output characteristic at 300K rads(Si).

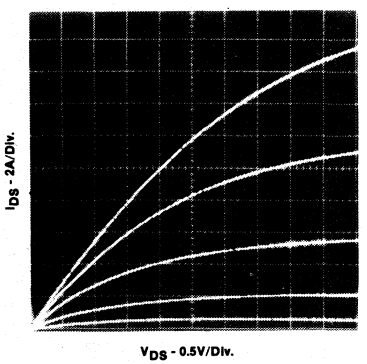


Fig. 18d - Typical output characteristic at 1M rad(Si).

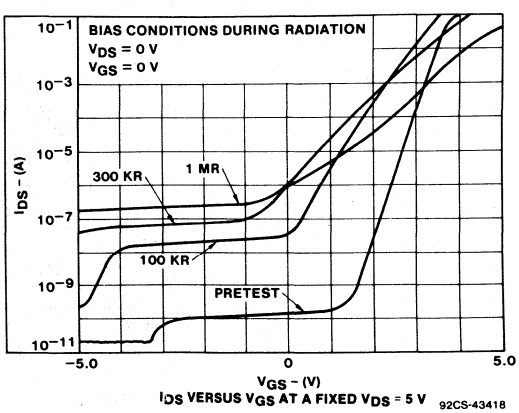


Fig. 18e - Drain source current as a function of gate bias.

FRM6756M, FRM6756D, FRM6756R, FRM6756H

TYPICAL TOTAL DOSE EFFECTS

Note: 1. Bias conditions during radiation were V_{GS} = 0V and V_{DS} = 80V.
2. Curves are for V_{GS} = 8V, 10V. 12V, 14V and 16V.

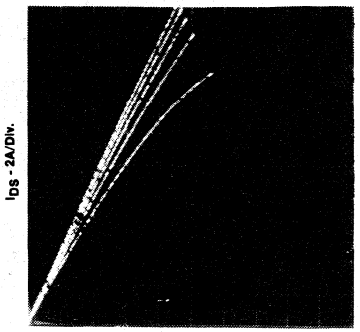


Fig. 19a - Typical output characteristics at pre-radiation.

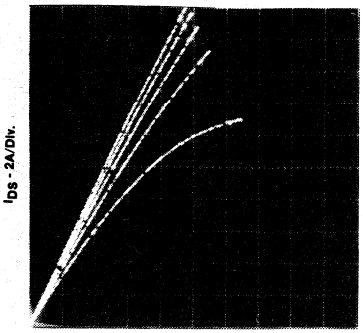


Fig. 19b - Typical output characteristic at 100K rads(Si).

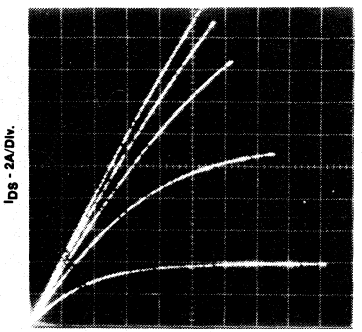


Fig. 19c - Typical output characteristic at 300K rads(Si).

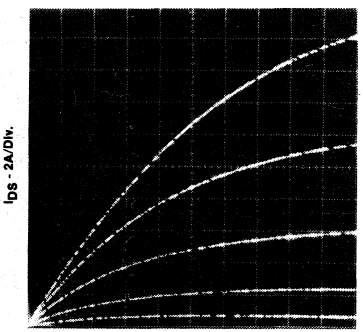
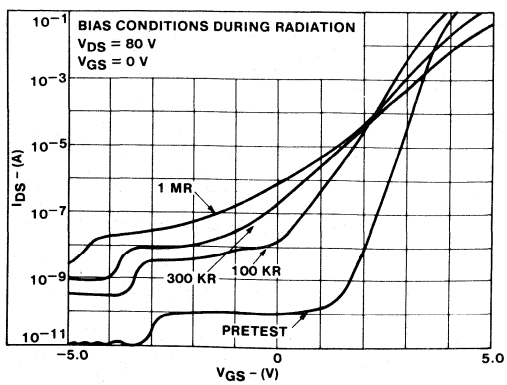


Fig. 19d - Typical output characteristic at 1M rad(Si).



IDS VERSUS VGS AT A FIXED VDS = 5 V

92CS-43419

Fig. 19e - Drain source current as a function of gate bias.

File Number **2171**

FRM6758M, FRM6758D
FRM6758R, FRM6758H

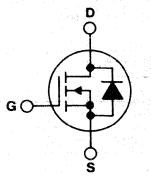
Radiation-Hardened N-Channel Power MOSFETs

Radiation-Hardened to: 1 Megarad (Si) 2 x 10^{12} Neutrons

N-CHANNEL ENHANCEMENT MODE

9 A, 200 V
$r_{DS}(on)$ = 0.4 Ω

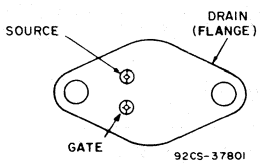
Features:
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *FRM6758M rated to 3K rads*
- *FRM6758D rated to 10K rads*
- *FRM6758R rated to 100K rads*
- *FRM6758H rated to 1000K rads*



92CS-43357

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

The FRM6758M, D, R, and H are n-channel enhancement-mode silicon-gate power field-effect transistors designed and specially processed to exhibit minimal characteristic changes to total dose (gamma), and neutron exposures. Although the FRM6758 family is not rated for other radiation exposures, survival has been observed for similar parts processed identically at full rated drain voltage for both SEU and a prompt gamma level of 2 x 10^{12} rads (Si)/second. These MOSFETs are well suited for applications exposed to radiation environments such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The FRM6758 family is supplied in the JEDEC TO-204AA steel package. See chart on page 11 for other package variants.

Total dose hardness is assured by sampling each production wafer lot prior to release. Additional high-rel screening for these parts is available. Contact the Harris Semiconductor High-Rel Marketing group.

The FRM6758 was formerly developmental type TA9799.

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

DRAIN-SOURCE VOLTAGE, V_{DS}	200	V
DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ) V_{DGR}	200	V
CONTINUOUS DRAIN CURRENT: I_D		
At T_C = 25°C	9	A
At T_C = 100°C	6	A
PULSED DRAIN CURRENT I_{DM}	15	A
GATE-SOURCE VOLTAGE V_{GS}	±20	V
POWER DISSIPATION: P_T		
At T_C = 25°C	75 (See Fig. 9)	W
At T_C = 100°C	30 (See Fig. 9)	W
Derate linearly above T_C = 25°C	0.6 (See Fig. 9)	W/°C
INDUCTIVE CURRENT, CLAMPED, L = 100 μH I_{LM}	15 (See Figs. 1 & 2)	A
OPERATING AND STORAGE TEMPERATURE T_J, T_{stg}	-55 to +150	°C
LEAD TEMPERATURE (During Soldering): T_L		
At distance > 0.063 in. (1.6 mm) from case for 10 s max.	300	°C

FRM6758M, FRM6758D, FRM6758R, FRM6758H

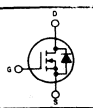
PRE-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless other specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0, I_D = 1 mA	200	—	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{DS} = V_{GS}, I_D = 1 mA	2	—	4	
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = 20 V	—	—	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20 V	—	—	100	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max. Rating, V_{GS} = 0	—	0.1	1	mA
		V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C	—	0.2	4	
Static Drain-Source On-State Voltage[1]	$V_{DS}(on)$	V_{GS} = 10 V, I_D = 9 A	—	—	3.6	V
Static Drain-Source On-State Resistance[1]	$r_{DS}(on)$	V_{GS} = 10 V, I_D = 6 A	—	0.26	0.4	Ω
		V_{GS} = 10 V, I_D = 6 A, T_C = 125°C	—	—	0.75	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 6 A	—	4.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	—	900	—	pF
Output Capacitance	C_{oss}		—	200	—	
Reverse-Transfer Capacitance	C_{rss}		—	50	—	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V, I_D = 6 A, Z_O = 15 Ω (See Figs. 11 & 12)	—	—	30	ns
Rise Time	t_r		—	—	50	
Turn-Off Delay Time	$t_d(off)$		—	—	50	
Fall Time	t_f		—	—	40	
Gate-Charge Threshold	Q_{gth}	V_{DD} = 100 V, I_D = 9 A Method 3471 from Mil-Std-750,Cond.A (See Fig. 13)	1.1	1.8	3.5	nC
Gate Charge	Q_g		14	25	39	
Gate-Charge Total	Q_{gm}		24	48	66	
Gate-Plateau Voltage	V_{gp}		4.5	6	7.5	V
Gate-Source Charge	Q_{gs}		2.2	5.7	8	nC
Gate-Drain ("Miller") Charge	Q_{gd}		8	12	24	

THERMAL RESISTANCE

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Junction-to-Case	$R_{\theta JC}$		—	—	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	—	0.1	—	
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	30	

BODY-DRAIN DIODE RATING AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse P-N junction rectifier 	—	—	9	A
Pulsed Source Current (Body Diode)	I_{SM}		—	—	15	
Diode Forward Voltage[1]	V_{SD}	T_C = 25°C, I_F = 9 A, V_{GS} = 0	0.8	—	1.6	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_{DM}, dI_F/dt = 100 A/μs	—	250	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

FRM6758M, FRM6758D, FRM6758R, FRM6758H

POST-RADIATION ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC		TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	All	I_D = 1 mA[2,3,4,5] (See Fig. 14)	180	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	FRM6758M	V_{GS} = V_{DS}, I_D = 1 mA[3,4,5] (See Fig. 15)	2	4	V
		FRM6758D		1.5	4.2	
		FRM6758R		1	4.5	
		FRM6758H		0.5	5	
		All	V_{GS} = V_{DS}, I_D = 1 mA[2]	1.5	4.2	
Gate-Body Leakage Forward	I_{GSSF}	All	V_{GS} = 20 V[2,3,4,5]	—	130	nA
Gate-Body Leakage Reverse	I_{GSSR}	All	V_{GS} = -20 V[2,3,4,5]	—	130	nA
Zero-Gate Voltage Drain Current	I_{DSS}	FRM6758M	V_{GS} = 0, V_{DS} = 160 V[3,4,5]	—	25	μA
		FRM6758D		—	30	
		FRM6758R		—	50	
		FRM6758H		—	100	
		All	V_{GS} = 0, V_{DS} = 160 V[2]	—	25	
Static Drain-Source On-State Resistance[1]	$r_{DS(on)}$	FRM6758M	V_{GS} = 10 V, I_D = 6 A[3,4,5]	—	0.40	Ω
		FRM6758D	V_{GS} = 10 V, I_D = 6 A[3,4,5]	—	0.40	
		FRM6758R	V_{GS} = 12 V, I_D = 6 A[3,4,5]	—	0.50	
		FRM6758H	V_{GS} = 16 V, I_D = 4 A[3,4,5]	—	0.75	
		All	V_{GS} = 10 V, I_D = 6 A[2]	—	0.45	
Static Drain-Source On-State Voltage[1]	$V_{DS(on)}$	FRM6758M	V_{GS} = 10 V, I_D = 9 A[3,4,5]	—	3.6	V
		FRM6758D	V_{GS} = 10 V, I_D = 9 A[3,4,5]	—	3.6	
		FRM6758R	V_{GS} = 12 V, I_D = 8 A[3,4,5]	—	3.6	
		FRM6758H	V_{GS} = 16 V, I_D = 5 A[3,4,5]	—	3.6	
		All	V_{GS} = 10 V, I_D = 9 A[2]	—	3.6	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Neutron Dose 1 x 10^{12} n°/cm^2, V_{GS} = V_{DS} = 0.
3. Total Dose Bias During Irradiation, V_{GS} = 10 V, V_{DS} = 0 V.
4. Total Dose Bias During Irradiation, V_{GS} = 0 V, V_{DS} = 160 V.
5. Total Dose Post-Rad End Points at 3K, 10K, 100K, 300K and 1000K rads (Si) for FRM6758M,D,R and H, respectively.

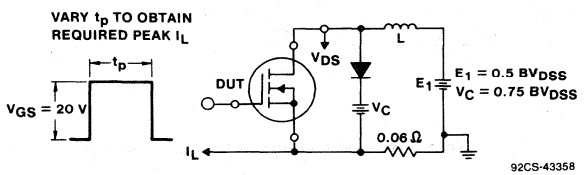


Fig. 1 - Clamped inductive test circuit.

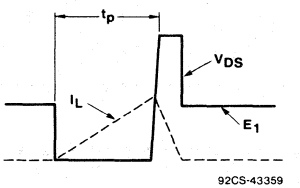


Fig. 2 - Clamped inductive waveforms.

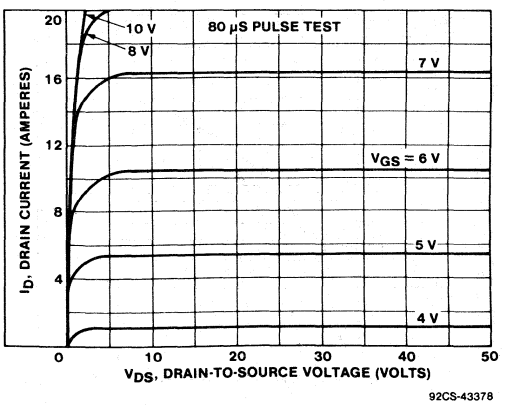


Fig. 3 - Typical output characteristics.

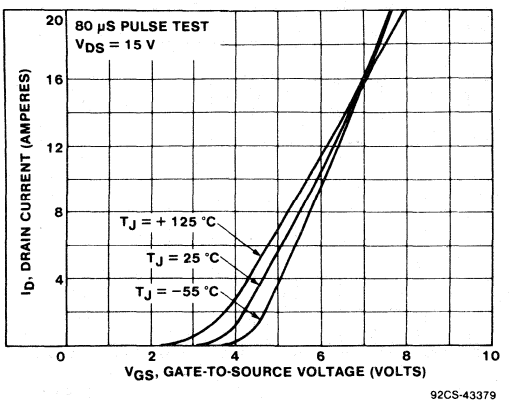


Fig. 4 - Typical transfer characteristics.

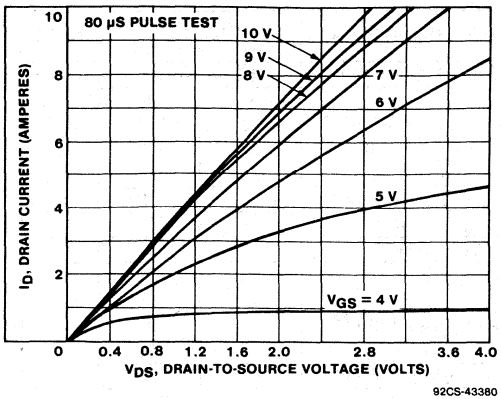


Fig. 5 - Typical saturation characteristics.

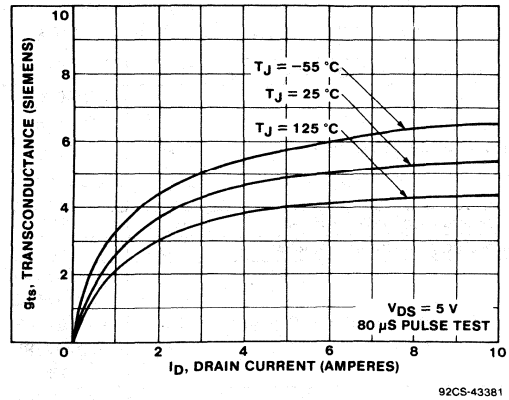


Fig. 6 - Typical transconductance vs. drain current.

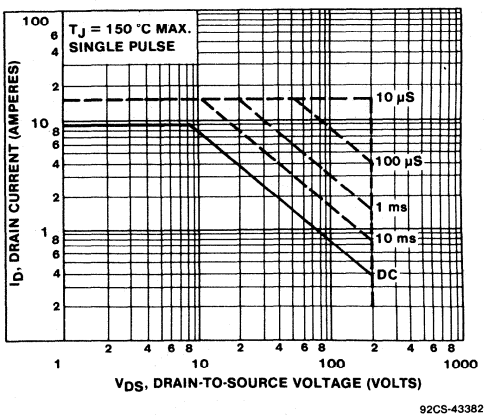


Fig. 7 - Maximum safe operating area.

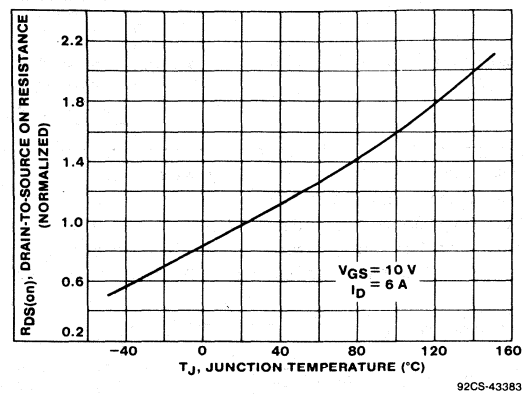


Fig. 8 - Normalized typical on-resistance vs. temperature.

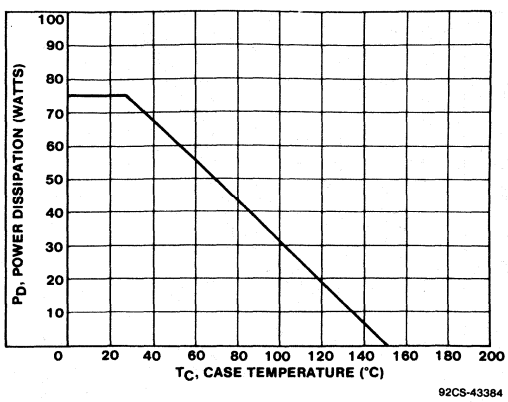


Fig. 9 - Power vs. temperature derating curve.

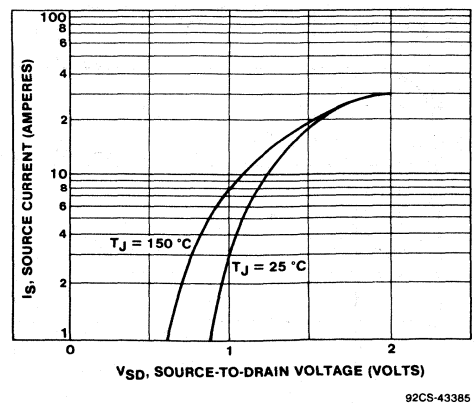


Fig. 10 - Typical body-drain diode forward voltage.

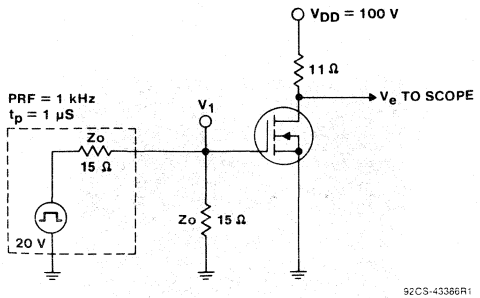


Fig. 11 - Switching time test circuit.

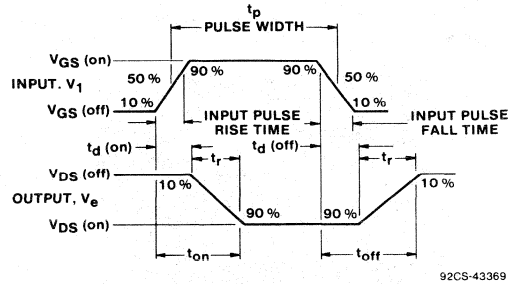


Fig. 12 - Switching time waveforms.

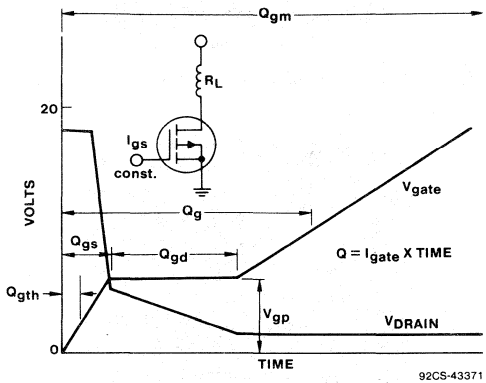


Fig. 13 - Gate charge waveforms.

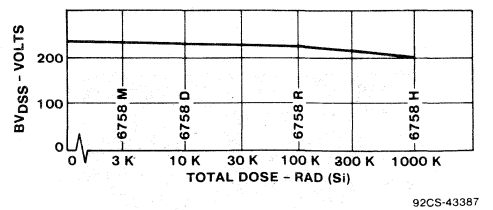


Fig. 14 - BV_{DSS} vs. dose.

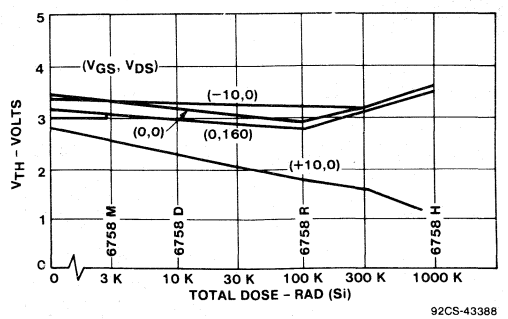


Fig. 15 - V_{TH} vs. dose.

Typical Conduction Losses and Blocking Losses vs. Total Dose vs. In Situ Bias

The photos in Figs. 16 through 19 are output curves for gate drive of 8, 10, 12, 14 and 16 volts. All photos have vertical sensitivity of I_D = 1 A/div. and horizontal sensitivity of ½V/div. The four FRM6758H devices were biased as noted in diagram (e) of each figure during irradiation and removed for testing at 0K, 100K, 300K and 1000K rads (Si) as noted in diagrams (a) through (d) for each device.

Diagram (e) presents the blocking losses by recording the same devices for log I_D vs. V_{GS}. Vertical scale is I_D from 1E-11 to 1A. Equipment compliance limits data to 1E-1A max. Drain voltage is set at +5 volts, but I_D is relatively independent of V_{DS}.

FRM6758M, FRM6758D, FRM6758R, FRM6758H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = -10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

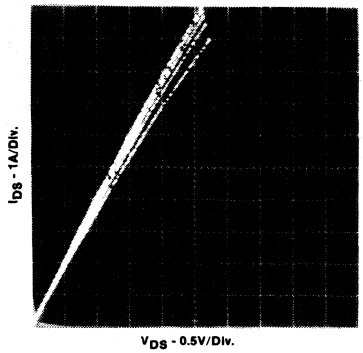


Fig. 16(a) - Typical output characteristics at pre-radiation.

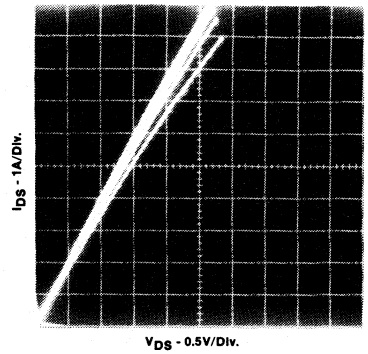


Fig. 16(b) - Typical output characteristics at 100K rads (Si).

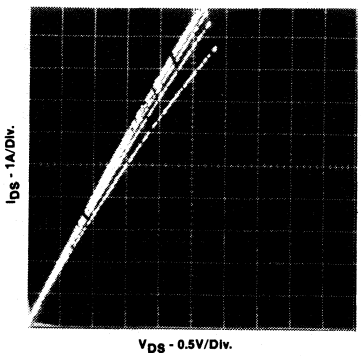


Fig. 16(c) - Typical output characteristics at 300K rads (Si).

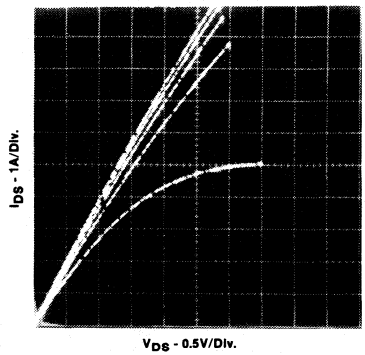


Fig. 16(d) - Typical output characteristics at 1M rad (Si).

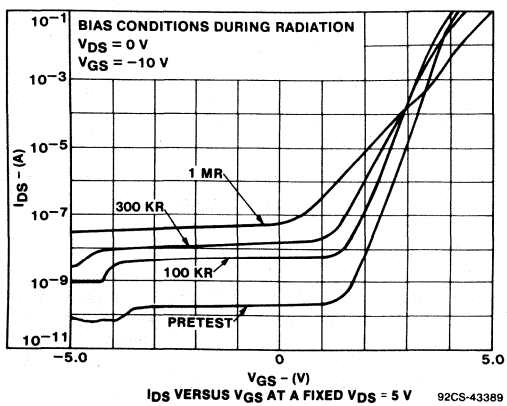


Fig. 16(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = +10 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

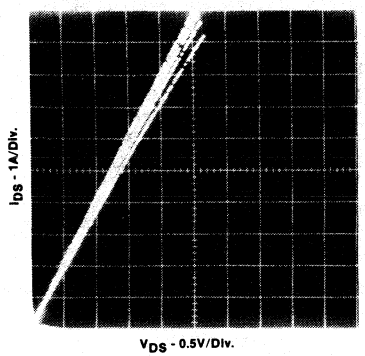


Fig. 17(a) - Typical output characteristics at pre-radiation.

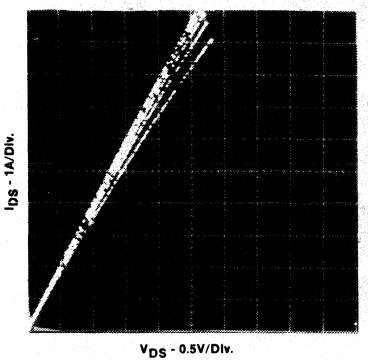


Fig. 17(b) - Typical output characteristics at 100K rads (Si).

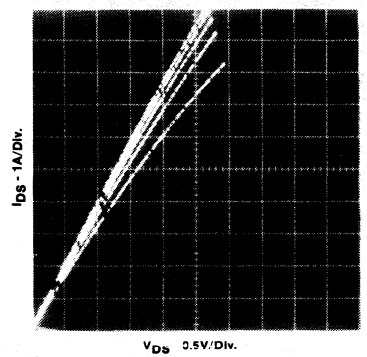


Fig. 17(c) - Typical output characteristics at 300K rads (Si).

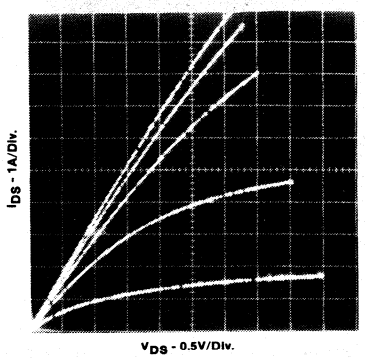


Fig. 17(d) - Typical output characteristics at 1M rad (Si).

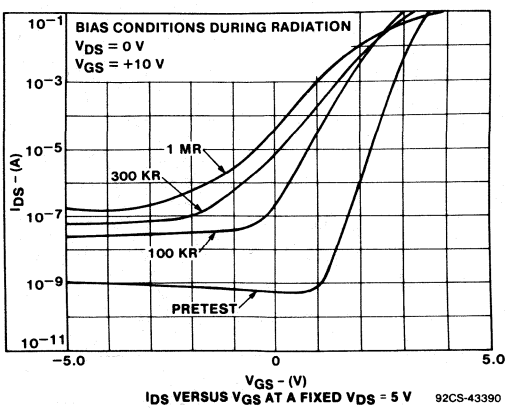


Fig. 17(e) - Drain source current as a function of gate bias.

FRM6758M, FRM6758D, FRM6758R, FRM6758H

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 0 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

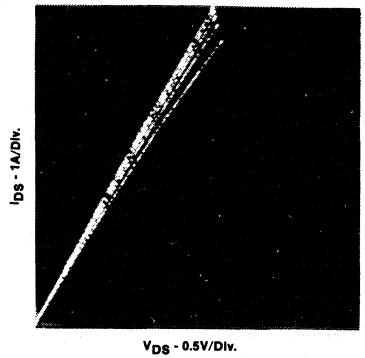


Fig. 18(a) - Typical output characteristics at pre-radiation.

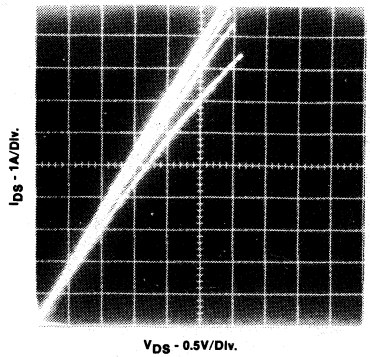


Fig. 18(b) - Typical output characteristics at 100K rads (Si).

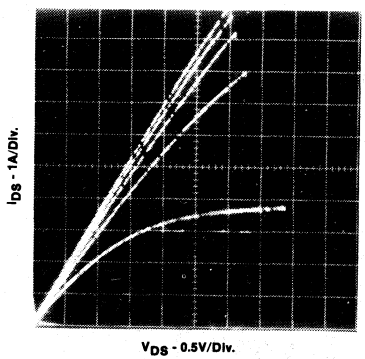


Fig. 18(c) - Typical output characteristics at 300K rads (Si).

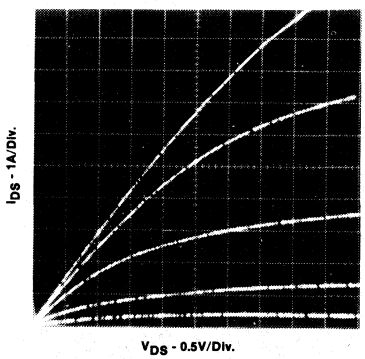


Fig. 18(d) - Typical output characteristics at 1M rad (Si).

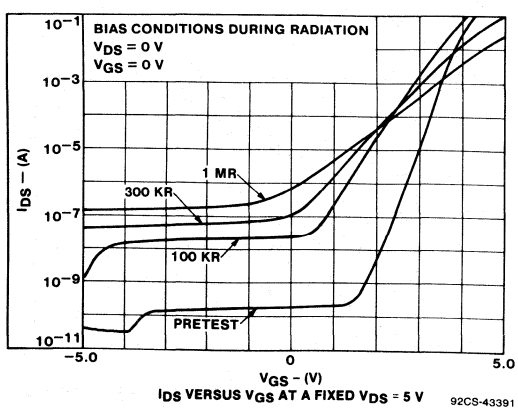


Fig. 18(e) - Drain source current as a function of gate bias.

TYPICAL TOTAL DOSE EFFECTS

Note:
1. Bias conditions during radiation were V_{GS} = 0 V and V_{DS} = 160 V.
2. Curves are for V_{GS} = 8 V, 10 V, 12 V, 14 V and 16 V.

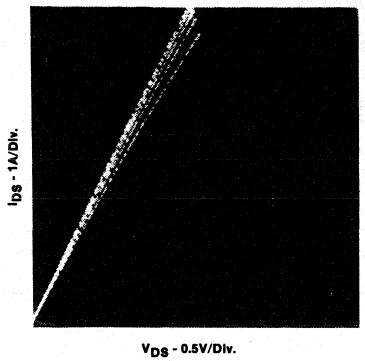


Fig. 19(a) - Typical output characteristics at pre-radiation.

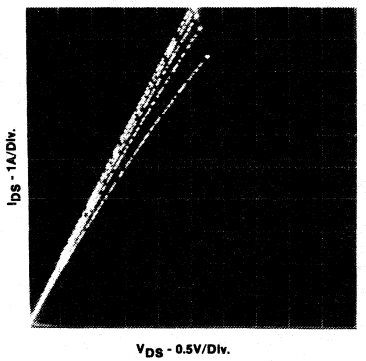


Fig. 19(b) - Typical output characteristics at 100K rads (Si).

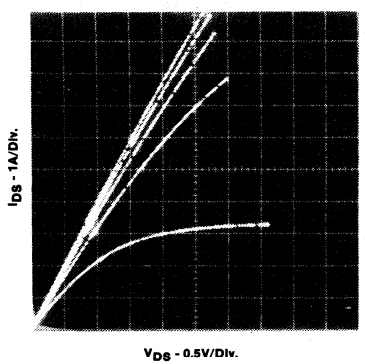


Fig. 19(c) - Typical output characteristics at 300K rads (Si).

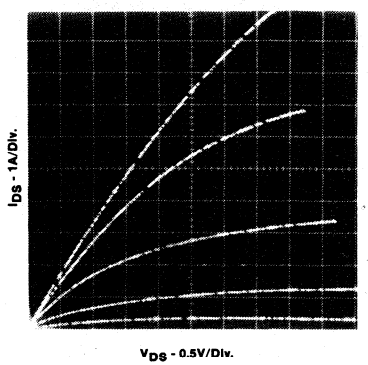


Fig. 19(d) - Typical output characteristics at 1M rad (Si).

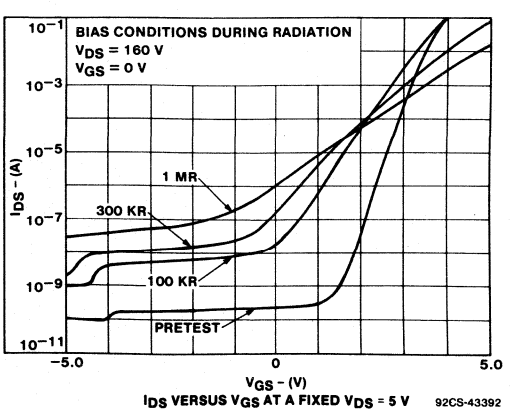


Fig. 19(e) - Drain source current as a function of gate bias.

Preview Products

GSI550, IGT7E50CS

File Number **2328**

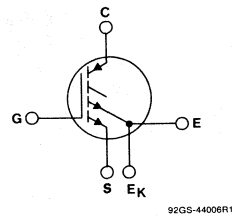
Current Sensing IGT™ Transistors

Insulated Gate Bipolar Transistors

50 A, 500 V
$r_{DS}(on)$ = 0.052 Ω

Features:
- *Low $V_{CE}(sat)$ - 1.5 V typ. @ 50 A*
- *Ultra-fast turn-on - 200 ns typical*
- *Polysilicon MOS gate - voltage controlled turn on/off*
- *High current handling - 50 A @ 60° C case*
- *Current sensing pilot*

TERMINAL DIAGRAM

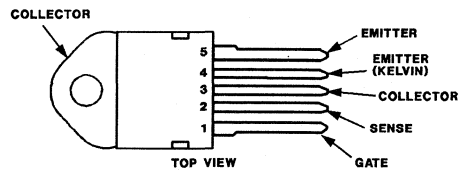


N-CHANNEL ENHANCEMENT MODE

The GSI550 and/or IGT7E50CS IGT™ Transistor (Insulated-Gate Bipolar Transistor) is a MOS-Gated power-switching device combining the best features of power MOSFETs and bipolar transistors with current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses of bipolar transistors. The gate characteristics of the IGT™ Transistor are similar to power MOSFETs but its equivalent $r_{ds}(on)$ drain resistance is ten times lower and varies only moderately between 25° C and 150° C, thus offering extended power handling capability.

The IGT™ Transistor is ideal for many high voltage switching applications up to 5 kHz where low conduction losses are essential; ac and dc motor controls, power supplies and drivers for solenoids, relays, and contactors.

TERMINAL DESIGNATION



TO-218 (5 LEAD)

MAXIMUM RATINGS

COLLECTOR-EMITTER VOLTAGE (V_{GE} = 0 V)	V_{CES}	500	V
COLLECTOR-GATE VOLTAGE (R_{GE} = 1 MΩ)	V_{CGR}	500	V
CONTINUOUS DRAIN CURRENT	I_C		
At T_C = 60° C		50	A
PULSED COLLECTOR CURRENT	I_{CM}*	200	A
GATE-EMITTER VOLTAGE	V_{GE}	±20	V
TOTAL POWER DISSIPATION	P_D		
At T_C = 25° C		200	W
Derate Above 25° C		1.6	W/° C
OPERATING AND STORAGE JUNCTION TEMPERATURE RANGE	T_J, T_{stg}	-40 to +150	°C
THERMAL RESISTANCE, JUNCTION TO CASE	$R_{\theta JC}$	0.7	°C/W
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES	T_L		
1/8 inch from case for 5 seconds		260	°C

*Repetitive Rating: Pulse width limited by maximum junction temperature. Gate control turn-off not allowed above 100 amperes.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, T_C = 25° C Unless Otherwise Specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 250 μA	500	—	—	V
Collector Cut-off Current	I_{CES}	V_{CE} = Max. Rating V_{GE} = 0 V, T_C = 25° C	—	—	250	μA
		V_{CE} = Max. Rating x 0.8 V_{GE} = 0 V, T_C = 125° C(1)	—	—	4	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V	—	—	±500	nA
ON CHARACTERISTICS(2)						
Gate Threshold Voltage	$V_{GE}(th)$	V_{CE} = V_{GE}, I_C = 1 mA				V
		T_C = 25° C	2	4	5.5	
		T_C = 150° C	—	2	—	
Collector-Emitter Saturation Voltage	$V_{CE}(sat)$	V_{GE} = 15 V, I_C = 50 A				
		T_C = 25° C	—	1.5	2.6	
		T_C = 150° C	—	1.6	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ies}	V_{GE} = 0 V	—	4600	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25 V	—	400	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	75	—	
SWITCHING CHARACTERISTICS(2) (See Figs. 8 & 9)						
Turn-on Delay Time	$t_d(on)$	Resistive Load, T_J = 150° C	—	100	—	ns
Rise Time	t_r	I_C = 50 A, V_{CE} = 400 V	—	200	—	
Turn-off Delay Time	$t_d(off)$	V_{GE} = 15 V	—	0.9	—	μs
Fall Time	t_f	$R_G(on)$ = 50 Ω, $R_G(off)$ = 50 Ω	—	3	—	
Turn-off Delay Time	$t_d(off)$	Inductive Load, T_J = 150° C L = 45 μH, I_C = 50 A	—	1.5	2.5	μs
Fall Time	t_f	$V_{CE}(clamp)$ = 400 V, V_{GE} = 15 V	—	1.2	1.6	
Turn-off Switching Losses	E_f	$R_G(on)$ = 50 Ω, $R_G(off)$ = 50 Ω	—	10	16	mJ
PILOT CHARACTERISTICS(2)(3)(4)						
Pilot - Emitter Kelvin Voltage	V_{PEK}	V_{GE} = 15 Vdc, R_P = 1 KΩ				V
I_C = 40 A			1	1.3	1.6	
I_C = 60 A			—	1.45	—	
I_C = 80 A			—	1.7	—	

(1) Applies for 3.3° C per watt maximum thermal resistance, case to ambient.

(2) Pulse test: Pulse widths ≤ 300 μs, duty cycle ≤ 2%.

(3) Refer to Fig. 5(a).

(4) When not in use connect P to Emitter.

GSI550, IGT7E50CS

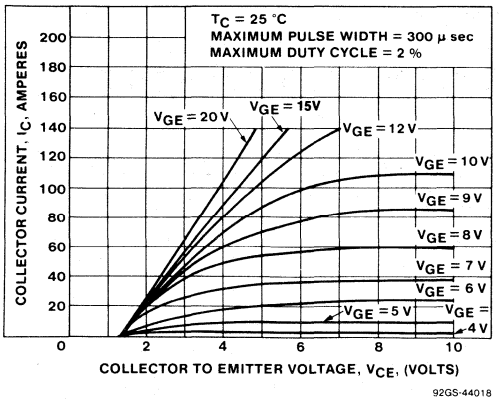


Fig. 1 - Typical output characteristics.

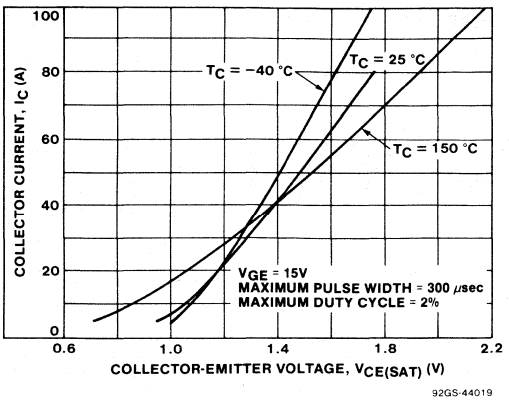


Fig. 2 - Typical collector-emitter saturation voltage

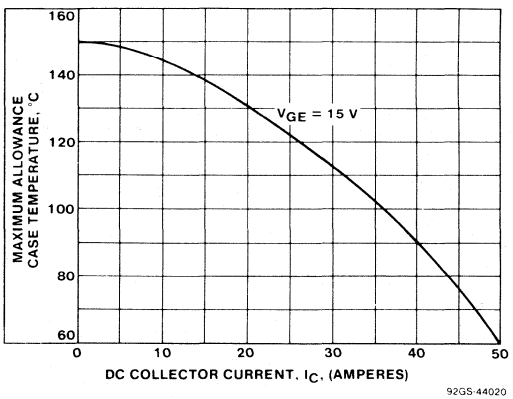


Fig. 3 - Maximum allowable dc collector current vs. case temperature.

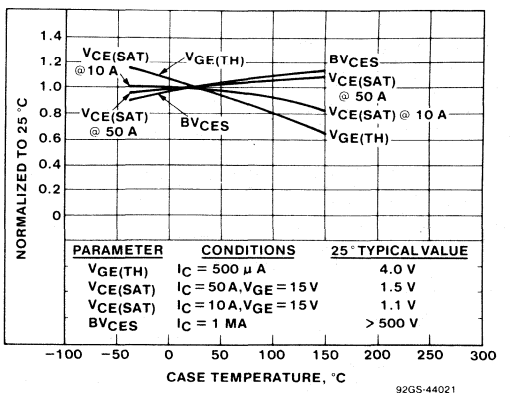


Fig. 4 - Typical temperature dependence of parameters.

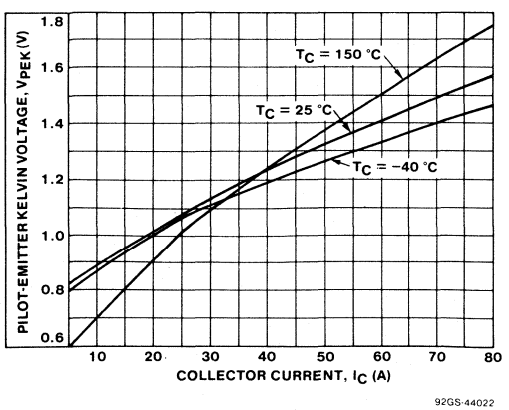


Fig. 5(a) - Typical emitter pilot characteristics - 1 KΩ pilot resistor.

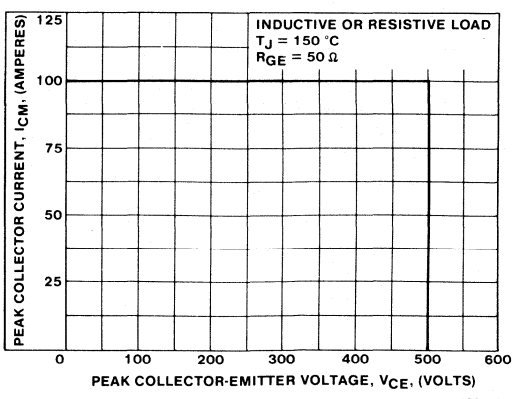


Fig. 5(b) - Turn-off safe operating area.

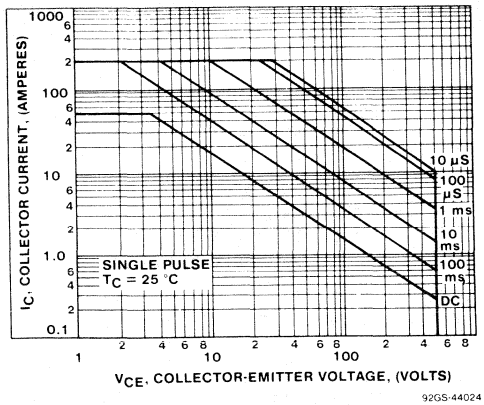


Fig. 6 - Active region safe operating area.

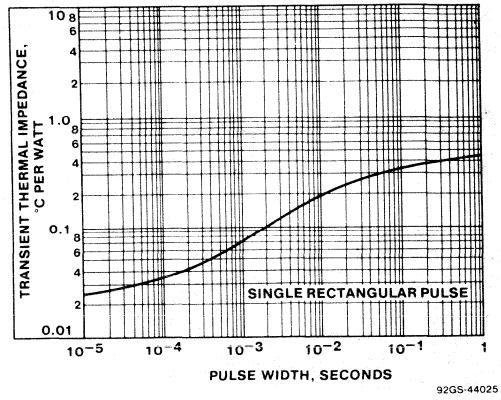


Fig. 7 - Maximum transient thermal impedance.

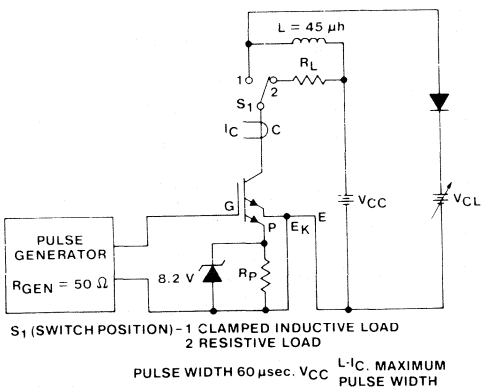


Fig. 8 - Basic switching test circuit.

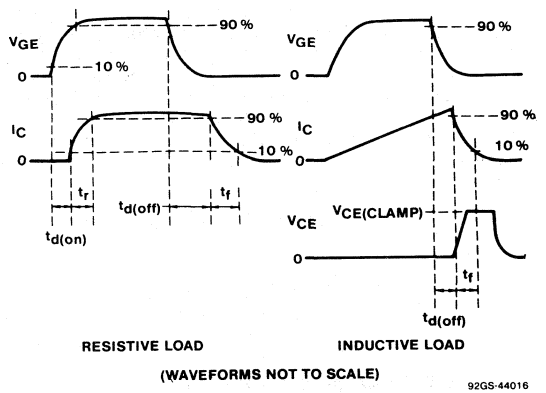


Fig. 9 - Switching waveforms.

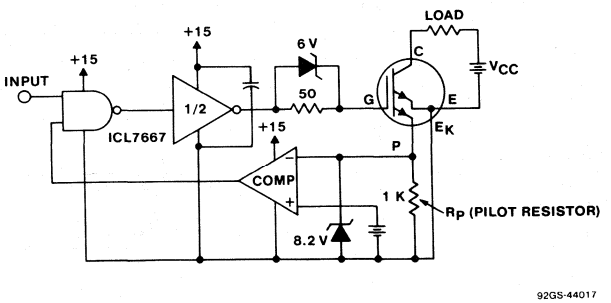


Fig. 10 - Typical circuit utilizing the pilot for overcurrent protection.

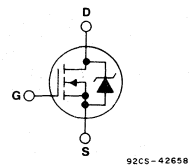
IRF360, IRF362 File Number **2276**

Avalanche-Energy-Rated N-Channel Power MOSFETs

25 A and 22 A, 400 V
$r_{DS(on)}$ = 0.20 Ω and 0.25 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

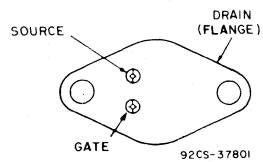


TERMINAL DIAGRAM

The IRF360 and IRF362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

TERMINAL DESIGNATION



JEDEC TO-204AE

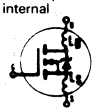
ABSOLUTE MAXIMUM RATINGS

	Parameter	IRF360	IRF362	Units
I_D @ T_C = 25°C	Continuous Drain Current	25	22	A
I_D @ T_C = 100°C	Continuous Drain Current	16	14	A
I_{DM}	Pulsed Drain Current ①	100	88	A
P_D @ T_C = 25°C	Max. Power Dissipation	300		W
	Linear Derating Factor	2.4		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	980 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ① (Repetitive or Non-Repetitive)	25		A
T_J T_{STG}	Operating Junction Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25°C Unless Otherwise Specified*

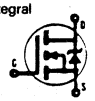
Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	400	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRF360	–	0.18	0.20	Ω	V_{GS} = 10V, I_D = 14A
		IRF362	–	0.20	0.25		
$I_{D(on)}$	On-State Drain Current ③	IRF360	25	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
		IRF362	22				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	14	21	–	S (℧)	I_{DS} = 14A, $V_{DS} \geq 50V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	–100	nA	V_{GS} = –20V
Q_g	Total Gate Charge	ALL	–	120	170	nC	V_{GS} = 10V, I_D = 25A
Q_{gs}	Gate-to-Source Charge	ALL	–	19	28	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	60	90	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	–	22	33	ns	V_{DD} = 200V, $I_D \approx$ 25A, R_G = 4.3Ω
t_r	Rise Time	ALL	–	94	140	ns	R_D = 7.5Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	80	120	ns	See Fig. 15
t_f	Fall Time	ALL	–	66	99	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	–	4000	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	550	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	97	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.42	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.12	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Typical socket mount

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	25	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	100	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	460	1000	ns	T_J = 25°C, I_F = 25A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.1	7.1	16	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$				



① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5)

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 2.8 mH, Peak I_L = 25A,

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

IRF360, IRF362

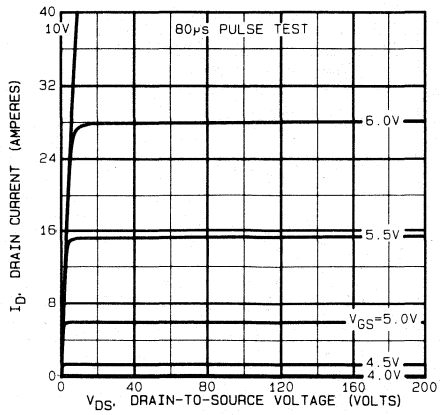


Fig. 1 - Typical output characteristics.

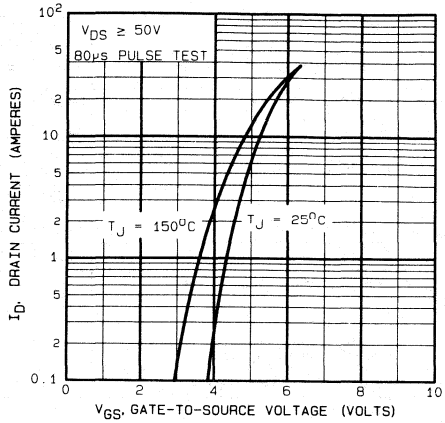


Fig. 2 - Typical transfer characteristics.

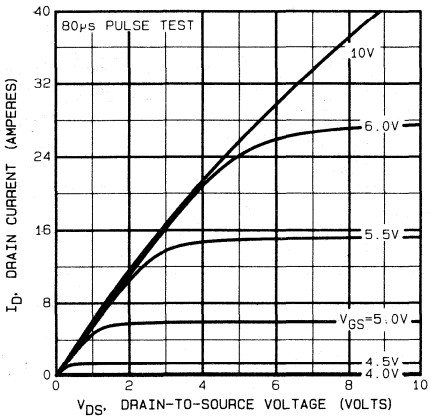


Fig. 3 - Typical saturation characteristics.

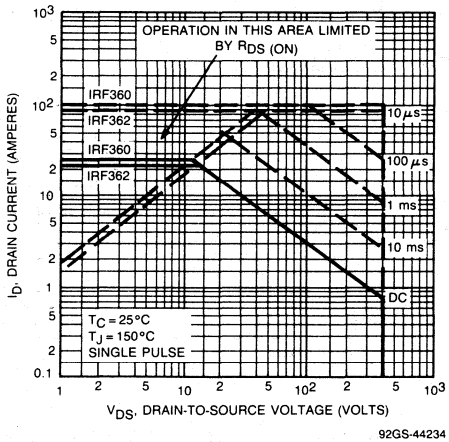


Fig. 4 - Maximum safe operating area.

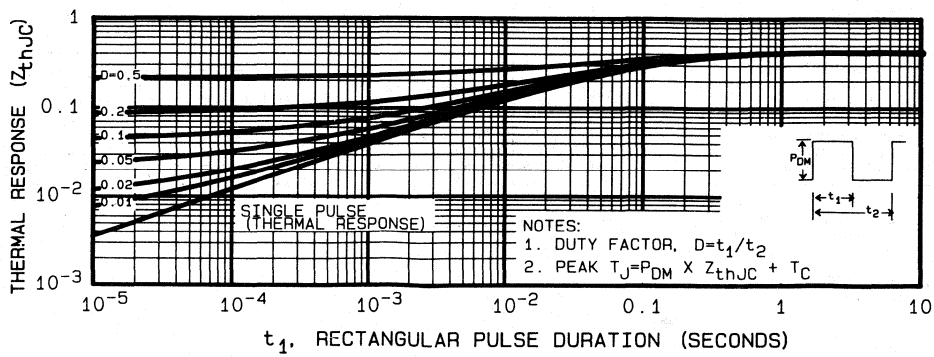


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

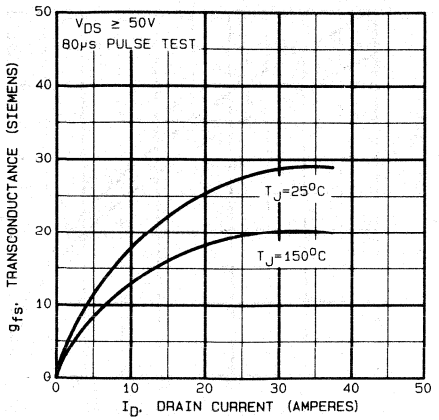


Fig. 6 - Typical transconductance vs. drain current.

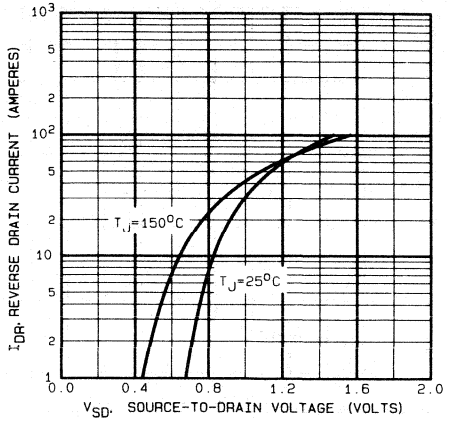


Fig. 7 - Typical source-drain diode forward voltage.

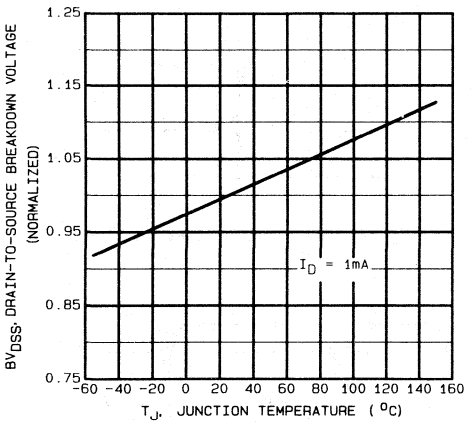


Fig. 8 - Breakdown voltage vs. temperature.

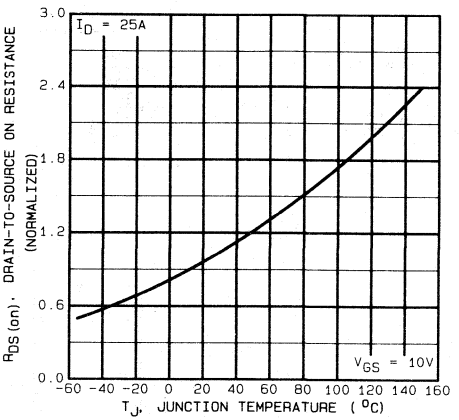


Fig. 9 - Normalized on-resistance vs. temperature.

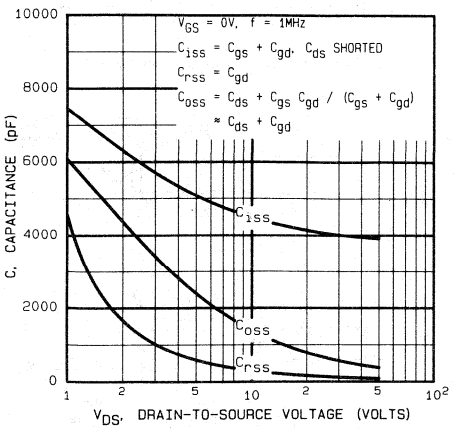


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

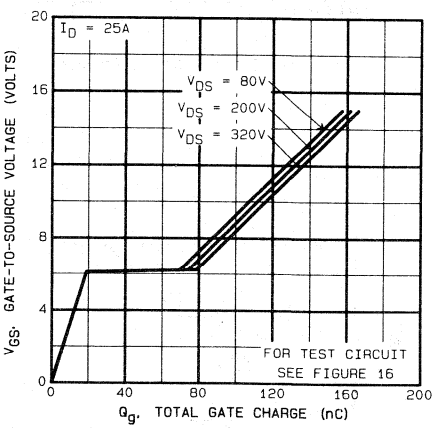


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

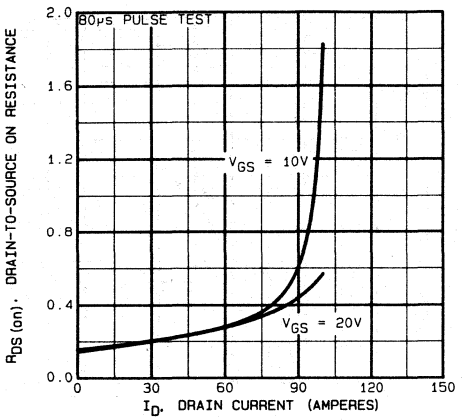


Fig. 12 - Typical on-resistance vs. drain current.

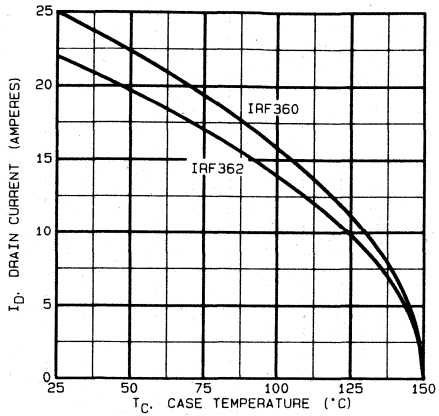


Fig. 13 - Maximum drain current vs. case temperature.

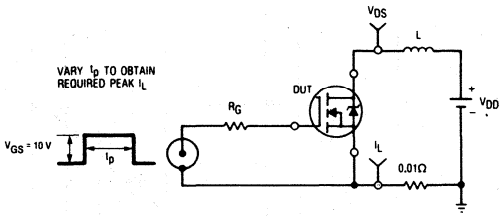


Fig. 14a - Unclamped inductive test circuit.

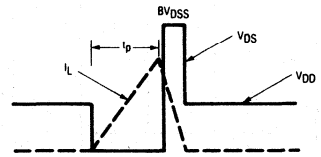


Fig. 14b - Unclamped inductive waveforms.

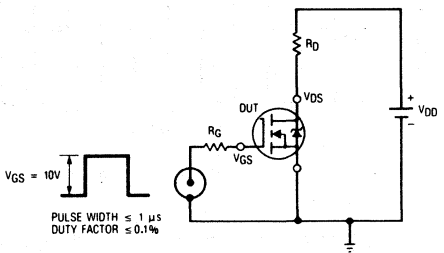


Fig. 15a - Switching time test circuit.

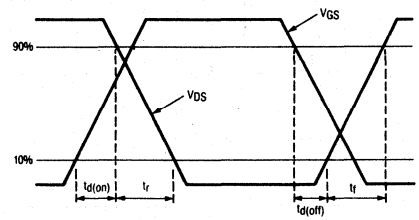


Fig. 15b - Switching time waveforms.

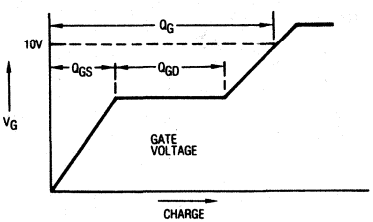


Fig. 16a - Basic gate charge waveform.

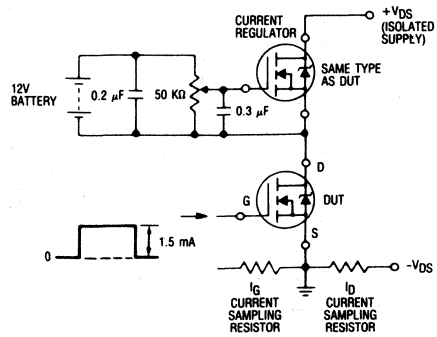


Fig. 16b - Gate charge test circuit.

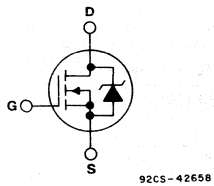
File Number **2277**

Avalanche-Energy-Rated N-Channel Power MOSFETs

21 A and 19 A, 500 V
$r_{DS(on)}$ = 0.27 Ω and 0.35 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

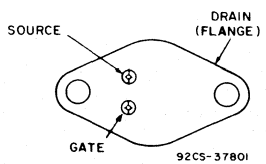


TERMINAL DIAGRAM

The IRF460 and IRF462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

TERMINAL DESIGNATION



JEDEC TO-204AE

ABSOLUTE MAXIMUM RATINGS

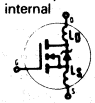
Parameter		IRF460	IRF462	Units
I_D @ T_C = 25°C	Continuous Drain Current	21	19	A
I_D @ T_C = 100°C	Continuous Drain Current	14	12	A
I_{DM}	Pulsed Drain Current ①	84	76	A
P_D @ T_C = 25°C	Max. Power Dissipation	300		W
	Linear Derating Factor	2.4		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	1200 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ①	21		A
T_J T_{STG}	Operating Junction Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

IRFP460, IRFP462

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25° C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRF460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 12A
		IRF462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRF460	21	–	–	A	V_{DS} > $I_{D(on)}$ X $R_{DS(on)}$ Max.
		IRF462	19	–	–		V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	13	20	–	S (℧)	V_{DS} ≥ 50V, I_{DS} = 12A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	–100	nA	V_{GS} = –20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A
Q_{gs}	Gate-to-Source Charge	ALL	–	18	27	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	93	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D ≈ 21A, R_G = 4.3Ω
t_r	Rise Time	ALL	–	81	120	ns	R_D = 12Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	See Fig. 15
t_f	Fall Time	ALL	–	65	98	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	480	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.42	°C/W	
R_{thJS}	Case-to-Sink	ALL	–	0.15	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Typical socket mount

Modified MOSFET symbol showing the internal inductances.



① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.9 μH, R_G = 25Ω, Peak I_L = 21A.

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	21	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	84	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

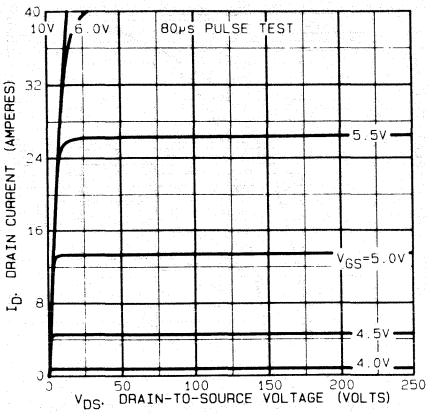


Fig. 1 - Typical output characteristics.

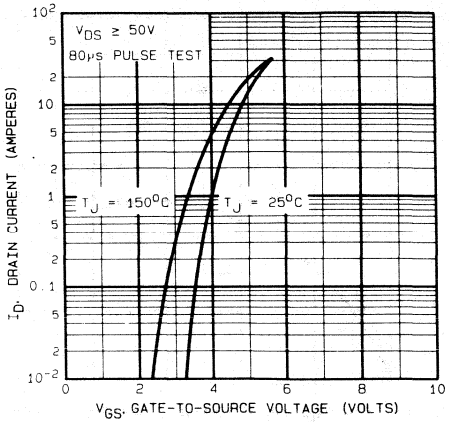


Fig. 2 - Typical transfer characteristics.

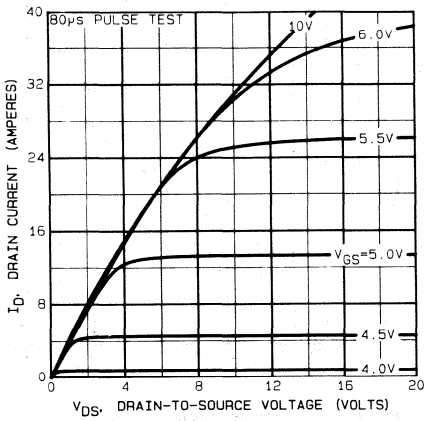


Fig. 3 - Typical saturation characteristics.

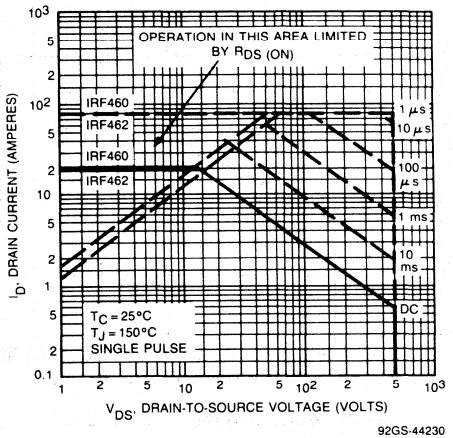


Fig. 4 - Maximum safe operating area.

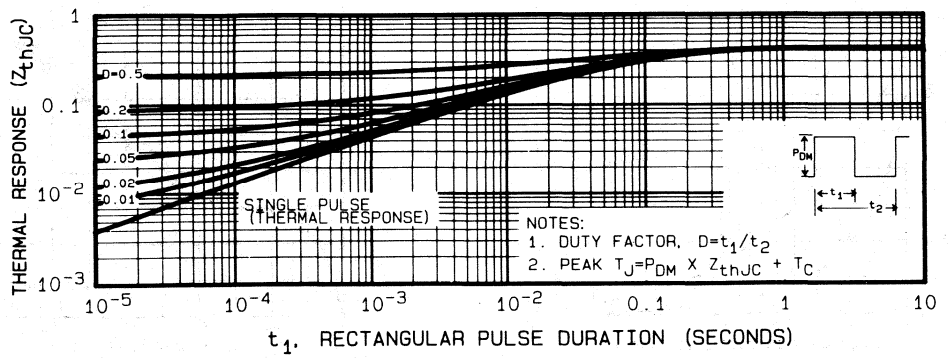


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

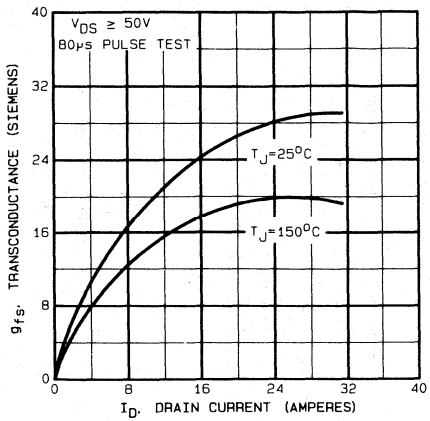


Fig. 6 - Typical transconductance vs. drain current.

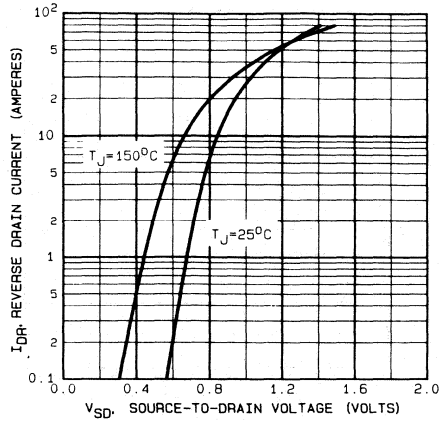


Fig. 7 - Typical source-drain diode forward voltage.

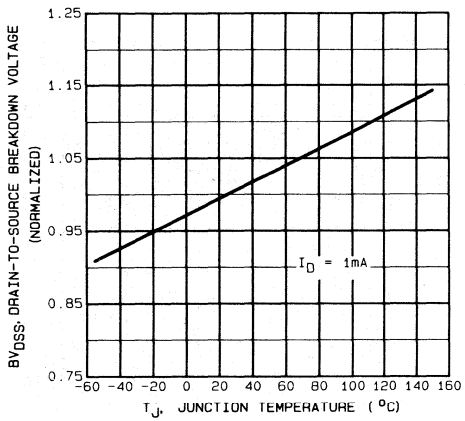


Fig. 8 - Breakdown voltage vs. temperature.

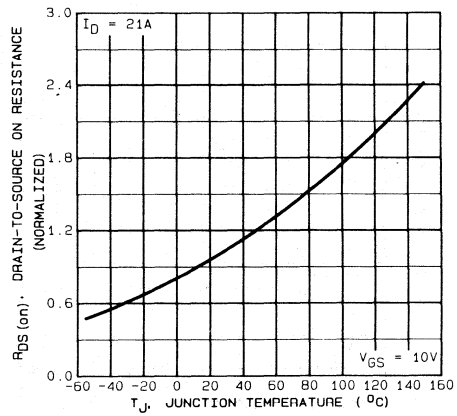


Fig. 9 - Normalized on-resistance vs. temperature.

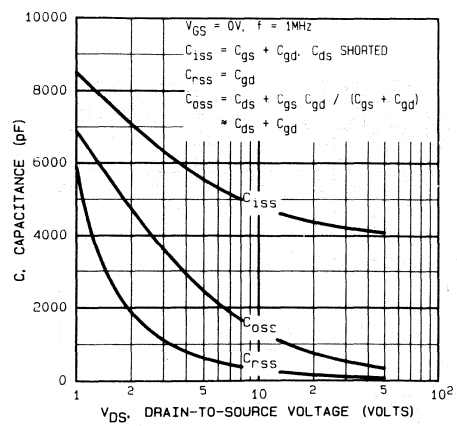


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

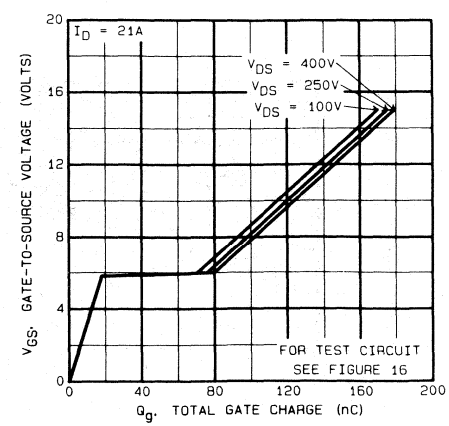


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

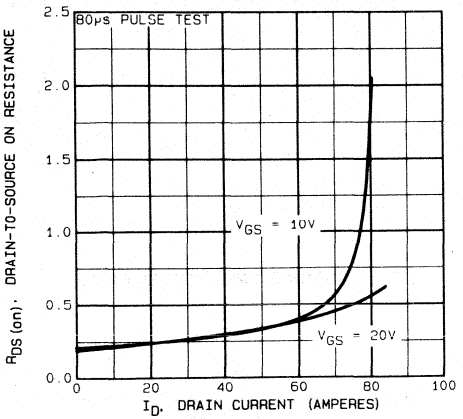


Fig. 12 - Typical on-resistance vs. drain current.

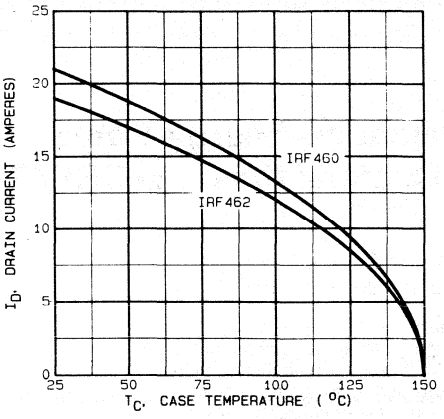


Fig. 13 - Maximum drain current vs. case temperature.

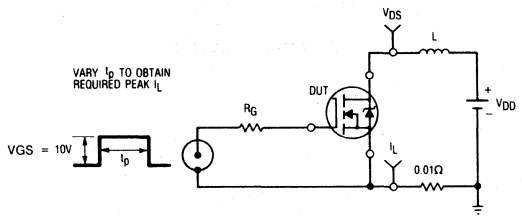


Fig. 14a - Unclamped inductive test circuit.

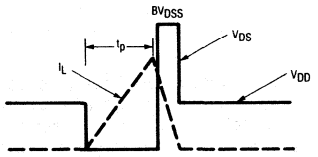


Fig. 14b - Unclamped inductive waveforms.

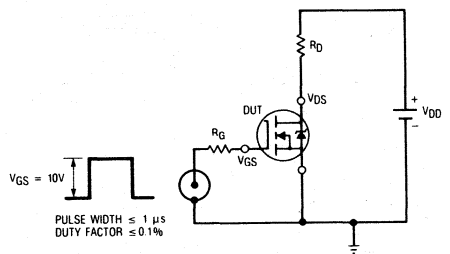


Fig. 15a - Switching time test circuit.

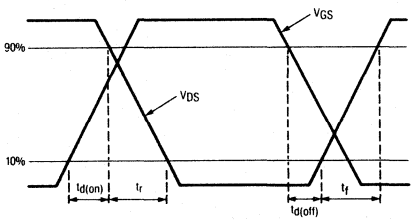


Fig. 15b - Switching time waveforms.

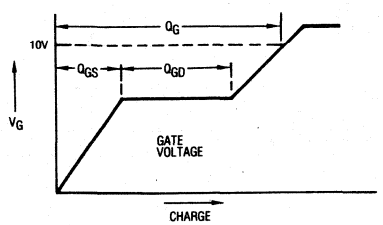


Fig. 16a - Basic gate charge waveform.

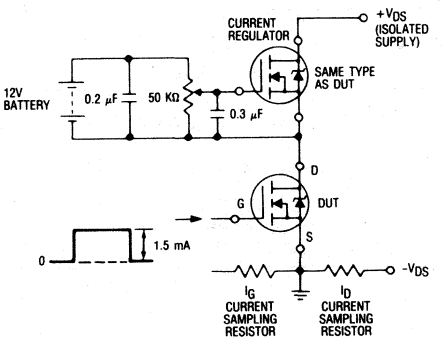


Fig. 16b - Gate charge test circuit.

IRFP360, IRFP362

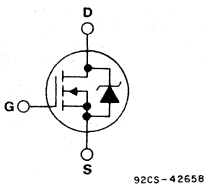
File Number **2290**

Avalanche-Energy-Rated N-Channel Power MOSFETs

23 A and 20 A, 400 V
$r_{DS(on)}$ = 0.20 Ω and 0.25 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

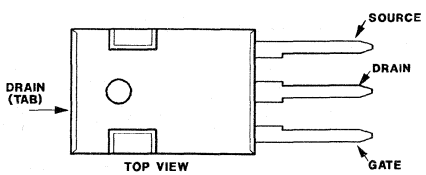


TERMINAL DIAGRAM

The IRFP360 and IRFP362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION

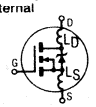


JEDEC TO-247

ABSOLUTE MAXIMUM RATINGS

Parameter		IRFP360	IRFP362	Units
I_D @ T_C = 25°C	Continuous Drain Current	23	20	A
I_D @ T_C = 100°C	Continuous Drain Current	14	13	A
I_{DM}	Pulsed Drain Current ①	92	80	A
P_D @ T_C = 25°C	Max. Power Dissipation	250		W
	Linear Derating Factor	2.0		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	1200 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ①	23		A
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25° C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFP360 IRFP362	400	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFP360	—	0.18	0.20	Ω	V_{GS} = 10V, I_D = 13A
		IRFP362	—	0.20	0.25		
$I_{D(on)}$	On-State Drain Current ③	IRFP360	23	—	—	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ Max. V_{GS} = 10V
		IRFP362	20				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	14	21	—	S(℧)	V_{DS} ≥ 50V, I_{DS} = 13A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 × Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	68	100	nC	V_{GS} = 10V, I_D = 25A V_{DS} = 0.8 × Max. Rating See Fig. 16 (Independent of operating temperature)
Q_{gs}	Gate-to-Source Charge	ALL	—	17	25	nC	
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	24	36	nC	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	22	33	ns	V_{DD} = 200V, I_D ≈ 25A, R_G = 4.3Ω R_D = 7.5Ω See Fig. 15 (Independent of operating temperature)
t_r	Rise Time	ALL	—	94	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	80	120	ns	
t_f	Fall Time	ALL	—	66	99	ns	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
							Modified MOSFET symbol showing the internal inductances. 
C_{iss}	Input Capacitance	ALL	—	4000	—	pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	550	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	97	—	pF	
R_{thJC}	Junction-to-Case	ALL	—	—	0.50	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.24	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	40	°C/W	Typical socket mount
	Mounting torque	ALL	—	—	10	in.•lbs.	Standard 6-32 screw

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.0mH, R_G = 25Ω, Peak I_L = 23A

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	23	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	—	—	92	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.8	V	T_J = 25°C, I_S = 23A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	460	1000	ns	T_J = 25°C, I_F = 25A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.1	7.1	16	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

IRFP360, IRFP362

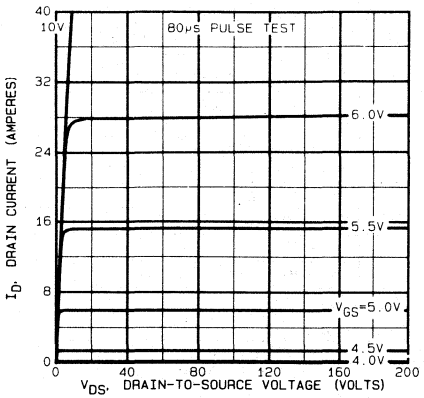


Fig. 1 - Typical output characteristics.

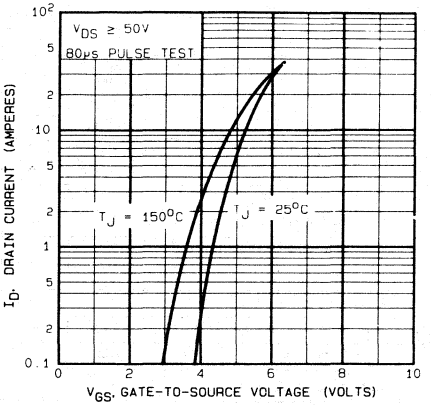


Fig. 2 - Typical transfer characteristics.

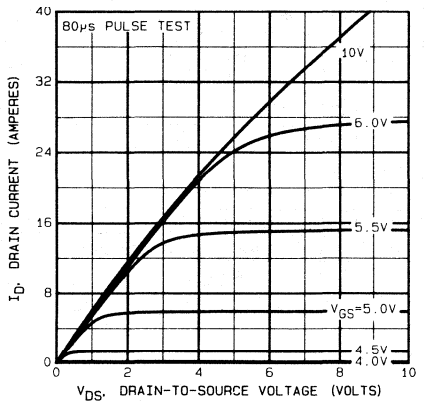


Fig. 3 - Typical saturation characteristics.

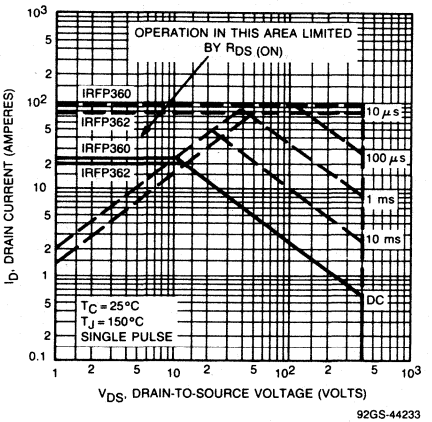


Fig. 4 - Maximum safe operating area.

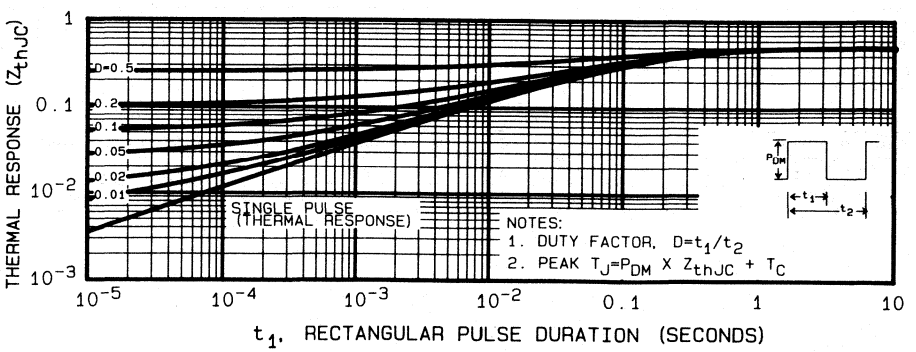


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

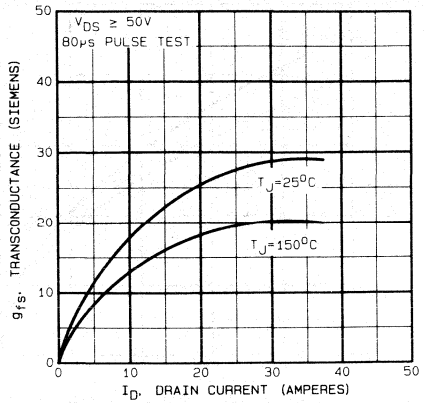


Fig. 6 - Typical transconductance vs. drain current.

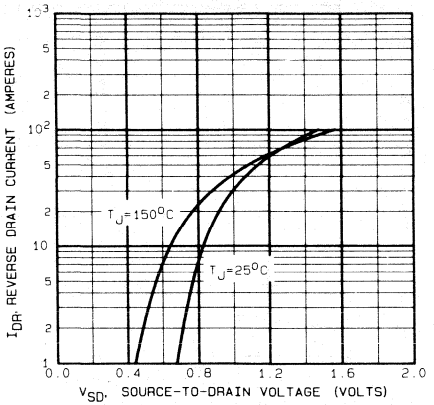


Fig. 7 - Typical source-drain diode forward voltage.

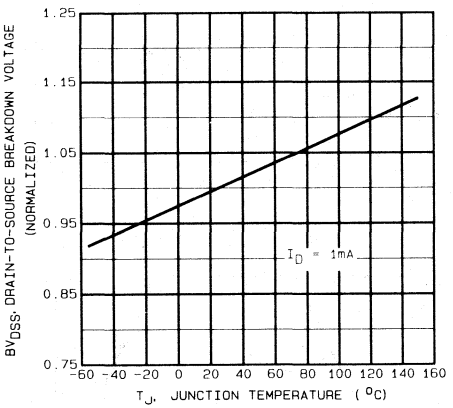


Fig. 8 - Breakdown voltage vs. temperature.

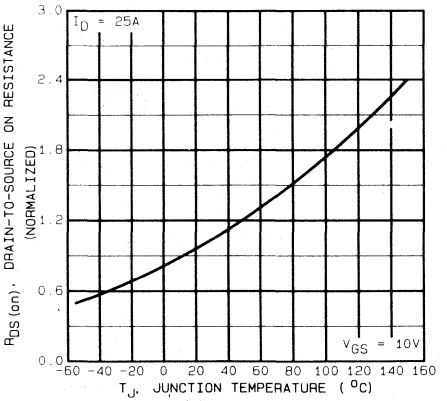


Fig. 9 - Normalized on-resistance vs. temperature.

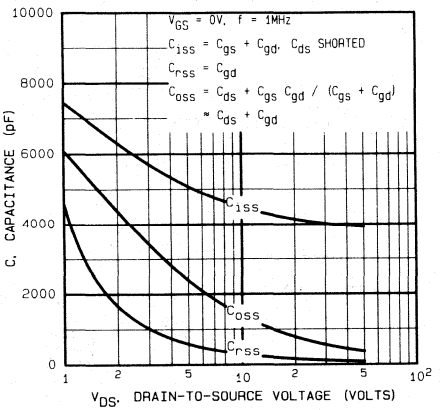


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

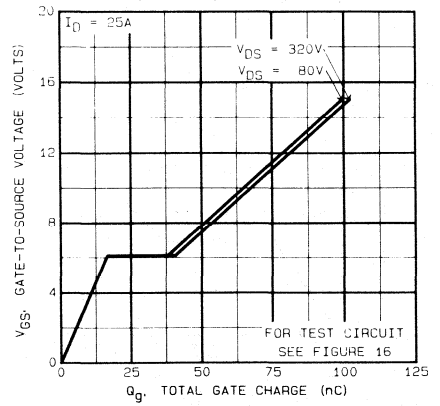


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRFP360, IRFP362

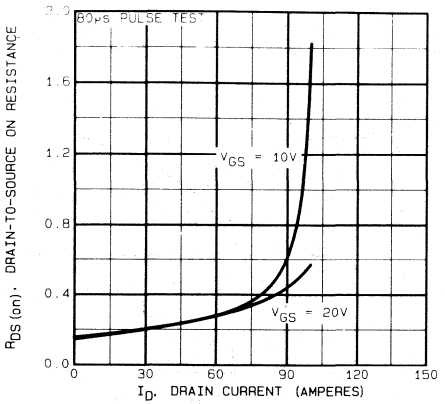


Fig. 12 - Typical on-resistance vs. drain current.

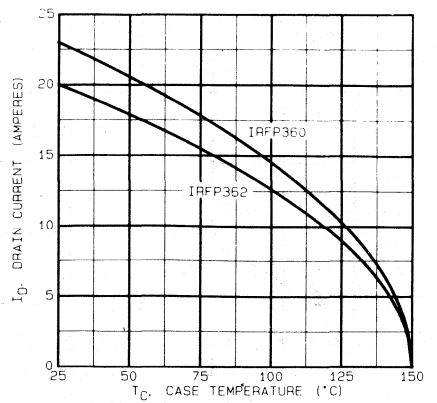


Fig. 13 - Maximum drain current vs. case temperature.

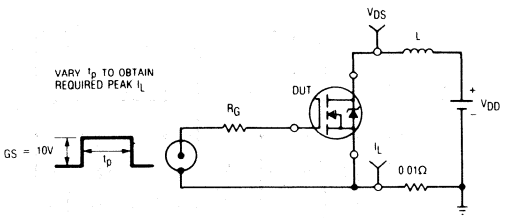


Fig. 14a - Unclamped inductive test circuit.

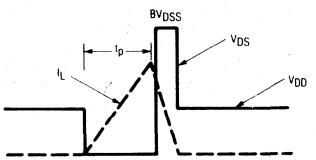


Fig. 14b - Unclamped inductive waveforms.

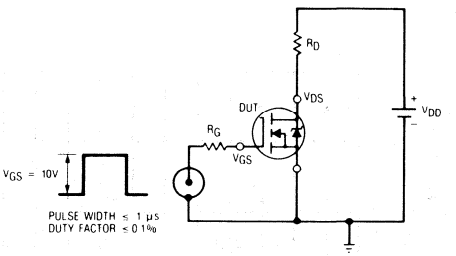


Fig. 15a - Switching time test circuit.

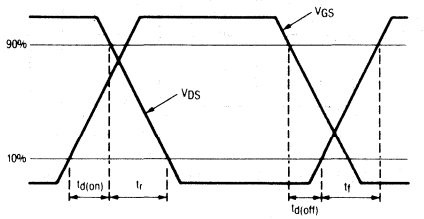


Fig. 15b - Switching time waveforms.

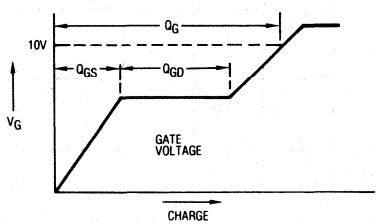


Fig. 16a - Basic gate charge waveform.

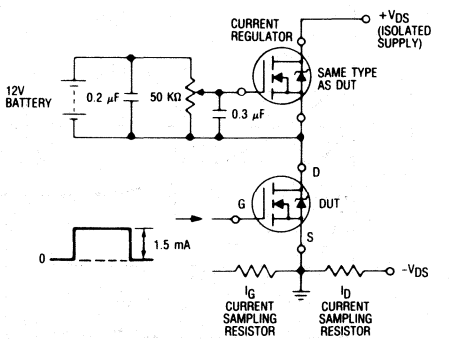


Fig. 16b - Gate charge test circuit.

File Number **2291**

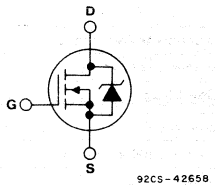
IRFP460, IRFP462

Avalanche-Energy-Rated N-Channel Power MOSFETs

20 A and 17 A, 500 V
$r_{DS(on)}$ = 0.27 Ω and 0.35 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

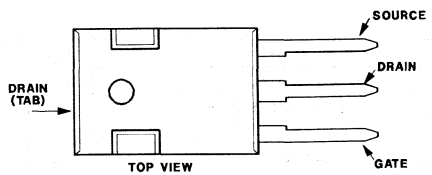


TERMINAL DIAGRAM

The IRFP460 and IRFP462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

ABSOLUTE MAXIMUM RATINGS

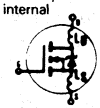
Parameter		IRFP460	IRFP462	Units
I_D @ T_C = 25°C	Continuous Drain Current	20	17	A
I_D @ T_C = 100°C	Continuous Drain Current	12	11	A
I_{DM}	Pulsed Drain Current ①	80	68	A
P_D @ T_C = 25°C	Max. Power Dissipation	250		W
	Linear Derating Factor	2.0		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	960 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ①	20		A
T_J T_{STG}	Operating Junction Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

IRFP460, IRFP462

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25°C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFP460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 11A
		IRFP462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRFP460	20	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max. V_{GS} = 10V
		IRFP462	17				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	13	19	–	S (℧)	V_{DS} = ≥ 50V, I_{DS} = 11A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A
Q_{gs}	Gate-to-Source Charge	ALL	–	18	27	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	93	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D ≈ 21A, R_G = 4.3Ω
t_r	Rise Time	ALL	–	81	120	ns	R_D = 12Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	See Fig. 15
t_f	Fall Time	ALL	–	65	98	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	480	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.50	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.166	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	40	°C/W	Typical socket mount
	Mounting Torque	ALL	–	–	10	in. • lbs.	Standard 6-32 screw

Modified MOSFET symbol showing the internal inductances



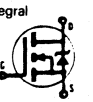
① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.3 mH, R_G = 25Ω, Peak I_L = 20A

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	20	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	80	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D				



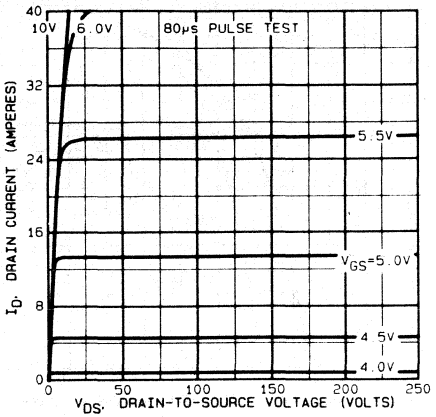


Fig. 1 - Typical output characteristics.

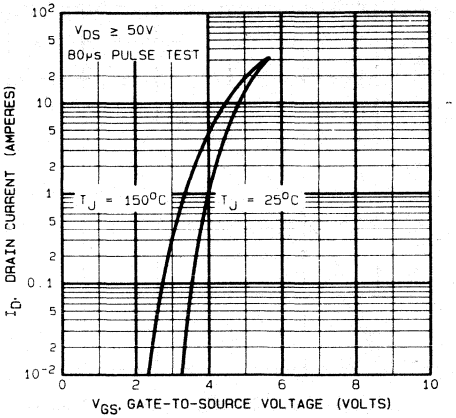


Fig. 2 - Typical transfer characteristics.

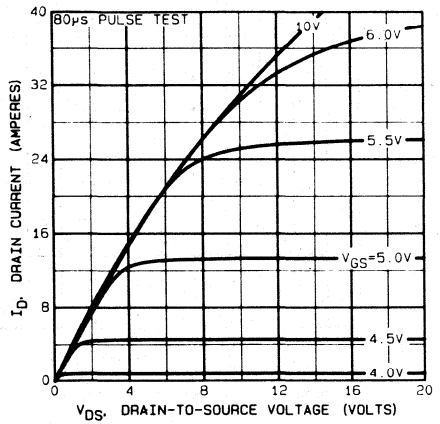


Fig. 3 - Typical saturation characteristics.

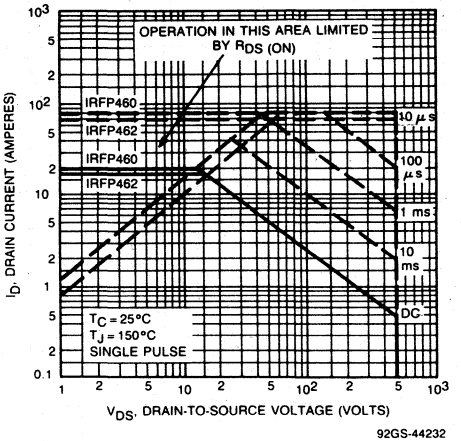


Fig. 4 - Maximum safe operating area.

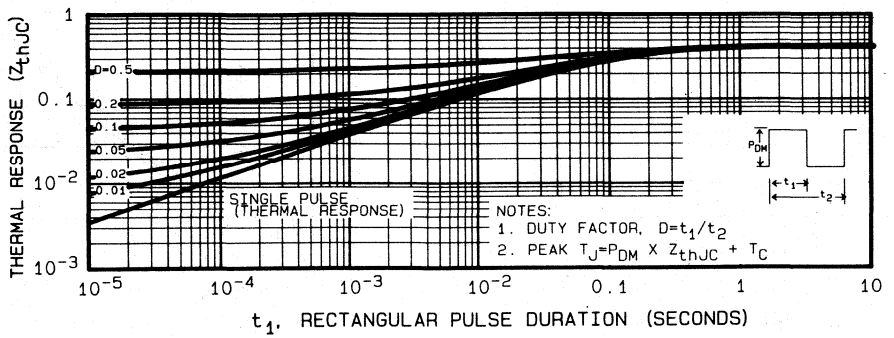


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFP460, IRFP462

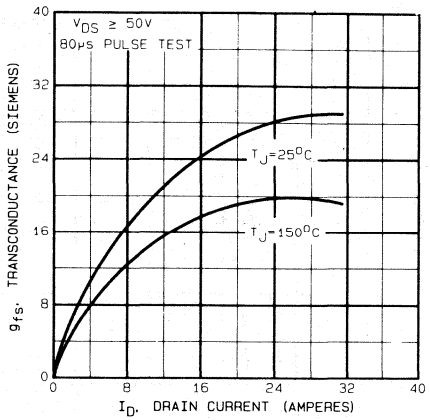


Fig. 6 - Typical transconductance vs. drain current.

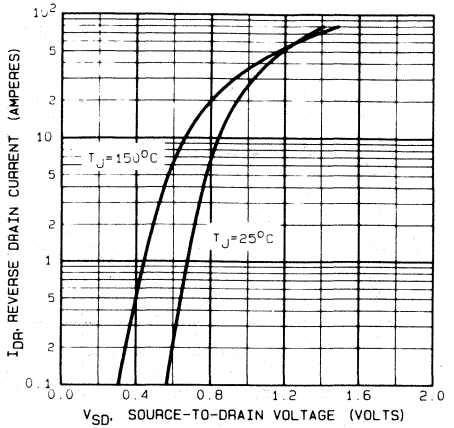


Fig. 7 - Typical source-drain diode forward voltage.

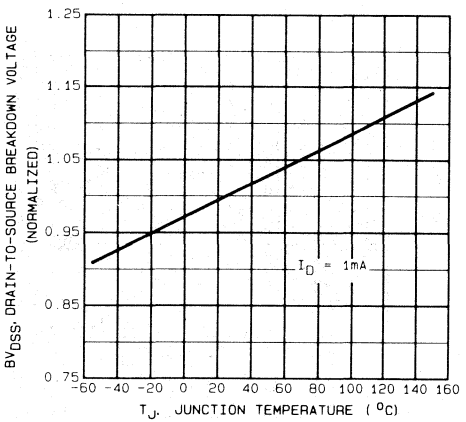


Fig. 8 - Breakdown voltage vs. temperature.

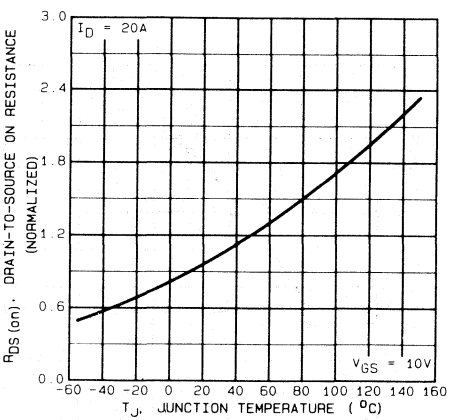


Fig. 9 - Normalized on-resistance vs. temperature.

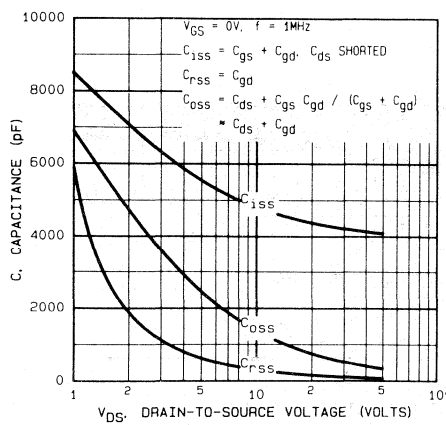


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

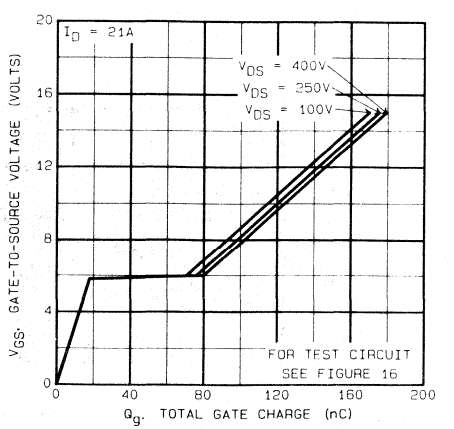


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

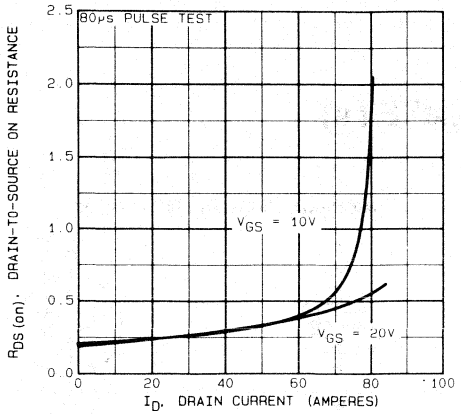


Fig. 12 - Typical on-resistance vs. drain current.

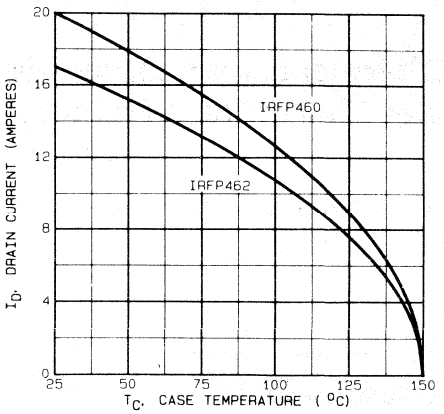


Fig. 13 - Maximum drain current vs. case temperature.

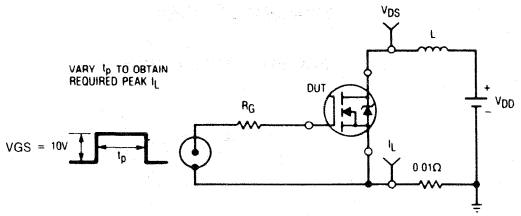


Fig. 14a - Unclamped inductive test circuit.

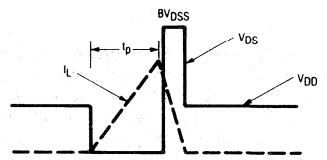


Fig. 14b - Unclamped inductive waveforms.

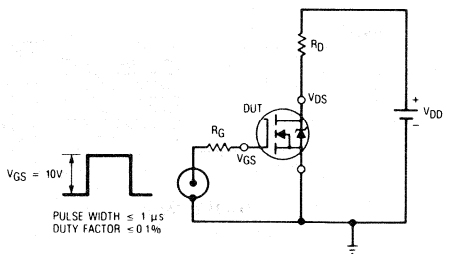


Fig. 15a - Switching time test circuit.

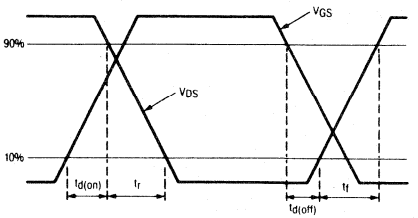


Fig. 15b - Switching time waveforms.

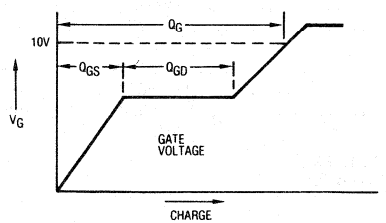


Fig. 16a - Basic gate charge waveform.

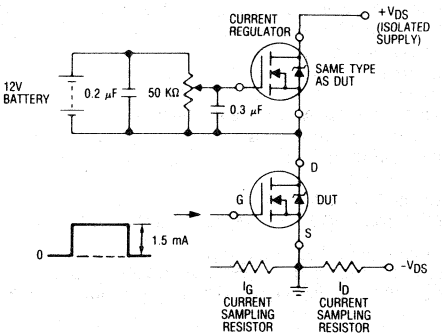


Fig. 16b - Gate charge test circuit.

RFH75N05, RFA100N05

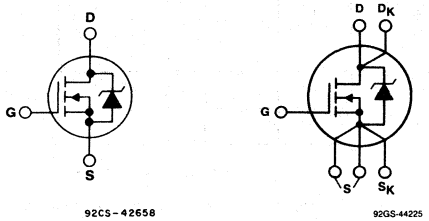
File Number **2275**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

75 A and 100 A, 50 V
$r_{DS(on)}$ = 0.010 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

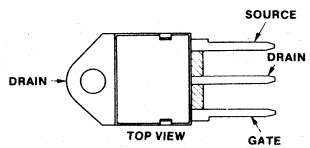
N-CHANNEL ENHANCEMENT MODE



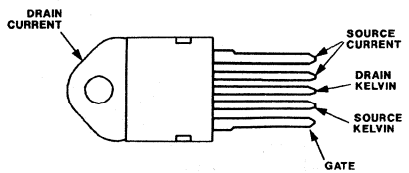
T0-218 (3 Lead) **T0-218 (5 lead)**

TERMINAL DIAGRAM

TERMINAL DESIGNATION



TO-218 (3 Lead)



TO-218 (5 lead)

The RFH75N05 and RFA100N05 n-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFH75N05 is supplied in the T0-218 (3 lead) plastic package, and the RFA100N05 is supplied in the T0-218 (5 lead) plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*	**RFH750N05**	**RFA100N05**
DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V	50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{GS} = 1 MΩ)	50 V	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±20 V	±20 V
DRAIN CURRENT:		
I_D, RMS Continuous	75 A●	100 A
I_{DM}, Pulsed	200 A	300 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{as}	800 mJ†	800 mJ††
AVALANCHE CURRENT, I_{AS}	75 A	100 A
POWER DISSIPATION, P_T:		
At T_C = 25°C	200 W	200 W
Derated above T_C = 25°C	1.60 W/°C	1.60 W/°C
OPERATING AND STORAGE TEMPERATURE, T_J, T_{stg}	-55 to +150°C	-55 to +150°C

● ID Current Limited by package.
† V_{DD} = 10 V, starting T_J = 25°C, L = 230 μHy, I_{peak} = 75 A, R_{gs} = 50 Ω, see Figs. 18 and 19.
†† V_{DD} = 10 V, starting T_J = 25°C, L = 130 μHy, I_{peak} = 100 A, R_{gs} = 50 Ω, see Figs. 18 and 19.

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFH75N05 MIN.	LIMITS RFH75N05 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ I_D = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_c = 150°C		— —	— 50	μA μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V		—	100	nA
On Resistance	$r_{DS(on)}$	I_D = 75 A, V_{GS} = 10 V		—	0.010	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25 V, I_D = 37.5 A R_L = 0.667 Ω $I_{G1} = I_{G2}$ = 3.0 A $V_{GS(CLAMP)}$ = +10 V, -0.5 V		—	125	ns
Turn-On Delay Time	$t_{d(on)}$			—	17 (typ)	ns
Rise Time	t_r			—	75 (typ)	ns
Turn-Off Delay Time	$t_{d(off)}$			—	70 (typ)	ns
Fall Time	t_f			—	17 (typ)	ns
Turn-Off Time	$t_{(off)}$			—	125	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-20 V	V_{DD} = 40 V I_D = 75 A R_L = 0.533 Ω	—	400	nC
Gate Charge at 10 Volts	$Q_{g(10)}$	V_{GS} = 0-10 V		—	220	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0-2 V		—	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 75 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 37.5 A L = 0.2 uH, $I_{G1} = I_{G2}$ = 3.0 A $V_{GS(CLAMP)}$ = +10 V, -0.6 V R_L = 0.667 Ω		—	300	μJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			—	0.625	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

Forward Voltage	V_{SD}	I_{SD} = 75 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 75 A dI_F/dt = 100 A/μs	—	125	ns

RFH75N05, RFA100N05

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFA100N05 MIN.	LIMITS RFA100N05 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_c = 150° C		— —	1 50	μA μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V		—	100	nA
On Resistance	$r_{DS(on)}$	I_D = 100 A, V_{GS} = 10 V		—	0.010	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25 V, I_D = 50 A R_L = 0.50 Ω I_{G1} = I_{G2} = 3.0 A $V_{GS(CLAMP)}$ = +10 V, -0.5 V		—	60	ns
Turn-On Delay Time	$t_{d(on)}$			—	17 (typ)	ns
Rise Time	t_r			—	8 (typ)	ns
Turn-Off Delay Time	$t_{d(off)}$			—	50 (typ)	ns
Fall Time	t_f			—	10 (typ)	ns
Turn-Off Time	$t_{(off)}$			—	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-20 V	V_{DD} = 40 V I_D = 100 A R_L = 0.40 Ω	—	430	nC
Gate Charge at 10 Volts	$Q_{g(10)}$	V_{GS} = 0-10 V		—	230	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0-2 V		—	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 100 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 50 A L = 0.2 uH, I_{G1} = I_{G2} = 3.0 A $V_{GS(CLAMP)}$ = +10 V, -0.6 V R_L = 0.50 Ω		—	500	μJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			—	0.625	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

Forward Voltage	V_{SD}	I_{SD} = 100 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 100 A dI_F/dt = 100 A/μs	—	125	ns

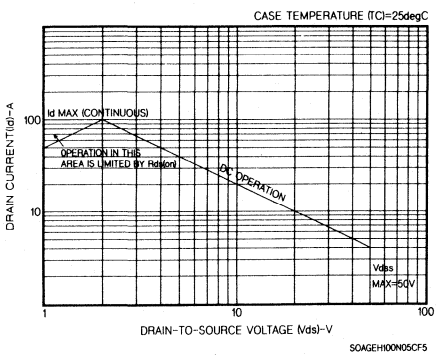


Fig. 1 - Safe-operating-area curve for the RFA100N05. (Curves must be derated linearly with increase in case temperature.)

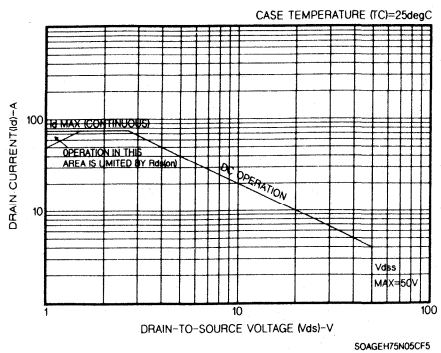


Fig. 2 - Safe-operating-area curve for the RFH75N05. (Curves must be derated linearly with increase in case temperature.)

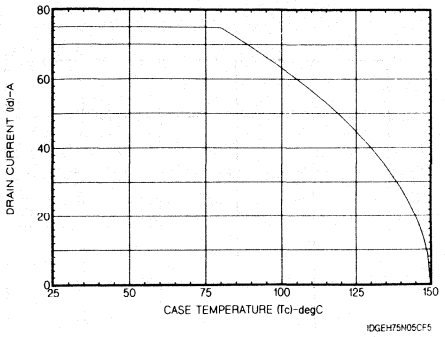


Fig. 3 - Maximum continuous drain current vs. temperature for the RFH75N05.

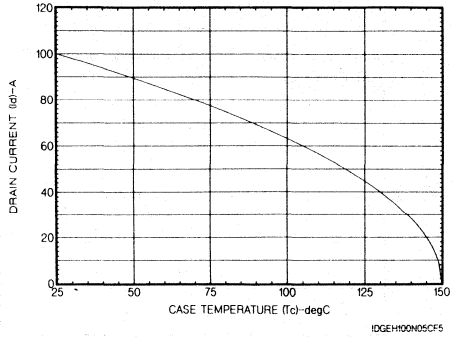


Fig. 4 - Maximum continuous drain current vs. temperature for the RFA100N05.

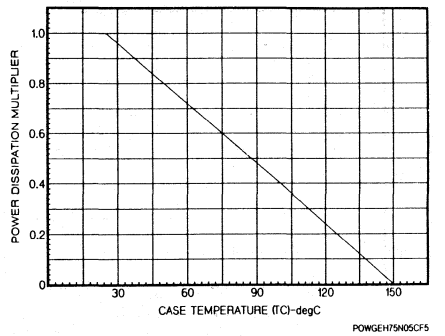


Fig. 5 - Normalized power dissipation vs. temperature derating curve for all types.

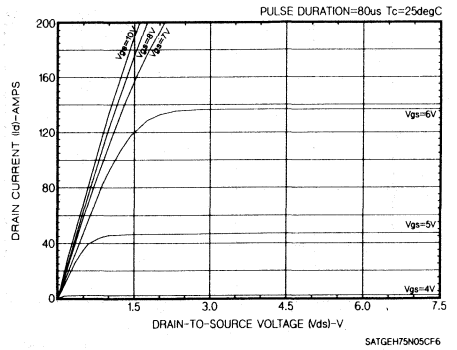


Fig. 6 - Typical saturation characteristics for the RFH75N05.

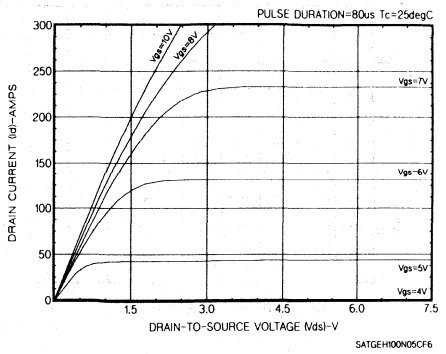


Fig. 7 - Typical saturation characteristics for the RFA100N05.

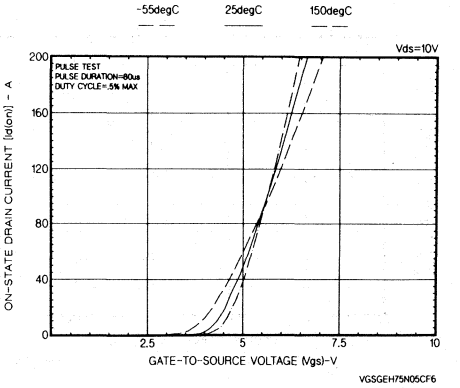


Fig. 8 - Typical transfer characteristics for the RFH75N05.

RFH75N05, RFA100N05

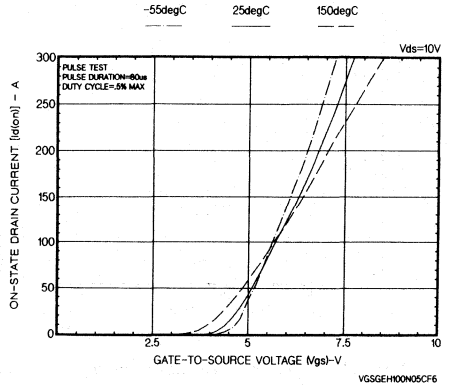


Fig. 9 - Typical transfer characteristics for the RFA100N05.

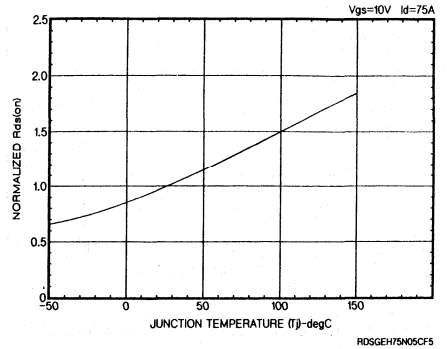


Fig. 10 - Normalized $r_{DS(on)}$ vs. junction temperature for the RFH75N05.

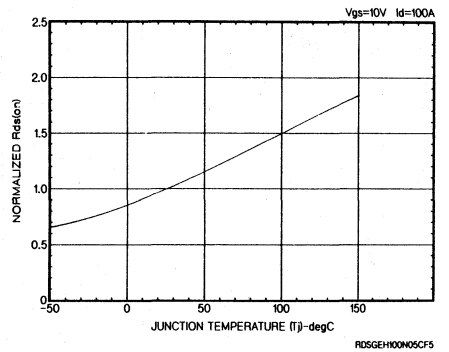


Fig. 11 - Normalized $r_{DS(on)}$ vs. junction temperature for the RFA100N05.

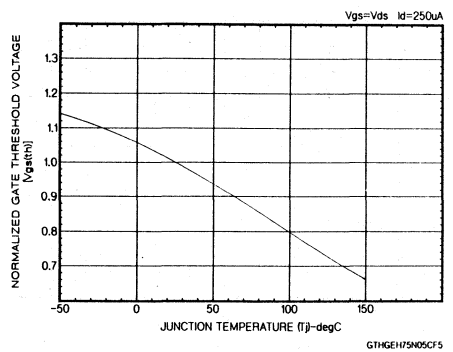


Fig. 12 - Normalized gate threshold voltage for all types.

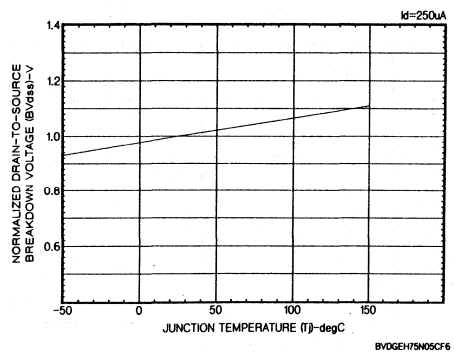


Fig. 13 - Normalized drain-to-source breakdown voltage vs. temperature for all types.

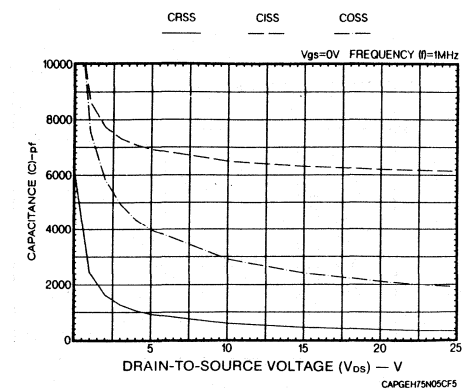


Fig. 14 - Typical capacitance vs. voltage for all types.

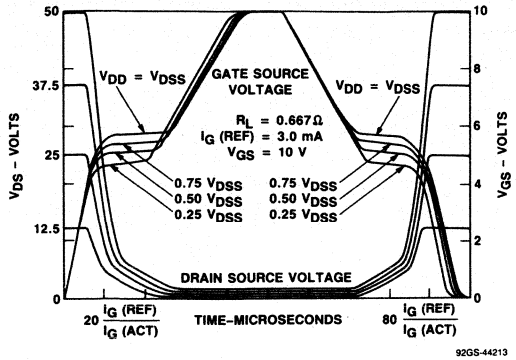


Fig. 15 - Normalized switching waveforms for constant gate-current for the RFH75N05. (Refer to RCA Application Notes AN-7254 and AN-7260.)

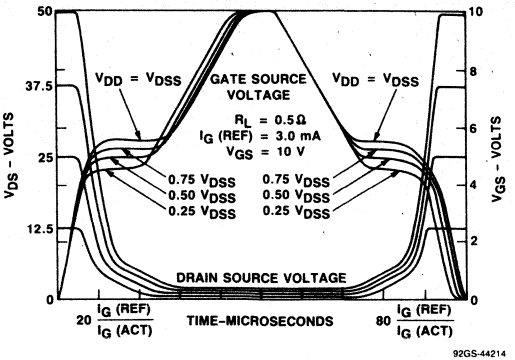


Fig. 16 - Normalized switching waveforms for constant gate-current for the RFA100N05. (Refer to RCA Application Notes AN-7254 and AN-7260.)

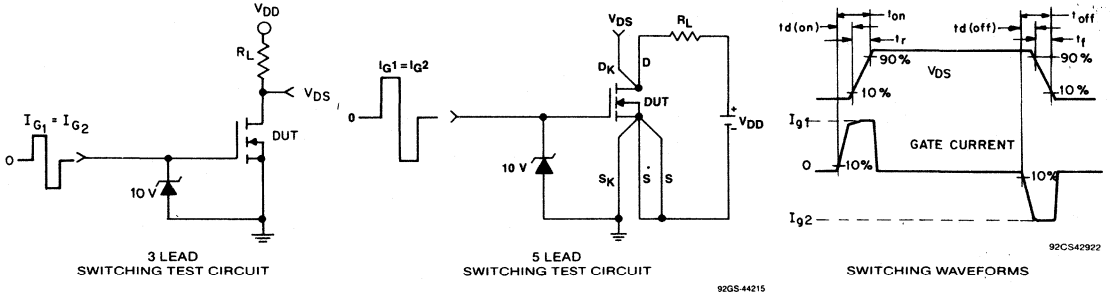


Fig. 17 - Resistive switching.

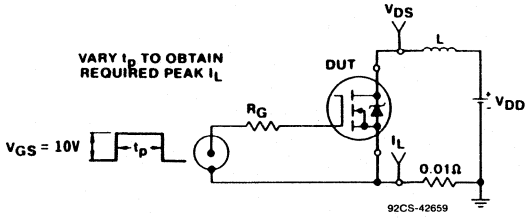


Fig. 18 - Unclamped energy test circuit.

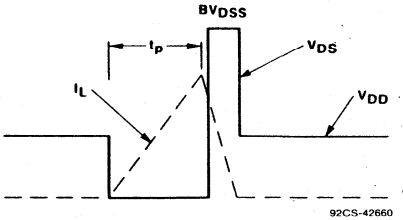


Fig. 19 - Unclamped energy waveforms.

Integrated Power Systems

GSI510, IGT5E10CS

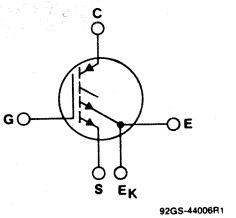
File Number **2326**

Current Sensing IGT™ Transistors
Insulated Gate Bipolar Transistors

10 A, 500 V
$r_{DS(on)}$ = 0.27 Ω

Features:
- *Low $V_{CE(sat)}$ - 2.5 V typ. @ 10 A*
- *Ultra-fast turn-on - 100 ns typical*
- *Polysilicon MOS gate - voltage controlled turn on/off*
- *High current handling - 10 A @ 100° C case*
- *Current sensing pilot*

TERMINAL DIAGRAM



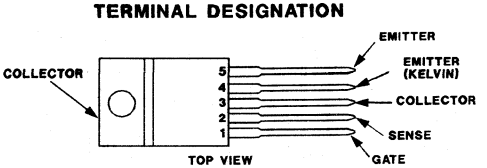
92GS-44006R1

N-CHANNEL ENHANCEMENT MODE

The GSI510 and/or IGT5E10CS Series IGT™ Transistor (Insulated Gate Bipolar Transistor) is a MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs, bipolar transistors, and current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGT™ Transistor are also similar to power MOSFETs. An important difference is the equivalent $r_{ds(on)}$ drain resistance which is modulated to a low value (10 times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between 25° C and 150° C offering extended power handling capability.

The IGT™ Transistor is ideal for many high-voltage switching applications operating at low frequencies and where low conduction losses are essential, such as AC and DC motor controls, power supplies and drivers for solenoids, relays, and contactors.

TERMINAL DESIGNATION



TO-220 (5 LEAD)

MAXIMUM RATINGS

COLLECTOR-EMITTER VOLTAGE (V_{GE} = 0 V)	V_{CES}	500	V
COLLECTOR-GATE VOLTAGE (R_{GE} = 1 MΩ)	V_{CGR}	500	V
CONTINUOUS DRAIN CURRENT	I_C		
At T_c = 100° C		10	A
At T_c = 25° C		18	A
PULSED COLLECTOR CURRENT	I_{CM}•	40	A
GATE-EMITTER VOLTAGE	V_{GE}	±25	V
TOTAL POWER DISSIPATION	P_D		
At T_C = 25° C		75	W
Derate Above 25° C		0.6	W/° C
OPERATING AND STORAGE JUNCTION TEMPERATURE RANGE	T_J, T_{stg}	-55 to +150	°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R_{\theta JC}$	1.67	°C/W
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES	T_L		
1/8 inch from case for 5 seconds		260	°C

•Repetitive Rating: Pulse width limited by maximum junction temperature.
Gate control turn-off not allowed above 50 amperes.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS T_C = 25° C Unless Otherwise Specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 25 μA	500	—	—	V
Collector Cut-off Current	I_{CES}	V_{CE} = Max. Rating, V_{GE} = 0 V, T_C = 25° C	—	—	250	μA
		V_{CE} = Max. Rating x 0.8, V_{GE} = 0 V, T_C = 150° C[1]	—	—	4	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V	—	—	±500	nA
ON CHARACTERISTICS[2]						
Gate Threshold Voltage	$V_{GE(th)}$	V_{CE} = V_{GE}, I_C = 250 μA T_C = 25°C T_C = 150°C	2 —	4 2.5	5 —	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_{GE} = 15 V, I_C = 10 A, T_C = 25°C V_{GE} = 15 V, I_C = 10 A, T_C = 150°C V_{GE} = 10 V, I_C = 10 A, T_C = 25°C	— — —	2.5 2.8 2.9	2.7 — —	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ies}	V_{GE} = 0 V	—	1050	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25 V	—	340	—	pF
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	10	—	pF
SWITCHING CHARACTERISTICS[2] (See Figs. 8 & 9)						
Turn-On Delay Time	$t_{d(on)}$	Resistive Load, T_J = 125°C	—	100	—	ns
Rise Time	t_r	I_C = 10 A, V_{CE} = 400 V	—	100	—	ns
Turn-Off Delay Time	$t_{d(off)}$	V_{GE} = 15 V	—	0.4	—	μs
Fall Time	t_f	$R_{G(on)}$ = 50 Ω, $R_{G(off)}$ = 100 Ω	—	2.5	—	μs
Turn-Off Delay Time	$t_{d(off)}$	Inductive Load, T_J = 125°C	—	0.8	1.2	μs
Fall Time	t_f	L = 45 μH, I_C = 10 A	—	0.8	1.0	μs
Equivalent Fall Time	$t_{f(eq)}$	$V_{CE(clamp)}$ = 400 V, V_{GE} = 15 V	—	0.6	0.8	μs
Turn-Off Switching Losses	E_f	$R_{G(on)}$ = 50 Ω, $R_{G(off)}$ = 100 Ω	—	1.6	2.0	mJ
PILOT CHARACTERISTICS[2] [3] [4]						
Pilot - Emitter Kelvin Voltage I_C = 5 A I_C = 10 A I_C = 20 A	V_{PEK}	V_{GE} = 15 Vdc, R_P = 2 KΩ	 — 1.4 —	 1.25 1.67 2.06	 — 1.8 —	V

[1] Applies for 3.3°C per watt maximum thermal resistance, case-to-ambient.
[2] Pulse test: Pulse widths ≤ 300 μs, duty cycle ≤ 2%.
[3] Refer to Fig. 10.
[4] When Not in Use Connect E_P to Emitter.

GSI510, IGT5E10CS

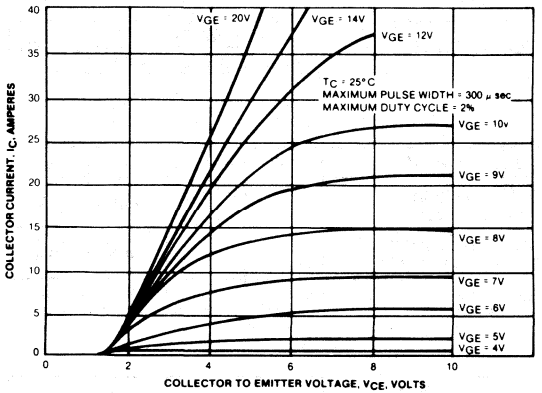


Fig. 1 - Typical output characteristics.

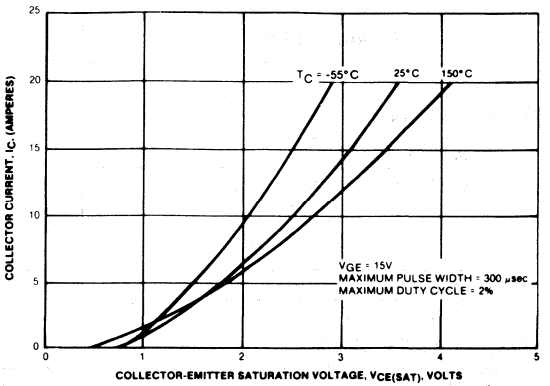


Fig. 2 - Typical collector-emitter saturation voltage.

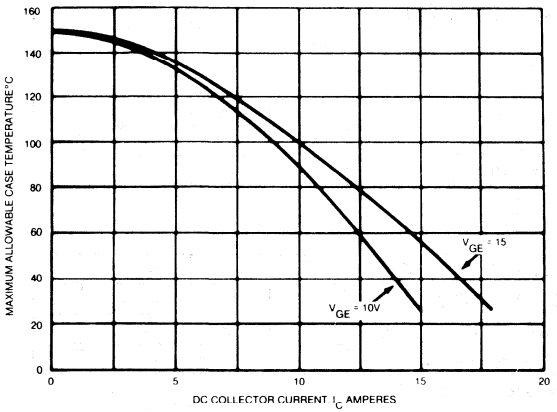


Fig. 3 - Maximum allowable case temperature vs. DC collector current.

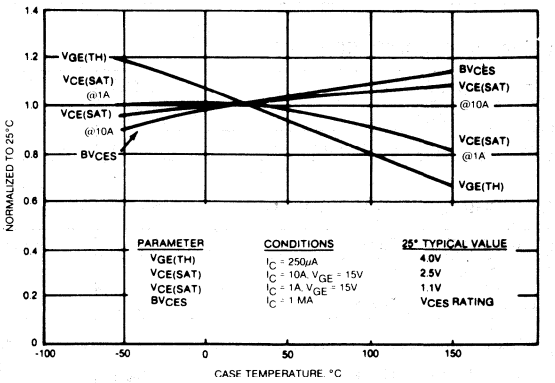


Fig. 4 - Typical temperature dependence of parameters.

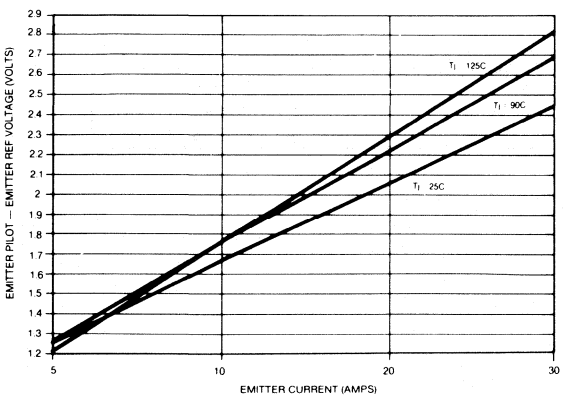


Fig. 5A - Typical emitter pilot characteristics 2 Kohm pilot resistor.

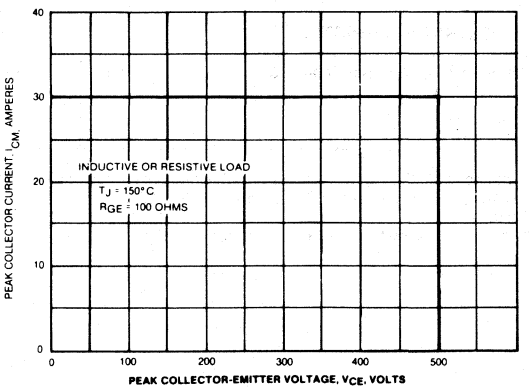


Fig. 5B - Turn-off safe operating area.

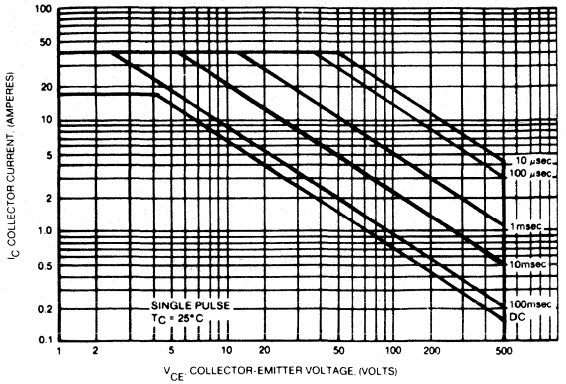


Fig. 6 - Turn-on safe operating area.

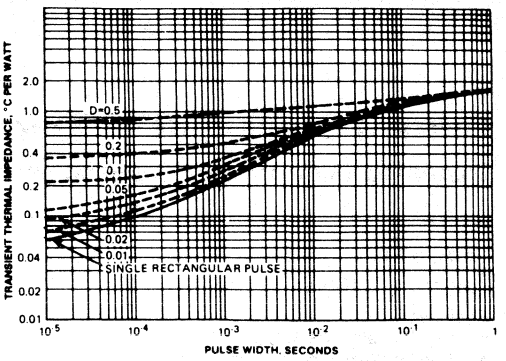


Fig. 7 - Maximum transient thermal impedance.

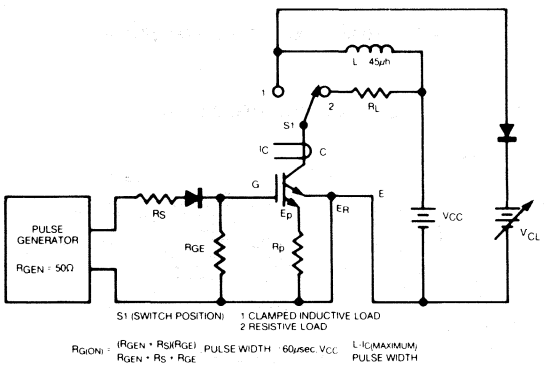


Fig. 8 - Basic switching test circuit.

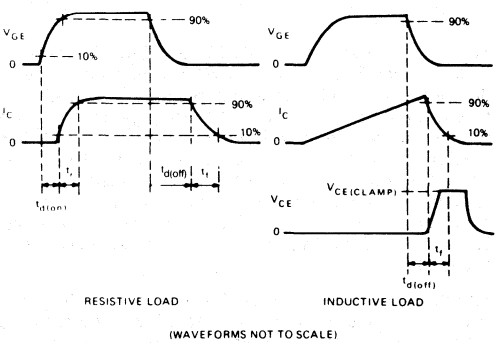


Fig. 9 - Switching waveforms.

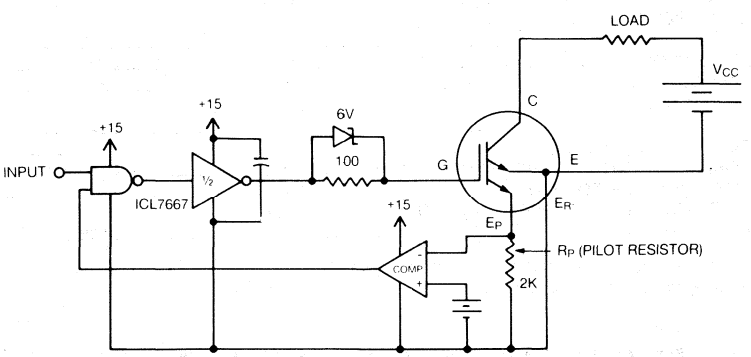


Fig. 10 - Typical circuit utilizing the emitter pilot for overcurrent protection.

GSI525, IGT7E20CS

File Number **2327**

Current Sensing IGT™ Transistors

Insulated Gate Bipolar Transistors

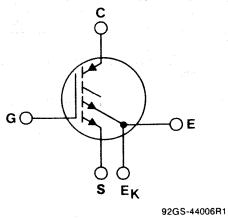
25 A, 500 V

$r_{DS}(on)$ = 0.105 Ω

Features:

- *Low $V_{CE}(sat)$ - 1.8 V typ. @ 25 A*
- *Ultra-fast turn-on - 150 ns typical*
- *Polysilicon MOS gate - voltage controlled turn on/off*
- *High current handling - 25 A @ 85° C case*
- *Current sensing pilot*

TERMINAL DIAGRAM

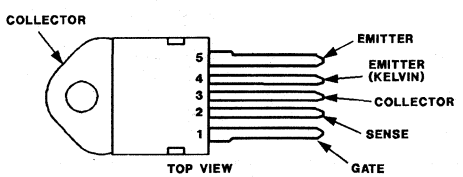


N-CHANNEL ENHANCEMENT MODE

The GSI525 and/or IGT7E20CS IGT™ Transistor (Insulated-Gate Bipolar Transistor) is a MOS-Gated power-switching device combining the best features of power MOSFETs and bipolar transistors with current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses of bipolar transistors. The gate characteristics of the IGT™ Transistor are similar to power MOSFETs but its equivalent $r_{ds}(on)$ drain resistance is ten times lower and varies only moderately between 25° C and 150° C, thus offering extended power handling capability.

The IGT™ Transistor is ideal for many high voltage switching applications up to 5 kHz where low conduction losses are essential; ac and dc motor controls, power supplies and drivers for solenoids, relays, and contactors.

TERMINAL DESIGNATION



TO-218 (5 LEAD)

MAXIMUM RATINGS

COLLECTOR-EMITTER VOLTAGE (V_{GE} = 0 V)	V_{CES}	500	V
COLLECTOR-GATE VOLTAGE (R_{GE} = 1 MΩ)	V_{CGR}	500	V
CONTINUOUS DRAIN CURRENT	I_C		
At T_C = 85° C		25	A
PULSED COLLECTOR CURRENT	I_{CM}•	80	A
GATE-EMITTER VOLTAGE	V_{GE}	±20	V
TOTAL POWER DISSIPATION	P_D		
At T_C = 25° C		125	W
Derate Above 25° C		1	W/° C
OPERATING AND STORAGE JUNCTION TEMPERATURE RANGE	T_J, T_{stg}	-40 to +150	° C
THERMAL RESISTANCE, JUNCTION TO CASE	$R_{\theta JC}$	1	° C/W
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES	T_L		
1/8 inch from case for 5 seconds		260	° C

•Repetitive Rating: Pulse width limited by maximum junction temperature. Gate control turn-off not allowed above 50 amperes.

Harris Semiconductor IGBT product is covered by one or more of the following U.S. patents:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,532,534	4,567,641
4,587,713	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162
4,644,637	4,682,195	4,684,413	4,717,679	4,794,432	4,801,986	4,803,533
4,809,045	4,810,665					

ELECTRICAL CHARACTERISTICS, T_C = 25° C Unless Otherwise Specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 250 μA	500	—	—	V
Collector Cut-off Current	I_{CES}	V_{CE} = Max. Rating V_{GE} = 0 V, T_C = 25° C	—	—	250	μA
		V_{CE} = Max. Rating x 0.8 V_{GE} = 0 V, T_C = 125° C(1)	—	—	4	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V	—	—	±500	nA
ON CHARACTERISTICS(2)						
Gate Threshold Voltage	$V_{GE}(th)$	V_{CE} = V_{GE}, I_C = 500 μA				V
		T_C = 25° C	2	4	5.5	
		T_C = 150° C	—	2	—	
Collector-Emitter Saturation Voltage	$V_{CE}(sat)$	V_{GE} = 15 V, I_C = 25 A				
		T_C = 25° C	—	1.8	2.6	
		T_C = 150° C	—	1.9	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ies}	V_{GE} = 0 V	—	2300	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25 V	—	250	—	
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	35	—	
SWITCHING CHARACTERISTICS(2) (See Figs. 8 & 9)						
Turn-on Delay Time	$t_d(on)$	Resistive Load, T_J = 150° C	—	100	—	ns
Rise Time	t_r	I_C = 25 A, V_{CE} = 400 V	—	150	—	
Turn-off Delay Time	$t_d(off)$	V_{GE} = 15 V	—	0.6	—	μs
Fall Time	t_f	$R_G(on)$ = 50 Ω, $R_G(off)$ = 50 Ω	—	3	—	
Turn-off Delay Time	$t_d(off)$	Inductive Load, T_J = 150° C L = 45 μH, I_C = 25 A	—	1.5	2.5	μs
Fall Time	t_f	V_{CE}(clamp) = 400 V, V_{GE} = 15 V	—	1.2	1.6	
Turn-off Switching Losses	E_f	$R_G(on)$ = 50 Ω, $R_G(off)$ = 50 Ω	—	5	8	mJ
PILOT CHARACTERISTICS(2)(3)(4)						
Pilot - Emitter Kelvin Voltage	V_{PEK}	V_{GE} = 15 Vdc, R_P = 1 KΩ				V
I_C = 20 A			1	1.3	1.6	
I_C = 30 A			—	1.45	—	
I_C = 40 A			—	1.7	—	

(1) Applies for 3.3° C per watt maximum thermal resistance, case to ambient.

(2) Pulse test: Pulse widths ≤ 300 μs, duty cycle ≤ 2%.

(3) Refer to Fig. 5(a).

(4) When not in use connect P to Emitter.

GSI525, IGT7E20CS

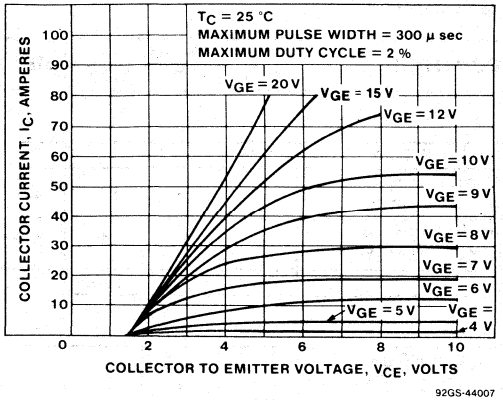


Fig. 1 - Typical output characteristics.

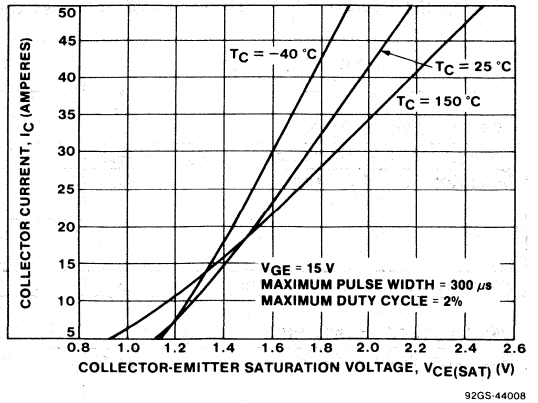


Fig. 2 - Typical collector-emitter saturation voltage

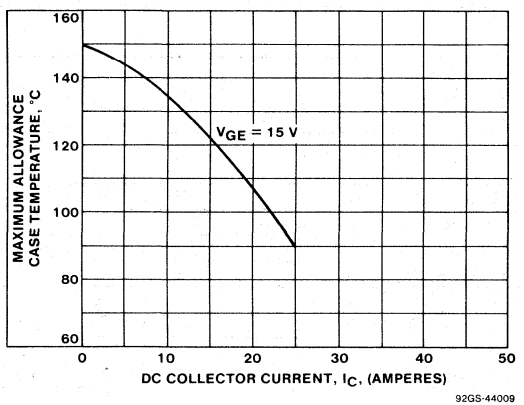


Fig. 3 - Maximum allowable dc collector current vs. case temperature.

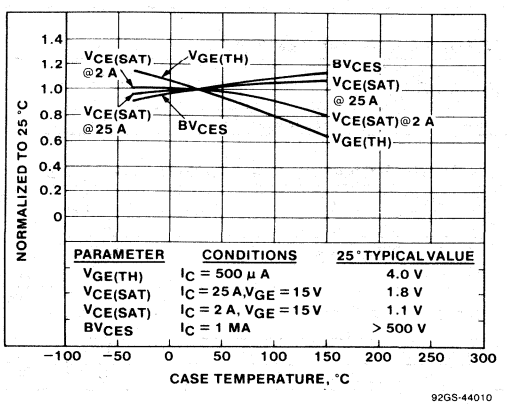


Fig. 4 - Typical temperature dependence of parameters.

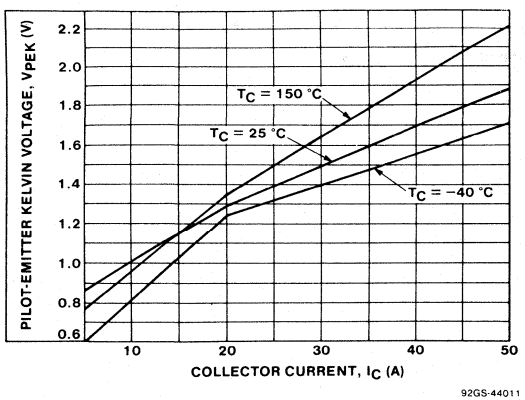


Fig. 5(a) - Typical emitter pilot characteristics - 1 KΩ pilot resistor.

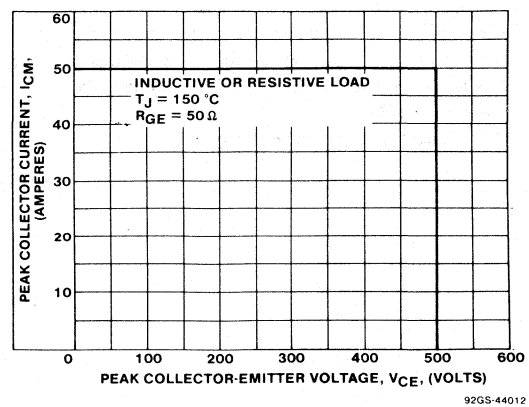


Fig. 5(b) - Turn-off safe operating area.

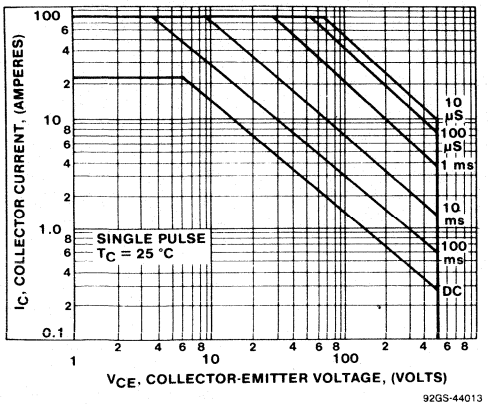


Fig. 6 - Active region safe operating area.

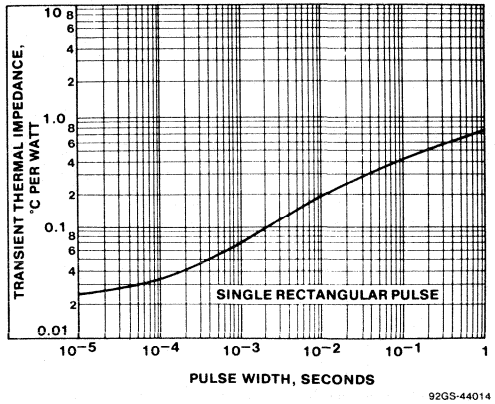


Fig. 7 - Maximum transient thermal impedance.

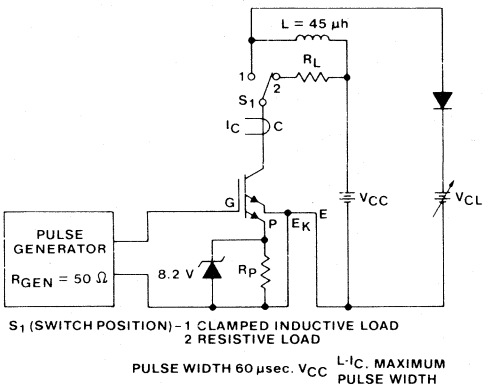


Fig. 8 - Basic switching test circuit.

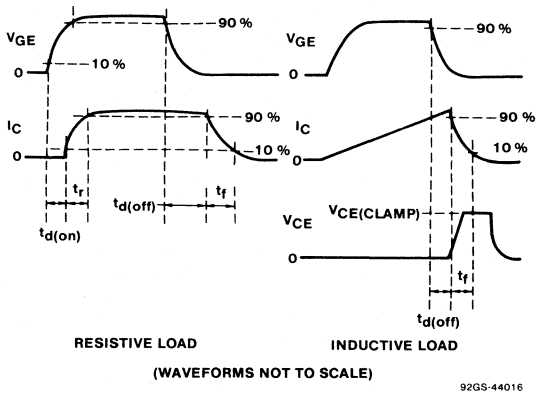


Fig. 9 - Switching waveforms.

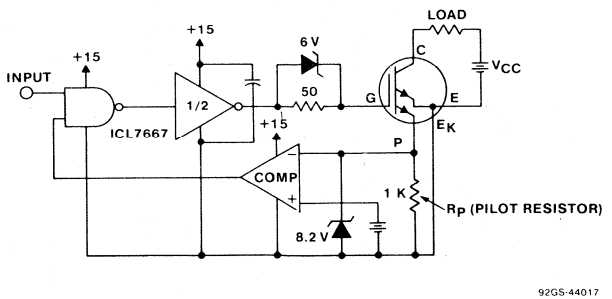
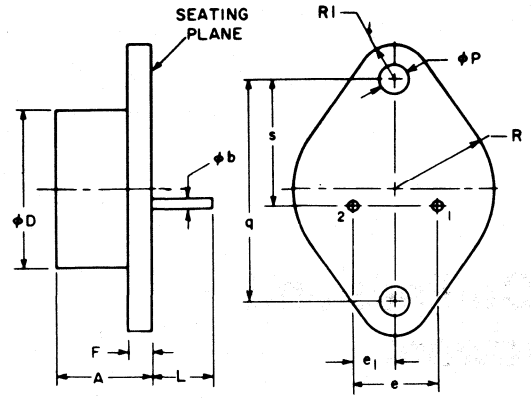


Fig. 10 - Typical circuit utilizing the pilot for overcurrent protection.

Dimensional Outlines and Mounting Hardware

Dimensional Outlines

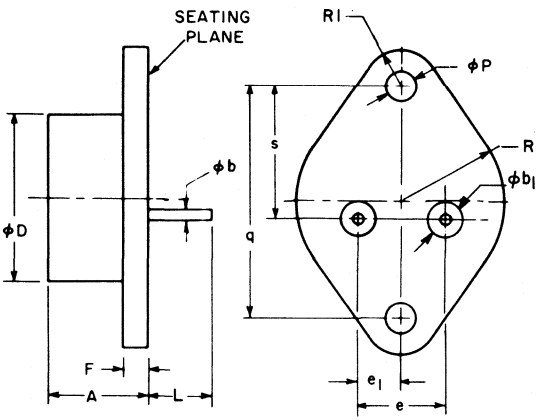
JEDEC TO-204AA



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
ϕb	0.038	0.043	0.966	1.092	
ϕD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	—	0.135	—	3.42	
L	0.312	—	7.93	—	
ϕP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	—	0.525	—	13.33	
R_1	—	0.188	—	4.77	
s	0.655	0.675	16.64	17.14	

92CS-37249R1

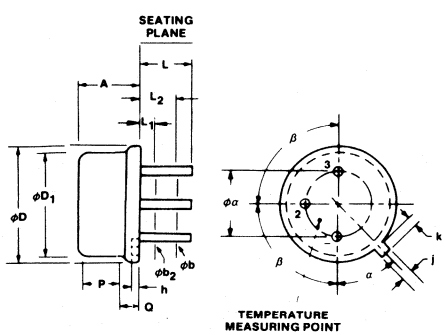
JEDEC TO-204AE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
ϕb	0.057	0.063	1.45	1.60	
$ϕb_1$	0.141 NOM		3.58 NOM		
ϕD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	0.060	0.135	1.53	3.42	
L	0.440	0.480	11.18	12.19	
ϕP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	0.495	0.525	12.58	13.33	
R_1	0.131	0.188	3.33	4.77	
s	0.655	0.675	16.64	17.14	

92CS-37523

JEDEC TO-205AF



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.200 BSC		5.08 BSC		4
A	0.160	0.180	4.07	4.57	
ϕb	0.016	0.021	0.41	0.53	5
$ϕb_2$	0.016	0.019	0.41	0.48	5
ϕD	0.340	0.370	8.64	9.39	
$ϕD_1$	0.315	0.355	8.01	9.01	2
h	0.009	0.041	0.23	1.04	
j	0.028	0.034	0.72	0.86	
k	0.029	0.045	0.74	1.14	1
L	0.500	0.750	12.70	19.05	5
L_1	—	0.050	—	1.27	5
L_2	0.250	—	6.35	—	5
P	0.070	—	1.78	—	2
Q	—	0.050	—	1.27	3
α	45° NOMINAL				
β	90° NOMINAL				

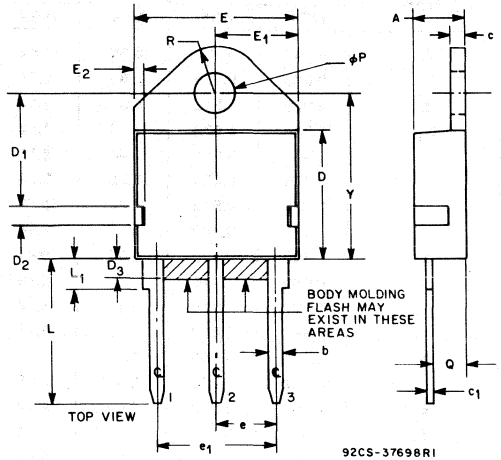
92CS-38248R1

Notes:

1. Dimension k measured from ϕD maximum.
2. $ϕD_1$ shall not vary more than 0.010 in Zone P. This zone controlled for automatic handling.
3. Details of outline in this zone optional.
4. Leads at gauge plane 0.054-0.055 below seating plane shall be within 0.007 radius of positional tolerance at MMC relative to tab at MMC. Device may be measured by direct methods or by gauge and gauging procedure described on JEDEC gauge drawing GS-1.
5. $ϕb_2$ applies between L_1 and L_2. ϕb applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond L minimum.

Dimensional Outlines

JEDEC TO-218AC



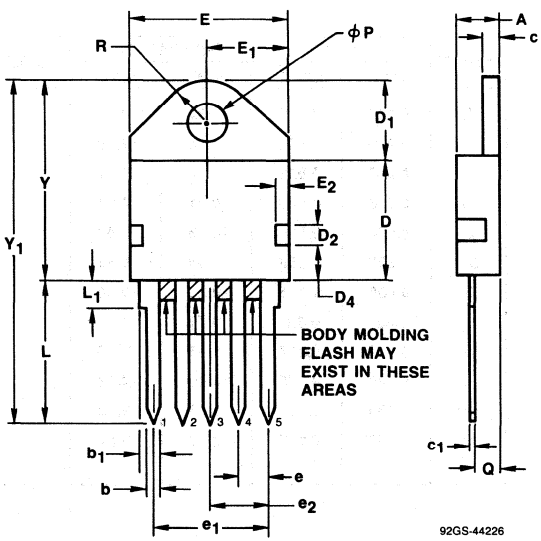
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.165	0.200	4.191	5.080	
b	0.040	0.065	1.016	1.651	
c	0.053	0.065	1.346	1.651	
c_1	0.015	0.030	0.381	0.762	
D	0.460	0.505	11.68	12.827	
D_1	0.395	0.415	10.033	10.541	
D_2	0.070	0.090	1.778	2.286	
D_3	—	0.600	—	1.524	
E	0.610	0.640	15.494	16.256	1
E_1	0.305	0.320	7.747	8.128	
E_2	0.040	0.060	1.016	1.524	
e	0.205	0.225	5.207	5.715	4
e_1	0.420	0.440	10.688	11.176	4
L	0.500	0.632	12.700	16.05	
L_1	—	0.150	—	3.81	2
φP	0.157	0.167	3.988	4.241	
Q	0.093	0.126	2.36	3.200	
R	0.170	0.190	4.318	4.826	1
Y	0.600	0.650	15.24	16.51	

92CS-37698R2

NOTES:

1. Tab outline optional within boundaries of dimensions E and R.
2. Lead dimensions uncontrolled in L_1.
3. Maximum radius of 0.050" on all body edges and corners.
4. Position of lead to be measured 0.185-0.190" from bottom of dimension D.
5. Controlling dimension: inch.

TO-218 (5 Lead) Plastic Package



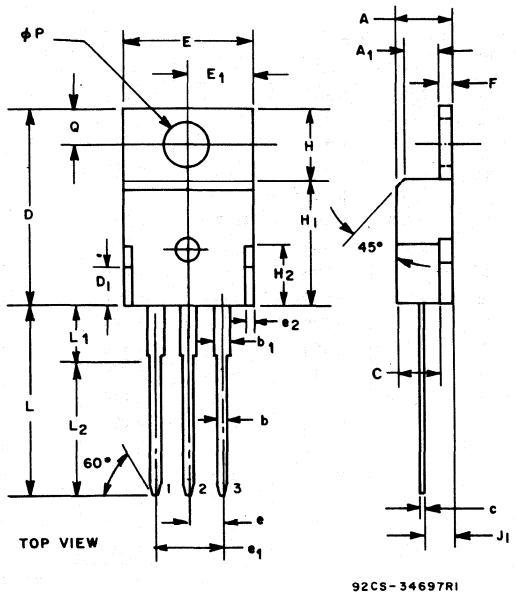
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.190	—	4.826	
b	0.049	0.053	1.243	1.346	
b_1	—	0.075	—	1.905	
c	0.059	0.061	1.499	1.549	
c_1	0.019	0.021	0.483	0.533	
D	0.475	0.495	12.065	12.973	
D_1	—	0.325	—	8.255	
D_2	—	0.080	—	2.032	
D_3	—	0.600	—	15.240	
E	0.615	0.625	15.621	15.875	1
E_1	—	0.310	—	7.874	
E_2	—	0.050	—	1.270	
e	0.105	0.113	2.667	2.870	4
e_1	0.430	0.446	10.922	11.328	4
e_2	0.215	0.223	5.461	5.664	
L	0.575	0.595	14.603	15.113	
L_1	—	0.110	—	2.794	2
φP	0.159	0.163	4.039	4.140	
Q	—	0.120	—	3.048	
R	—	0.181	—	4.597	1
Y	0.800	0.820	20.320	20.828	
Y_1	—	1.395	—	35.433	

NOTES:

1. Tab outline optional within boundaries of dimensions E and R.
2. Lead dimensions uncontrolled in L_1.
3. Maximum radius of 0.050" on all body edges and corners.
4. Position of lead to be measured 0.185-0.190" from bottom of dimension D.
5. Controlling dimension: inch.

Dimensional Outlines

JEDEC TO-220AB



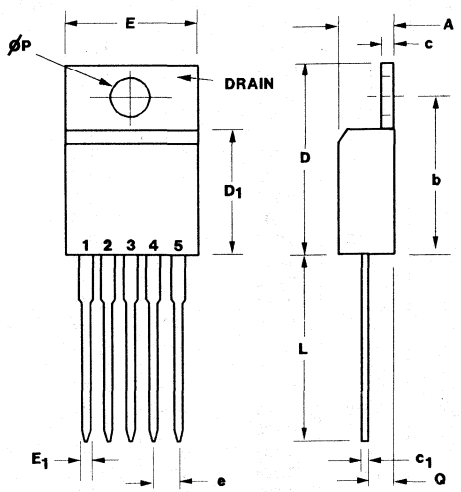
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.140	0.190	3.56	4.82
A_1	0.080	0.085	2.03	2.16
b	0.020	0.045	0.51	1.14
b_1	0.045	0.070	1.14	1.77
C	—	0.125	—	3.18
c	0.015	0.025	0.38	0.63
D	0.560	0.625	14.23	15.87
D_1	—	0.100	—	2.54
E	0.380	0.420	9.66	10.66
e	0.090	0.110	2.29	2.79
e_1	0.190	0.210	4.83	5.33
e_2	—	0.030	—	0.76
F	0.045	0.055	1.14	1.39
H	0.230	0.270	5.85	6.85
H_1	0.355	0.370	9.02	9.40
H_2	—	0.160	—	4.06
J_1	0.080	0.115	2.04	2.92
L	0.500	0.562	12.70	14.27
L_1	—	0.250	—	6.35
L_2	0.400	0.410	10.16	10.41
φP	0.139	0.161	3.531	4.089
Q	0.100	0.120	2.54	3.04

NOTES:

1. Position of lead to be measured 0.250-0.255 in. (6.350-6.477 mm) from case.

92CS-34697R1

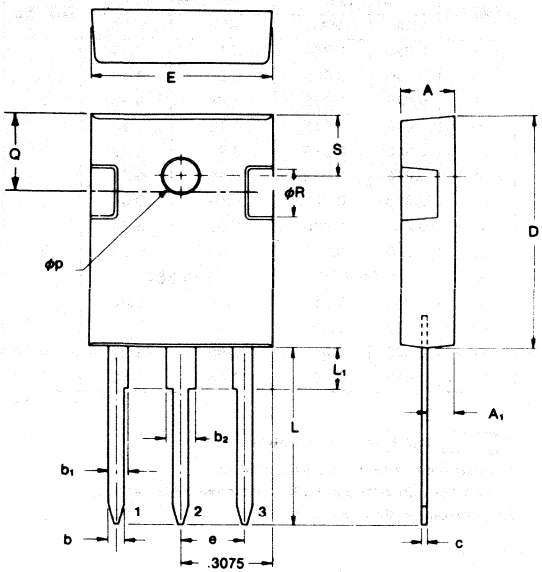
Case Style TO-220 Plastic Package (5 Lead)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.180	4.32	4.57	
b	0.470	0.500	11.94	12.70	
c	0.048	0.052	1.22	1.32	
c_1	0.016	0.020	0.41	0.51	
D	0.580	0.594	14.73	15.09	
D_1	0.330	0.350	8.38	8.89	
E	0.405	0.415	10.29	10.54	
E_1	0.28	0.32	0.71	0.81	
e	0.057	0.077	1.45	1.96	
L	0.530	0.575	13.46	14.61	
φP	0.139	0.149	3.53	3.78	
Q	0.107	0.117	2.72	2.97	

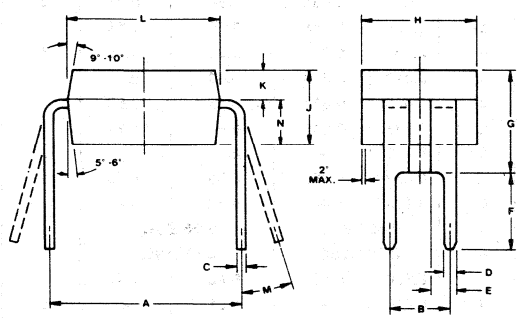
Dimensional Outlines

JEDEC TO-247 Style



SYMBOL	INCHES		mm		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.175	0.185	4.45	4.7	
A_1	0.090	0.115	2.3	2.9	
b	0.046	0.056	1.17	1.42	
b_1	0.060	0.083	1.52	2.11	
b_2	0.095	0.105	2.41	2.67	
c	0.017	0.022	0.43	0.56	
D	0.800	0.820	20.3	20.85	
E	0.610	0.625	15.5	15.85	
e	0.219 BSC		5.56 BSC		
L	0.620	0.635		16.15	
L_1	0.137	0.147	3.5	3.73	
ϕp	0.126	0.135	3.18	3.43	
Q	0.270	0.285	6.86	7.24	
ϕR	0.160	0.166	4.06	4.22	
S	0.215 BSC		5.45 BSC		

4-PIN DIP

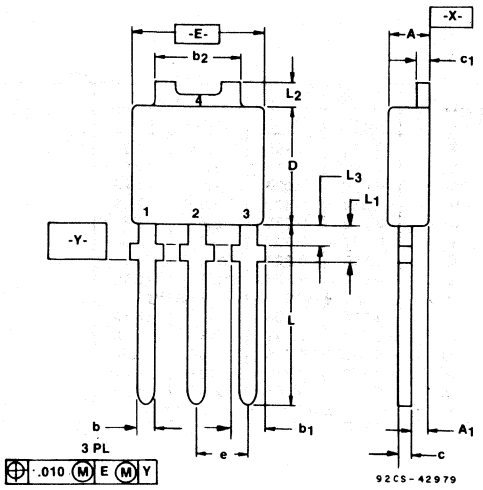


SYMBOL	INCHES		MILLIMETER		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.300	–	7.62	–	
B	.100 NOM.		2.54 NOM.		
C	.013	.017	.34	.43	
D	.020	.024	.51	.60	
E	.035	.045	.89	1.14	
F	.140	.160	3.56	4.06	
G	.160	.180	4.07	4.57	
H	.194	.198	4.93	5.02	
J	.124	.134	3.15	3.40	
K	.034	.044	.87	1.11	
L	.238	.248	6.05	6.29	
M	0°	15°	0°	15°	
N	.085	.095	2.16	2.41	

NOTE: CONTROLLING DIMENSIONS: MILLIMETERS

Dimensional Outlines

JEDEC TO-251AA



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.086	0.094	2.19	2.38	
A_1	0.035	0.045	0.89	1.14	
b	0.025	0.035	0.64	0.89	2
b_1	0.030	0.045	0.76	1.14	
b_2	0.205	0.215	5.21	5.46	4
c	0.018	0.023	0.46	0.58	
c_1	0.018	0.023	0.46	0.58	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	2
e	0.090 BSC		2.28 BSC		
L	0.350	0.380	8.89	9.65	
L_1	0.075	0.090	1.91	2.28	
L_2	0.035	0.050	0.89	1.27	4
L_3	0.045	0.060	1.15	1.52	3

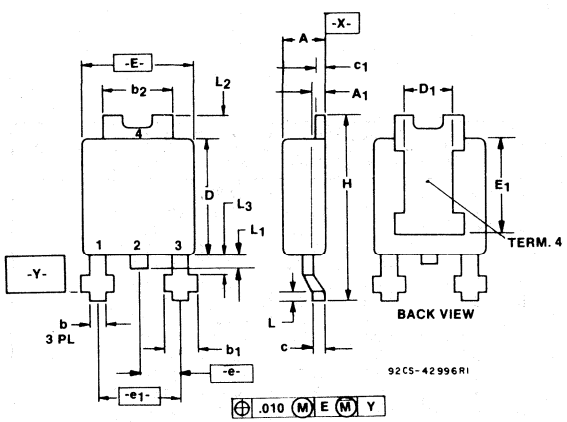
92CS-42862

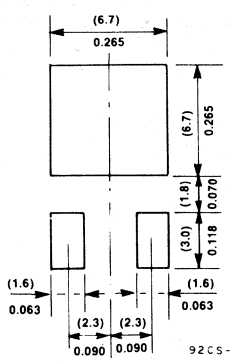
NOTES:

1. -X- is datum surface. (seating plane)
2. -E- and -Y- are datums.
3. Lead dimension uncontrolled in L_3.
4. Tab contour optional within dimensions b_2 and L_2.
5. Controlling dimension: inch.

JEDEC TO-252AA

SM SUFFIX





MINIMUM PAD SIZES RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.086	0.094	2.19	2.38	
A_1	0.035	0.045	0.89	1.14	
b	0.025	0.035	0.64	0.88	2
b_1	0.030	0.045	0.76	1.14	
b_2	0.205	0.215	5.21	5.46	4
c	0.018	0.023	0.46	0.58	
c_1	0.018	0.023	0.46	0.58	
D	0.235	0.245	5.97	6.22	
D_1	0.170	—	4.32	—	1, 5
E	0.250	0.265	6.35	6.73	2
E_1	0.170	—	4.32	—	1, 5
e	0.090 BSC		2.28 BSC		
e_1	0.180 BSC		4.57 BSC		
H	0.370	0.410	9.40	10.42	
L	0.020	—	0.51	—	6
L_1	0.025	0.040	0.64	1.02	
L_2	0.035	0.050	0.88	1.27	4
L_3	0.045	0.060	1.15	1.52	3

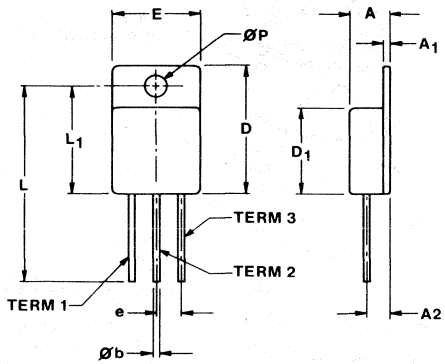
92CS-42863

NOTES:

1. -X- is datum surface. (seating plane)
2. -E- and -Y- are datums.
3. Lead dimension uncontrolled in L_3.
4. Tab contour optional within dimensions b_2 and L_2.
5. D_1 and E_1 establishes a minimum mounting surface for Terminal 4.
6. L is the terminal length for soldering.
7. Controlling dimension: inch.

Dimensional Outlines

JEDEC TO-254AA

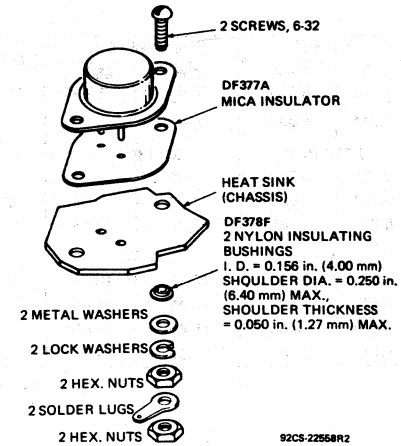


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.249	0.260	6.32	6.60	
A_1	0.040	0.050	1.02	1.27	
A_2	0.150 BSC		3.81 BSC		
øb	0.035	0.045	0.89	1.14	
D	0.790	0.800	20.07	20.32	3
D_1	0.535	0.545	13.59	13.84	
e	0.150 BSC		3.81 BSC		
E	0.535	0.545	13.59	13.84	3
L	1.195	1.236	30.35	31.40	
L_1	0.665	0.685	16.89	17.40	
øP	0.139	0.149	3.53	3.78	

92CS-43444

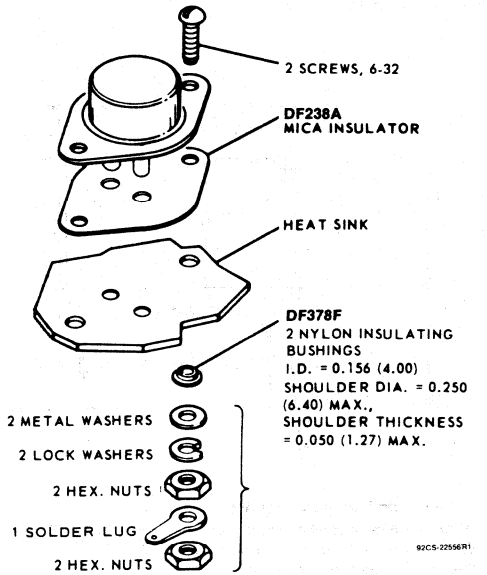
Notes:
1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5.M. 1982.
3. Glass meniscus included in Dim. D and E.
4. Controlling dimension: inch.

Mounting Hardware

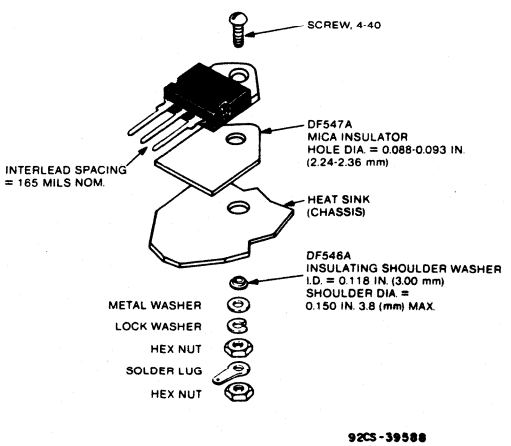


NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 12 in.-lbs. (0.14 kgf m).

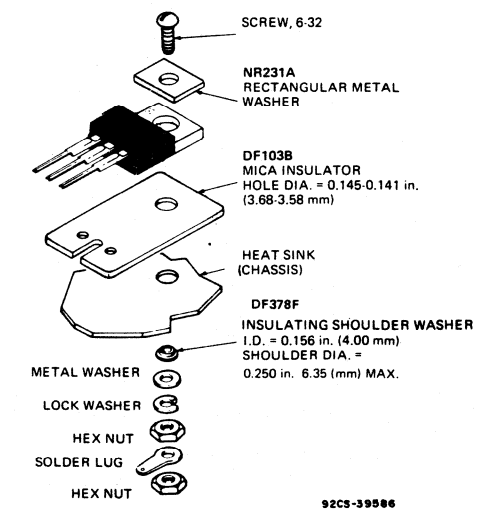
Suggested mounting hardware for JEDEC TO-204AA (formerly JEDEC TO-3)



Suggested mounting hardware for JEDEC TO-204AE (formerly JEDEC TO-3)



Suggested mounting hardware for JEDEC TO-218AC



NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 8 in.-lb. (0.09 kgf m)

Suggested mounting hardware for JEDEC TO-220AB

Application Notes

Publication No.	Title	Page
AN-7244	Understanding Power MOSFETs	14-2
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AN-7260	Power MOSFET Switching Waveforms: A New Insight	14-13
AN-7332	The Application of Conductivity-Modulated Field-Effect Transistors	14-20
SSD-8602	The COMFET-A New High Conductance MOS-Gated Device	14-25
SSD-8603	Improved COMFETs with Fast Switching Speed and High-Current Capability	14-28

Understanding Power MOSFETS

by Tom McNulty

Power MOSFETs (Metal Oxide Semiconductor, Field-Effect Transistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This Note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the body by silicon contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor present a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Fig. 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Fig. 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely diffent from that of a bipolar transistor, which always retain its n-p-n character.

By virture of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful byproduct of the MOSFET process is the internal parasitic diode formed between source and drain, Fig. 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

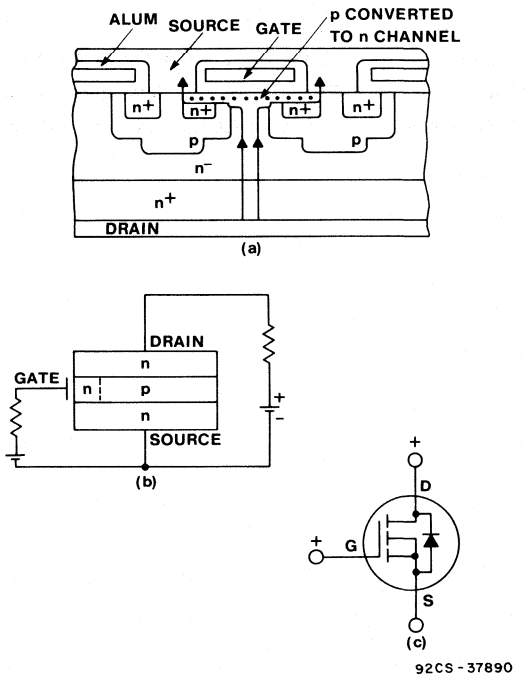


Fig. 1 - The MOSFET, a voltage-controlled device with an electrically isolated gate, uses majority carriers to move current from source to drain (a). The key to MOSFET operation is the creation of the inversion channel beneath the gate when an electric charge is applied to the gate (b). Because of the MOSFET's construction, an integral diode is formed on the device (c), and the designer can use this diode for a number of circuit functions.

Structure

RCA's power MOSFETs are manufactured using the vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cells varies according to the dimensions of the chip. For example, a 120-mil^2 chip contains about 5,000 cells; a 240-mil^2 chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(on)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(on)}$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_n, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(on)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(on)}$ value:

$$r_{DS(on)} = R_N/N$$

where N is the number of cells.

In reality, $r_{DS(on)}$ is composed of three separate resistances. Fig. 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(on)}$. The value of $r_{DS(on)}$ at any point of the curve is found by adding the values of the three components at that point:

$$r_{DS(on)} = R_{bulk} + R_{chan} + R_{ext}$$

where R_{chan} represents the resistance of the channel beneath the gate, and R_{ext} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{bulk} represents the resistance resulting from the narrow neck of n material between the two p layers, as shown in Fig. 1(a), plus the resistance of the current path below the neck and through the body of the device to the drain.

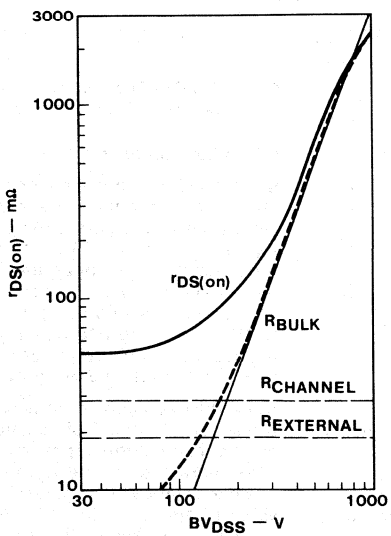
Note in Fig. 2 that R_{chan} and R_{ext} are completely independent of voltage, while R_{bulk} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(on)}$ is dominated by the sum of R_{chan} and R_{ext}. Above 150 volts, $r_{DS(on)}$ is increasingly dominated by R_{bulk}. Table I gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(on)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(on)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{bulk} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and more resistive to support high voltages, the bulk component of resistance rapidly increases (see Fig. 2) and begins to dominate the channel and external resistance. The $r_{DS(on)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(on)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(on)}$ in Fig. 2 holds only for a relatively small chip. Using a larger chip results in a lower value for $r_{DS(on)}$ because a large chip has more cells (See Fig. 3). A larger chip also increases MOSFET breakdown voltage capability.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(on)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the orginal. Although the cost does not rise exponentially, it is substantially more than the original cost.



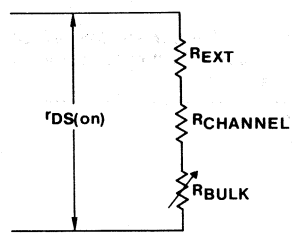


TABLE I
PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

BV_{DSS}	40 V	150 V	500 V
$R_{CHANNEL}$	50 %	23 %	2.4 %
R_{BULK}	35 %	70 %	97 %
$R_{EXTERNAL}$	15 %	7 %	<1 %

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Fig. 2 - The drain-to-source resistance ($r_{DS(on)}$) of a MOSFET is not one but three separate resistance components.

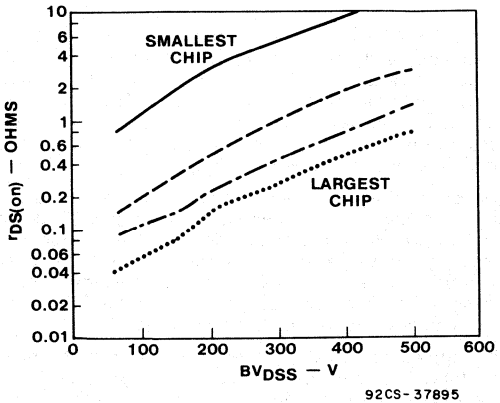


Fig. 3 - As chip size increases, $r_{DS(on)}$ decreases, and voltage handling capability increases.

Effects of Temperature

The high operating temperatures of bipolar transistors are a frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dicates that the carriers slow down as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Fig. 4.

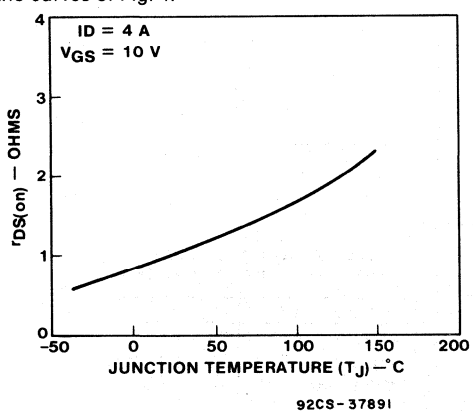


Fig. 4 - MOSFETs have a positive temperature coefficient of resistance, which greatly reduces the possibility of thermal runaway as temperature increases.

The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Fig. 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R, and capacitance, C. The capacitance, called C_{iss} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

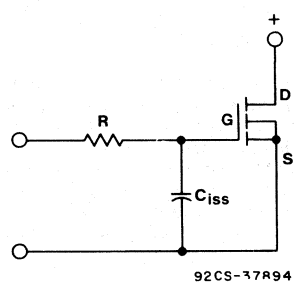


Fig. 5 - A MOSFET's switching speed is determined by its input resistance R and its input capacitance C_{iss}.

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure (R in Fig. 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFET in high-frequency (greater than 20 MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from data-sheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20 Ω/□. But whereas the total R value is not found on data sheets, the C value (C_{iss}) is; it is recorded as both a maximum value and in graphical form as

a function of drain-to-source voltage. The value of C_{iss} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1 to 10 MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic, shown in Fig. 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage ($_{gs}$). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{gs} level required to operate a MOSFET, note, from Fig. 6, that the device is not turned on (no drain current flows) unless V_{gs} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally V_{gs} for many types of DMOS devices is at least 2 volts. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Fig. 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10 volts, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5 volts, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of 10 volts, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

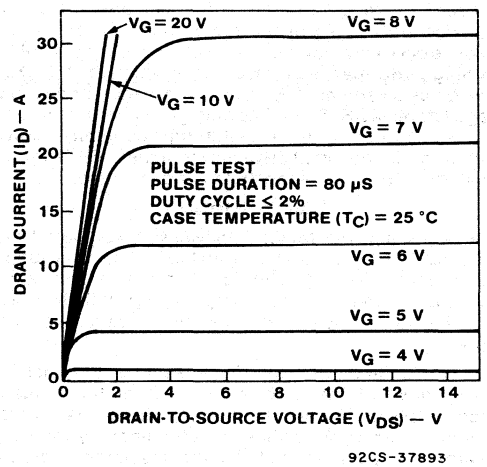


Fig. 6 - MOSFETs require a high input voltage (at least 10 V) in order to deliver their full rated drain current.

Switching Waveforms of the L²FET: A 5-Volt Gate-Drive Power MOSFET

by C. Frank Wheatley, Jr. and Harold R. Ronan, Jr.

The switching waveforms of a newly announced series of power-MOSFET devices called Logic-Level-FETs (L^2FETs) and featuring a 5-volt gate drive are presented and contrasted with those of the more conventional 10-volt-gate-drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascode from a low-voltage lateral MOS. The 2:1 advantage in rise and fall-time and the 4:1 reduction in switching "dynamic V(sat)" dissipation with constant drive power of the L^2FET over the 10-volt MOSFET are demonstrated and discussed.

BACKGROUND

A new series of power-MOSFET devices called Logic-Level FETs, or L^2FETs, is compatible with the 5-volt power supply used for logic circuitry. L^2FETs retain the on-resistance, drain-current, and blocking-voltage ratings of their 10-volt predecessors, but operate from a much less costly 5-volt supply.

The reduction in gate-drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100 nm to 50 nm (500 Å). Since the surface inversion of the MOS channel is determined by the gate-insulator voltage field, halving the insulator thickness halves the applied gate voltage without compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate-oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L^2FET over its 100-nm predecessor, where gate drive power is the same for both devices. The "dynamic V(sat)" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded-gate, depletion-mode, vertical JFET driven in cascode by a grounded-source, enhancement-mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L^2FET Characteristics Compared to Standard Types—A Brief Review

Thirty-two different power MOSFETs of the L^2FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figs. 1, 2, and 3, which are comparisons of the industry-standard RFM10N15 with its Logic-Level-FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L^2FET product currently available is limited to n-channel devices handling 200 volts or less, with 15 ampere ratings or less.)

Figs. 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L^2FET gate voltage is in parenthesis. The low-drain-voltage curves of Fig. 2 demonstrate that R_{on} has not been sacrificed in the L^2FET. Fig. 3 is the transfer characteristic comparison for

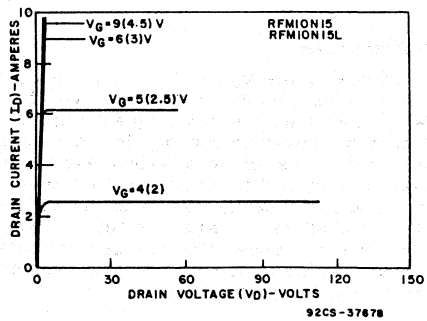


Fig. 1 - Drain-current versus drain-voltage curves for representative standard and L^2FET devices.

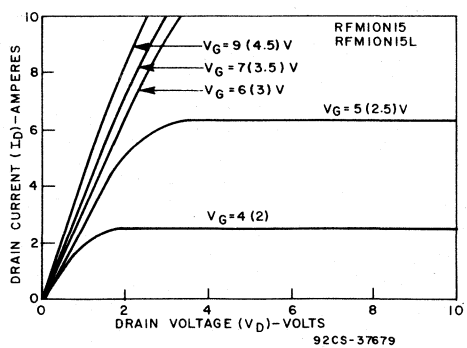


Fig. 2 - Drain-current versus low-drain-voltage curves for representative standard and L^2FET devices demonstrating that R_{on} has not been sacrificed in the L^2FET.

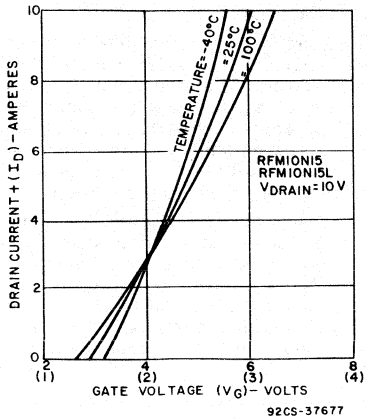


Fig. 3 - Transfer characteristic.

three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, L^2FET values are in parentheses. It is evident from this curve that:

1. The threshold voltage is scaled down by a factor of two for the L^2FET.
2. The threshold-voltage temperature coefficient in mV/° C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L^2FETs have similar relationships to their respective predecessors.

SWITCHING WAVEFORMS WITH CONVENTIONAL DRIVE

The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal." If the standard device is driven between zero and ten volts with an R_g of 25 ohms, impedance transformation dictates that the L^2FET should be driven between zero and five volts with an R_g of 6-1/4 ohms, thereby transforming open-circuit voltage and short-circuit current by factors of 2 (or 1/2). With these parameters, either drive system will supply a peak R_g, or generator dissipation, of one watt.

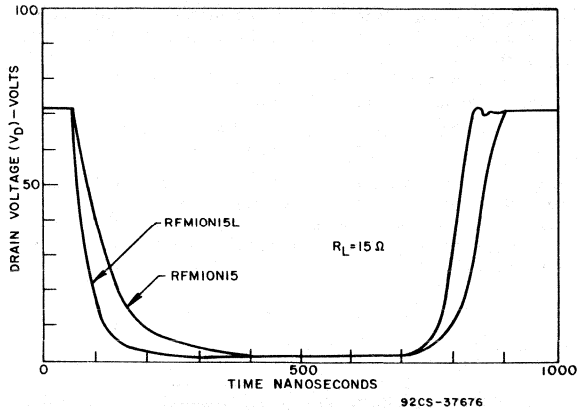
Fig. 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5-ampere, 75-volt resistive load line. The time scale is 100 nanoseconds per division. The table under the graph compares on-delay time, rise time, off-delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input-voltage and output-voltage waveforms.
Note that:

1. The rise and fall times are not symmetrical.
2. The L^2FET is faster.
3. There is a "dynamic V(sat)" type of behavior.
4. The "dynamic V(sat)" is of a lesser amplitude for the L^2FET.

These observations are discussed below.

SWITCHING WAVEFORMS WITH CONSTANT CURRENT DRIVE

The power MOSFET is a current-driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first-order approximation to a constant current where the



Type	Gate Drive	R_g (ohms)	td(on) (ns)	t(rise) (ns)	td(off) (ns)	t(fall) (ns)
RFM10N15 (100 nm)	0-10V	25	15	120	123	73
RFM10N15L (50 nm)	0-5V	6.25	11	57	104	62

Fig. 4 - Drain voltage versus time curves for representative standard and L^2FET devices.

voltage compliance is determined by ground potential or the drive-circuit power-supply voltage. The on current may not equal the off current; this situation is addressed below.

Fig. 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{g1} = I_{g2}$, with gate-voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L^2FET receives less drive power or energy. The value for I_{g1} and I_{g2} was chosen as 5 mA; the time scale is 1 μs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic V(sat)" even at slow switching speeds.

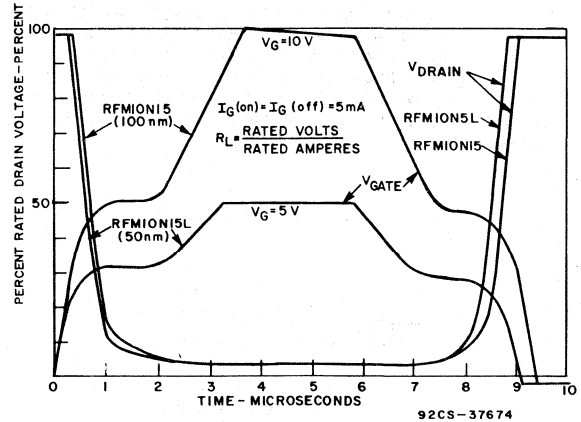


Fig. 5 - Characterization curves for representative devices driven from a current generator.

4. The "dynamic V(sat)" curves are symmetrical during the low-drain-voltage portion of the turn-on and turn-off portion.
5. The "dynamic V(sat)" curves are lower in amplitude by a factor of approximately two for the L^2FET.

LARGE-SIGNAL EQUIVALENT CIRCUIT OF THE MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional power MOSFET must first be understood. Fig. 6 shows a properly proportioned cross-sectional view of the power MOSFET.

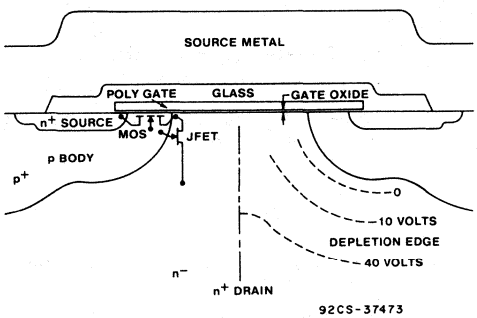


Fig. 6 - Cross section of power MOSFET.

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n^- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion-mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n^+ region usually thought of as being the MOSFET drain. This situation is shown in Fig. 6, where the cross-sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Fig. 6. The right half indicates the edge of the depletion width for several drain voltages. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Fig. 7. Note that the third-quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

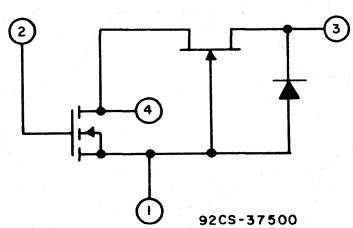


Fig. 7 - Schematic representation of the cross section of Fig. 6.

Interelectrode Capacitance

The equivalent circuit of Fig. 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the small-signal equivalent circuit of the MOS and the JFET. Of course, the MOS and JFET small-signal equivalent circuits are nonlinear functions of voltage and current and invariant with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three-terminal characterization of this four-node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reduces the power MOSFET to the capacitor network of Fig. 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

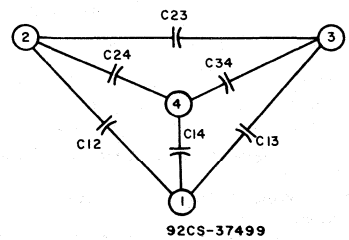


Fig. 8 - Capacitor-network representation of the power MOSFET.

When current does flow, node (4) of Fig. 7 is a low-impedance node due to the source-follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate-To-Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Fig. 6 shows that the gate-to-source capacitance (C_{12}) is that from the poly gate upward through the thick oxide to the source metal. In addition, there is a contribution from the poly gate to the n^+ source through the thin gate oxide. Additionally a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate-To-Drain Capacitance, C_{23}

Capacitor C_{23} exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C_{23} exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate-to-Internal-Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the middle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n^- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulation layer ceases to exist when the external drain voltage minus the IR drop through the n^- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

WAVEFORMS EXPECTED FROM THE MODEL

The following discussion relates the prior model discussion to the waveforms of Fig. 5. The discussion begins with the gate voltage at +5 or +10 volts and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to I_D(max) and the drain voltage equals I_D(max) times r_{DS}(on).

Gate-Voltage Slope — t_{off} Delay

As time progresses, I_g = -5 mA, which must flow through C_{12} + C_{23} + C_{24} of Fig. 8 because the MOS and the JFET are both heavily biased into conduction. Therefore, $dV_4/dt = dV_3/dt$ = nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_g/dt = I_g/(C_{12} = C_{24}) \quad (1)$$

Gate-Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant-current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no long flows from C_{12} during the constant gate-voltage plateau.

Drain-Voltage Shallow Slope

Since C_{23} is still zero, all gate current must flow from C_{24}. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Fig. 7 must ramp at a linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_d/dt = I_g/C_{24} \quad (2)$$

Again this curve will approximate a straight line.

Drain-Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n^- voltage directly beneath the gate oxide, and differs from the drain voltage by an amount nearly equal to $I_D r_{DS}$[on].)

Since the drain voltage is still fairly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_d/dt.

JFET Pinch-Off Voltage — Drain-Voltage Steep Slope

As the drain voltage approaches the pinch-off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET source-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate-Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain-voltage waveform.

Gate-Voltage Slope — t(on) Delay

When the drain is totally off, most of the gate current flows from C_{12}. Again, this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_g/dt = I_g/C_{12} \quad (3)$$

NEW SWITCHING CHARACTERIZATION FOR POWER MOSFETS

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant-current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate-charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive circuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit — Drive

A test circuit is shown in Fig. 9. The heart of this circuit is the RCA-CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Fig. 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximately 0.9). The actual value depends upon the input differential-input voltage. As a comparator, the differential voltage is large, resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5 mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads to parallel the chips rather than wiring many sockets. However, this arrangement may require an increase in the bypass-capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1 megohm or 10 megohm shunting impedance of the scope would load the high-impedance circuitry associated with the MOSFET gate.

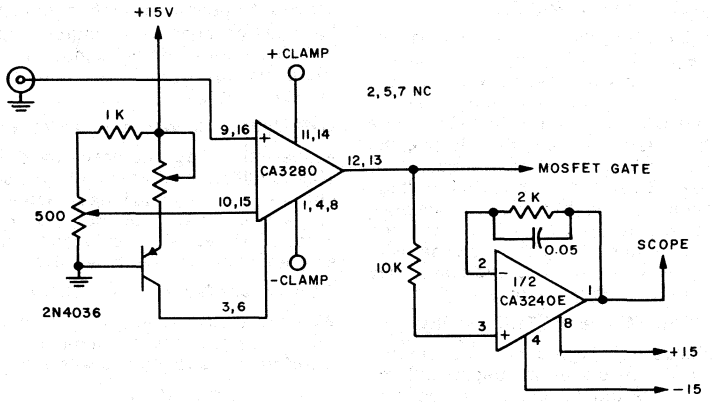


Fig. 9 - Test circuit. 92CS-37501

Testing Conditions

A pulse generator is set for 50-μs on-time duration and approximately 25-ms repetition rate (about 0.2% duty cycle). The $\pm$ clamp voltages are set to the appropriate values. The power-MOSFET load resistor is chosen to equal the maximum-rated voltage divided by the maximum-rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several microseconds exists at the +10-volt level. Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased to maximum-rated value. The L^2FETs would be tested at +5-volts gate clamp.

Fig. 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Fig. 10(a) is the 3-volt signal to the CA3280. Fig. 10(b) is the power-MOSFET gate current. In this example, the amplitude is $\pm$1 mA with a third state of 0 mA. Fig. 10(c) displays the gate voltage and the drain voltage, 10 volts peak-to-peak and 150 volts peak-to-peak. Fig. 10(d) is a piece-wise linear approximation of Fig. 10(c). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Fig. 10 is 100 microseconds full scale.

There are some features of the gate and drain-voltage waveforms that should be noted. These features are consistent with the equivalent-model discussion.

1. The waveforms during the positive gate-current time are symmetrical to those during the negative gate-current time. Exceptions will occur for very fast or very slow switching, and for nonsymmetrical current drive. These exceptions are discussed below.
2. The drain-voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain-voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain-voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS}(on)$.
5. The gate-voltage waveform contains three near-straight-line segments during the positive-gate-current transition time.

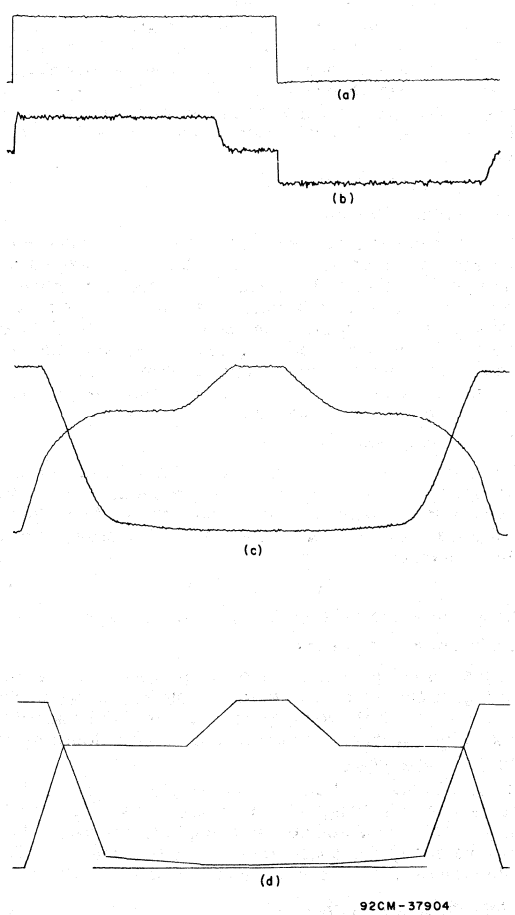


Fig. 10 - (a) 3-volt signal to the CA3280, (b) power-MOSFET gate current, (c) gate and drain voltage, (d) piece-wise linear approximation of 10(c).

Application of the Switching Data

Fig. 11 is a family of curves similar to Fig. 10(c), where the drain supply voltage is fixed at four values. Note that the ordinate is 10-volts full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_g) microseconds full scale, where I_g is the actual gate-drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

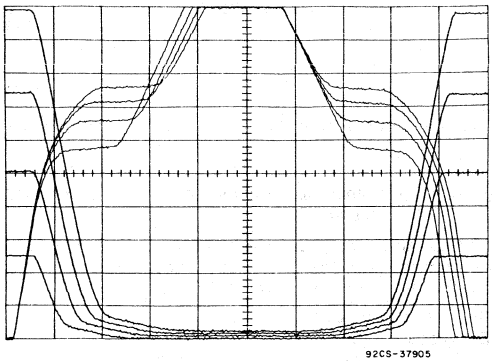


Fig. 11 - Curves similar to those of Fig. 10(c) with drain supply voltage fixed at four values.

Symmetrical Current Drive

Waveforms of Fig. 11 will scale in an inverse manner with gate current. Driving current was varied from ±200 mA to ±2 μA for the device of Fig. 11. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Fig. 12 and compared to the inverse scaling suggested by Fig. 11.

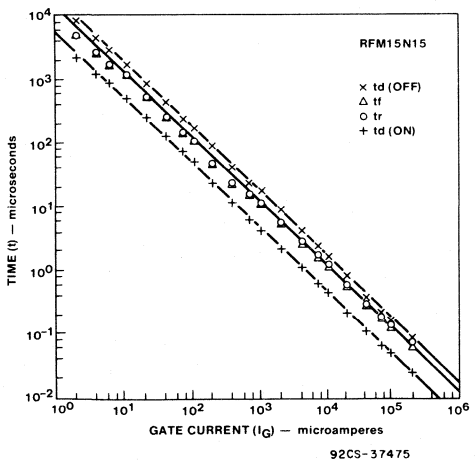


Fig. 12 - Various time measurements compared to the inverse scaling suggested by Fig. 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the inverse scaling. This condition was not noted on Fig. 12 for gate currents as low as ±2 μA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. As a result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Fig. 12, even though the gate current was increased to ±200 mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piece-wise linear methods will yield the gate current, which will permit the proper piece-wise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Fig. 11, dividing it into 10 equal voltage segments; for example, V_g = 0, 1, 2, ... 9, 10 volts.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piece-wise linear gate current for each time segment. I_{g1} = (10 - 0.5)/100 = 95 mA, I_{g2} = (10 - 1.5)/100 = 85 mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Fig. 11 corresponding to an average gate voltage of 9.5, 8.5, ... 1.5, 0.5 volts. Call these segments 11, 12, ... 19, 20.
7. In that the pulse-generator voltage is now zero volts, calculate I_g as:
   I_{g11} = (0 - 9.5)/100 = -95 mA, I_{g12} = (0 - 8.5)/100 = -85 mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Fig. 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymmetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Fig. 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100 mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

AN-7254

GATE-VOLTAGE PROPAGATION EFFECTS

Most power-MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage wavefront applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figs. 13(a), (b), and (c) show the increasing effect of gate-voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Fig. 13(c).

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher R_{ON}).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield "breakthrough" devices unless used in combination.

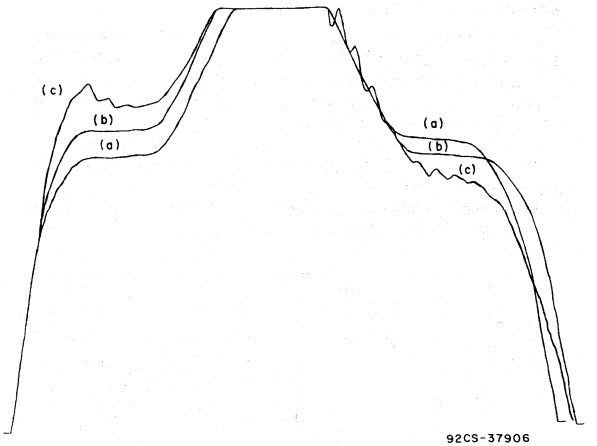


Fig. 13 - Curves showing the increasing effect of gate-voltage propagation.

Any of the above methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of R_{ON} per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

REFERENCES

1. "Power MOSFET Switching Waveforms—A New Insight," H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.
2. "Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed," E. Oxner, Proc. Powercon 9, April 1982.

Power MOSFET Switching Waveforms: A New Insight

by Harold R. Ronan, Jr. and C. Frank Wheatley, Jr.

The examination of power MOSFET voltage and current waveforms during switching transitions reveals that the device characterization now practiced by industry is inadequate. In this Note, device waveforms are explained by considering the interaction of a vertical JFET driven in cascode from a lateral MOSFET in combination with the interelectrode capacitances. Particular attention is given to the drain-voltage waveform and its dual-slope nature. The three terminal capacitances now published by the industry are shown to be valid only for zero drain current. For cases where the gate drive is a voltage step generator with internal fixed resistance, the drain voltage characteristics are inferred from the gate current drive behavior and compared to observed waveforms. The nature of the "asymmetric switching times" is explained.

A waveform family is proposed as a more descriptive and accurate method of characterization. This new format is a plot of drain voltage and gate voltage versus normalized time. A family of curves is presented for a constant load resistance with V_{DD} varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

DEVICE MODELS

The keystone of an understanding of power MOSFET switching performance is the realization that the active device is bimodal and must be described using a model that accounts for the dual nature. Buried in today's power MOSFET devices is the equivalent of a depletion layer JFET that contributes significantly to switching speed. Fig. 1 is a cross-sectional view of a typical power MOSFET, with MOSFET/JFET symbols superimposed on the structure.

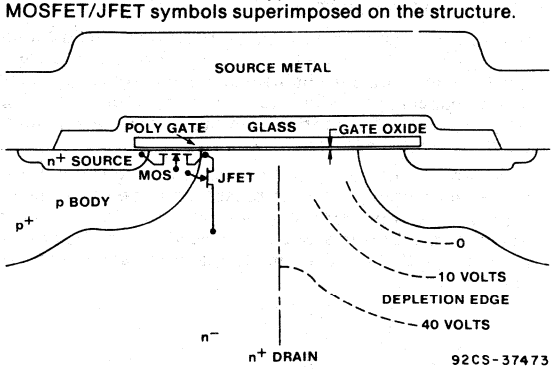


Fig. 1 - Cross-sectional view of MOSFET showing equivalent MOS transistor and JFET.

Fig. 2 is obtained by taking the lateral MOS and vertical JFET from this conception and adding all the possible node-to-node capacitances. Computed values of the six capacitances for a typical device structure suggest that device behavior may be adequately modeled using only three capacitors in the manner of Fig. 3. This is the model to be employed for analysis and study.

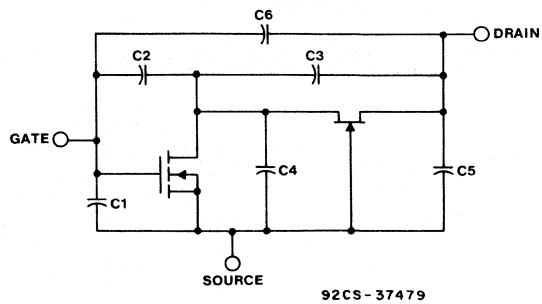


Fig. 2 - MOS transistor with cascode-connected JFET and all capacitors.

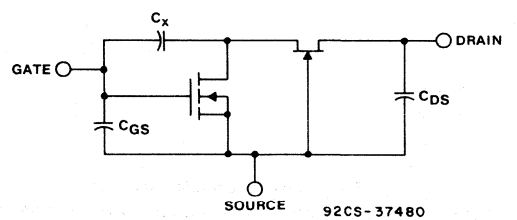


Fig. 3 - Fig. 2 simplified.

GATE DRIVE: CONSTANT VOLTAGE OR CONSTANT CURRENT

Before moving on to the study of the equivalent circuit states of the model, a gate-drive forcing function which is easy to represent, relates to reality, and best illustrates device behavior must be chosen. The choice may be immediately narrowed to two:

(1) An instantaneous step voltage with internal resistance R, Fig. 4.
(2) An instantaneous step current with infinite internal resistance, Fig. 5.

Power MOSFET devices are highly capacitive in nature; hence, simple capacitor responses to the forcing functions offer a good vehicle for comparison. The advantageous choice is immediately obvious: Fig. 5. Voltage/time responses dominated by capacitance are straight lines (when constant current is used). The slope of these lines is

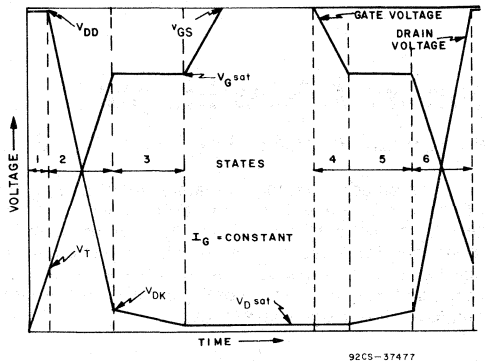
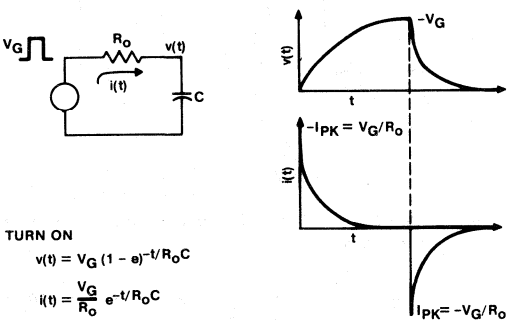


Fig. 4 - Idealized power-MOSFET waveforms.



TURN ON

$$v(t) = V_G(1 - e)^{-t/R_oC}$$

$$i(t) = \frac{V_G}{R_o} e^{-t/R_oC}$$

TURN OFF

$$v(t) = V_G e^{-t/R_oC}$$

$$i(t) = \frac{-V_G}{R_o} e^{-t/R_oC}$$

Fig. 5 - Step-voltage forcing function.

proportional to current and inversely proportional to capacitance. Analytically, then, constant current is most convenient. It is quite another matter, however, to build a bidirectional current drive that is accurate across the many decades of both current and time required to establish experimental verification.

SIX STATES

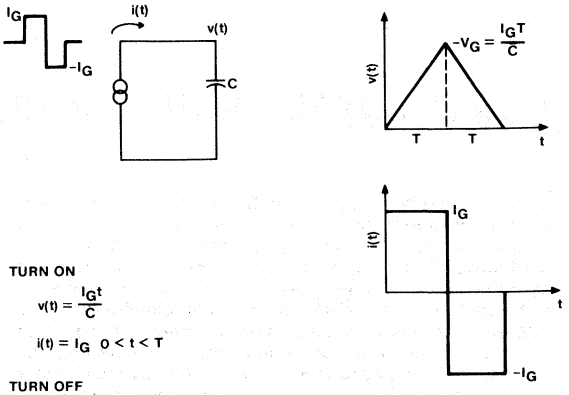
To completely characterize power MOSFET switching waveforms, the six states that a device assumes, Fig. 6, must be addressed:

STATE	MOS	JFET
Turn-on 1	Off	Off
Turn-on 2	Active	Active
Turn-on 3	Active	Saturated*
Turn-off 4	Saturated	Saturated
Turn-off 5	Active	Saturated
Turn-off 6	Active	Active

*The term saturated is taken to mean a constant low-voltage drain-source condition.

Equivalent Circuit

The lumped-parameter model of Fig. 3, with the cascode-connected JFET, can now be reduced to the linear equivalent circuit of Fig. 7, and the six device states investigated from full off to full on.



TURN ON

$$v(t) = \frac{I_G t}{C}$$

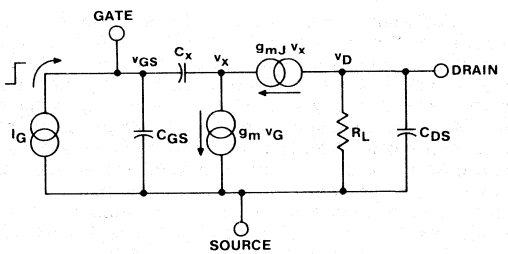
$$i(t) = I_G \quad 0 < t < T$$

TURN OFF

$$v(t) = 2V_G \frac{-I_G t}{C}$$

$$i(t) = I_G \quad T < t < 2T$$

Fig. 6 - Step-current forcing function.



LEGEND

v_{GS}	- Gate Voltage	C_{DS}	- Drain-Source Capacitance
v_x	- JFET Driving Voltage	g_m	- MOSFET Transconductance
v_D	- Drain Voltage	g_{mJ}	- JFET Transconductance
C_{GS}	- Gate-Source Capacitance	R_L	- Drain Load Resistance
C_x	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

Fig. 7 - Power MOSFET equivalent circuit.

State 1: MOS Off, JFET Off

In a power-MOSFET device, no drain current will flow until the device gate threshold voltage, V_T, is reached. During this time, the gate current drive is only charging the gate-source capacitance. More accurately, I_G is charging C_{iss} ($C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted), the capacitance designation published by the industry.

The current generators, $g_m v_G$ and $g_{mJ} v_x$ are open circuits for zero drain current, and R_L is presumed to be so low as to represent a short circuit (generally true for practical applications). This is academic however since C_{GS} is very much larger that C_6. The time to reach threshold, then, is simply:

$$t = \frac{C_{iss} V_T}{I_G}$$

State 2: MOS Active, JFET Active

This state graphically illustrates the dramatic influence that the JFET has on the power MOSFET drain-voltage waveform. Instead of having to discharge Cx from V_{DD} to ground, the lateral MOSFET need only swing v_x to ground, a much smaller voltage thanks to the grounded gate JFET. Since

the interaction of R_L with the device capacitances has a second-order effect on the drain voltage, the equivalent circuit of Fig. 7 predicts a drain voltage change of:

$$dv_G/dt = g_m R_L I_G/[C_{GS} + C_x(1 + g_m/g_{mJ})]$$

In all but the smallest power-MOSFET devices, C_x is several thousand picofarads and g_m/g_{mJ} is of the order of 3:1. Power-MOSFET devices exhibit a high dv_D/dt switching rate because of the cascode-connected JFET, not because C_{rss} ($C_{rss} = C_{GD}$) is a small value, as zero-drain-current data-sheet capacitance values might lead one to believe. If C_{rss} were, in actuality, small, long drain voltage tails would not exist. The tail response is a direct result of JFET saturation. In order to delineate the transition from state 2 to state 3, a drain voltage at which the transition occurs must be defined. V_{DK} is the knee voltage at which linear extrapolations of drain-voltage slopes intersect. The time duration of state 2 is:

$$t = (V_{DD} - V_{DK})[C_{GS} + C_x(1 + g_m/g_{mJ})]/g_m R_L I_G$$

State 3: MOS Active, JFET Saturated

When the JFET saturates, the $g_{mJ}V_x$ current generator becomes a short circuit and the equivalent circuit predicts:

$$dv_D/dt = g_m R_L I_G/[C_{GS} + C_x(1 + g_m R_L)]$$

This is the Miller effect so often referred to in older texts that describe the behavior of grounded-cathode vacuum-tube amplifier circuits. Allowing for the fact that $1 + g_m R_L$ is approximately equal to $g_m R_L$ and $C_x(1 + g_m R_L)$ is very much larger than C_{GS}, the expression for drain-voltage tail time is:

$$t = (V_{DK} - V_D[sat])C_x/I_G$$

State 4: MOS Saturated, JFET Saturated (Turn-Off)

In this state, in addition to $g_{mJ}V_x$ being shorted, the $g_m V_G$ current generator is shorted, and I_G is occupied with charging C_x and C_{GS}, in parallel, from the peak value of V_G to V_G(sat). The time required for this is:

$$t = (V_G - V_G(sat))(C_{GS} + C_x)/I_G$$

Since a value for C_{GS} may be measured independently of switching time, the method described is the simplest way of determining C_x.

On turn-off, the state time equations are equally applicable, but in reverse order (states 5 and 6); see the idealized waveform of Fig. 4.

Experimental Verification

The four switching states just analyzed indicate that for a given device, all four switching state times are inversely proportional to the magnitude of the gate drive current. Fig. 8 illustrates the switching performance of a typical power MOSFET across three decades of gate drive current and time. In each case the data slope is almost a perfect -1.

A NEW DEVICE CHARACTERIZATION

Fig. 8 could not be a reasonable device data sheet presentation because it does not give the designer any information on a typical value for C_x, nor does it convey how V_{DK}, g_m, g_m/g_{mJ}, and V_G(sat) vary with drain current. What would be of enormous value to the designer is a plot of $v_D(t)$, $v_G(t)$ for selected values of V_{DD} and I_D within device ratings. A reasonable characterization would be as follows:

1. The x axis would be normalized in terms of gate current drive.
2. The y axis would be normalized in terms of percent maximum rated V_D (0 to 100%).
3. $R_L = V_D(max)/I_D(max)$ would define the drain load resistance.
4. Four plots of $v_D(t)$, $v_G(t)$ at 100%, 75%, 50%, and 25% $V_D(max)$ would be shown.

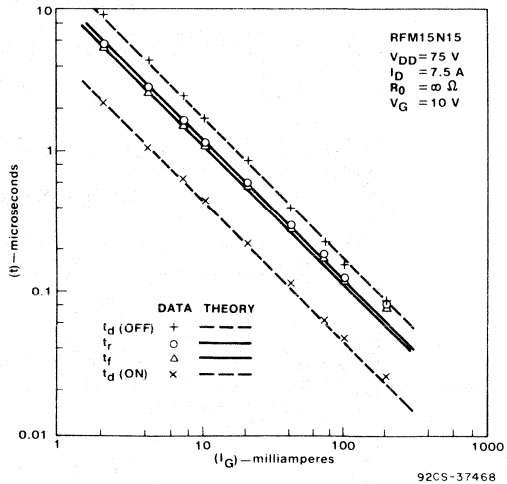


Fig. 8 - Constant gate current switching time.

Fig. 9 is such a plot for the RFM15N15 power MOSFET. With such a plot, a designer can estimate device switching performance under any resistive gate/drain conditions.

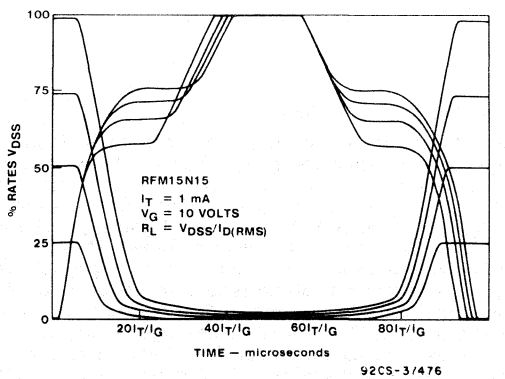


Fig. 9 - Normalized RFM15N15 switching waveforms for constant gate-current drive.

STEP-VOLTAGE GATE DRIVE

The majority of power MOSFET applications employ a step gate-voltage input with a finite source resistance R_o. Often R_o for turn-on is not the same as R_o for turn-off. How can switching times for these situations be estimated using the switching characterization curves just described? The analysis for resistive step voltage inputs, which is complex because the gate current is no longer constrained to be constant, but is a function of device gate-voltage response, is covered in Appendix A. (A second, shorter appendix, B, has been added to illustrate the estimation of R_o for some practical gate drive circuits.) Table I summarizes the common switching equations, and indicates the appropriate I_G to be used in each state for relating step voltage drives to the characterization curves.

Table I - Common Switching Equations

	CONSTANT CURRENT	STATE 1: MOS OFF, JFET OFF	CONSTANT VOLTAGE
TURN ON	$t = \frac{C_{iss} V_T}{I_G}$		$t = R_o C_{iss} \ln \frac{[1]}{[1 - V_T/V_G]}$
	$I_G = I_T$	STATE 2: ACTIVE, ACTIVE	$I_G = (V_G - V_T)/R_o$
	$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		
	$I_G = I_T$	STATE 3: ACTIVE, SATURATED	$I_G = (V_G - V_{Gsat})/R_o$
	$t = \frac{(V_{DK} - V_{Dsat})C_X}{I_G}$		
TURN OFF	$I_G = -I_T$	STATE 4: SATURATED, SATURATED	$I_G = -V_G/R_o$
	$t = \frac{(C_{GS} + C_X)(V_G - V_{Gsat})}{I_G}$		$t = R_o(C_{GS} + C_X) \ln (V_G/V_{Gsat})$
	$I_G = -I_T$	STATE 5: ACTIVE, SATURATED	$I_G = -V_{Gsat}/R_o$
	$t = \frac{(V_{DK} - V_{Dsat})C_X}{I_G}$		
	$I_G = -I_T$	STATE 6: ACTIVE, ACTIVE	$I_G = -V_{Gsat}/R_o$
	$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		

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Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_o$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Fig. 10 is merely a variation of Fig. 8. Using the relationships of Table I, the observed differences between Figs. 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_o equalling the constant I_G, $t_d(on)$, t_r, $t_d(off)$, and t_f will all be longer, as predicted by the ratios of the gate drive currents of Table I. Notice also that t_r, t_f switching symmetry is disrupted by the use of a step voltage with source resistance R_o.

For states 2 and 6 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_T}$$

For states 3 and 5 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_G(sat)}$$

Utilization of available maximum gate drive voltage and current can be optimized for fastest power MOSFET switching speed through the use of constant-current gate drive at the expense of increased gate-drive circuit complexity.

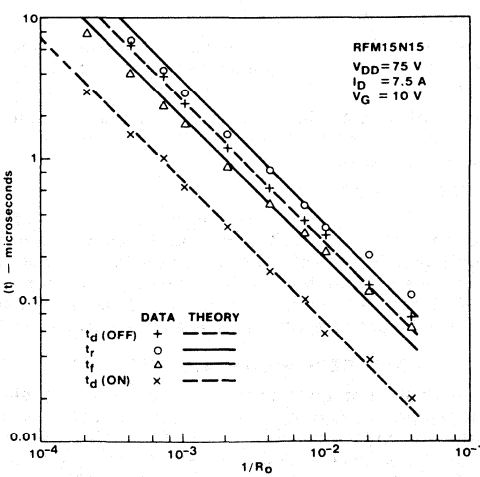

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Fig. 10 - Constant gate voltage switching time.

USING THE CHARACTERIZATION CURVES, FIG. 9

To estimate the switching times for an RFM15N15 power MOSFET under the conditions V_G = 10V, V_{DD} = 75V, R_o = 100 ohms, and R_L = 10 ohms, proceed as follows.

State 1: MOS Off, JFET Off

This time can be estimated without recourse to the curves.

$$t = 100(1200\times10^{-12})\ \ln[1/(1 - 4/10)]$$

$$t = 61\ \text{ns}$$

State 2: MOS Active, JFET Active

$$I_G = (10 - 4)/100 = 60\ \text{mA}$$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{60} = \frac{9}{60} = 150\ \text{ns}$$

State 3: MOS Active, JFET Saturated

$$I_G = (10 - 7)/100 = 30\ \text{mA}$$

$$t = \frac{(\text{curve division}) \times I_T\ \mu s}{30} = \frac{14}{30} = 467\ \text{ns}$$

State 4: MOS Saturated, JFET Saturated

$$C_{GS} + C_x = (\text{gate voltage slope})\ (\text{test current})$$

$$= (1.5 \times 10^{-6}\text{s}/5\ \text{volts})\ (10\ \text{mA})$$

$$= 3000\ \text{pF}$$

$$t = 100(3000 \times 10^{-12})\ \ln[10/6.6]$$

$$t = 125\ \text{ns}$$

State 5: MOS Active, JFET Saturated

$$I_G = 6.6/100 = 66\ \text{mA}$$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{66} = \frac{8}{66} = 121\ \text{ns}$$

Fig. 11 shows RFM15N15 waveforms using the conditions specified in the example.

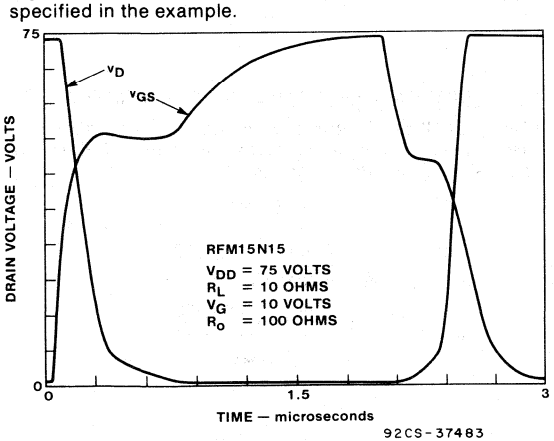


Fig. 11 - Step gate voltage input to an RFM15N15.

State	Calculated Time (t_c, ns)	Measured Time (t_m, ns)	Ratio (t_c/t_m)
1	61	60	1.02
2 + 3	671	670	0.92
4	125	137	0.91
5 + 6	318	375	0.85

For peak gate voltages other than 10 volts, and load resistances other than $V_{DSS}/I_{D(rms)}$, the equations of Table I may be used in conjunction with slope estimates from the characterization curves for C_x and $C_{GS} + C_x(1 + g_m/g_{mJ})$ at the appropriate drain-current level.

CHARACTERIZATION-CURVE LIMITS

The switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of microamperes, device dissipation is the limiting factor. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. However, as Fig. 12 graphically shows, the characterization is valid across five decades of gate current and switching time, allowing all but a very few switching applications to be described by the characterization curves of Fig. 9.

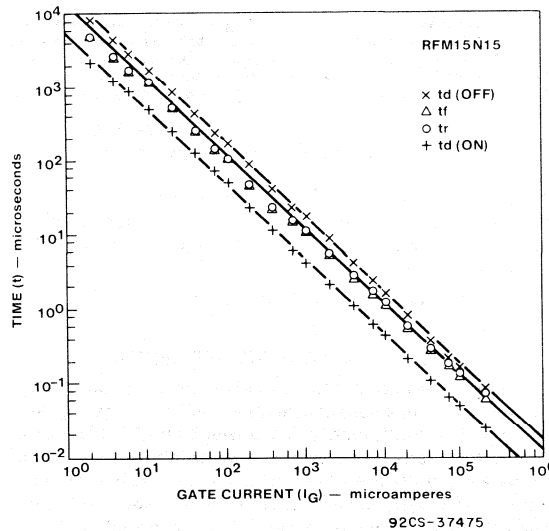


Fig. 12 - Five decades of linear response.

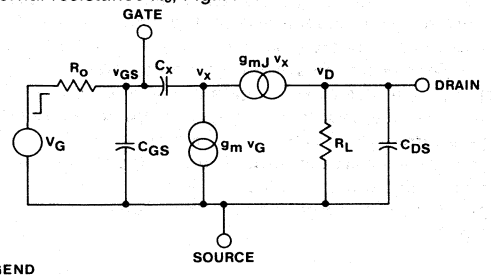
CONCLUSIONS

The viability of the proposed characterization curves using constant current has been demonstrated and the limits of application defined. The existence of a vertical JFET in a power MOSFET makes data-sheet capacitances of little use for estimating switching times. The classical method of defining switching time by 10% and 90% is a poor representation for power MOSFETs because of the dual-slope nature of the drain waveforms. Switching influences are masked because the 10% level is controlled by one mechanism and the 90% level by another. Device comparisons based on the classical switching definition can be very misleading.

APPENDIX A - ANALYSIS FOR RESISTIVE STEP VOLTAGE INPUTS

STEP VOLTAGE GATE DRIVE

To obtain the necessary relationships, six device switching states must be examined using the same device equivalent circuit as was used for the constant-gate-current case, but with the forcing function replaced with a step voltage with internal resistance R_o, Fig. A-1.



LEGEND

v_{GS}	- Gate Voltage	C_{DS}	- Drain-Source Capacitance
v_x	- JFET Driving Voltage	g_m	- MOSFET Transconductance
v_D	- Drain Voltage	g_{mJ}	- JFET Transconductance
C_{GS}	- Gate-Source Capacitance	R_L	- Drain Load Resistance
C_x	- MOSFET Feedback Capacitance	V_G	- Constant Voltage Amplitude

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Fig. A-1 - Power MOSFET equivalent circuit.

STATE 1: MOS OFF, JFET OFF

As before, both current generators are open circuits, reducing the equivalent circuit to simply charging C_{iss} through R_o.

$$t = R_o C_{iss} \ln(1/(1 - V_T/V_G))$$

$$I_{PK1} = V_G/R_o$$

STATE 2: MOS ACTIVE, JFET ACTIVE

Before proceeding, it is wise to examine an actual device response and make use of available simplifications. Fig. A-2 shows $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage. For truly resistive switching, realize that these waveforms are only mirror images of their voltage counterparts $v_G(t)$ and $v_D(t)$. Using Fig. A-2, applicable gate currents for each of the device states may be listed.

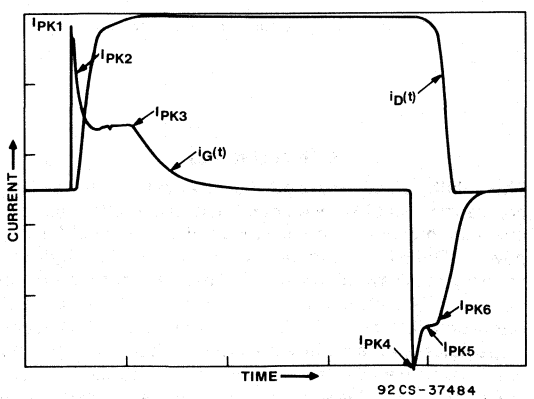

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Fig. A-2 - $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage.

Turn-On

State 1: MOS Off, JFET Off

$$I_{PK1} = V_G/R_o$$

State 2: MOS Active, JFET Active

$$I_{PK2} = (V_G - V_T)/R_o$$

State 3: MOS Active, JFET Saturated

$$I_{PK3} = (V_G - V_G(sat))/R_o$$

Turn-Off

State 4: MOS Saturated, JFET Saturated

$$I_{PK4} = V_G/R_o$$

State 5: MOS Active, JFET Saturated

$$I_{PK5} = V_G(sat)/R_o$$

State 6: MOS Active, JFET Active

$$I_{PK6} = V_G(sat)/R_o$$

The equivalent circuit of Fig. A-1 predicts that:

$$dv_D/dt = -g_m R_L(V_G - V_T)e^{-t/T1}/T1$$

where $T_1 = R_o C_{GS} + (1 + g_m/g_{mJ})R_o C_x$

Note that $g_m R_L(V_G - V_T)$ is usually an order of magnitude greater than V_{DD}, indicating that the drain voltage is discharging toward a very large negative value. The device operation, then, is on the early, almost linear, portion of the exponential, where $e^{-t/T1}$ approximates unity. The drain current of Fig. A-2, and hence the drain voltage, does indeed exhibit a linear decrease with time.

Thus, for state 2:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PK2}}$$

where $I_{PK2} = (V_G - V_T)/R_o$

STATE 3: MOS ACTIVE, JFET SATURATED

Because of the Miller effect, the gate voltage and, hence, the gate current, is almost constant during the tail time. The equivalent circuit then predicts:

$$\frac{dv_D}{dt} = \frac{g_m R_L I_G}{C_{GS} + (1 + g_m R_L)C_x} = \frac{I_G}{C_x}$$

$$I_G = I_{PK3} = (V_G - V_G[sat])/R_o$$

$$\text{and } t = \frac{(V_{DK} - V_D[sat])C_x}{I_{PK3}}$$

STATE 4: MOS SATURATED, JFET SATURATED (TURN-OFF)

Both equivalent-circuit generators are short circuits, and the gate drive is discharging C_x in parallel with C_{GS} through R_o.

$$t = R_o(C_{GS} + C_x) \ln[V_G/V_G(sat)]$$

$$I_{PK4} = V_G/R_o$$

APPENDIX A (Cont'd)

STATE 5: MOS ACTIVE, JFET SATURATED

The JFET current generator $v_x g_{mJ}$ remains shorted and the MOS generator, $v_G g_m$, is operative.

$$t = \frac{(V_{DK} - V_D[sat])C_x}{I_{PK5}}$$

$$I_{PK5} = V_G(sat)/R_o$$

STATE 6: MOS ACTIVE, JFET ACTIVE

The Miller effect is now reduced by the activation of $V_G g_{mJ}$, and the equivalent circuit predicts:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PK6}}$$

$$I_{PK6} = V_G(sat)/R_o$$

APPENDIX B - ESTIMATING R_O FOR SOME TYPICAL GATE-DRIVE CIRCUITS

CASE 1: TYPICAL PULSE-GENERATOR DRIVE, FIG. B-1

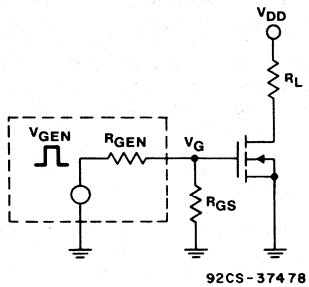

Fig. B-1 - Typical pulse-generator drive circuit.

Turn-On and Turn-Off

$R_o = R_{GEN}R_{GS}/(R_{GEN} + R_{GS})$

For the typical case where R_{GEN} = 50 ohms, and a coaxial-cable termination of 50 ohms, R_o = 25 ohms and $V_G = V_{GEN}/2$

CASE 2: VOLTAGE-FOLLOWER GATE DRIVE, FIG. B-2

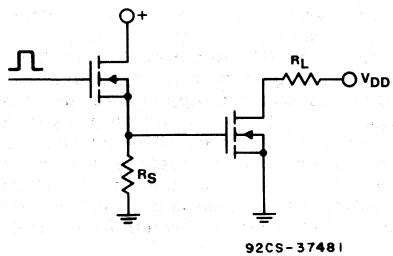

Fig. B-2 - Voltage-follower gate-drive circuit.

Turn-On

R_o is approximately equal to $1/g_m$ for R_s very much greater than $1/g_m$.

g_m = transconductance of driving MOSFET transistor.

Turn Off

$R_o = R_s$

CASE 3: COMMON-SOURCE GATE DRIVE, FIG. B-3

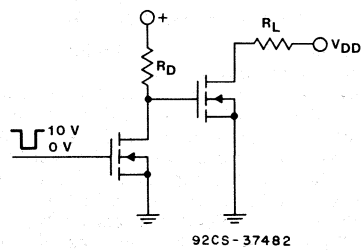

Fig. B-3 - Common-source gate-drive circuit.

Turn-On

$R_o = R_D$ (drain-to-ground capacitance of driving device adds to C_{GS} of driven MOSFET.)

Turn-Off

$R_o = R_{DS}(on)$ of driving MOSFET

R_D is very much greater than $R_{DS}(on)$

The Application of Conductivity-Modulated Field-Effect Transistors

by Jack Wojslawowicz

SUMMARY

The development of conductivity-modulated field-effect transistors, FETs, makes available to the system designer another solid-state device that can be used to implement power switching control. This paper reviews differences between the standard and the newly developed FET. It shows the significant advantages that the conductivity-modulated FET has over the standard FET. Several applications are presented to show that this new type of device works well in practical situations. The relative inmaturity of the conductivity-modulated FET may limit its initial utilization. But as the family grows and product innovation and refinement takes place, this newest member of the power semiconductor family will become a viable alternative to the other members.

GENERAL CONSIDERATIONS

The development of the power field-effect transistor has made available to the power-stage designer an entire new family of power semiconductors. Over the past 5 to 6 years, the breadth of product has grown to encompass the requirements of a large number of applications. A limiting factor that has slowed the utilization of power FETs in the high-current, high-voltage applications is the fact that the on-state resistance ($R_{DS}(on)$) in a standard FET is related to its breakdown voltage (BV_{DSS}) by a nearly cubic power, i.e., $R_{DS}(on) \approx BV_{DSS}$ 2.8. What this implies, as Fig. 1 shows, is that as the breakdown voltage increases, the on-state resistance climbs even faster.

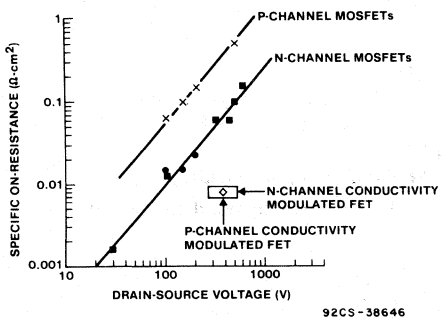

Fig. 1 - Specific on-resistance of p and n-channel MOSFETs and conductivity-modulated FETs versus forward blocking voltage.

The MOSFET on-state resistance is contributed to primarily by three components of the transistor: the MOS channel, the neck region, and the extended drain region. The extended drain region contributes the most to the on-state resistance in high-voltage MOSFETs. To achieve a lower on-state resistance at a given blocking voltage, the usual technique is simply to make the die larger. However, increasing the die size has its limitations from a manufacturing point of view, since MOSFETs, with their very fine horizontal geometries, are highly defect-yield sensitive. As die size increases, the likelihood of a defect resulting in a nonfunctional part increases exponentially. This tendency, combined with a smaller number of parts per wafer, limits the availability of low-on-state-resistance, high-voltage MOSFETs.

A change in the horizontal geometry of the MOSFET can lower the specific on-state resistance per unit area. By using more channel width with smaller source cells placed closer together, a reduction in on-state resistance can be achieved. A limitation on how close these cells can be placed arises from a possible localization of field concentrations that will limit the voltage breakdown of the structure to less than the theoretical rating due only to impurity concentrations. Therefore, for a given breakdown voltage, there exists a minimum spacing of the cell structure. Generally, the higher the required breakdown voltage, the further apart the cells must be placed.

As stated earlier, the extended drain region of the MOSFET generally contributes the most to the on-state resistance in high-voltage MOSFETs. As the required blocking voltage is increased, this region must be made thicker and more lightly doped to be able to support the desired voltage. It is this region's contribution to on-state resistance that the condictivity-modulated field-effect transistor drastically reduces. This reduction occurs as the result of the injection of minority carriers from the substrate and, in specific on-state resistance per unit area, is about 10 times less than in a standard MOSFET at the 400-volt BV_{DSS} level, as shown in Fig. 1.

Further analysis has shown that the specific on-state resistance may be nearly independent of blocking-voltage level. This finding implies that at a BV_{DSS} of 1000 volts, the reduction in conductivity-modulated FETs over the standard MOSFETs could be perhaps 50 to 1. These reductions in on-state resistance per unit area that the conductivity-modulated FETs can achieve present the possibility that high-voltage high-current FET-type devices can become more readily available because of the smaller die sizes associated with conductivity-modulated FETs.

COMPARISON OF STANDARD AND CONDUCTIVITY-MODULATED FETs

Standard and conductivity-modulated FETs share some characteristics, but are substantially different in others. Shown in Table I is a listing of the major characteristics that make the conductivity-modulated FETs unique among power semiconductor families. Foremost, it is a voltage-gated device; its input characteristics are similar to standard power MOSFETs of comparable chip size. Very little drive power is required at low to moderate switching frequencies. The device remains under the control of the gate within its normal operating conditions. It exhibits the normal linear mode as well as the fully saturated on-state of conventional power MOSFETs. When the gate voltage is removed, the device turns off, unlike the thyristor family of power semiconductors, which must be either externally or naturally (internally) commutated.

Table I - Conductivity-Modulated FET Characteristics

Voltage Gated	—	Small gate power required. Similar to standard power MOSFET.
Turn Off	—	When gate drive is removed... Unlike an SCR!
Nonlinear On-State Voltage Drop	—	Like that of an SCR.
Turn On Speed	—	Fast! - Comparable to a standard power MOSFET.
Turn-Off Speed	—	Slow! - Comparable to a bipolar transistor.
Temperature Independent On-State Voltage Drop	—	Unlike the typical 2x variation of a power MOSFET.

The on-state voltage drop or resistance characteristic of a conductivity-modulated FET is markedly different from that of a standard power MOSFET, and is similar to that of a thyristor family member, the SCR. There is an offset voltage component (typically 0.6 volt) due to the p-n junction on the drain side, and a somewhat nonlinear resistive component, both of which are in series between the drain and source terminals. This series arrangement results in a highly nonlinear equivalent resistance, unlike the linear resistive characteristic of $V_{DS}(on)$ of a standard FET.

The structure of the conductivity-modulated FET operates during its turn on just as a standard FET does, hence its turn-on speed is very similiar to that of a standard FET. With its high input impedance and its short propagation delay, the turn-on transistion of the conductivity-modulated FET, as well as the standard power FET, is easily controlled by the gate driving circuit. This characterstic allows the designer the ability to control EMI and RFI generation easily. With other power semiconductors, it may be necessary to employ elaborate circuit schemes to limit rapidly rising in-rush currents.

A significant characteristic that must be considered in power switching applications is that of turn-off speed. The internal action that makes the conductivity-modulated FET such a silicon-efficient device also makes it an inherently slower device during turn-off. The injection of the minority carriers during the on-state conduction of current results in these carriers being present at the moment of turn-off. Without any way of removing these carriers by external means, they must recombine within the structure itself before the device can revert to its fully off-state condition. The quantity of these carriers and how fast they can deplete themselves determines the turn-off switching speed of the conductivity-modulated FET. This process of recombination is considerably slower than the simple discontinuance of majority carrier flow by which the standard power FET turns off. Hence, again, the conductivity-modulated FET is an inherently slower device. Its turn-off speed lies somewhere between the performance of a thyristor and that of a bipolar transistor.

The final characteristic that makes the conductivity-modulated FET different from a conventional FET is the variance of on-state voltage with temperature. The characteristic of the conductivity-modulated FET is similar to that of an SCR, varying about -0.6 mV/°C. The conventional FET has a positive temperature coefficient such that on high-voltage devices the $R_{DS}(on)$ will double from its 25°C value when the junction temperature reaches 150°C. The system designer must take this characteristic into consideration when the heat sink is being designed for the system.

It is these similarities and differences that make the conductivity-modulated FET a unique member of the family of power-semiconductor switching devices. Applications of this alternative power switching device invariably make use of one or more of its unique characteristics.

APPLICATIONS

Automotive Ignition

An application that can take advantage of the low drive-power capability of the conductivity-modulated FET is the electronic automotive ignition system. In Fig. 2, the control IC takes the signal from the pickup coil located in the distributor and regulates the current through the ignition coil. At the proper time, the IC removes base drive from the bipolar transistor, which all systems currently employ as their coil driver. This removal of base drive allows the transistor to shut off which, in turn, causes a rapid decrease in the ignition-coil primary current. As the primary current decreases to zero, the energy stored in the field surrounding the primary is transferred to the secondary coil. The secondary coil, consisting of many more turns than the primary, transforms this energy into a higher voltage, resulting in a spark being generated in the cylinder. The control IC determines when this spark occurs, so as to derive usable power. With the use of a bipolar transistor, it is estimated that approximately two-thirds of the power dissipation that occurs in the control IC is the result of the need to be able to drive the required base current of the ignition output transistor. The high-impedance input of the conductivity-modulated FET virtually eliminates the base-current drive dissipation of the control IC.

With improved silicon usage, the conductivity-modulated FET brings to power semiconductor switching devices the die size necessary to attain the required voltage and current-handling capabilities of the electronic ignition. This smaller-sized die makes possible smaller modules, whether they be hybrid or standard PC-based systems, than those currently implemented with bipolar-transistor technology.

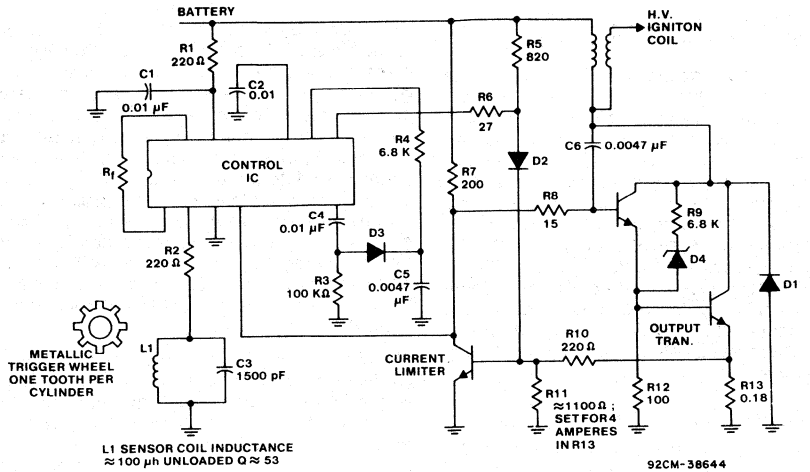

Fig. 2 - Typical ignition system.

Brushless DC Motors

Another emerging application that can make use of conductivity-modulated FETs is the emerging field of brushless dc motors. In this class of application, the solid-state devices are used to electronically switch the voltage to the multiplicity of windings that are employed. The motor consists of an armature that has a number of N and S poles consisting of high-strength permanent magnets. The stator is made up of the multiplicity of windings that were mentioned above; the windings are spaced incrementally about the outside frame of the housing. The voltages to these windings are all electronically switched to create a rotating magnetic field. The armature then rotates to maintain its relative position within the moving magnetic field. The switching of the voltage on the stator windings is done by means of power semiconductor devices. A basic block diagram of such a system is shown in Fig. 3.

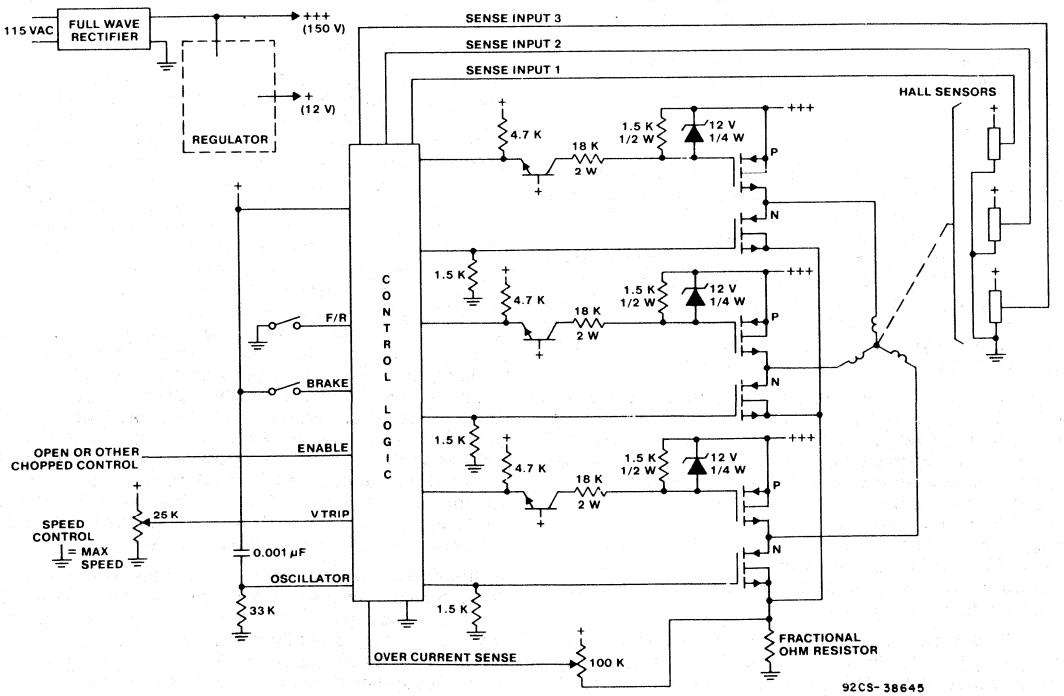

Fig. 3 - Control circuit for three-phase brushless dc motor.

The control logic provides the proper sequence of drive signals based on the rotation direction desired, the speed desired, and the enable input. These requirements are combined with the inputs from the hall-effect sensors to determine which power devices should be activated. Since the current through the stator windings must be bidirectional, the half-bridge or totem-pole output configuration is used to steer the current. This circuit implementation is generally performed with complementary devices, although single-polarity devices can be used with increased circuit complexity.

In a typical 120-volt off-line system, like the one shown in Fig. 3, the switching devices must have a 300 to 400-volt blocking capability. For larger size motors, where larger currents are necessary, the use of power FETs generally implies the use of large die to achieve a low power dissipation to meet the heat-dissipation capability of the packaging. The conductivity-modulated FET, with its temperature-independent on-state-voltage-drop characteristic, helps this situation by keeping the dissipation lower than can be achieved with a standard power FET because of the increasing $R_{DS}(on)$ characteristic of that device. The small die size of the conductivity-modulated FET, the result of better silicon utilization, again makes them the practical choice in motor control not only because of their electrical characteristics, but also because of the lower manufacturing cost of the die.

As stated above, system complexity can be reduced with complementary devices. Although p-channel conductivity-modulated FETs are not yet commerically available, laboratory samples have been fabricated which offers better silicon utilization efficiency than their conventional p-channel counterparts. This statement is based on the fact that p-channel MOSFETs require a 2.5 times larger area than an n-channel device for the same $R_{DS}(on)$.

The easier drive requirements for the n-channel (directly driven from the control IC) and the simplified voltage-translation circuit for driving the p-channel devices, combined with the smaller die size with potentially lower device cost for comparable power handling capability, makes the conductivity-modulated FET a natural for the brushless dc motor application.

Switching Power Supply

One final application that has the potential for conductivity-modulated FET usage is the switching power supply. A half bridge configuration implementation is presented in Fig. 4. The system shown uses a standard PWM control IC to drive the conductivity-modulated FETs through the T2 transformer. The voltage drive characteristic of these devices makes the design of transformer T2 quite simple. The control IC is more lightly loaded because it does not have to supply a continuous base drive, as would be necessary with bipolar transistors.

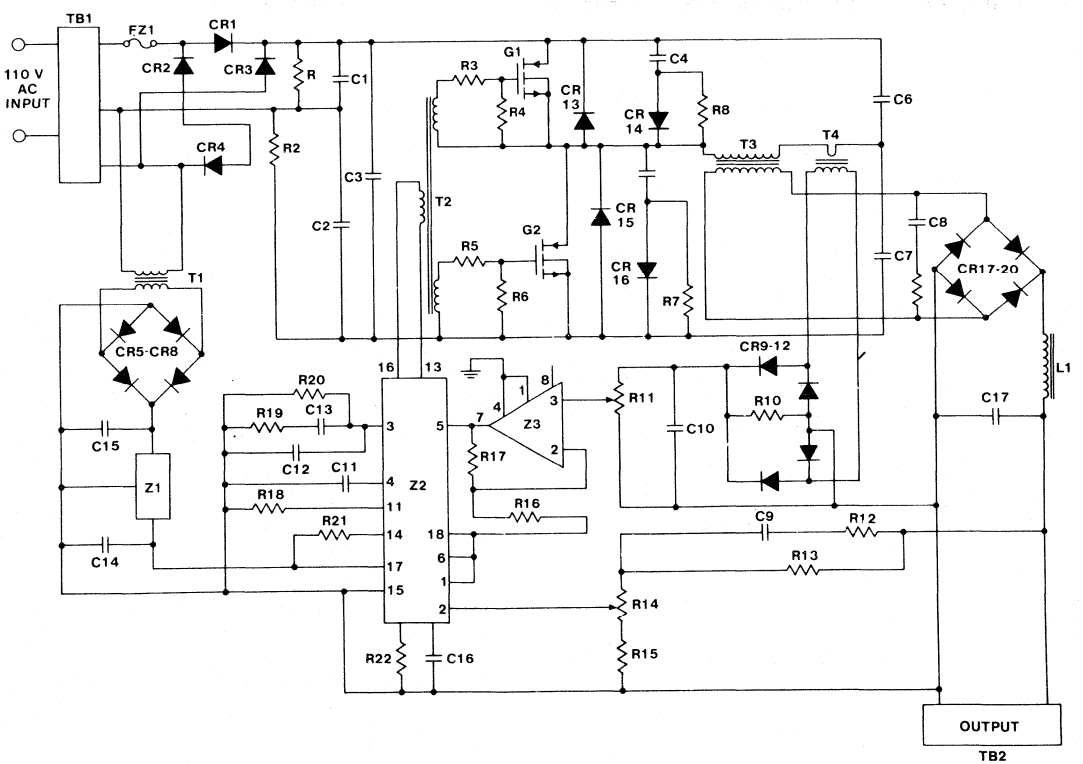

Fig. 4 - Half-bridge switching power supply.

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The operating frequency and the "dead time" are the limitations placed on this system when conductivity-modulated FETs are used. The inherent lower switching speeds of these types of devices make these limitations necessary. The system is currently limited to the 20 to 30-kHz range, with dead times as low as 1 to 2 microseconds. This characteristic is comparable to many existing bipolar systems.

Improvements in switching speeds will occur as the conductivity-modulated FET matures. It is, however, unlikely that they will ever have the same switching speeds as standard power FETs. This limitation prohibits their use in some of the newer higher-frequency power supplies being designed now with conventional FETs. However, in higher-power supplies, where conventional FETs must be paralled to achieve a low enough $R_{DS}(on)$ for good efficiency, the conductivity-modulated FET may present a viable alternative with its smaller die size. Although the operating frequency of the system may have to be compromised to use them.

CONCLUSION

The conductivity-modulated FET represents a progression in the ever-advancing state-of-the-art development that occurs in the world of solid-state devices. The unique structure of these devices presents characteristics that make them equivalent in many ways to conventional FETs but superior in other ways. The system designer must take into account these similar and dissimilar characteristics to properly use them. The capabilities of the conductivity-modulated FETs allow them to make inroads into applications currently served by bipolar transistors, and in some cases conventional power FETs. As the devices mature through innovation and product refinement, conductivity-modulated FETs will become vital members of the family of solid-state power-semiconductor devices.

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The COMFET—A New High Conductance MOS-Gated Device

J. P. Russell, A. M. Goodman
L. A. Goodman and J. M. Neilson

ABSTRACT

A new MOS gate-controlled power switch with a very low on-resistance is described. The fabrication process is similar to that of an n-channel power MOSFET but employs an n^--epitaxial layer grown on a p^+ substrate. In operation, the epitaxial region is conductivity modulated (by excess holes and electrons) thereby eliminating a major component of the on-resistance. For example, on-resistance values have been reduced by a factor of about 10 compared with those of conventional n-channel power MOSFETs of comparable size and voltage capability.

INTRODUCTION

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times, and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability, [1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. In this letter, we describe the fabrication and characteristics of a new vertical power MOSFET structure that provides an on-resistance value about 10 times smaller than that of conventional power MOSFETs of the same size and voltage capability. In this device, the conductivity of the epitaxial drain region of a conventional MOSFET is dramatically increased (modulated) by injected carriers; this mechanism results in a significant reduction in the device on-resistance and leads to the acronym COMFET (COnductivity-Modulated FET).

This device, while similar in structure to the MOS-gated thyristor,[4,5] is different in a fundamental way; it maintains gate control (doesn't latch) over a wide range of anode current and voltage.[6] The structure and the equivalent circuit for the COMFET are shown in Fig. 1(a) and (b); they are similar to those of an MOS-gated thyristor, except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET except that the n^--epitaxial Si layer is grown on a p^+ substrate instead of an n^+ substrate. The heavily doped p^+ region in the center of each unit cell, combined with the sintered aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance shown in Fig. 1(b). This has the effect of lowering the current gain of the n-p-n transistor (α_{n-p-n}) so that $\alpha_{n-p-n} + \alpha_{p-n-p} < 1$. Thus latching is prevented and gate control is maintained within a large operating range of anode voltage and current.[6]

In the remainder of this note we describe the operation and characteristics of this device.

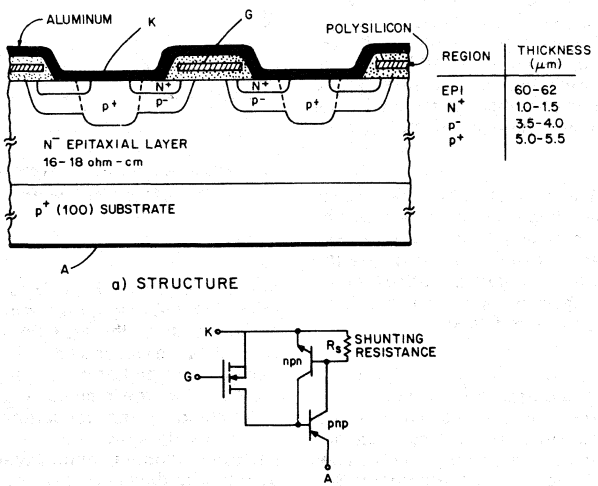

Fig. 1 - (a) Schematic diagram of COMFET structure; (b) Equivalent circuit.

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DEVICE OPERATION

The COMFET is a four-layer (n-p-n-p) device with an MOS-gated channel connecting the two n-type regions. In the normal mode of operation, a positive voltage is applied to the anode (A) relative to the cathode (K). When the gate (G) is at zero potential with respect to K, no anode current (i_A) flows for anode voltage v_A below the breakdown level V_{BF}. When $v_A < V_{BF}$ and the gate voltage is larger than the threshold value V_{gt}, electrons pass into the n^--region (base of the p-n-p transistor). These electrons lower the potential of the n^--region, forward biasing the $p^+ - n^-$ (substrate-epi-layer) junction, thereby causing holes to be injected from the p^+ substrate into the n^- epi-layer region. The excess electrons and holes modulate the conductivity of the high-resistivity n^- region, which dramatically reduces the on-resistance of the device. During normal operation, the shunting resistor (R_S) keeps the emitter current of the n-p-n transistor very low, which keeps α_{n-p-n} very low. However, for sufficiently large i_A, significant emitter injection may occur in the n-p-n transistor, causing α_{n-p-n} to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering i_A below some "holding" value, as is typical of a thyristor.

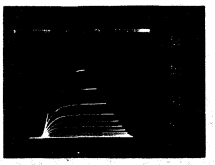
DEVICE CHARACTERIZATION

Two different lots of COMFET structures, consisting of about 10 wafers/lot, have been successfully prepared to date. From these wafers, 1.5 and 3-mm square devices were fabricated using a standard HEXFET geometry[7] with a polysilicon gate electrode over an SiO_2 gate dielectric. Several hundred COMFETs were mounted in standard TO-3 and TO-66 packages and characterized under dc and pulsed conditions, as described below.

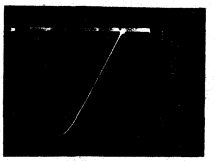
With zero gate bias, the forward characteristic of a COMFET shows very low current (< 1 nA) up to about 390 V, where it breaks up sharply to much larger current levels with only a slight increase in voltage. If the internal junction between the p^+ substrate and the n^- epitaxial layer had been edge-passivated, a similar reverse breakdown characteristic would be expected. The actual reverse breakdown voltage for our devices was about 100 V because edge passivation was not used.

Fig. 2(a) shows the MOSFET-like transfer characteristics of a COMFET in the low gate-voltage region. A noteworthy feature of the COMFET characteristic is the ~ 0.7 V offset, from the origin, of the steeply rising portion of the i(v) characteristics. This offset is the voltage required to forward bias the $p^+ - n^-$ (substrate-epi-layer) junction, and is an integral characteristic of the present device.

Fig. 2(b) shows the i(v) characteristic of a COMFET with v_g = 20 V, and demonstrates the low on-resistance of the device (~ 0.084 Ω at 20 A). The on-resistance values of nearly all of the many COMFETs fabricated to date have been less than 0.1 Ω (at 20 A) for the 3-mm square devices. Such values compare very favorably with those of conventional power MOS structures, as illustrated in Fig. 3. Here, the open data points (and the upper curve) are from data sheet specifications of commercial power MOSFETs (RCA, IRC, and Motorola). The solid data points (and the lower curve) are those of Baliga, which he labelled "state-of-the-art",[3] supplemented with some of the "best" of RCA's commercial



a) MOSFET - Like Characteristic



b) COMFET i(v) with v_g = 20V

Fig. 2 - (a) MOSFET-like characteristic; (b) COMFET i(v) with v_g = 20 V.

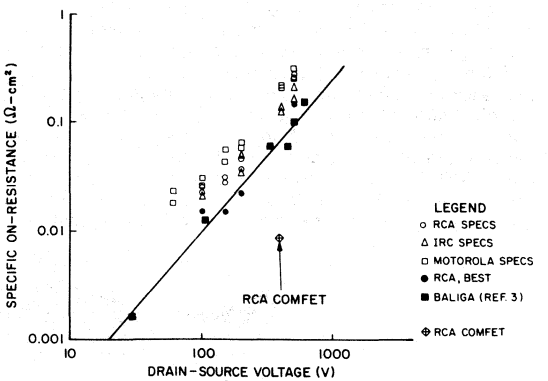


Fig. 3 - Specific on-resistance versus drain-source voltage capability for state-of-the-art power MOSFETs and the COMFET.

and developmental MOSFETs. Note that the on-resistance of the COMFETs is approximately 10 times less than that of a 400-V state-of-the-art MOSFET. Moreover, similarly low on-resistance values should be obtainable from COMFETs designed for higher drain-source voltages. This is due to the fact that the resistance of the modulated region is determined by the concentrations and mobilities of the excess carriers (as in a p-i-n diode)[8] rather than by the background doping of the layer. In particular, the epi-layer doping and thickness of our present COMFET structures were designed for 600 V, but V_{BF} was limited to 400 V by the edge design of the device. An improved edge design should provide a blocking capability closer to bulk breakdown, without altering the on-resistance of the device. This would make the COMFET on-resistance of less than 0.1 Ω even more attractive for high-voltage applications.

TRANSIENT RESPONSE MEASUREMENT

Switching time measurements under pulsed gate-voltage operation were used to characterize the transient operation of the device. The response of the anode current to a square-wave gate-voltage pulse is comprised of a rapid turn-on (with a typical time less than 1 μs) and a somewhat slower turn-off. We observed that the turn-off transient consists of an initial "fast" component, followed by a "slow" tail, as shown in Fig. 4.

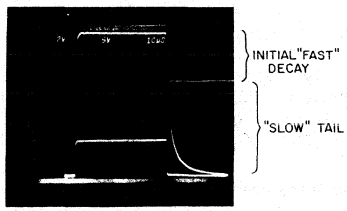


Fig. 4 - Gate voltage (lower trace) and anode current (upper trace) waveforms for $i_A(max) = 8$ A.

We believe that the initial rapid decay is due to the turn-off of the MOS portion of the equivalent circuit, and the turn-off tail is due to the time required for the excess carriers in the epitaxial drain region to decay. In general, turn-off times in the range of 5 to 20 μs were observed, with the precise value depending on circuit conditions and the turn-off time of the gate pulse.

The n-p-n-p structure of the COMFET is similar to that of a thyristor and can be forced to latch under sufficiently high drive conditions. We have observed latching currents in the range 10-30 A in 3-mm square chips. The magnitude of the latching current has been found to depend on both anode voltage and temperature, decreasing with increasing anode voltage or increasing temperature.

More interestingly, the latching current is also strongly influenced by the gate voltage turn-off time. Slow gate turn-off ($\sim$ 10 μs) permits anode currents up to 30 A without latching. However, rapid gate turn-off ($\lesssim$ 1 μs) leads to latching at a much lower anode current level ($\sim$ 10 A) in the same device. We believe that latching during rapid turn-off of the gate voltage is due to current being forced through the n-p-n transistor causing α_{n-p-n} to increase, and leading to the condition for latching, $\alpha_{n-p-n} + \alpha_{p-n-p} = 1$. Slow turn-off of the gate voltage prevents this, since the induced channel turns off slowly and partially shunts the n-p-n transistor; the small current through this transistor keeps α_{n-p-n} sufficiently low to avoid latching.

SUMMARY

A new MOS-gate-controlled power device, the COMFET, has been described. The device has the desirable feature of a very low on-resistance similar to that of a thyristor, but is capable of maintaining gate control of the anode current over a wide range of operating conditions. The low on-resistance is due to conductivity modulation of the n^- epitaxial layer equivalent to the extended drain in a power MOSFET; this carries with it the penalty of slow switching compared with that of a conventional power MOSFET.

ACKNOWLEDGMENT

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Added Note: Following submission of this Note, a similar device was described by B. J. Baliga in a presentation on December 14, 1982 at the International Electron Devices Meeting in San Francisco, CA. (B. J. Baliga et al., "The Insulated Gate Rectifier (IGR): A New Power-Switching Device", in IEDM Tech. Dig. 1982, pp 264-267.

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Improved COMFETs with Fast Switching Speed and High-Current Capability

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C. J. Nuese, and J. M. Neilson*

ABSTRACT

Conventional vertical power MOSFETs are limited at high voltages (>500 V) by the appreciable resistance of their epitaxial drain region. In a new MOS-gate controlled device called a COMFET (or an IGR), this limitation is overcome by modulating the conductivity of the resistive drain region, thereby reducing the on-resistance of the device by a factor of at least 10. However, the device previously described is slow in turn-off, having a fall time in the range 8 to 40 μs.

The purpose of our present work has been to reduce the fall time significantly and to increase the latching current level of the COMFET, while retaining its desirable features. By modification of the epitaxial structure and addition of recombination centers, we have achieved fall times as low as 0.1 μs and latching currents as high as 50 A, while retaining on-resistance values < 0.2 ohm for a 0.09 cm^2 chip area. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping. For a series of COMFETs (with forward-blocking voltage capabilities of 400-600 V), the fall time can be reduced by more than one order of magnitude with a penalty of less than a 20% increase in on-resistance.

INTRODUCTION

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. This limitation has been effectively overcome by the development of a new MOS power device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate.[4-6] We have called this device a COMFET—an acronym for COnductivity Modulated Field Effect Transistor;[4] the device has also been called an IGR or insulated gate rectifier.[5]

The devices, as originally described, had most of the advantages of conventional power MOSFETs; in addition, they exhibited more than an order-of-magnitude reduction in high current on-resistance values, permitting improved utilization of silicon chip area. However, they also had two disadvantages:

1. When a COMFET (or IGR) is turned off, the injected minority carriers that remain in the epitaxial drain region decay by recombination with majority carriers at a rate determined by the minority-carrier lifetime, τ. Large values of τ resulted in anode-current fall time, t_f, in the range 8-40 μs.[4, 5]
2. The maximum operating current is limited by latchup of the parasitic thyristor that is inherent in the device structure. Typical latching current levels of $I_L \lesssim 10$ A were observed in 0.09 cm^2 area devices when the gate voltage was turned off rapidly (< 1 μs); for slower gate voltage turnoff (~ 10 μs), I_L values as high as ~ 30 A were observed.

The purpose of the present work has been to reduce t_f and to increase I_L while retaining the desirable features of the device. By modifying the epitaxial structure and adding recombination centers to the epitaxial drain region, we have achieved t_f values as low as 100 ns and I_L values as high as 50 A with rapid gate voltage turnoff.

MODIFIED STRUCTURE

A schematic diagram of the original COMFET structure[4] is shown in Fig. 1(a), and the equivalent circuit is shown in Fig. 1(b); they are similar to those of an MOS-gated thyristor

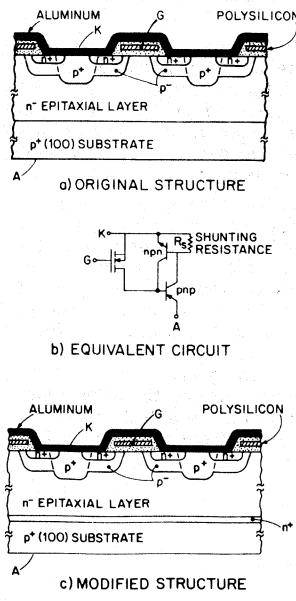

Fig. 1 - (a) Schematic diagram of original COMFET structure. (b) Equivalent circuit. (c) Schematic diagram of modified structure.

except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET, except that the n^--epitaxial layer is grown on a p^+ substrate instead of an n^+ substrate. The heavily doped p^+ region in the center of each unit cell, combined with the aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance R_S. This has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit so that $\alpha_{npn} + \alpha_{pnp} < 1$, thereby preventing latching over a large operating range of anode voltage v_A and anode current i_A. However, for sufficiently large i_A, emitter injection in the n-p-n transistor will increase, accompanied by an increase in α_{npn}. When $\alpha_{npn} + \alpha_{pnp}$ increases to 1, the four-layer device will latch; the level of i_A at which this occurs is the latching current level, I_L. Thus, it can be seen that a structure modification that lowers α_{pnp} will allow a greater range of i_A (and α_{npn}) without latching; that is, a reduction in α_{pnp} corresponds to an increase in I_L.

The modified structure shown in Fig. 1(c) differs from that in Fig. 1(a) by the addition of a thin (~ 10 μm) layer of n^+ silicon in the epitaxial structure between the n^- region and the p^+ substrate. This n^+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in I_L by a factor of 2 to 3. In addition, there is also a reduction in t_f.

These results are illustrated in Fig. 2, in which t_f is plotted versus i_A for each device structure. It should be noted that COMFETs with the modified structure can block high voltage only in the forward voltage direction since the emitter junction ($p^+ - n^+$) of the p-n-p transistor breaks down at a low level when the polarity of the applied voltage is reversed.

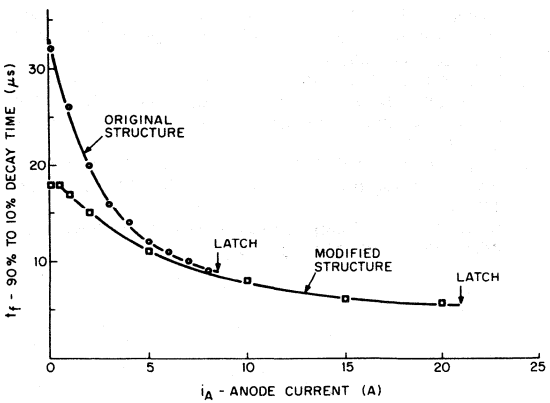

Fig. 2 - Anode-current fall time t_f versus anode current for original structure and modified structure.

ADDITION OF RECOMBINATION CENTERS

We have used a variety of techniques to add recombination centers to COMFETs; these include high-energy electron, gamma-ray, and fast-neutron irradiation, as well as heavy metal doping. The irradiations were carried out after completion of all of the high-temperature processing steps, but in each case an additional heat treatment was necessary to stabilize the devices by annealing out gate-oxide charge, as well as those radiation-induced defects in the silicon (recombination centers) that would otherwise anneal out slowly at the device operating temperature.[7] Typical values of t_f of the order of 1 μs or less were achievable using any of the techniques.

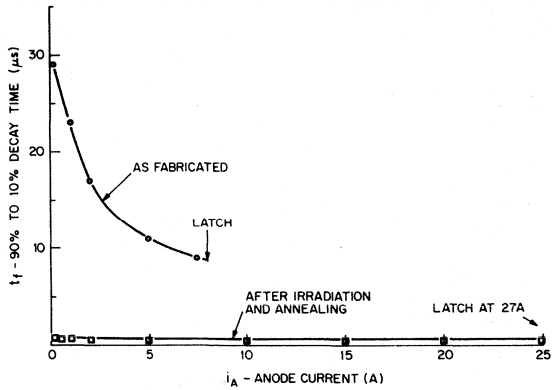

Fig. 3 - Anode-current fall time t_f versus anode current for an as-fabricated device and after 14 MeV neutron irradiation (10^{13}n/cm^2) followed by annealing at 300° C.

An example of the variation of t_f with i_A (1) as fabricated and (2) after irradiation with 14 MeV neutrons and annealing is shown in Fig. 3. Here, the neutron fluence was ~ 10^{13} n/cm^2; this was followed by annealing at 300° C. Note that t_f has not only been drastically reduced, but is virtually constant at ~ 0.6 μs; i.e., almost independent of i_A.

It is possible to lower t_f still further by appropriate irradiation and annealing or by heavy metal doping procedures, although this is not necessarily desirable for reasons that are discussed below. The smallest values of t_f that we have obtained for fully stabilized COMFETs are in the range 100 to 200 ns. This is illustrated in Fig. 4.

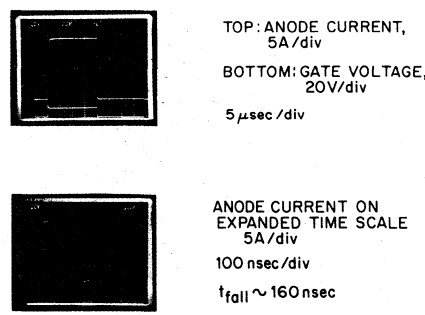

Fig. 4 - COMFET anode current and gate voltage waveforms.

The reduction in minority-carrier lifetime that allows faster switching also carries with it a penalty—higher forward voltage drop when the device is turned on; i.e., higher on-resistance. Since, in the forward conduction of a COMFET, current and voltage are not linearly related, it is necessary to specify a current level at which to compare on-resistance values of different devices. In Fig. 5 we plot the on-resistance (at i_A=20 A) of a series of devices with 0.09 cm^2 chip area against their t_f values after irradiation and annealing. All t_f values shown were obtained at i_A=5 A; for the devices with short switching times, t_f is virtually independent of i_A. Clearly, there is a tradeoff involved, and the optimum choice of a value for t_f and the corresponding

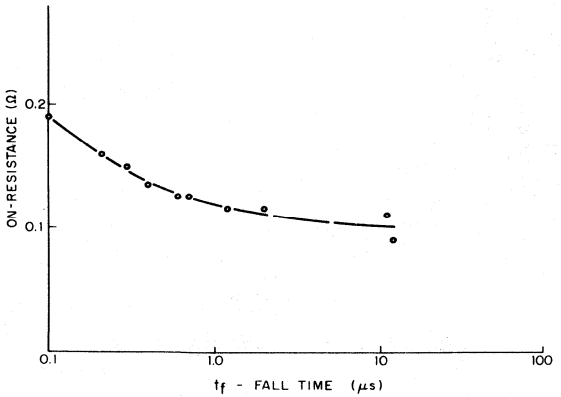

Fig. 5 - On-resistance versus anode-current fall time t_f for a series of COMFETs after various irradiation and annealing treatments.

on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100 ns), the on-resistance value of 0.2 ohm is approximately an order-of-magnitude less than that of comparably-sized n-channel MOSFETs.

TEMPERATURE DEPENDENCE OF t_f AND I_L

All of the device performance data presented thus far have been measured at room temperature. However, power devices are often operated at elevated temperatures, and it is important to determine how their performance varies with temperature. In Fig. 6 the variation of t_f and I_L for a device

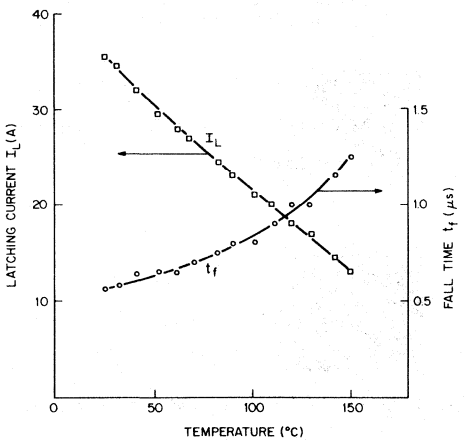

Fig. 6 - Variation of anode-current fall time t_f and latching current I_L with temperature.

that has been irradiated and annealed is plotted versus temperature in the range 25 to 150°C. This behavior is typical of all of the devices we have tested; i.e., t_f increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval 25°C to 150°C.

SUMMARY

By modification of the epitaxial structure of the COMFET and the addition of recombination centers, we have achieved anode-current fall times as low as 100 ns in COMFETs with latching currents as high as 50 A for a 0.09 cm^2 chip area. We have described the tradeoff between on-resistance and anode-current fall time that may be obtained, and have demonstrated the variation of anode-current fall time and latching current with operating temperature.

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